July 2013

FAN7340
LED Backlight Driving Boost Switch

Features

- Single-Channel Boost LED Switch
- Internal Power MOSFET for PWM Dimming: $R_{DS(on)}$ = 3.4 Ω at V_{GS}=10 V, BV_{DSS}=400 V
- Current Mode PWM Control
- Internal Programmable Slope Compensation
- Wide Supply Voltage Range: 10 V to 35 V
- LED Current Regulation: ±1%
- Programmable Switching Frequency
- Analog and PWM Dimming
- Wide Dimming Ratio: On Time=10 µs to DC
- Cycle-by-Cycle Current Limiting
- Thermal Shutdown: 150°C
- Open-LED Protection (OLP)
- Over-Voltage Protection (OVP)
- Over-Current Protection (OCP)
- Error Flag Generation (for External Load Switch)
- Internal Soft-Start
- 16-Lead SOIC Package

Applications

- LED Backlight for LCD TV
- LED Backlight for LCD Monitor
- LED Lighting

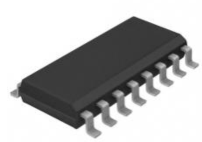
Description

The FAN7340 is a single-channel boost controller that integrates an N-channel power MOSFET for PWM dimming using Fairchild's proprietary planar Double-diffused MOS (DMOS) technology.

The IC operates as a constant-current source for driving high-current LEDs.

It uses Current Mode control with programmable slope compensation to prevent subharmonic oscillation. The IC provides protections including: open-LED protection, over-voltage protection, and direct-short protection for high system reliability.

The IC internally generates a FAULT signal with delay if an abnormal LED string condition occurs. PWM dimming and analog dimming functions can be implemented independently. Internal soft-start prevents inrush current flowing into output capacitor at startup.



Ordering Information

Part Number	Operating Temperature Range	Package	Packaging Method
FAN7340MX	-40°C to +125°C	16-Lead, Small-Outline Integrated Circuit (SOIC)	Tape & Reel

Block Diagram

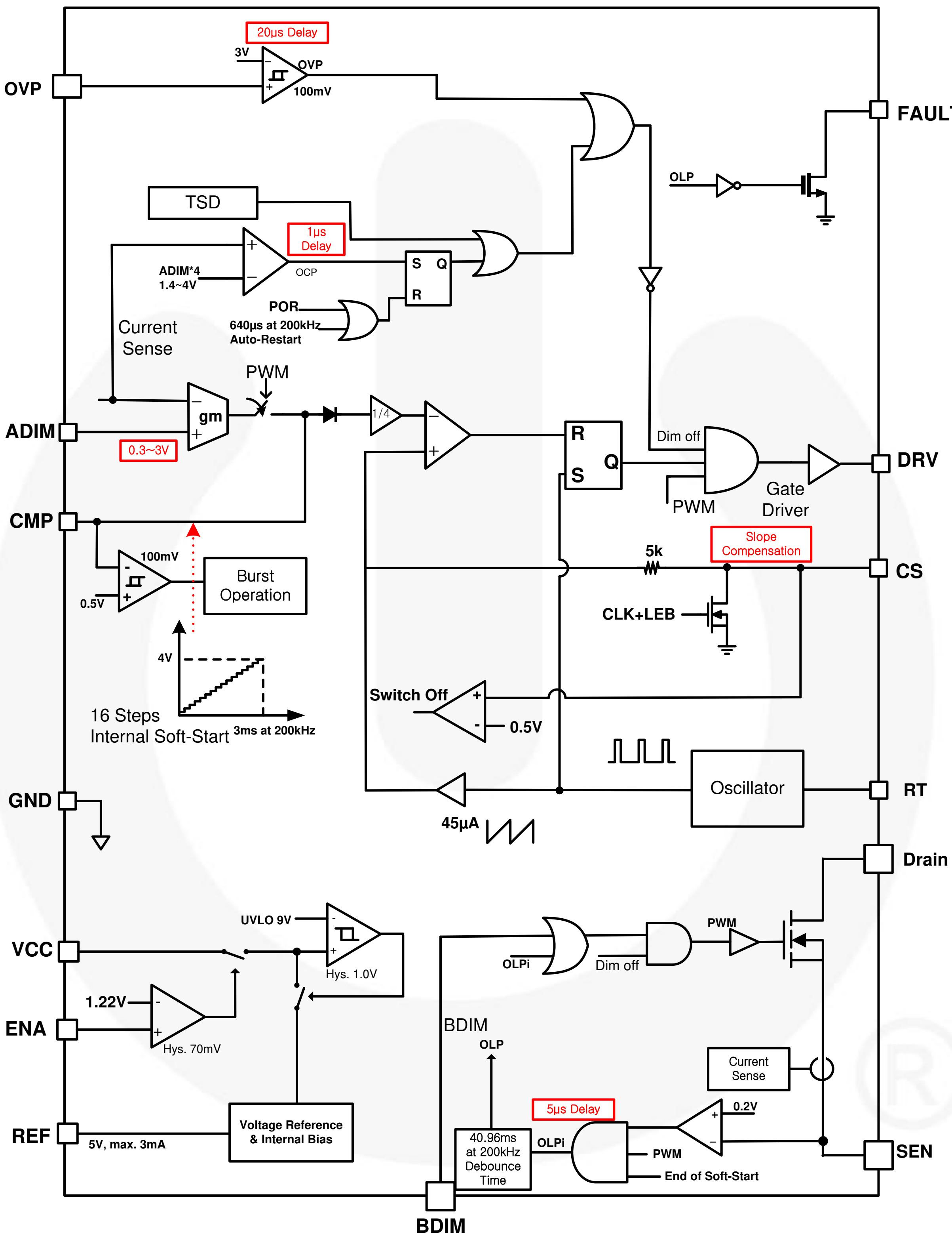


Figure 1. Internal Block Diagram

Pin Assignments

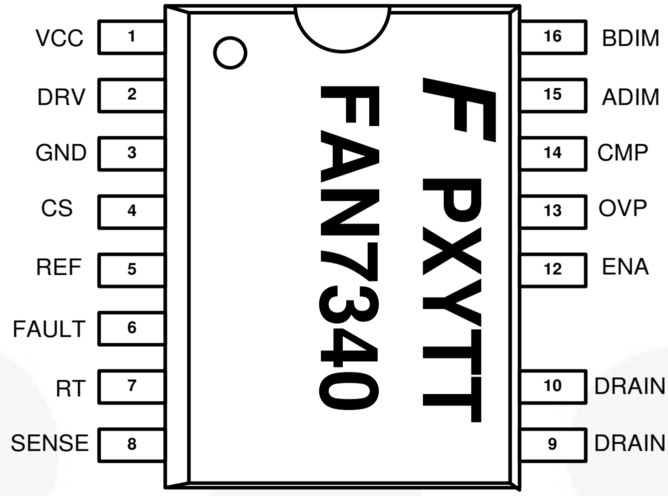


Figure 2. Package Diagram

Pin Definitions

Pin #	Name	Description
1	VCC	This pin is the supply voltage of the IC.
2	DRV	This pin is the gate drive signal of the boost switch.
3	GND	This pin is the ground of the IC.
4	CS	This pin is for sensing the current flowing through an external MOSFET. It includes a built-in 300 ns blanking time. The peak of the current flowing through the MOSFET is limited to this pin voltage. Slope compensation of the boost controller can be programmed through the series resistor of this pin.
5	REF	This pin is the 5 V reference voltage pin. Maximum current capability is 3 mA.
6	FAULT	This pin is for indicating the fault signal. This pin is connected to the open drain. When OLP protection is occurred, the FAULT pin is pulled HIGH.
7	RT	Oscillator frequency set of the boost switch (50 kHz ~ 300 kHz).
8	SENSE	This pin is for sensing the current flowing through the LEDs. A sensing resistor is connected from this pin to ground. This pin is connected to the negative input of the internal error amplifier.
9, 10	DRAIN	Drain pin of PWM dimming power MOSFET.
12	ENA	Enable input pin. If voltage of this pin is higher than 1.22 V, IC is starting to operate. If the voltage of this pin is lower than 1.15 V, the IC stops operating.
13	OVP	Over-voltage protection input pin. Output voltage of the boost circuit is connected to this pin through a resistor divider circuit. If this pin voltage is higher than 3 V, OVP is triggered.
14	CMP	This pin is the error amplifier output. Typically, a compensation capacitor and resistor are connected to this pin from the ground.
15	ADIM	This pin is for setting the current flowing through the LEDs. This pin is connected to the positive inputs of the internal error amplifier. Linear voltage range of ADIM is 0.3 V~3.0 V.
16	BDIM	This pin is for the burst dimming signal. If this pin voltage is HIGH, the internal dimming MOSFET is turned on. If this pin voltage is LOW, the dimming MOSFET is turned off.

Note:
1. Pin 11 is a “No Connect” pin (not shown in Figure 2).

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. T_A=25°C unless otherwise specified.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	10	35	V
T_A	Operating Temperature Range	-40	+125	°C
T_J	Junction Temperature		+150	°C
T_{STG}	Storage Temperature Range	-65	+150	°C
Θ_{JA}	Thermal Resistance Junction-to-Ambient[2, 3]		120	°C/W
P_D	Power Dissipation		0.9	W

Notes:

2. Thermal resistance test board; size 76.2 mm x 114.3 mm x 1.6 mm (1S0P); JEDEC standard: JESD51-2, JESD51-3.
3. Assume no ambient airflow.

Pin Breakdown Voltage

Pin #	Name	Value	Unit
1	VCC	35	V
2	DRV	20	V
3	GND		V
4	CS	6	V
5	REF	6	V
6	FAULT	35	V
7	RT	6	V
8	SENSE	6	V

Pin #	Name	Value	Unit
9	DRAIN	400	V
10	DRAIN	400	V
11	N/A		V
12	ENA	6	V
13	OVP	6	V
14	CMP	6	V
15	ADIM	6	V
16	BDIM	6	V

Electrical Characteristics

For typical values, T_A = 25°C and V_{CC} = 15 V unless otherwise specified. Specifications to -40°C ~ 125°C are guaranteed by design based on final characterization results.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Supply Voltage Section						
V_{CC}	Input DC Supply Voltage Range(4)		10		35	V
I_{SD}	Shutdown Mode Supply Current	BDIM Connected to GND		2	4	mA
Under-Voltage Lockout Section						
V_{th}	Start Threshold Voltage		8.3	9.0	9.7	V
$V_{th,hys}$	Start Threshold Voltage Hysteresis		0.5	1.0	1.5	V
I_{st}	Standby Current	V_{CC}=V_{th}-0.2		200	300	µA
ON/OFF Section						
V_{on}	On-State Input Voltage		2		5	V
V_{off}	Off-State Input Voltage				0.8	V
Error Amplifier Section						
G_m	Error Amplifier Transconductance(4)	V_{ADIM}=1 V	100	300	500	µmho
A_{V_ro}	Error Amplifier Output impedance(4)			20		MΩ
A_V	Error Amplifier Open-Loop Gain(4)			60		dB
V_{offset}	Input Offset Voltage	V_{ADIM}=1 V	-10		10	mV
I_{sin}	CMP Sink Current	V_{ADIM}=1 V, V_{SENSE}=2 V	100	200	300	µA
I_{sur}	CMP Source Current	V_{ADIM}=1 V, V_{SENSE}=0 V	100	200	300	µA
V_{IDR}	Input Differential Voltage Range		0		3	V
V_O	Output Voltage Range		0.7		4.0	V
Oscillator Section						
f_{osc}	Boost Oscillator Frequency	Min.		50		kHz
		R_T=100 kΩ	190	200	210	kHz
		Max.		300		kHz
D_{max}	Maximum Duty Cycle(4)		86	90	94	%
Reference Section						
V_{REF}	5V Regulation Voltage		4.9	5.0	5.1	V
$V_{REF,Line}$	5V Line Regulation				25	mV
$V_{REF,Load}$	5V Load Regulation	0<I5<3 mA			25	mV
PWM Dimming Section						
$V_{PDIM,L}$	PWM Dimming Input Low Voltage				0.8	V
$V_{PDIM,H}$	PWM Dimming Input High Voltage		2		5	V
R_{PDIM}	PWM Dimming Pull-Down Resistance		100	160	220	kΩ
FET Section (for Dimming)						
BV_{DSS}	Drain-Source Breakdown Voltage(4)	V_{CC}=0 V, I_D=250 µA	400			V
I_{DSS}	Zero-Gate-Voltage Drain Current(4)	V_{DS}=250 V, T_A=25°C		1	30	µA
$R_{DS(ON)}$	Drain-Source On-State Resistance	V_{GS}=10 V, I_D=1 A		3.4		Ω
C_{ISS}	Input Capacitance(4)	V_{DS}=25 V, V_{GS}=0V, f=1 MHz		173	225	pF
C_{OSS}	Output Capacitance(4)	V_{DS}=25 V, V_{GS}=0V, f=1 MHz		30	40	pF

Continued on the following page…

Electrical Characteristics (Continued)

For typical values, T_A = 25°C and V_{CC} = 15 V, unless otherwise specified. Specifications to -25°C ~ 85°C are guaranteed by design based on final characterization results.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Output Section (Boost / Dimming)						
V_{DRV}	Gate Output Voltage	V_{CC}=15 V	10.8	11.8	12.8	V
V_{uv}	Gate Output Voltage Before Startup		-0.5		0.5	V
I_{dsur}	Gate Output Drive Source Current(4)		80	180	280	mA
I_{dsin}	Gate Output Drive Sink Current(4)		80	180	280	mA
t_{rh}	Gate Output Rising Time (Boost)(4)	C_L=2.0 nF		200		ns
t_{fl}	Gate Output Falling Time (Boost)(4)	C_L=2.0 nF		120		ns
Current Sense Section						
t_{blank}	Leading-Edge Blanking(4)		150	300	450	ns
$t_{delay,cl}$	Delay to Output of Current-Limit Comparator(4)				180	ns
$V_{offset,clc}$	Offset Voltage of Current-Limit Comparator(4)		-20		20	mV
Slope Compensation Section						
I_{slope}	Ramp Generator Current		36	45	54	µA
R_{slope}	Slope Compensation Resistor(4)			5		kΩ
Soft-Start Section						
t_{ss}	Soft-Start Period(4)	f_{osc}=200 kHz		3		ms
Protection Section						
$t_{d,ovp.tr}$	Delay for Triggering Over-Voltage Protection(4)		15	20	25	µs
$t_{d,ovpr}$	Delay for Releasing Over-Voltage Protection(4)		10	14	18	µs
$t_{d.ocp}$	Delay for Over-Current Protection(4)			1		µs
t_{AR}	Auto-Restart Time for Over-Current Protection(4)	f_{osc}=200 kHz		640		µs
$t_{d,olpi}$	Delay for Triggering Open-LED Protection(4)		3	5	7	µs
$t_{d,olp}$	Delay for Open-LED Protection	f_{osc}=200 kHz		40.96		ms
$V_{th,ovp}$	Over-Voltage Protection Threshold Voltage		2.85	3.00	3.15	V
$V_{hys,ovp}$	Over-Voltage Protection Voltage Hysteresis			0.1		V
$V_{th.csocp}$	Boost Switch Current Limit Threshold Voltage		0.45	0.50	0.55	V
$V_{th,ocp}$	LED Over-Current Protection Threshold Voltage		1.4 (Min. Clamp)	4.0xV_{ADIM}	4.0 (Max. Clamp)	V
$V_{th,olp}$	Open-LED Protection Threshold Voltage(4)		0.15	0.20	0.25	V
T_{SD}	Thermal Shutdown Temperature(4)		140	150	160	°C
T_{HYS}	Thermal Shutdown Hysteresis(4)			20		°C

Notes:

4. These parameters, although guaranteed, are not tested in production.

Typical Performance Characteristics

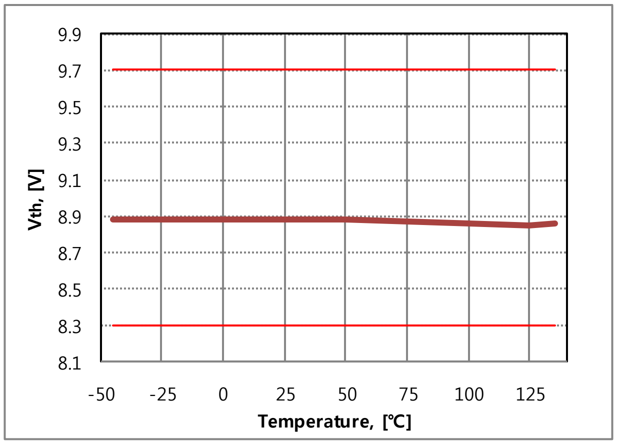


Figure 3. Start Threshold Voltage vs. Temperature

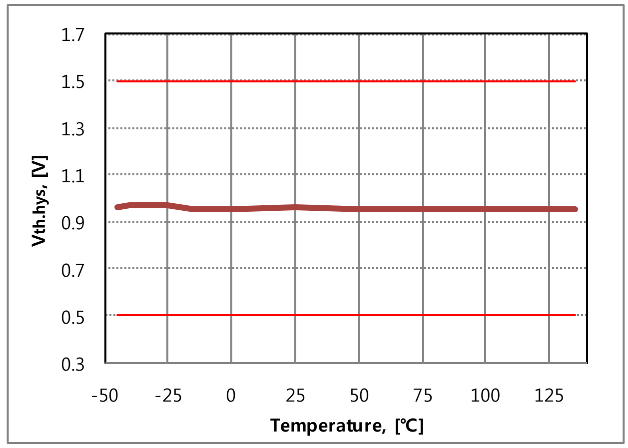


Figure 4. Start Threshold Voltage Hysteresis vs. Temperature

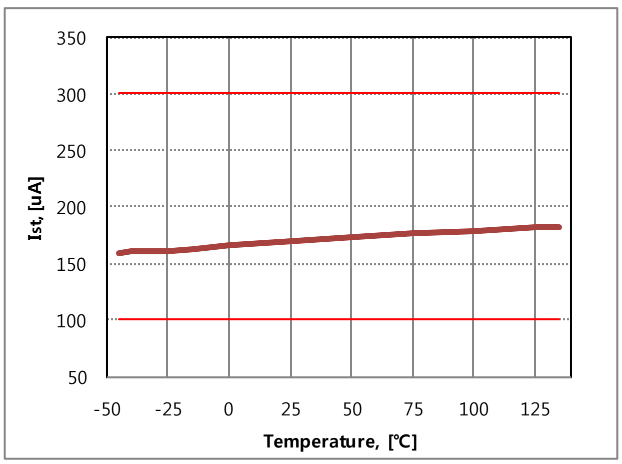


Figure 5. Standby Current vs. Temperature

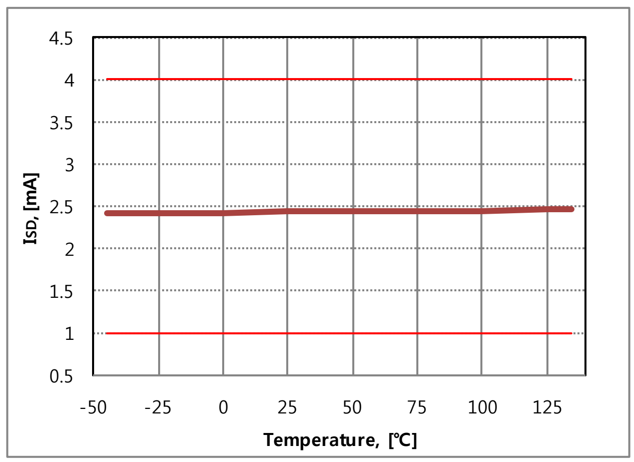


Figure 6. Shutdown Mode Supply Current vs. Temperature

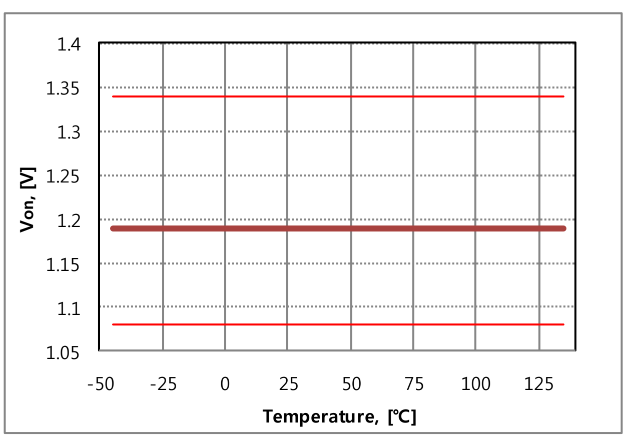


Figure 7. On-State Input Voltage vs. Temperature

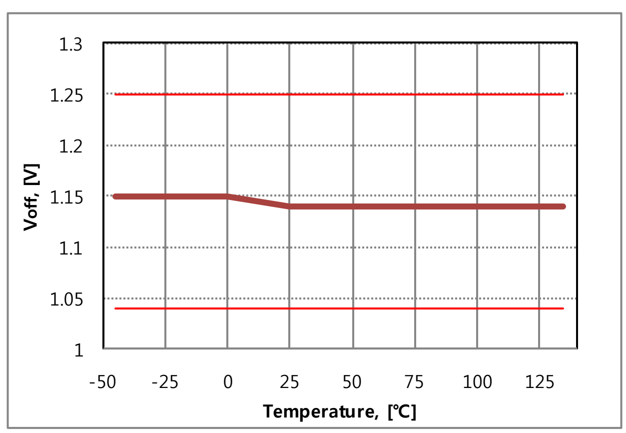


Figure 8. Off-State Input Voltage vs. Temperature

Typical Performance Characteristics (Continued)

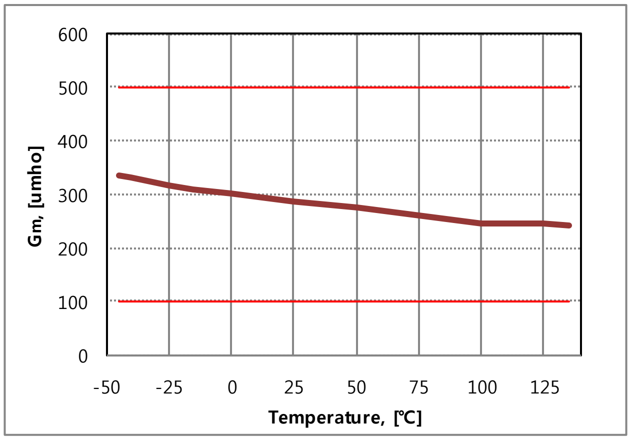


Figure 9. Error Amplifier Transconductance vs. Temperature

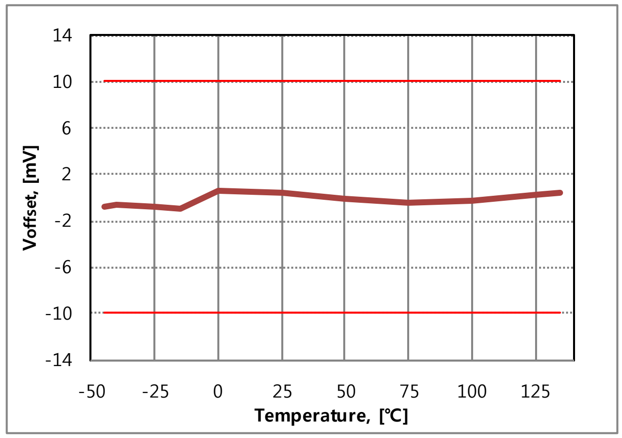


Figure 10. Input Offset Voltage vs. Temperature

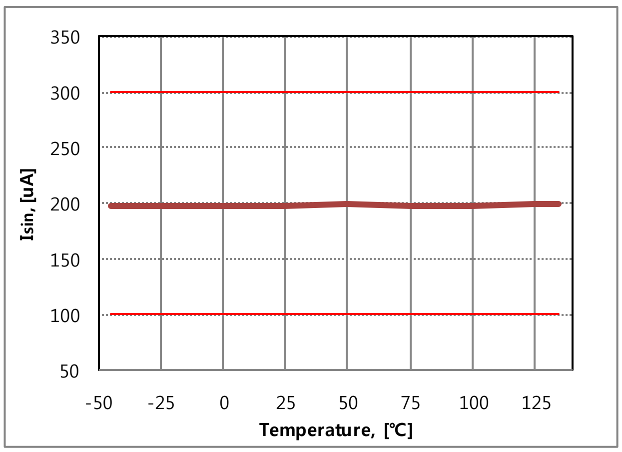


Figure 11. CMP Sink Current vs. Temperature

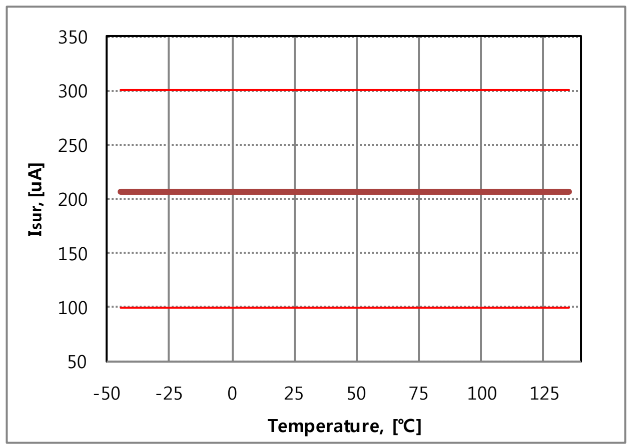


Figure 12. CMP Source Current vs. Temperature

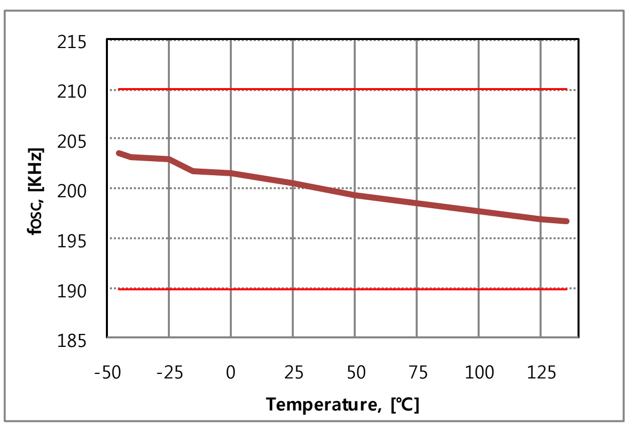


Figure 13. Boost Oscillator Frequency vs. Temperature

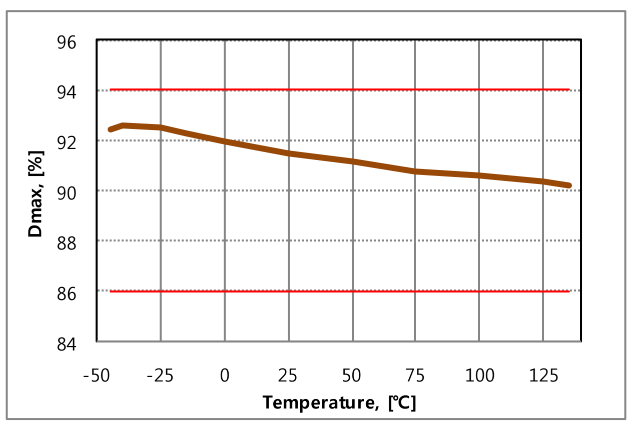


Figure 14. Maximum Duty Cycle vs. Temperature

Typical Performance Characteristics (Continued)

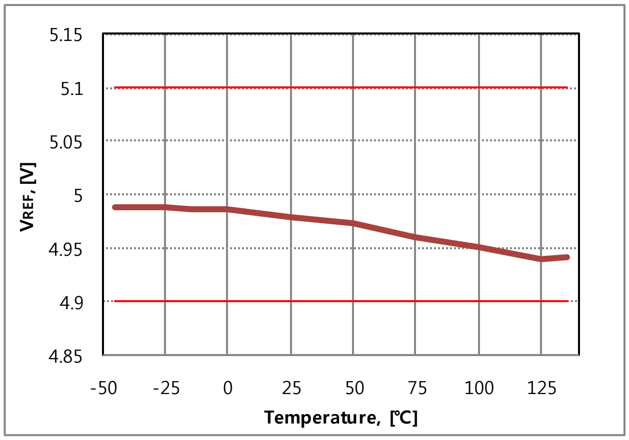


Figure 15. 5V Regulation Voltage vs. Temperature

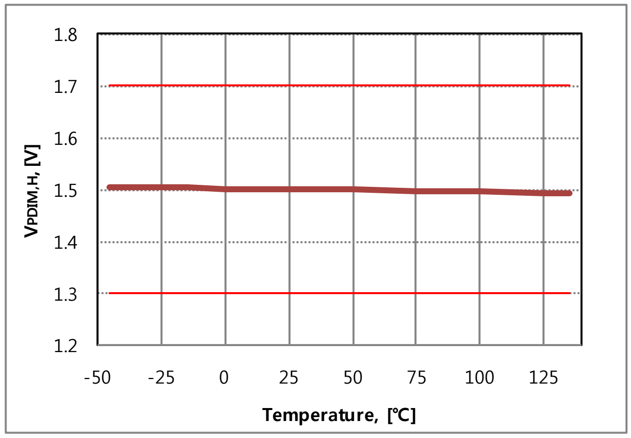


Figure 16. PWM Dimming Input High Voltage vs. Temperature

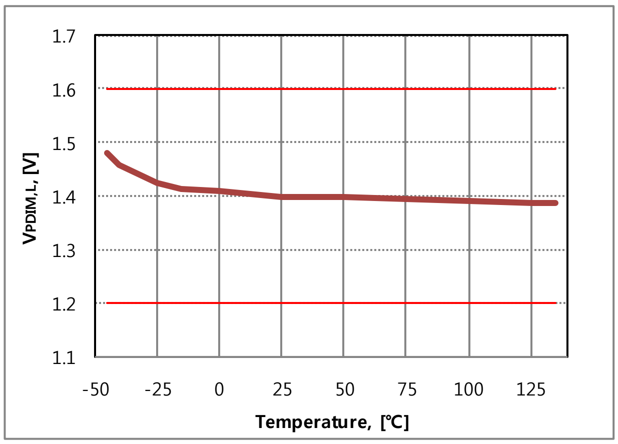


Figure 17. PWM Dimming Input Low Voltage vs. Temperature

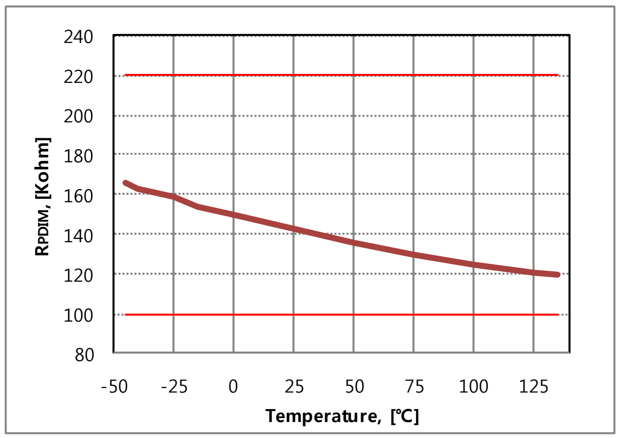


Figure 18. PWM Dimming Pull-Down Resistance vs. Temperature

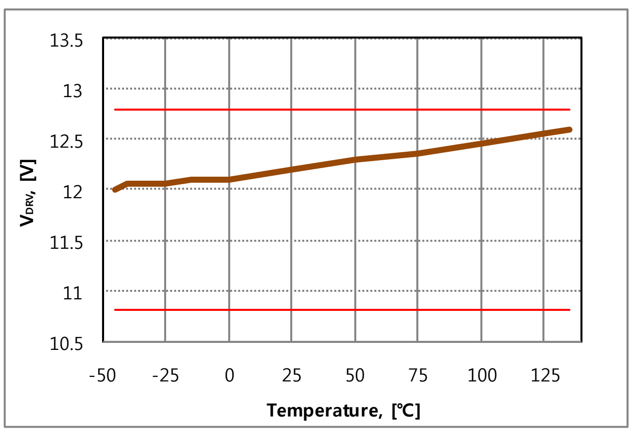


Figure 19. Gate Output Voltage vs. Temperature

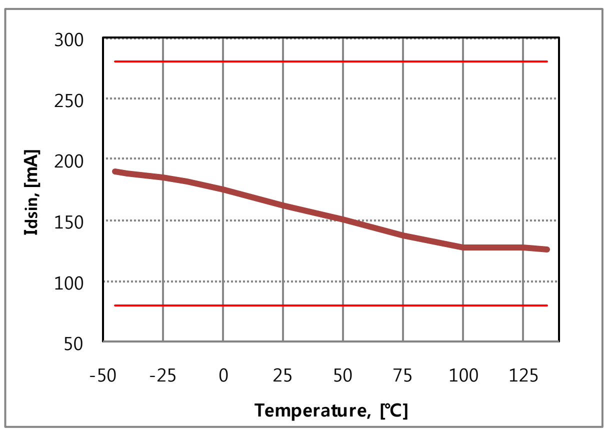


Figure 20. Gate Output Drive Sink Current vs. Temperature

Typical Performance Characteristics (Continued)

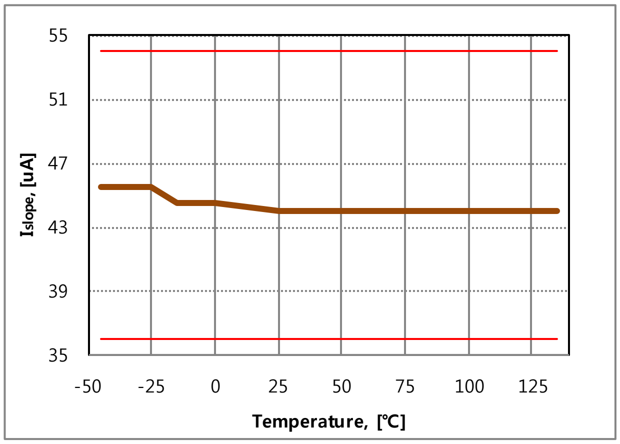


Figure 21. Ramp Generator Current vs. Temperature

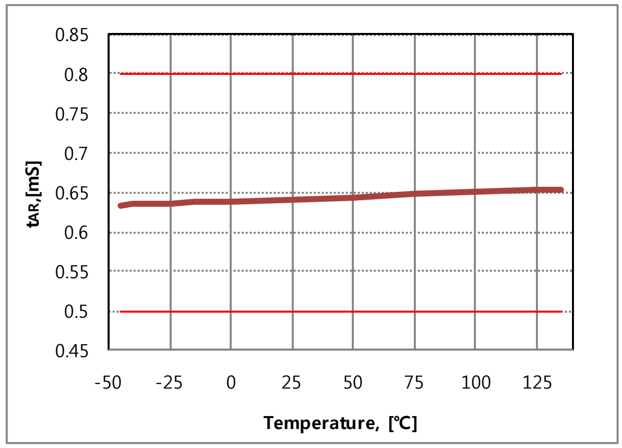


Figure 22. Auto-Restart Time for OCP vs. Temperature

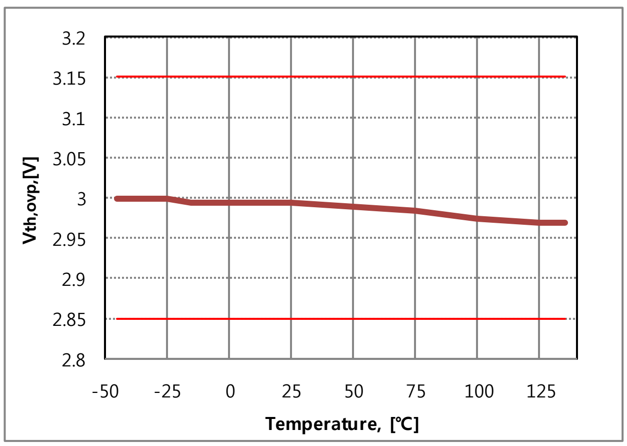


Figure 23. OVP Threshold Voltage vs. Temperature

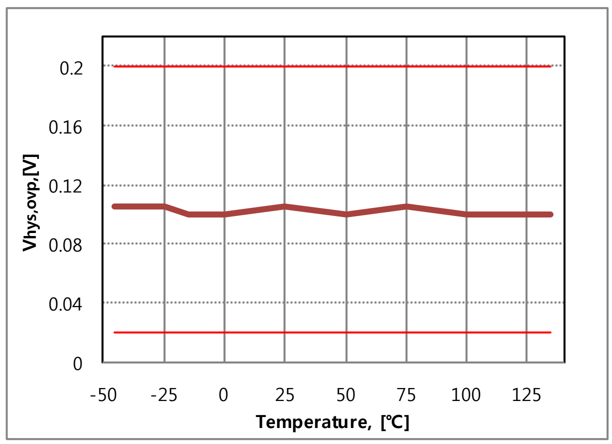


Figure 24. OVP Hysteresis Voltage vs. Temperature

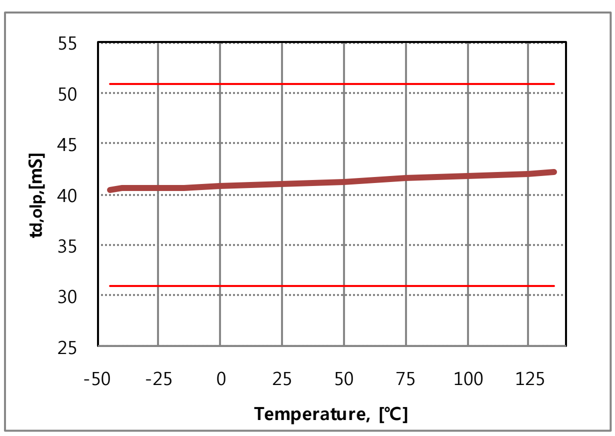


Figure 25. Delay for Over-Current Protection vs. Temperature

Functional Description

The FAN7340 operates as a constant-current source for driving high-current LEDs. It uses Current-Mode control with programmable slope compensation to prevent sub-harmonic oscillation.

The IC provides protections such as open-LED protection, over-voltage protection, and over-current protection for improved system reliability. The IC internally generates a FAULT OUT signal with a delay in case an abnormal LED string condition occurs. PWM dimming and analog dimming functions can be implemented independently. Internal soft-start prevents inrush current flowing into output capacitor at startup. Circuit operation is explained in the following sections.

V_{CC} Under-Voltage Lockout (UVLO)

An internal regulator provides the regulated 5 V used to power the IC. The Under-Voltage Lockout (UVLO) turns off the IC in the event of the voltage dropping below the specific threshold level. The UVLO circuit inhibits powering the IC until a voltage reference is established, up to predetermined threshold level.

Enable

Applying voltage higher than 1.22 V (typical) to the ENA pin enables the IC. Applying voltage lower than 1.15 V (typical) to the ENA pin disables the IC. If ENA pin voltage is higher than 1.22 V (typical) and V_{CC} is higher than 9.0 V (typical.), the IC starts to supply 5 V reference voltage from V_{CC}.

Oscillator (Boost Switching Frequency)

Boost switching frequency is programmed by the value of the resistor connected from the RT pin to ground. RT pin voltage is set to 2 V. The current through the RT pin resistor determines boost switching frequency according to formula:

$$f_{OSC} = \frac{1}{(46.5 \times RT[k\Omega] + 350) \times 10^{-6}} [kHz] \quad (1)$$

Soft-Start Function at Startup

During initial startup, the switching device can be damaged due to the over-current coming from the input line by the negative control. This can result in the initial overshoot of the LED current. Therefore, during initial startup, the soft-start control gradually increases the duty cycle so that the output voltage can rise smoothly to control inrush current and overshoot.

FAN7340 adapts the soft-start function in the boost converter stage. During soft-start period, boost switch turn-on duty is limited by clamped CMP voltage. The soft-start period is dependent on boost switching frequency, which is decided by the RT resistor (Equation (1)). Soft-start period is set to be cumulative time when the BDIM (PWM dimming) signal is HIGH:

$$T_{SS} = 600 / f_{OSC} [sec] \quad (2)$$

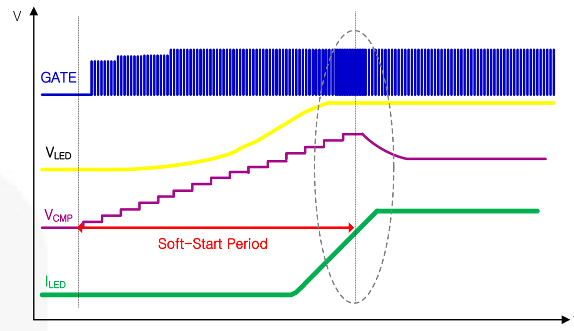


Figure 26. Soft-Start Waveforms

LED Current Setting

During the boost converter operating periods, the output LED current can be set by equation:

$$I_{LED} = \frac{ADIM(V)}{R_{SENSE} + 60m\Omega} \quad (3)$$

where ADIM(V) is ADIM pin applied voltage and, R_{SENSE} is the sensing resistor value. An additional 60 mΩ comes from an internal wire bonding resistor. To calculate LED current precisely, consider the wire bonding resistor.

Analog Dimming and PWM Dimming

Analog dimming is achieved by varying the voltage level at the ADIM pin. This can be implemented either with a potentiometer from the VREF pin or from an external voltage source and a resistor divider circuit. The ADIM voltage level is adjusted to be the same as the feedback level (V_{SENSE}). A V_{ADIM} range from 0.3 V to 3 V is recommended.

PWM dimming (BDIM) helps achieve a fast PWM dimming response in spite of the shortcomings of the boost converter. The PWM dimming signal controls three nodes in the IC; gate signal to the switching FET, gate signal to the dimming FET, and output connection of the trans-conductance amplifier. When the PWM dimming signal is HIGH, the gates of the switching FET and dimming FET are enabled. At the same time, the output of the transconductance ap-amp is connected to the compensation network. This allows the boost converter to operate normally.

Dynamic Contrast Ratio

The Dynamic Contrast Ratio (DCR) means the maximum contrast ratio achievable by adjusting the amount of light (dimming) of the screen instantaneously using the backlight during the extremely short period of time. FAN7340 can normally drive the LED backlight under 0.1% dimming duty cycle at 200 Hz dimming frequency. Even operating at 5 µs-dimming FET turn-on time and extremely low dimming duty, FAN7340 can operate LEDs with normal peak current level.

Internal Dimming MOSFET

A dimming MOSFET (400 V N-channel MOSFET; such as FDD3N40) is incorporated in the FAN7340. The power transistor is produced using Fairchild's proprietary, planar stripe, DMOS technology. This advanced technology is tailored to minimize on-state resistance ($R_{DS(on)}$=3.4 Ω), to provide superior switching performance. This device is suited for high-efficiency SMPS and shows desirable thermal characteristic during operation. To prevent initial LED current overshoot at low V_{ADIM} levels, gate resistance of the internal dimming FET is designed as 5 kΩ experimentally.

Feedback Loop Compensation

Stable closed-loop control can be accomplished by connecting a compensation network between COMP and GND. The compensation needed to stabilize the converter can be either a Type-I circuit (a simple integrator) or a Type-II circuit (and integrator with and additional pole-zero pair). The type of the compensation circuit required is dependent on the phase of the power stage at the crossover frequency.

FAN7340 adopts a Type-II compensator circuit.

Programmed Current Control

FAN7340 uses a Current-Mode control method. Current-Mode control loops: an outer feedback loop that senses output voltage (current) and delivers a DC control voltage to an inner feedback loop, which senses the peak current of the inductor and keeps it constant on a pulse-by-pulse basis. One of the advantages of the Current-Mode control is line/load regulation, which is corrected instantaneously against line voltage changes without the delay of an error amplifier.

Programmable Slope Compensation

When the power converter operates in Continuous Conduction Mode (CCM), the current programmed controller is inherently unstable when duty is larger than 50%, regardless of the converter topology. The FAN7340 uses a Peak-Current-Mode control scheme with programmable slope compensation and includes an internal transconductance amplifier to accurately control the output current over all line and load conditions.

An internal R_{slope} resistor (5 kΩ) connected to sensing resistor R_S and an external resistor R_1 can control the slope of V_{SC} for the slope compensation. Although the normal operating mode of the power converter is DCM, the boost converter operates in CCM in the case of rapid LED current increase. As a result, slope compensation circuit is an important feature.

The value of an external series resistor (R_1) can be programmed by the user. In normal DCM operation, 5 kΩ is recommended.

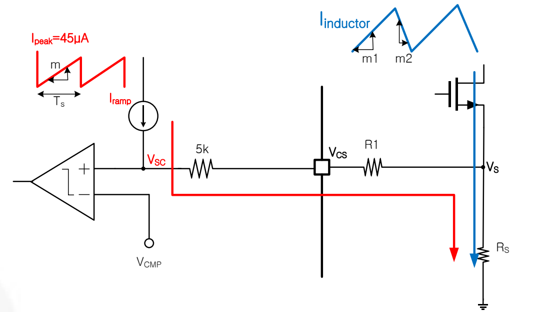


Figure 27. Slope Compensation Block Diagram

Cycle-by-Cycle Over-Current Protection

In boost topology, the switch can be damaged in abnormal conditions (inductor short, diode short, output short). It is always necessary to sense the switch current to protect against over-current failures. Switch failures due to excessive current can be prevented by limiting I_d.

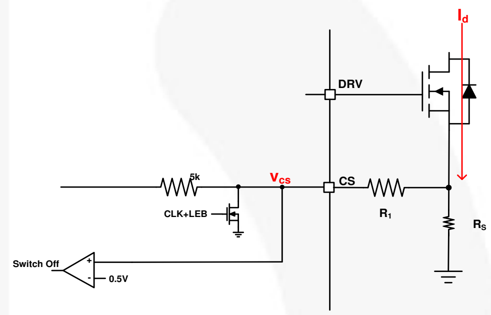


Figure 28. Cycle-by-Cycle OCP Circuit

When the voltage drops at R_1 and R_S exceed a threshold of approximately 0.5 V, the power MOSFET over-current function is triggered after minimum turn-on time or LEB time (300 ns).

The peak voltage level at CS terminal:

$$V_{cs\_peak} = 45\mu \times (R_1 + R_s) \times DT_s + i_d \times R_s \qquad (4)$$

Choose the boost switch current-sensing resistor (R_{CS}):

$$R_{CS} \geq \frac{0.25}{i_{L\_peak}} \qquad (5)$$

Open-LED Protection (OLP)

After the first PWM dimming-HIGH signal, the feedback sensing resistor (RSENSE) starts sensing the LED current. If the feedback voltage of the SENSE pin drops below 0.2 V, the OLP triggers to generate an error flag signal. Because OLP can be detected only in PWM dimming-HIGH; if OLP detecting time is over 5 μs, PWM dimming signal is pulled HIGH internally regardless of external dimming signal. If OLP signal continues over blanking time, an error flag signal is triggered.

OLP blanking time is dependent on boost switch frequency per Equation (6). FAULT OUT signal is made through the FO pin, which needs to be connected 5 V reference voltage through a pull-up resistor. In normal operation, FO pin voltage is pulled down to ground. In OLP condition, FO pin voltage is pulled HIGH.

$$t_{d.olp} = 8192 / f_{OSC} \text{ [sec]} \qquad (6)$$

In system operation, OLP is triggered in only direct-short condition. Direct short means that some point of the LED string is shorted to set ground. In direct-short condition, the boost controller cannot control the LED current and a large current flows into the LED string directly from input power. To prevent this abnormal condition, the FO signal is used to turn off input power or the total system. FO signal is only triggered in OLP condition.

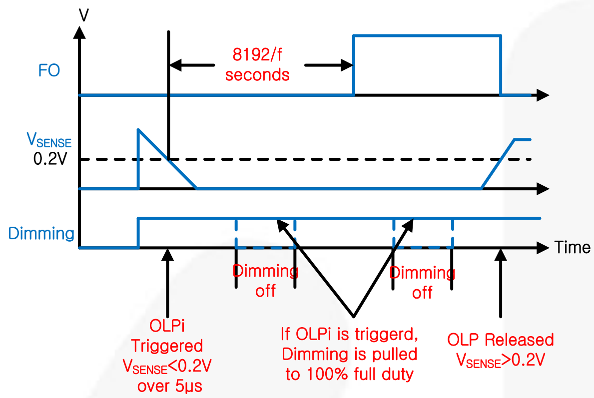


Figure 29. Open-LED Protection

In LED open load condition, OVP is triggered ahead of OLP.

Over-Voltage Protection (OVP)

Over-voltage protection is triggered when the voltage of the external output voltage trip point meets 3 V. After triggering OVP, the dimming switch and boost switch are turned off. The protection signal is recovered when the output voltage divider is below 2.9 V.

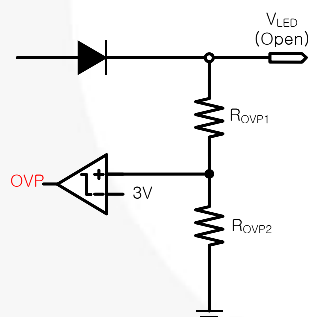


Figure 30. Over-Voltage Trip Point

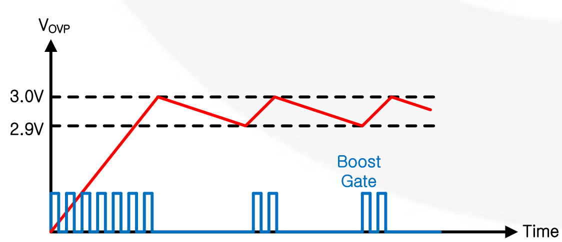


Figure 31. OVP Trigger and Release

LED Over-Current Protection (OCP)

The primary purpose of the over-current protection function is to protect the internal dimming MOSFET from excessive current. The OCP is triggered when the feedback voltage meets the clamping level (1.4 V ~ 4 V) of the ADIM voltage x4. At 1 µs delay after the OCP is triggered, the IC turns off both the boost FET and dimming FET and restarts the gate signal every t_{AR} automatically. t_{AR} can be calculated as:

$$\mathbf{t_{AR}} = 128 / f_{OSC}\ [sec] \tag{7}$$

1. When V_{ADIM}=0.3 V (V_{ADIM}x4=1.2 V).
2. OCP threshold level is set to 1.4 V.
3. OCP is triggered at feedback voltage level = 1.4 V.

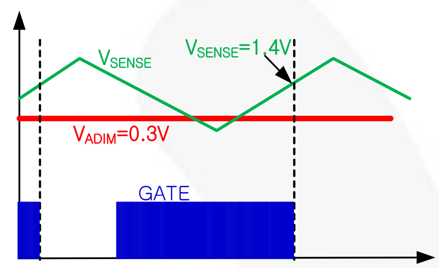


Figure 32. OCP Waveforms at V_{ADIM}=0.3 V

1. When V_{ADIM}=0.8 V (V_{ADIM}x4=3.2 V).
2. OCP threshold level is set to 3.2 V.
3. OCP is triggered at V_{SENSE} = 3.2 V.

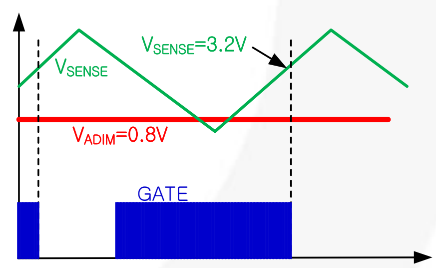


Figure 33. OCP Waveforms at V_{ADIM}=0.8 V

1. When V_{ADIM}=1.2 V (V_{ADIM}x4=4.8 V).
2. OCP threshold level is set to 4.0 V.
3. OCP is triggered at V_{SENSE} = 4.0 V.

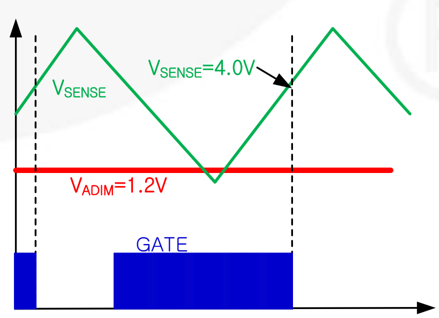


Figure 34. OCP Waveforms at V_{ADIM}=1.2 V

Typical Application Circuit (Boost Topology for LED Backlight)

Application	Input Voltage Range	Rated Output Power	Output current (Rated Voltage)	LED
LED Backlight TV	120 V_{DC} ±10%		250 mA (230 V)	72-LEDs/1-String

Features

- High Efficiency
- Constant Current Boost Converters
- High-Voltage, High-Current LED Driving

Typical Application Circuit

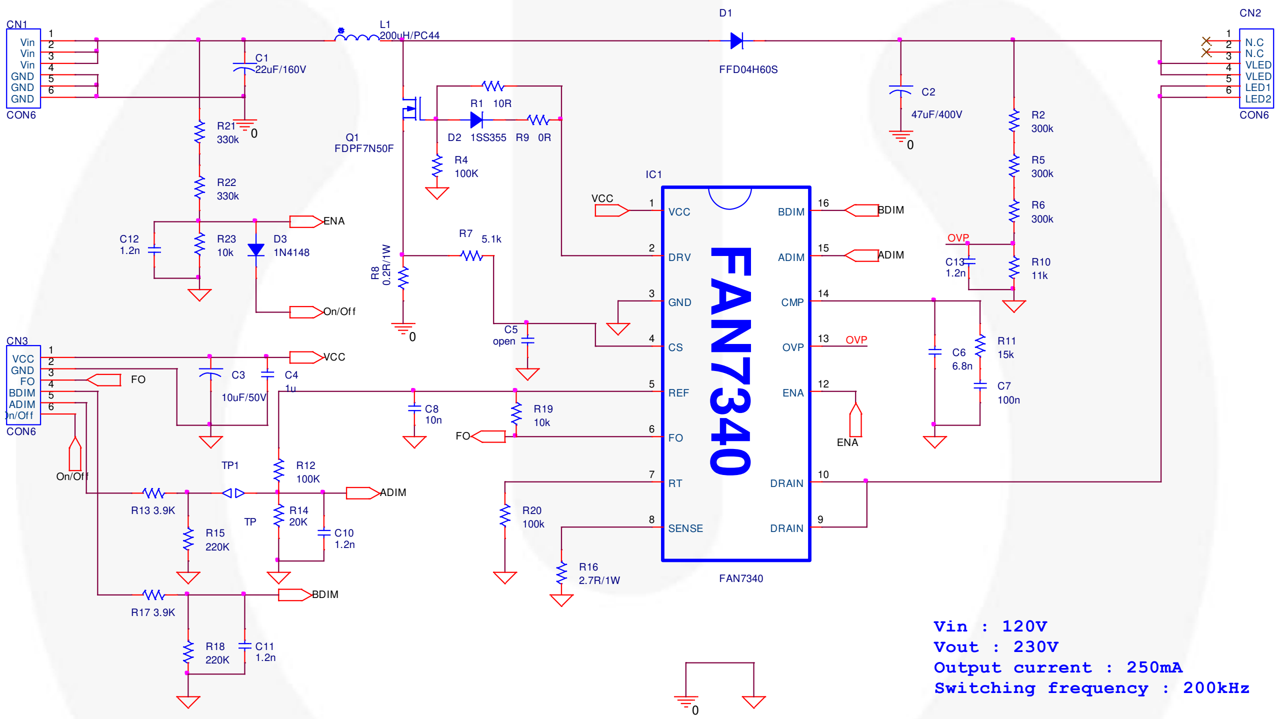


Figure 35. Typical Application Circuit

Physical Dimension

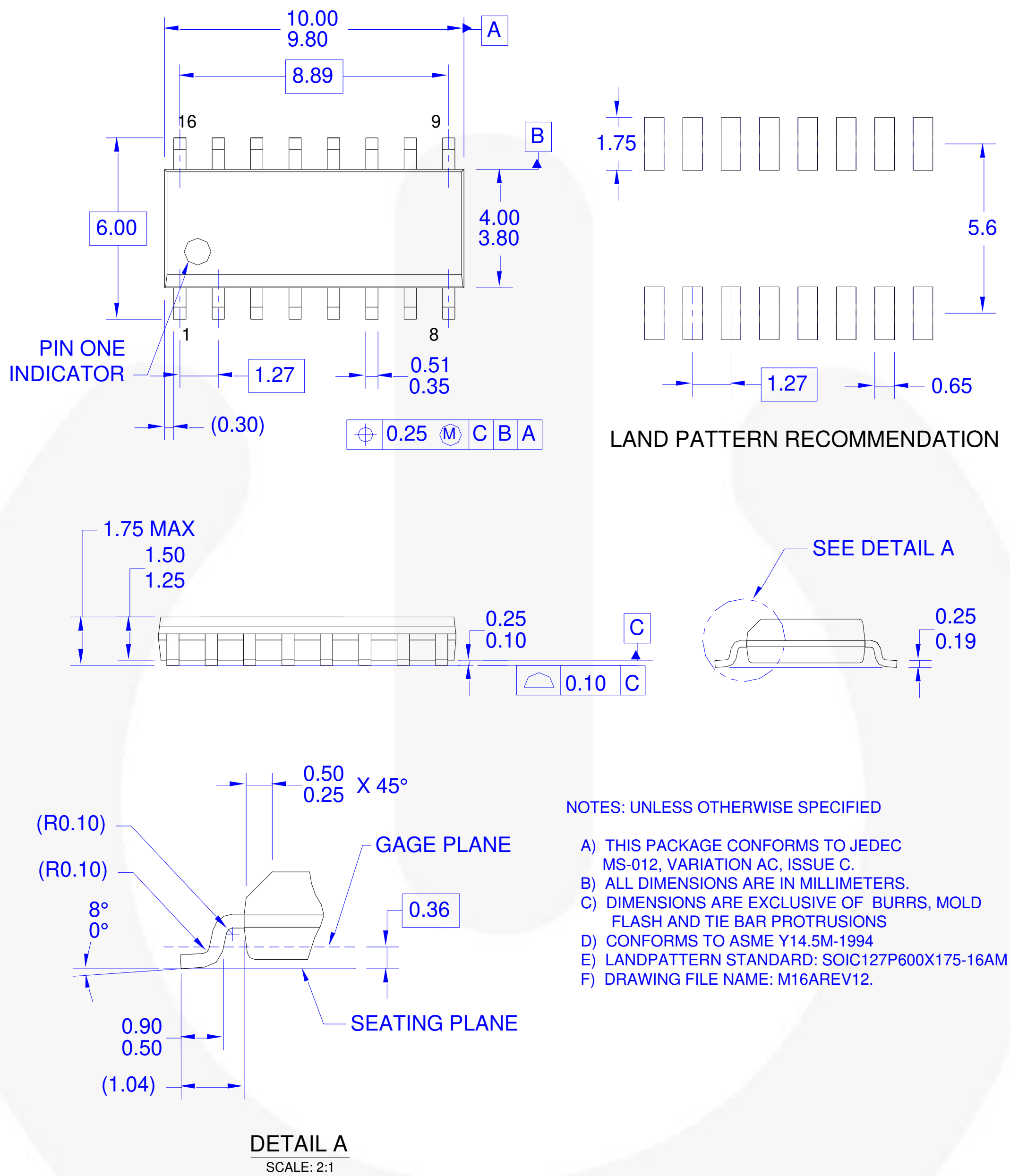


Figure 36. 16-Lead, Small Outline Integrated Circuit (SOIC)

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