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# STA-6033(Z)

## 4.9GHz to 5.9GHz 3.3V POWER AMPLIFIER

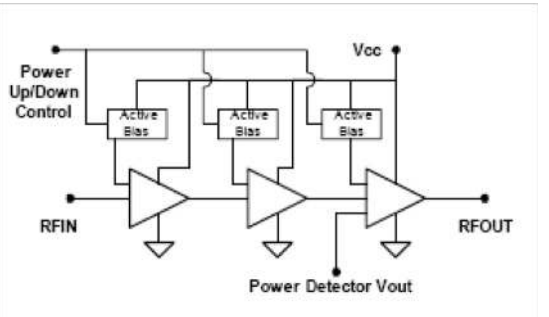
Package: QFN, 16 pin, 3mmx3mm

## Product Description

RFMD's STA-6033 is a high efficiency class AB Heterojunction Bipolar Transistor (HBT) amplifier housed in a low-cost surface-mountable plastic package. This HBT amplifier is made with InGaP on GaAs device technology and fabricated with MOCVD for an ideal combination of low cost and high reliability. This product is specifically designed as a final stage for 802.11a equipment in the 4.9GHz to 5.9GHz band. It can be run from a 3V to 6V supply. Optimized on-chip impedance matching circuitry provides a 50Ω nominal RF input impedance. A single external output allows for matching circuit covers the entire 4.9GHz to 5.9GHz band. The external output match allows for load line optimization for other applications or optimized for other applications or optimized performance over narrower bands. It is designed as a drop in replacement for similar parts in its class. This product is available in RoHS Compliant and Green package with matte tin finish, designated by the "Z" package suffix.

**Optimum Technology Matching® Applied**

- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☑ InGaP HBT
- ☐ SiGe BiCMOS
- ☐ Si BiCMOS
- ☐ SiGe HBT
- ☐ GaAs pHEMT
- ☐ Si CMOS
- ☐ Si BJT
- ☐ GaN HEMT
- ☐ RF MEMS




## Features

- 802.11a 54Mb/s Class AB Performance
- $P_{OUT}$=18dBm at 3% EVM, 3.3V, 210mA
- High Gain=27dB
- Output Return Loss <12dB for Linear Tune
- On-Chip Output Power Detector
- Simultaneous 4.9GHz to 5.9GHz Broadband
- Robust - Survives RF Input Power=+20dBm
- Power Up/Down Control <1µs

## Applications

- 802.11a WLAN, OFDM, 5.8GHz ISM Band
- 802.16 WiMax, Fixed Wireless, UNII

| Parameter | Specification | | | Unit | Condition |
|---|---|---|---|---|---|
| | Min. | Typ. | Max. | | |
| Frequency of Operation | 4900 | | 5900 | MHz | |
| Output Power at 1dB Compression | | 26.5 | | dBm | 4.9GHz |
| | 24.0 | 25.5 | | dBm | 5.875GHz |
| Gain | 27.5 | 29.5 | 31.5 | dB | 4.9GHz |
| | 22.0 | 24.0 | 26.0 | dB | 5.875GHz |
| Output power | | 18.0 | | dBm | 5.15GHz, 3% EVM 802.11a 54Mb/s |
| | | 18.0 | | dBm | 5.875GHz |
| Third Order Intermod | | -38.0 | -34.0 | dBc | 5.875MHz, $P_{OUT}$=15dBm per tone |
| Noise Figure, (NF) | | 5.7 | | dB | 5.875GHz |
| Worst Case Input Return Loss | 11.0 | 15.0 | | dB | 4.9GHz to 5.875GHz |
| Worst Case Output Return Loss | 8.0 | 12.0 | | dB | 4.9GHz to 5.875GHz |
| Output Voltage Range | | 0.8 to 1.5 | | V | $P_{OUT}$=7dBm to 23dBm |
| $V_{CC}$ Quiescent Current | 130 | 165 | 190 | mA | |
| Power Up Control Current | | 1.5 | | mA | $V_{PC}$=3.3V ($I_{VPC1}$+$I_{VPC2}$+$I_{VPC3}$) |
| Off $V_{CC}$ Leakage Current | | 5 | 100 | uA | $V_{PC}$=0V |
| Thermal Resistance | | 28 | | °C/W | junction - lead |

Test Conditions: $Z_O$=50Ω, $V_{CC}$=$V_{PC}$=3.3V, $I_{CQ}$=165mA, $T_{BP}$=30°C





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## Absolute Maximum Ratings

| Parameter | Rating | Unit |
|---|---|---|
| VC3 Collector Bias Current (pin 14) | 400 | mA |
| VC2 Collector Bias Current (pin 15) | 140 | mA |
| VC1 Collector Bias Current (pin 16) | 50 | mA |
| Device Voltage ($V_D$) | 4.5 | V |
| Power Dissipation | 1.4 | W |
| Operating Lead Temperature ($T_L$) | -40 to +85 | °C |
| RF Input Power for 50Ω load | 20 | dBm |
| Storage Temperature Range | -40 to +150 | °C |
| Operating Junction Temperature ($T_J$) | 150 | °C |
| ESD Rating - Human Body Model, Class 1C (HBM) | 1000 | V |

Operation of this device beyond any one of these limits may cause permanent damage. For reliable continuous operation, the device voltage and current must not exceed the maximum operating values specified in the table on page one.

Bias Conditions should also satisfy the following expression:

$I_D V_D < (T_J - T_L) / R_{TH, j\text{-}l}$

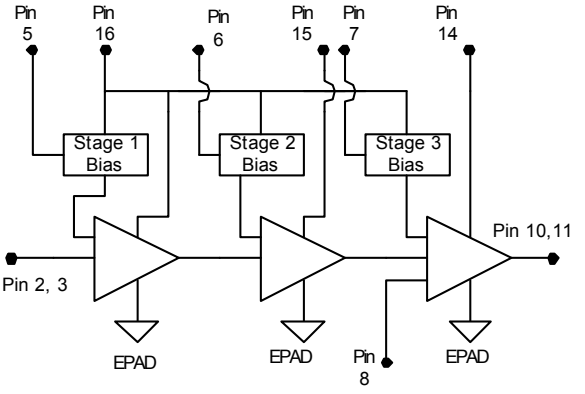
**Caution!** ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EUDirective2002/95/EC (at time of this document revision).



## Simplified Device Schematic



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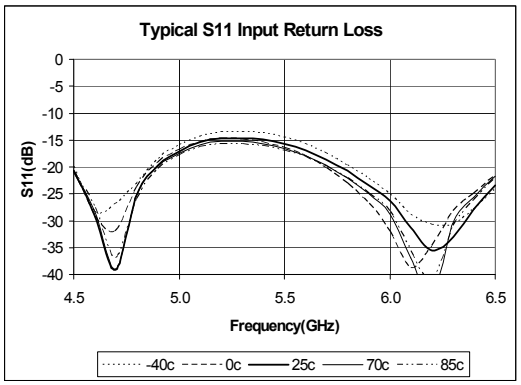
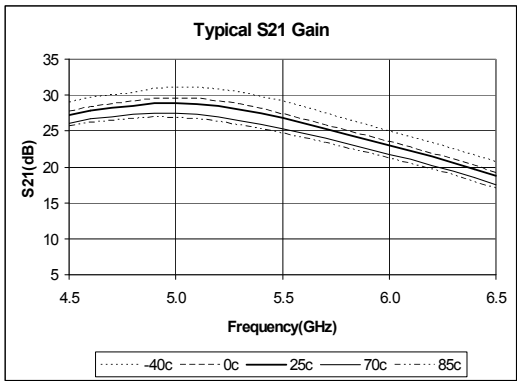
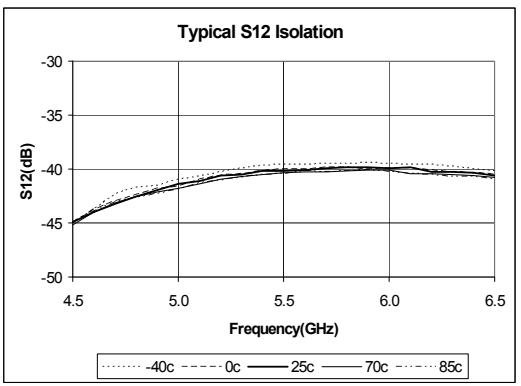
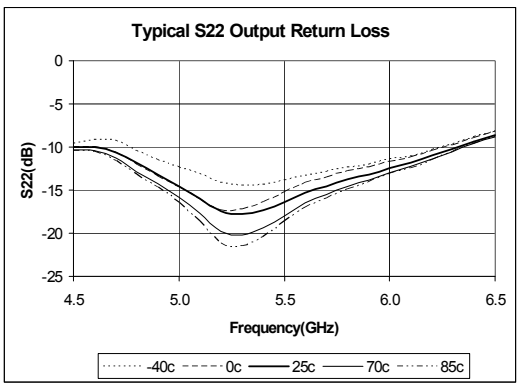
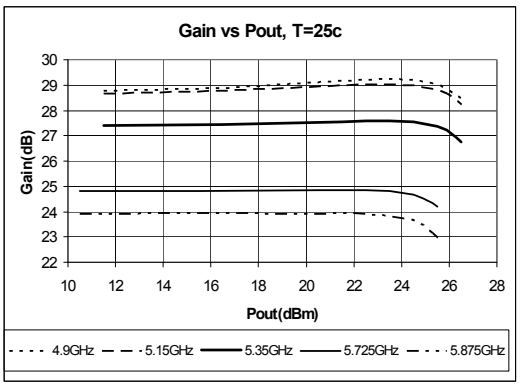
### 4.9 - 5.9 GHz Evaluation Board Data (Vcc = Vpc = 3.3V, $I_q$ = 165mA)

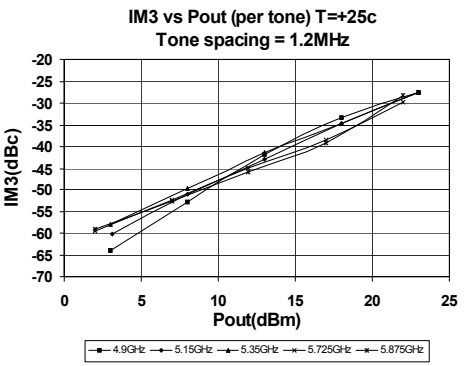


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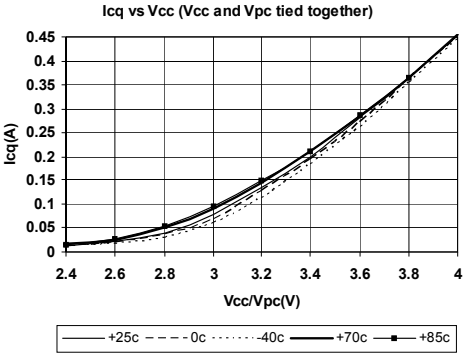


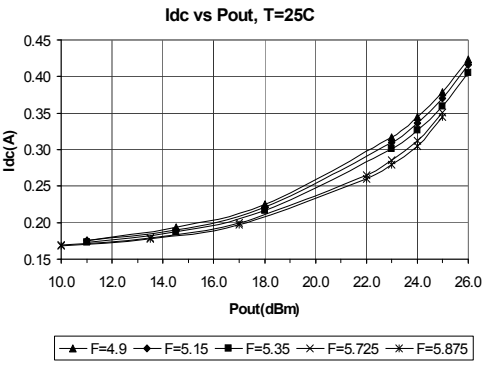


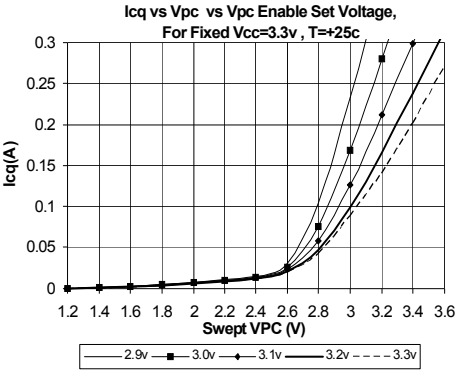


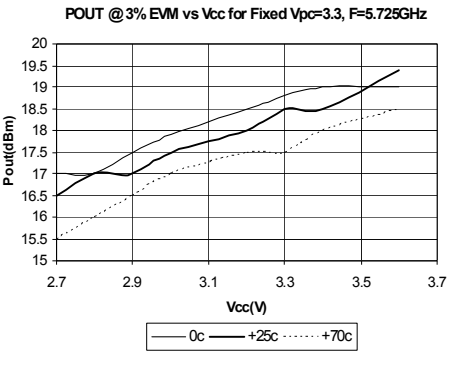


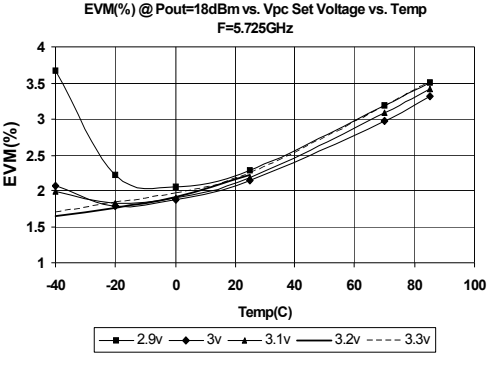


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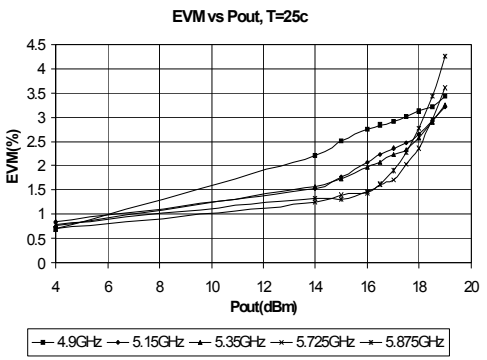
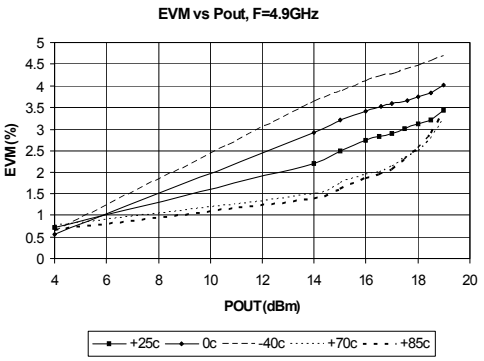
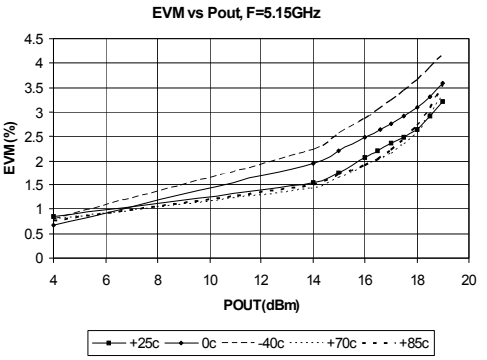
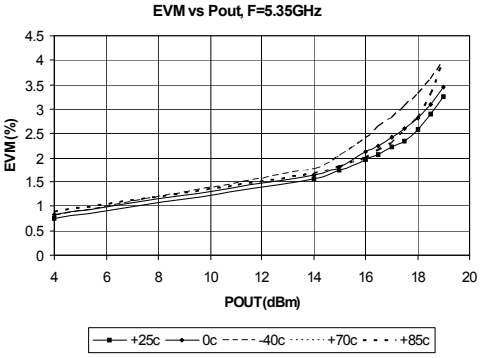
### 4.9 - 5.9 GHz Evaluation Board Data (Vcc = Vpc = 3.3V, $I_q$ = 165mA)

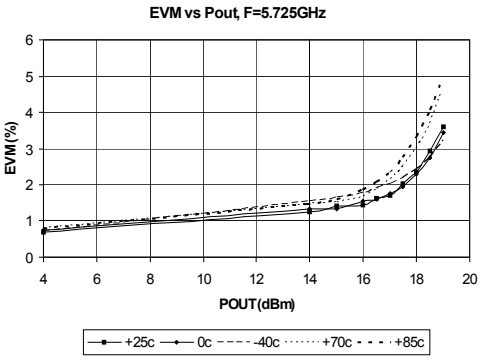
802.11a EVM, OFDM, 54Mb/s, 64QAM

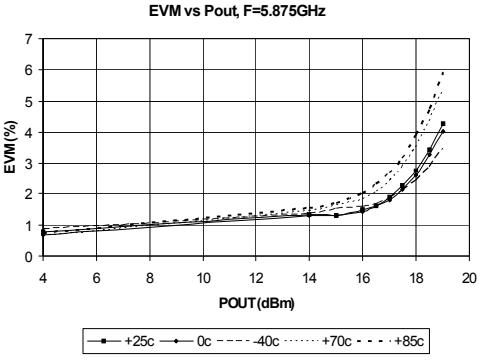


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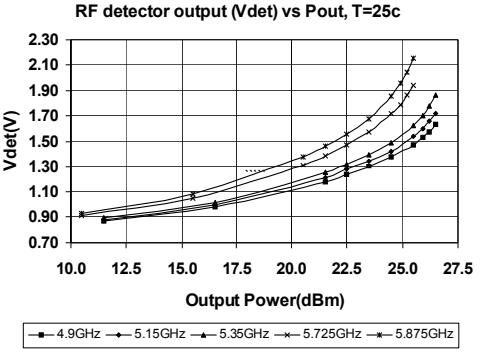


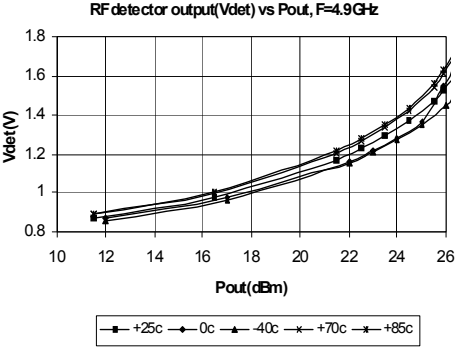


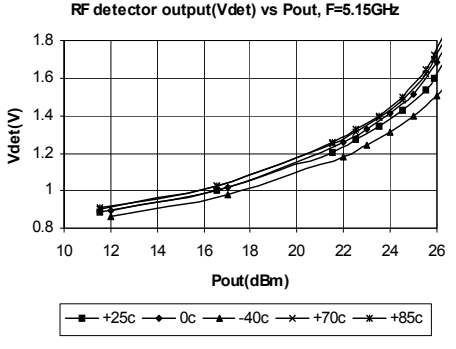


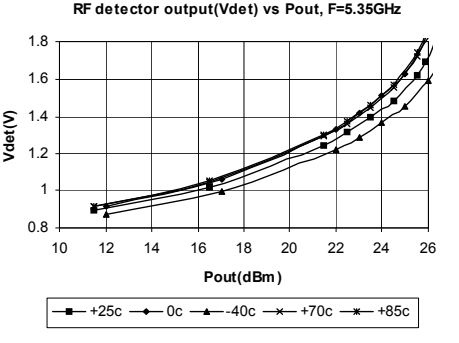


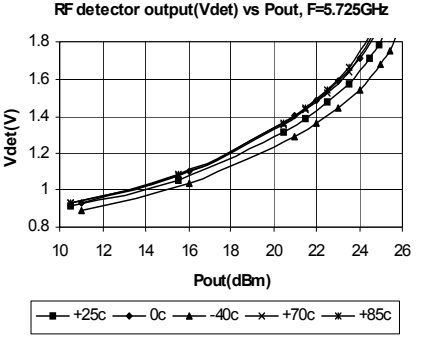


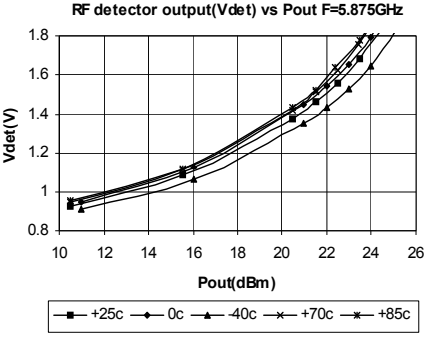




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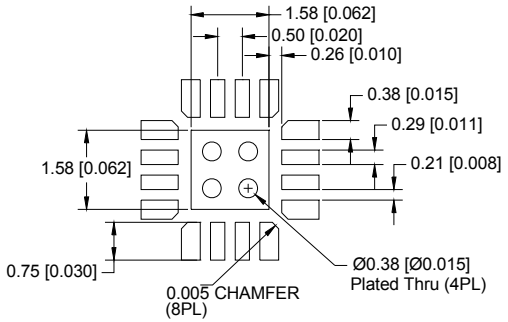
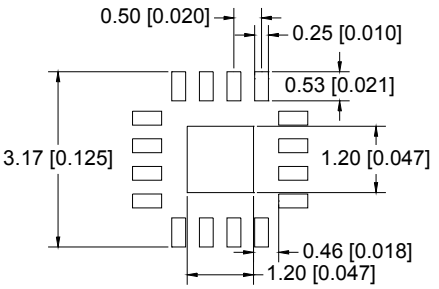
| Pin | Function | Description |
|---|---|---|
| 1, 4, 9, 12, 13 | N/C | Pins are not used. May be grounded, left open, or connected to adjacent pin. |
| 5 | VPC1 | VPC1 is the bias control pin for the stage 1 active bias circuit. An external series resistor is required for proper setting of bias levels. Refer to the evaluation board schematic for resistor value.To prevent potential damage, do not apply voltage to this pin that is +1V greater than voltage applied to pin 16 (Vbias) unless Vpc supply current capability is less than 10mA. |
| 6 | VPC2 | VPC2 is the bias control pin for the stage 2 active bias circuit. An external series resistor is required for proper setting of bias levels. Refer to the evaluation board schematic for resistor value.To prevent potential damage, do not apply voltage to this pin that is +1V greater than voltage applied to pin 16 (Vbias) unless Vpc supply current capability is less than 10mA. |
| 7 | VPC3 | VPC3 is the control pin for the stage 3 active bias circuits. An external series resistor is required for proper setting of bias levels. Refer to the evaluation board schematic for resistor value.To prevent potential damage, do not apply voltage to this pin that is +1V greater than voltage applied to pin 16 (Vbias) unless Vpc supply current capability is less than 10mA. |
| 8 | Vdet | Output power detector voltage. Load with 10K to 100KΩ to ground for best performance. |
| 2, 3 | RFIN | RF input pins. This is DC grounded internal to the IC. Do not apply voltage to this pin. All three pins must be used for proper operation. |
| 10, 11 | RFOUT | RF output pin. This is also another connection to the 3rd stage collector |
| 14 | VC3 | 3rd stage collector bias pin. Apply 3.0V to 3.6V to this pin. |
| 15 | VC2 | 2nd stage collector bias pin. Apply 3.0V to 3.6V to this pin. |
| 16 | VC1,Vbias | 1st stage collector bias pin and active bias network VCC. Apply 3.0V to 3.6V to this pin. |
| EPAD | Gnd | Exposed area on the bottom side of the package needs to be soldered to the ground plane of the board for optimum thermal and RF performance. Several vias should be located under the EPAD as shown in the recommended land pattern). |

## Land Pattern and PCB Soldermask

**Recommended Land Pattern (dimensions in mm[in].):**

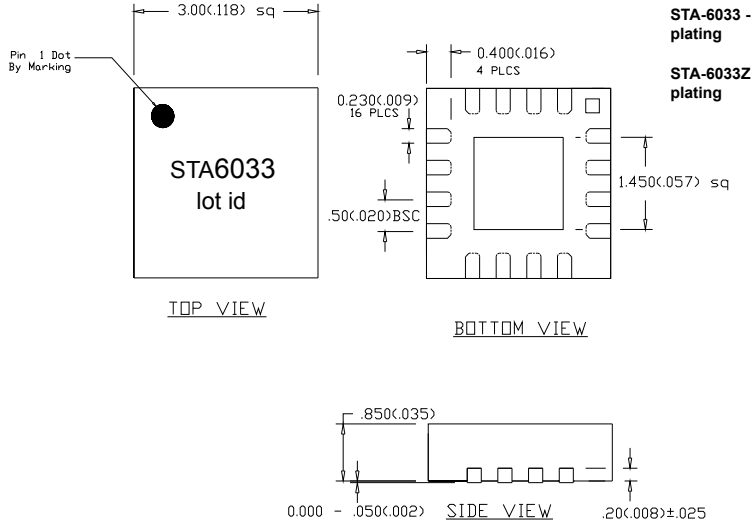



**Recommended PCB Soldermask (SMOBC) for Land Pattern(dimensions in mm[in]):**



## Package Drawing

Dimensions in millimeters (inches)
Refer to drawing posted at www.rfmd.com for tolerances.

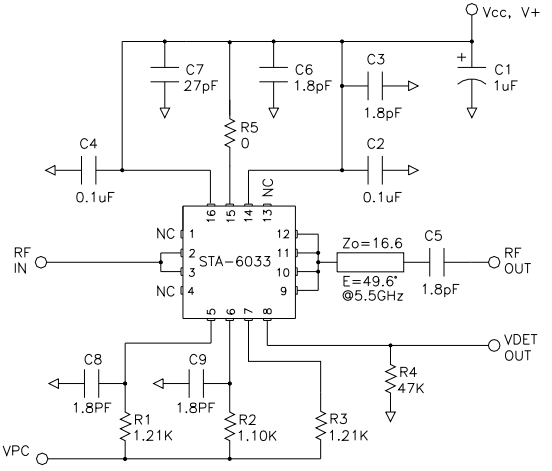



**STA-6033 - 85/15 Sn/Pb plating**

**STA-6033Z - Matte Sn plating**

## Evaluation Board Schematic

**4.9 - 5.9 GHz Evaluation Board Schematic For Vcc = Vpc = V+ = 3.3V Supply**




**Notes:**

R5 (0 ohm jumper) is required for parasitic inductance (~0.4nH).

R4 simulates external circuit loading to ground. Recommended load range is 47K-100K ohms.

Pins 1,4,9,12,13 are unwired (N/C) inside the package. Refer to page 2 for detailed pin descriptions. Some of these pins are wired to adjacent pins or grounded as shown in the application circuit. This is to maintain consistency with the evaluation board layout shown below. It is recommended to use this layout and wiring to achieve the specified performance.

To prevent potential damage, do not apply voltage to the Vpc pin that is +1V greater than voltage applied to pin 16 (Vbias/Vcc) unless Vpc supply current capability is less than 10 mA.

See table below for other Vpc logic level resistor values.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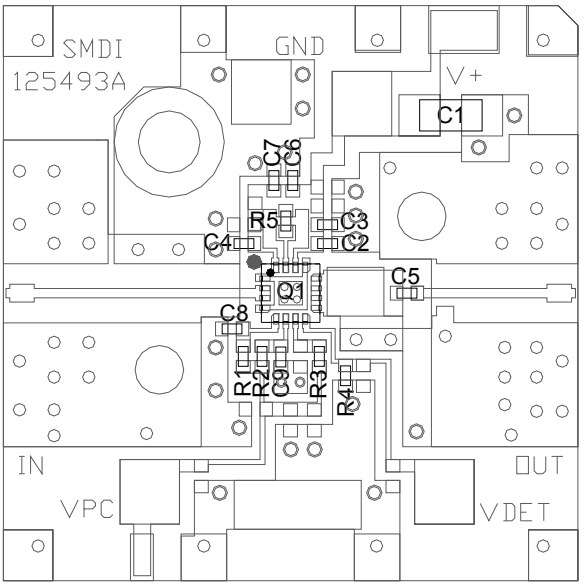
## Evaluation Board Layout

### 4.9 - 5.9 GHz Evaluation Board Layout For Vcc = Vpc = V+ = 3.3V Supply

- Board material GETEK, 10mil thick, Dk=3.9, 2 oz. copper finish




| DESG | DESCRIPTION |
|---|---|
| Q1 | STA-6033 |
| R1 | 1.21K OHM, 1% 0402 |
| R2 | 1.10K OHM, 1%, 0402 |
| R3 | 1.21K OHM, 1% 0402 |
| R4 | 47K OHM, 0402 |
| R5 | 0 OHM, 0402 |
| C1 | 1uF CERAMIC, 1206 |
| C2,4 | 0.1uF CAP, 0402 |
| C3,5,6,8,9 | 1.8pF CAP, 0402 |
| C7 | 27pF CAP, 0402 |

Resistor Table for Vcc=3.3V
(1% values are recommended)

| VPC(V) | R1(ohm) | R2(ohm) | R3(ohm) |
|---|---|---|---|
| 2.9 | 374 | 237 | 100 |
| 3.0 | 562 | 464 | 374 |
| 3.1 | 750 | 665 | 619 |
| 3.2 | 1K | 887 | 909 |
| 3.3 | 1.21K | 1.10K | 1.21K |

## Ordering Information

| Part Number | Reel Size | Devices/Reel |
|---|---|---|
| STA6033 | 13” | 3000 |
| STA6033Z | 13” | 3000 |
| STA6033ZPCK-EVB1 | Fully assembled evaluation board tuned for 4.9 to 5.9GHz and 5 piece loose samples | |

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