ANALOG DEVICES

Wide-Bandwidth Precision Operational Amplifier ($A_V \geq 10$)

OP-61

FEATURES

- High Gain-Bandwidth Product .... 200MHz Typ
- Low Voltage Noise .... 3.4nV/$\sqrt{Hz}$ @ 1kHz
- High Speed .... 45V/µs Typ
- Fast Settling Time (0.01%) .... 330ns Typ
- High Gain .... 475V/mV Typ
- Low Offset Voltage .... 100µV Typ

APPLICATIONS

- Low Noise Preamplifier
- Wideband Signal Conditioning
- Pulse/RF Amplifiers
- Wideband Instrumentation Amplifiers
- Active Filters
- Fast Summing Amplifiers

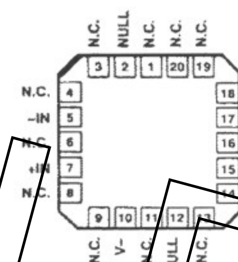
GENERAL DESCRIPTION

The OP-61 is a wide-bandwidth, precision operational amplifier designed to meet the requirements of fast, precision instrumentation systems. The OP-61's combination of DC accuracy with high bandwidth, fast slew rate and low noise, makes it unique among high-speed amplifiers. It is ideal for wideband systems requiring high signal-to-noise ratio, such as fast 12-16 bit data acquisition systems. The OP-61 maintains less than 3nV/$\sqrt{Hz}$ of input referred spot voltage noise over its closed-loop bandwidth.

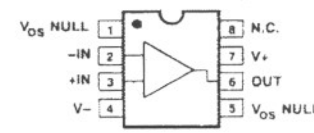
The OP-61 offers noise and gain performance similar to that of the industry standard OP-27/37 amplifiers, but maintains a much larger gain-bandwith product of 200MHz. With slew rate exceeding 45V/µs, and settling time for 12 bits (0.01%) typically 330ns, the OP-61 has excellent dynamic accuracy.

The OP-61 is an excellent upgrade for circuits using slower op amps such as the HA-5111, and the HA-5147. The OP-61 can also be used as a high-speed alternative to the HA-5101, HA-5127, HA-5137, OP-27, and OP-37 amplifiers, where closed-loop gains are greater than 10.

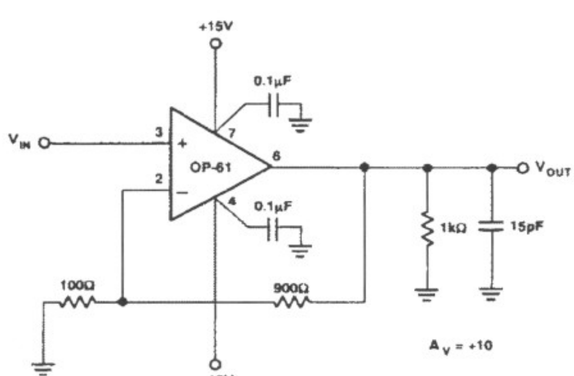
PIN CONNECTIONS

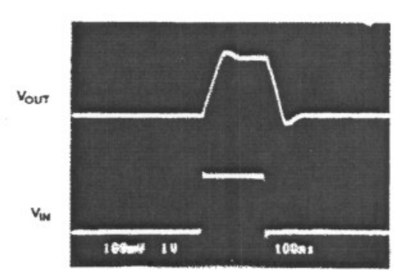


OP-61 ARC/883
20-CONTACT LCC
(RC-Suffix)



EPOXY MINI-DIP
(P-Suffix)
8-PIN CERDIP (Z-Suffix)
8-PIN SO (S-Suffix)





OP-61

ORDERING INFORMATION †

PACKAGE			OPERATING TEMPERATURE RANGE
CERDIP 8-PIN	PLASTIC 8-PIN	LCC 20-CONTACT	
OP61AZ*	–	OP61ARC/883*	MIL
OP61FZ	OP61GP	–	XIND
–	OP61GS	–	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, and plastic DIP packages.

ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage .... ±18V
Differential Input Voltage .... ±5.0V
Input Voltage .... Supply Voltage
Output Short-Circuit Duration .... Continuous
Storage Temperature Range
P, RC, S, Z Package .... –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) .... 300°C
Junction Temperature (T_j) .... 150°C
Operating Temperature Range
All A Grades .... –55°C to +125°C
F & G Grades .... –40°C to +85°C

PACKAGE TYPE	Θ_{jA} (Note 1)	Θ_{jC}	UNIT
8-Pin Hermetic DIP (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
20-Contact LCC (RC)	98	38	°C/W
8-Pin SO (S)	158	43	°C/W

NOTES:
1. Θ_{jA} is specified for worst case mounting conditions, i.e., Θ_{jA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; Θ_{jA} is specified for device soldered to printed circuit board for SOpackage.
2. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-61A MIN	OP-61A TYP	OP-61A MAX	OP-61F MIN	OP-61F TYP	OP-61F MAX	OP-61G MIN	OP-61G TYP	OP-61G MAX	UNITS
Input Offset Voltage	V_{OS}		–	100	500	–	150	750	–	200	1000	μV
Input Offset Current	I_{OS}	V_{CM} = 0V	–	30	150	–	40	200	–	40	200	nA
Input Bias Current	I_B	V_{CM} = 0V	–	130	500	–	200	600	–	200	600	nA
Input Noise Voltage Density	e_n	f_O = 1000Hz	–	3.4	–	–	3.4	–	–	3.4	–	nV/√Hz
Input Noise Current Density	i_n	f_O = 10kHz	–	1.7	–	–	1.7	–	–	1.7	–	pA/√Hz
Input Voltage Range	IVR	(Note 1)	±11.0	–	–	±11.0	–	–	±11.0	–	–	V
Common-Mode Rejection	CMR	V_{CM} = ±11V	100	108	–	94	100	–	94	100	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±5V to ±18V	–	1.2	4.0	–	2.0	5.6	–	2.0	5.6	μV/V
Large-Signal Voltage Gain	A_{VO}	R_L = 10kΩ	225	475	–	175	425	–	175	425	–	V/mV
		R_L = 2kΩ	200	400	–	150	350	–	150	350	–	
		R_L = 1kΩ	150	340	–	120	300	–	120	300	–	
Output Voltage Swing	V_O	R_L = 1kΩ	±12.0	±13.2	–	±12.0	±13.2	–	±12.0	±13.2	–	V
		R_L = 500Ω	±11.0	±12.8	–	±11.0	±12.8	–	±11.0	±12.8	–	
Slew Rate	SR	R_L = 1kΩ, C_L = 50pF	40	45	–	35	45	–	35	45	–	V/μs
Gain Bandwidth Prod.	GBWP	f_O = 1MHz	–	200	–	–	200	–	–	200	–	MHz
SettlingTime	t_s	A_V = -10, 10V Step, 0.01%	–	300	–	–	330	–	–	330	–	ns
Supply Current	I_{SY}	No Load	–	6.1	7.5	–	6.1	7.5	–	6.1	7.5	mA

NOTES:
1. Guaranteed by CMR test.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, –55°C ≤ T_A ≤ +125°C, unless otherwise noted.

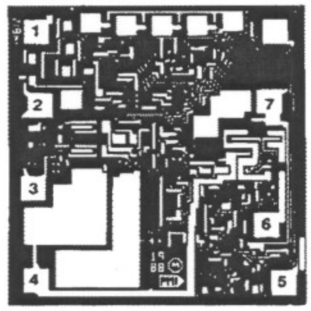
PARAMETER	SYMBOL	CONDITIONS	OP-61A MIN	OP-61A TYP	OP-61A MAX	UNITS
Input Offset Voltage	V_{OS}		–	200	1000	µV
Average Input Offset Drift	TCV_{OS}		–	1.0	5.0	µV/°C
Input Offset Current	I_{OS}	V_{CM} = 0V	–	70	400	nA
Input Bias Current	I_B	V_{CM} = 0V	–	180	800	nA
Input Voltage Range	IVR	(Note 1)	±11V	–	–	V
Common-Mode Rejection	CMR	V_{CM} = ±11V	94	104	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±5V to ±18V	–	2.0	5.6	µV/V
Large-Signal Voltage Gain	A_{VO}	R_L = 10kΩ R_L = 2kΩ R_L = 1kΩ	175 150 120	400 340 260	– – –	V/mV
Output Voltage Swing	V_O	R_L = 1kΩ R_L = 500Ω	±11.0 ±10.0	±13.0 ±12.7	– –	V
Supply Current	I_{SY}	No Load	–	6.5	8.0	mA

ELECTRICAL CHARACTERISTICS at V_S = ±15V, –40°C ≤ T_A ≤ +85°C.

PARAMETER	SYMBOL	CONDITIONS	OP-61F MIN	OP-61F TYP	OP-61F MAX	OP-61G MIN	OP-61G TYP	OP-61G MAX	UNITS
Input Offset Voltage	V_{OS}		–	300	1250	–	400	1500	µV
Average Input Offset Drift	TCV_{OS}		–	3.0	7.0	–	3.0	7.0	µV/°C
Input Offset Current	I_{OS}	V_{CM} = 0V	–	125	500	–	125	500	nA
Input Bias Current	I_B	V_{CM} = 0V	–	250	900	–	250	900	nA
Input Voltage Range	IVR	(Note 1)	±11V	–	–	±11V	–	–	V
Common-Mode Rejection	CMR	V_{CM} = ±11V	88	96	–	88	96	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±5V to ±18V	–	4.0	10.0	–	4.0	10.0	µV/V
Large-Signal Voltage Gain	A_{VO}	R_L = 10kΩ R_L = 2kΩ R_L = 1kΩ	150 120 100	350 300 240	– – –	150 120 100	350 300 240	– – –	V/mV
Output Voltage Swing	V_O	R_L = 1kΩ R_L = 500Ω	±11.0 ±10.0	±13.0 ±12.7	– –	±11.0 ±10.0	±13.0 ±12.7	– –	V
Supply Current	I_{SY}	No Load	–	6.4	8.0	–	6.4	8.0	mA

NOTES:
1. Guaranteed by CMR test.

DICE CHARACTERISTICS



DIE SIZE 0.064 x 0.068 inch, 4,352 sq. mils
(1.63 x 1.73 mm, 2.81 sq. mm)

1. V_{OS} NULL
2. –IN
3. +IN
4. V–
5. V_{OS} NULL
6. OUT
7. V+

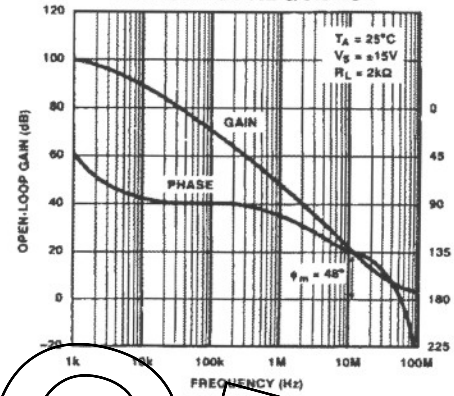
WAFER TEST LIMITS at $V_S = \pm15V$, $T_A = 25°C$.

PARAMETER	SYMBOL	CONDITIONS	OP-61GBC LIMITS	UNITS
Input Offset Voltage	V_{OS}		750	µV MAX
Input Offset Current	I_{OS}		200	nA MAX
Input Bias Current	I_B		600	nA MAX
Input Voltage Range	IVR		±11.0	V MIN
Common-Mode Rejection	CMR	$V_{CM} = \pm11V$	94	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm5V$ to $\pm18V$	5.6	µV/V MAX
Large-Signal Voltage Gain	A_{VO}	$R_L = 10k\Omega$ $R_L = 2k\Omega$ $R_L = 1k\Omega$	175 150 120	V/mV MIN
Output Voltage Swing	V_O	$R_L = 1k\Omega$ $R_L = 500\Omega$	±12.0 ±11.0	V MIN
Slew Rate	SR	$R_L = 1k\Omega$ $C_L = 50pF$	35	V/µs MIN
Supply Current	I_{SY}	No Load	7.5	mA MAX

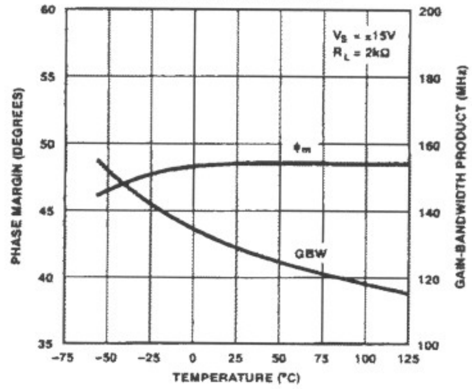
NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

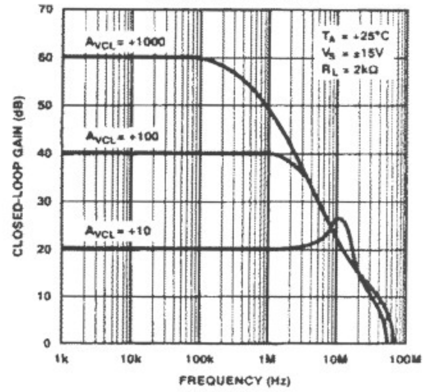
OPEN-LOOP GAIN, PHASE vs FREQUENCY



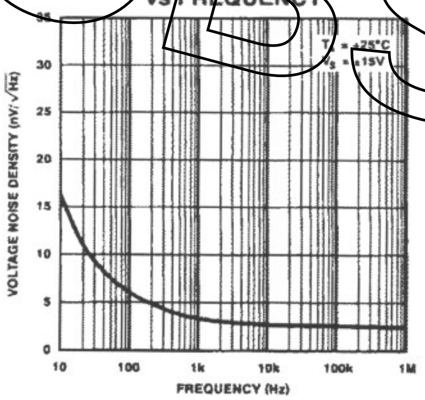
GAIN-BANDWIDTH PRODUCT, PHASE MARGIN vs TEMPERATURE



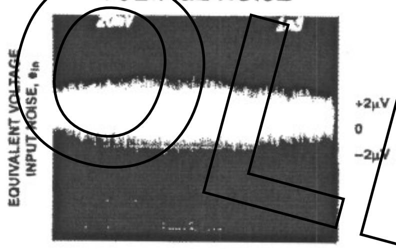
CLOSED-LOOP GAIN vs FREQUENCY



VOLTAGE NOISE DENSITY vs FREQUENCY

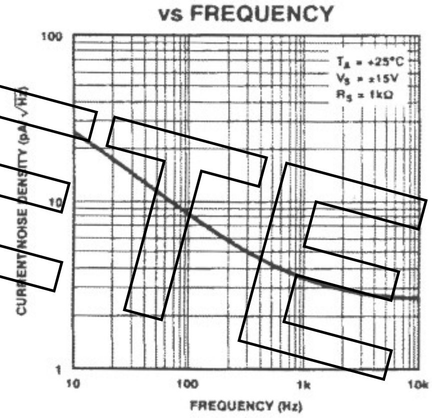


WIDEBAND PEAK-TO-PEAK VOLTAGE NOISE

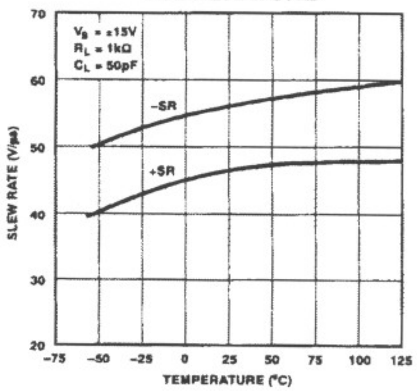


BANDWIDTH: 1kHz TO 100kHz
T_A = +25°C
V_S = ±15V

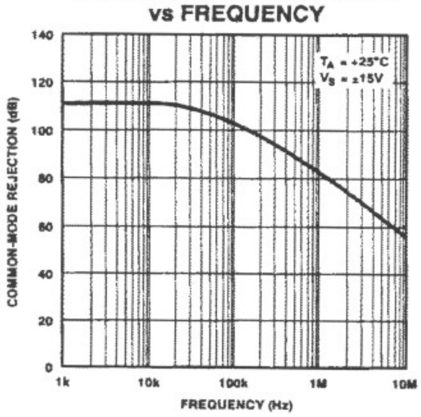
CURRENT NOISE DENSITY vs FREQUENCY



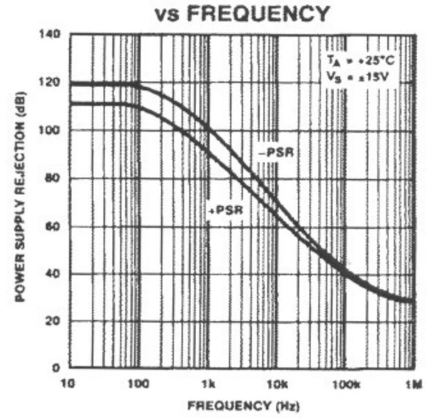
SLEW RATE vs TEMPERATURE



COMMON-MODE REJECTION vs FREQUENCY



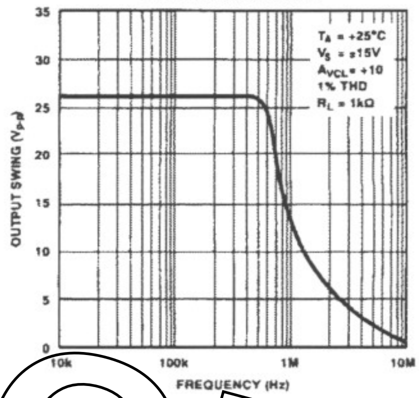
POWER SUPPLY REJECTION vs FREQUENCY



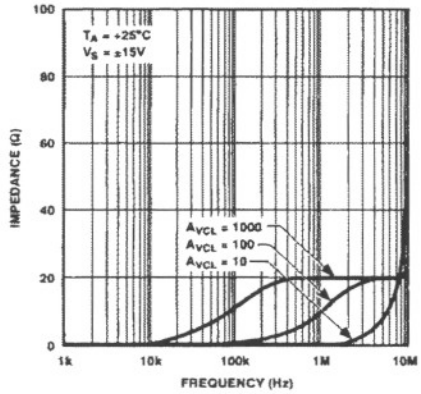
OP-61

TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

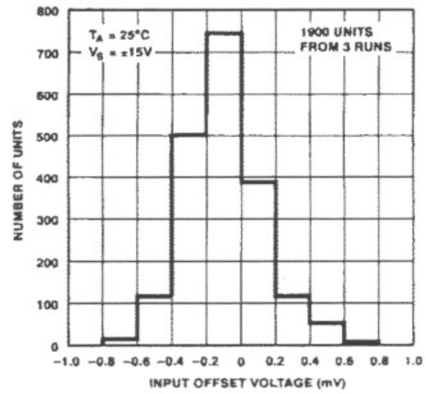
MAXIMUM OUTPUT SWING vs FREQUENCY



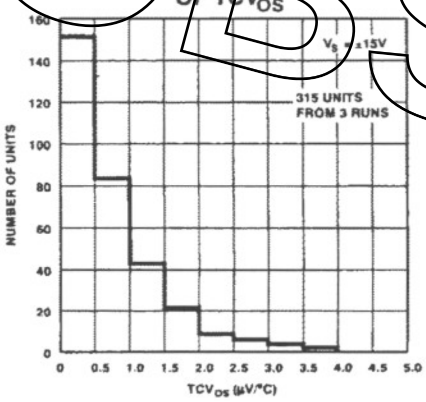
CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY



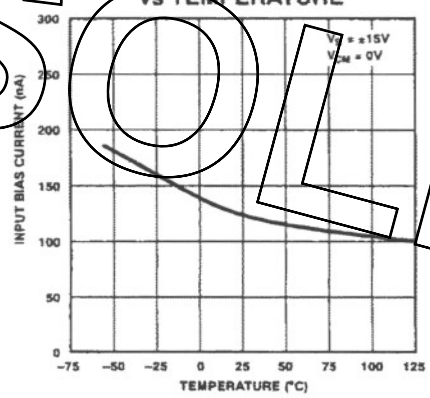
TYPICAL DISTRIBUTION OF INPUT OFFSET VOLTAGE



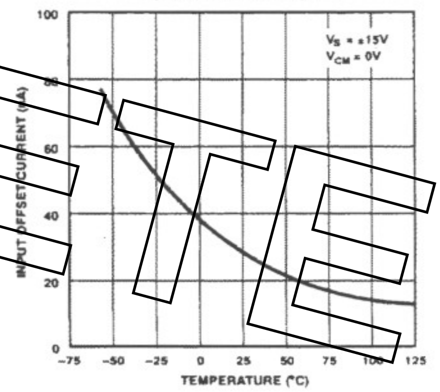
TYPICAL DISTRIBUTION OF TCV_{OS}



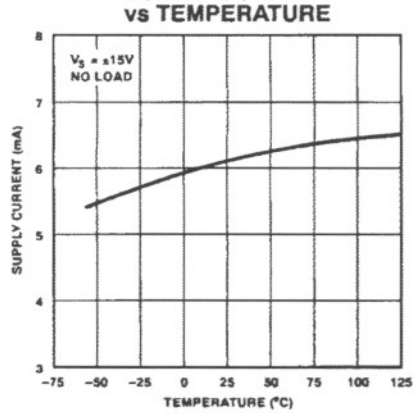
INPUT BIAS CURRENT vs TEMPERATURE



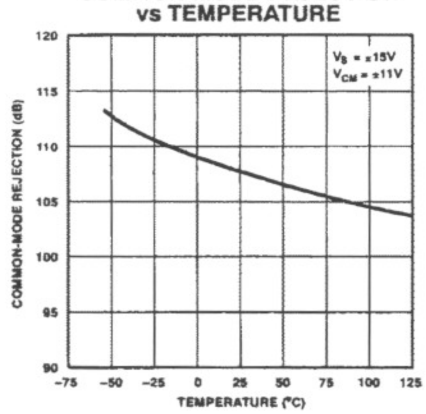
INPUT OFFSET CURRENT vs TEMPERATURE



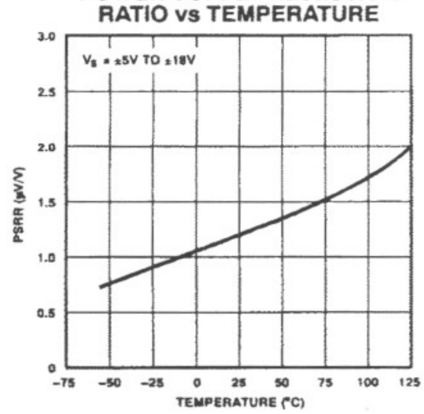
SUPPLY CURRENT vs TEMPERATURE



COMMON-MODE REJECTION vs TEMPERATURE

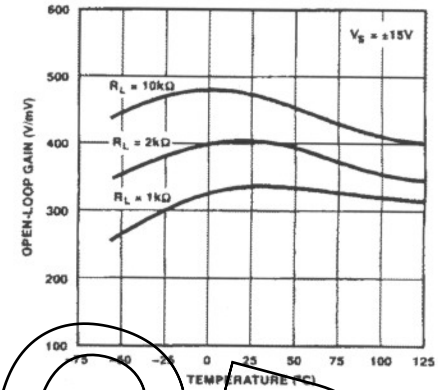


POWER SUPPLY REJECTION RATIO vs TEMPERATURE

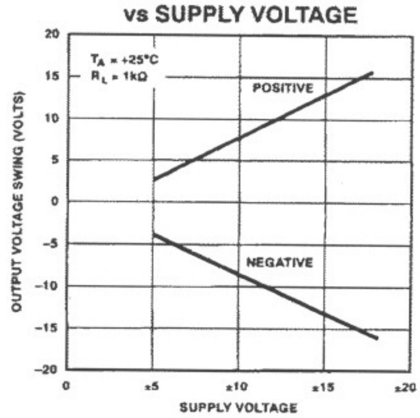


TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

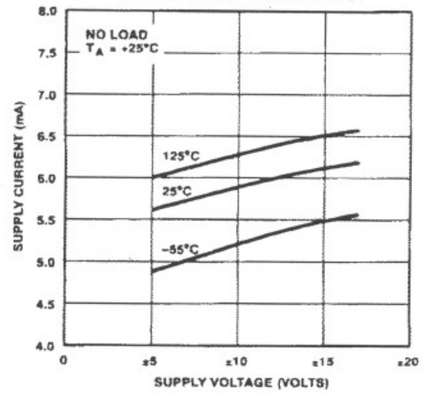
OPEN-LOOP GAIN vs TEMPERATURE



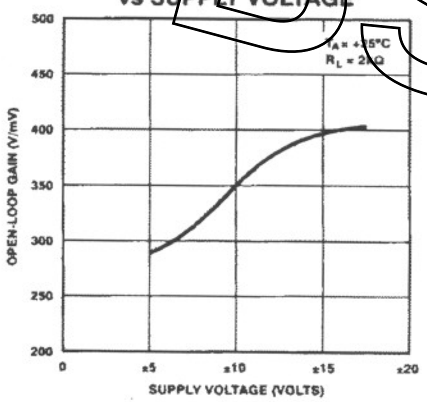
OUTPUT VOLTAGE SWING vs SUPPLY VOLTAGE



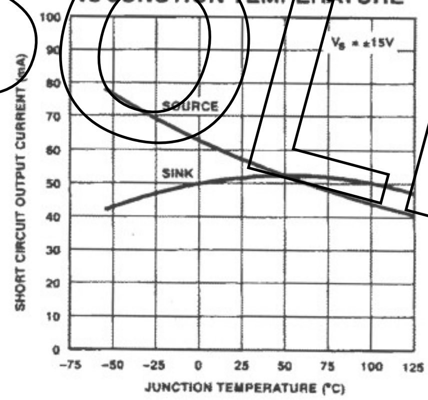
SUPPLY CURRENT vs SUPPLY VOLTAGE



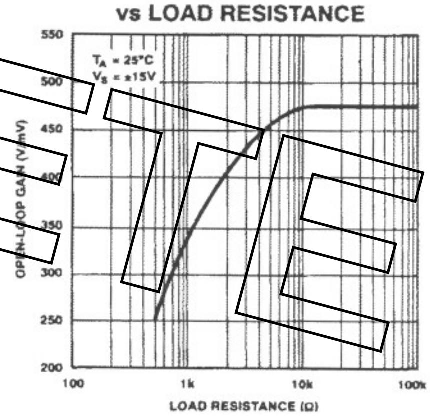
OPEN-LOOP GAIN vs SUPPLY VOLTAGE



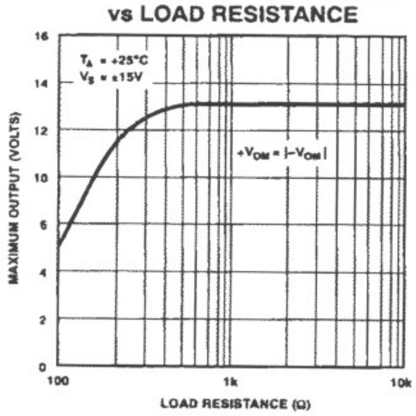
SHORT CIRCUIT OUTPUT CURRENT vs JUNCTION TEMPERATURE



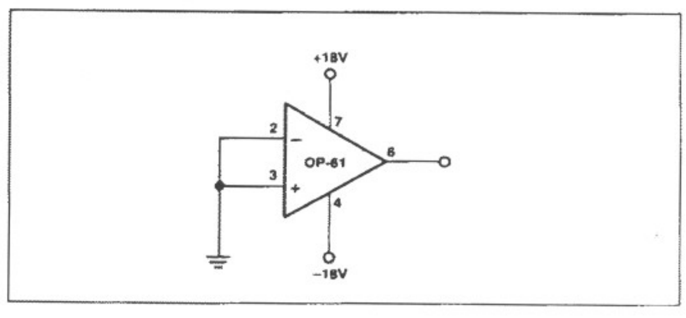
OPEN-LOOP GAIN vs LOAD RESISTANCE



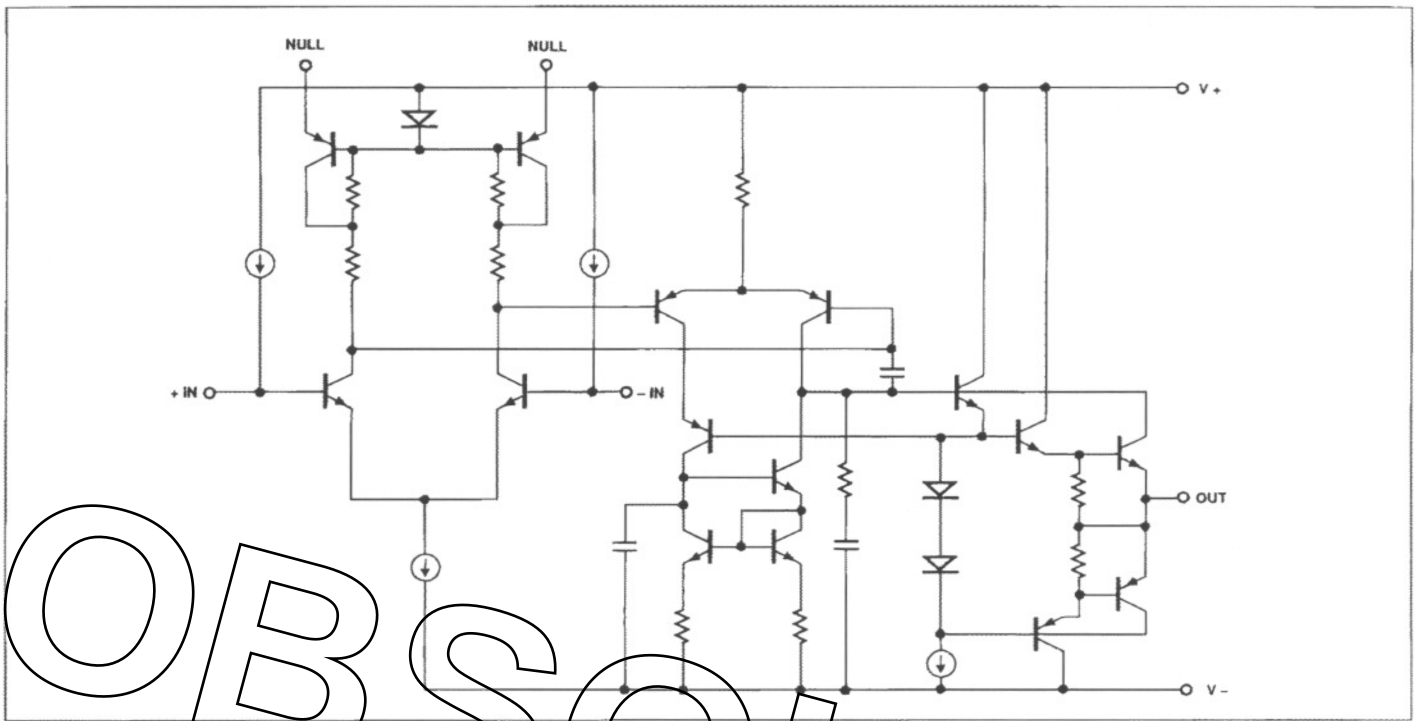
MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE



BURN-IN CIRCUIT



SIMPLIFIED SCHEMATIC



APPLICATIONS INFORMATION

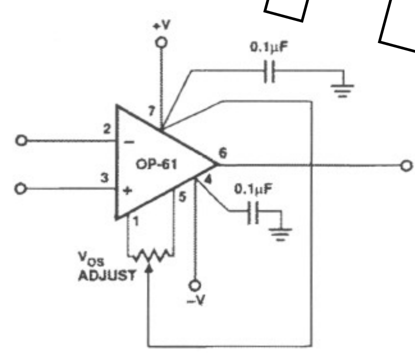
The OP-61 combines high speed with a level of precision and noise performance normally only found with slower amplifiers. Data acquisition and instrumentation technology has progressed to where dynamic accuracy and high resolution are both maintained to a very high level. The OP-61 was specifically designed to meet the stringent requirements of these systems.

Signal-to-noise ratio degrades as input referred noise or bandwidth increases. The OP-61 has a very wide bandwidth, but its input noise is only $3nV/\sqrt{Hz}$. This makes the total noise generated over its closed-loop bandwidth considerably less than previously available wideband operational amplifiers.

The OP-61 provides stable operation in closed-loop gain configurations of 10 or more. Large load capacitances should be decoupled with a resistor placed inside the feedback loop (see Driving Large Capacitive Loads).

OFFSET VOLTAGE ADJUSTMENT

Offset voltage can be adjusted by a potentiometer of 10kΩ to 100kΩ resistance. This potentiometer should be connected between pins 1 and 5 with the wiper connected directly to the OP-61 V+ pin (see Figure 1). By connecting this line directly to the op amp V+ terminal, common impedance paths shared by both return currents and the null inputs will be avoided. Nulling inputs to any op amp are simply another set of sensitive differentially balanced inputs. Therefore, care must always be exercised in laying out signal paths by not placing the trimmer, or the nulling input lines, directly adjacent to high frequency signal lines.



POTENTIOMETERS RANGING FROM 10kΩ TO 100kΩ CAN BE USED TO OBTAIN A MINIMUM OF ±2mV OF V_{OS} ADJUSTMENT.

FIGURE 1: *Input Offset Voltage Nulling*

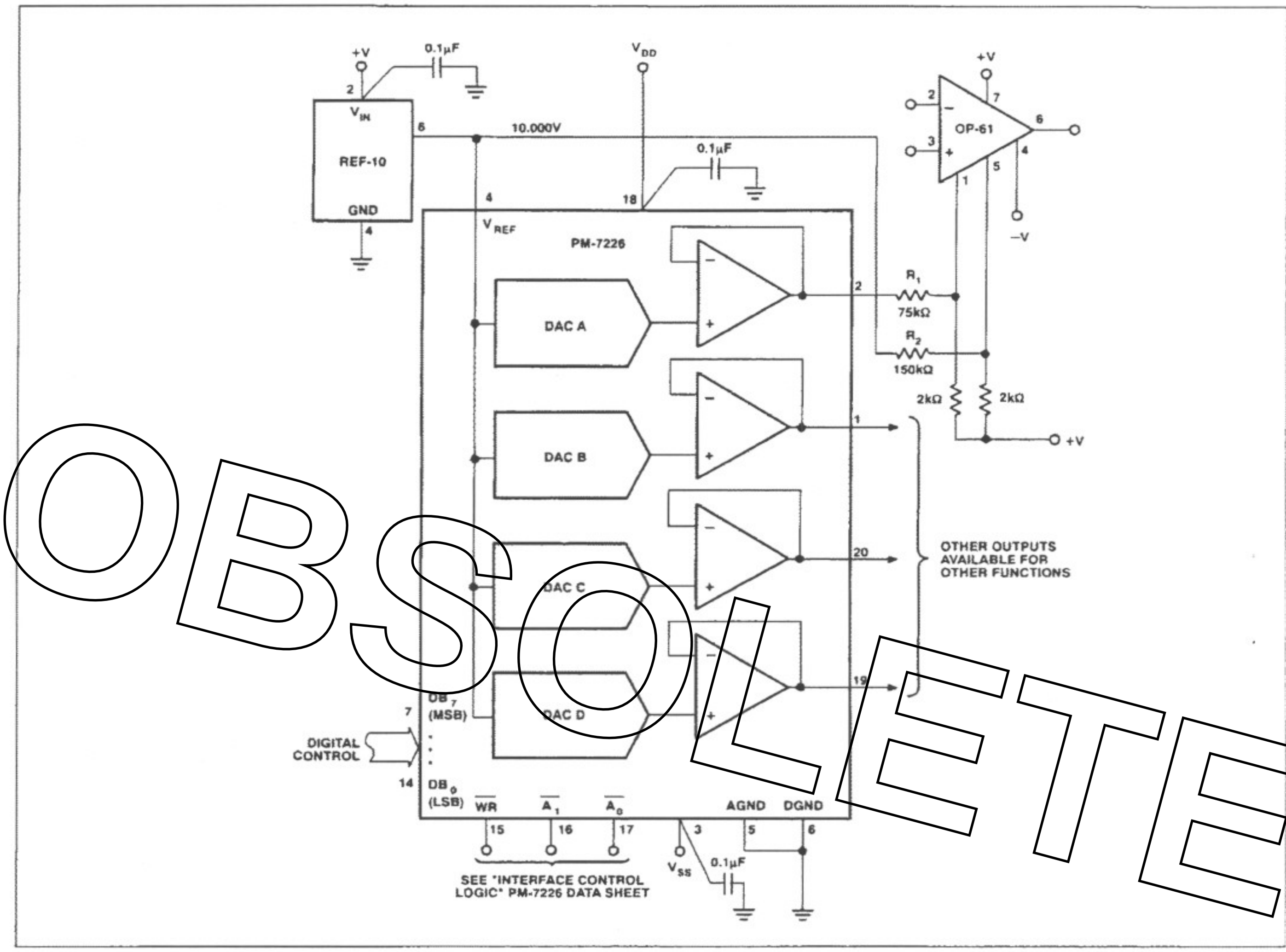


FIGURE 2: *Trimming OP-61 Voltage Offset with 0 to 10V Voltage Output, PM-7226 Quad D/A*

D/A converters can also be used for offset adjustments in systems that are microprocessor controlled. Figure 2 illustrates a PM-7226 quad, 8-bit D/A, used to null the OP-61's offset voltage. A stable fixed bias current is provided into pin 5 of the OP-61, from R_2, and a REF-10, +10V precision voltage reference. Current through R_1, from the D/A voltage output provides the programmed V_{OS} adjustment control. Symmetric control of the offset adjustment is effected since equal currents are sourced into R_1 and R_2 when the D/A is at half scale, binary input code = 10000000.

With the circuit components shown in Figure 2, the maximum V_{OS} adjustment range is ±500mV, referred to the input of the OP-61. Incremental adjustment range is approximately 2µV per bit, allowing V_{OS} to be trimmed to ±2µV.

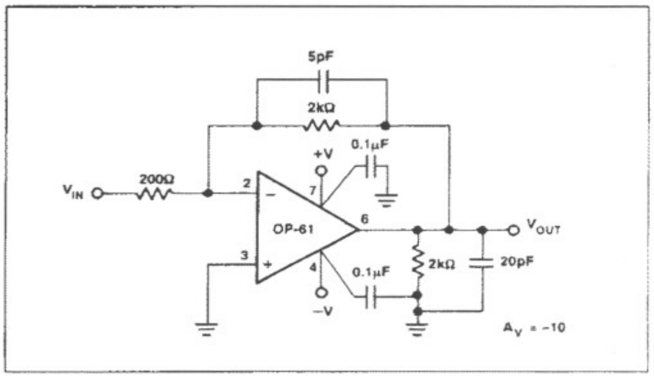


FIGURE 3: *Large- and Small-Signal Response Test Circuit*

OP-61

TRANSIENT RESPONSE PERFORMANCE

Figures 4 and 5, respectively, show the small-signal and large-signal transient response of the OP-61 driving a 20pF load from the circuit in Figure 3. Both waveforms are symmetric and exhibit only minimal overshoot. The slew rate symmetry, apparent from the large-signal response, decreases the DC offsets that occur when processing input signals that extend outside the range of the OP-61's full-power bandwidth.

FIGURE 4: *Small-Signal Transient Response*

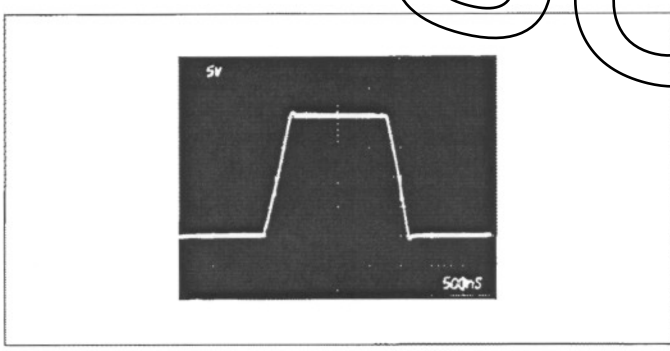


FIGURE 5: *Large-Signal Transient Response*

DRIVING CAPACITIVE LOADS

Direct capacitive loading will reduce the phase margin of any op amp. A pole is created by the combination of the op amp's output impedance and the capacitive load that induces phase lag and reduces stability. However, high-speed amplifiers can easily drive a capacitive load indirectly. This is shown in Figure 6. The OP-61 is driving a 1000pF capacitive load. R_1 and C_1 serve to counteract the loss of phase margin by feedforwarding a small amount of high frequency output signal back to the amplifier's inverting input,

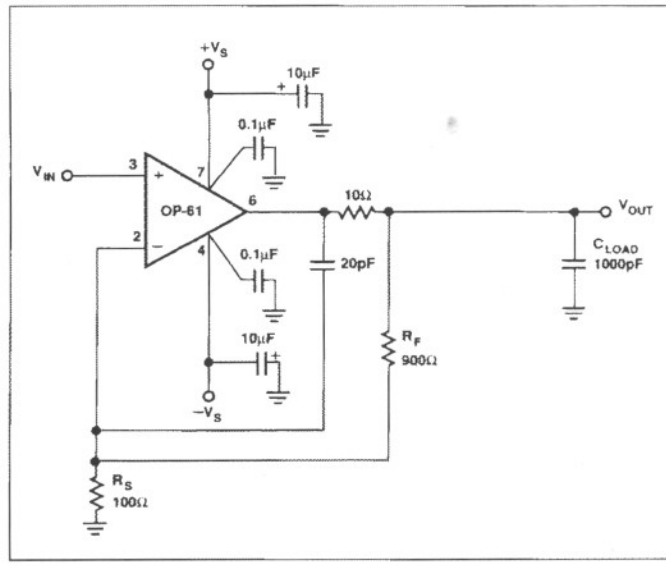


FIGURE 6: *OP-61 Noninverting Gain of 10 Amplifier, Compensated to Handle Large Capacitive Loads*

thereby preserving adequate phase margin. The resulting pulse response can be seen in Figure 7. Extra care may be required to ensure adequate decoupling by placing a 1µF to 10µF capacitor in parallel with the existing decoupling capacitor. Adequate decoupling ensures a low impedance path for high frequency energy transferred from the decoupling capacitors through the amplifier's output stage to a reactive load.

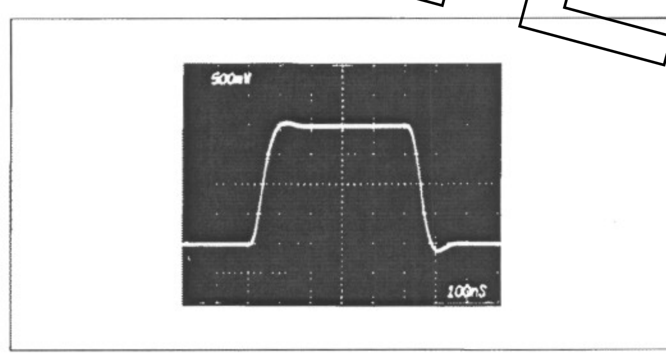


FIGURE 7: *Pulse Response of Compensated X10 Amplifier in Figure 6, V_{IN} = 100m$V_{p\text{-}p}$, V_{OUT} = 1$V_{p\text{-}p}$, Frequency of Square Wave = 1MHz, C_{LOAD} = 1000pF!*

DECOUPLING AND LAYOUT GUIDELINES

The OP-61 op amp is a superb choice for a wide range of precision high-speed, low noise amplifier applications. However, care must be exercized in both the design and layout of high-speed circuits in order for the specified performance to be realized.

Although the OP-61 has excellent power supply rejection over a wide bandwidth, the negative supply rejection is limited at high frequencies since the amplifier's internal integrator is biased via the negative supply line. This operation is typical performance for all monolithic op amps, and not unique to the OP-61. Since the negative supply rejection will approach zero for signals above the close-loop bandwidth, high-speed transients and wideband power supply noise, on the negative supply line, will result in spurious signals being directly added to the amplifier's output. Adequate power supply decoupling prevents this problem.

Generally, a 0.1μF tantalum decoupling capacitor, placed in close proximity across the amplifier's actual power supply pin and ground is recommended. This will satisfy most decoupling requirements, especially when the circuit is built on a low impedance ground plane. When a heavy copper clad ground plane is not used, it becomes especially important to confine the high frequency output load currents confined to as small a high-frequency signal path as possible, as suggested in Figure 8.

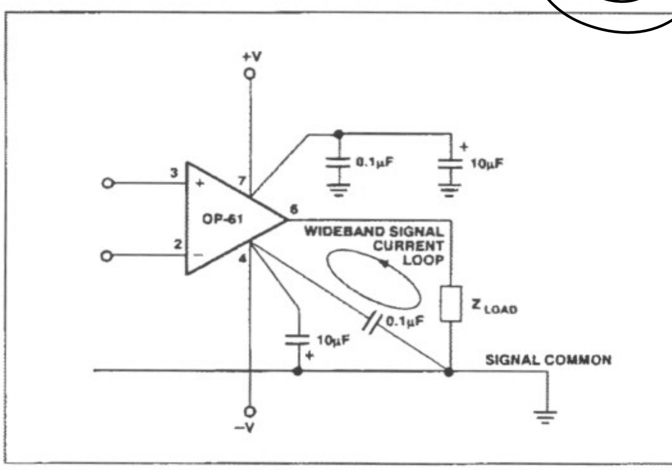


FIGURE 8: *Proper power supply bypassing is required to obtain optimum performance with the OP-61. Maintain as small wideband signal current path as possible. Where signal common is a low impedance ground plane, simply decouple 0.1μF to ground plane near the OP-61.*

Power management of complex systems sometimes results in a complex L-C network that has high frequency natural resonances that cause stability problems in circuits internal to the system. Resistors added in series to the supply lines can lower the Q of the undesired resonances, preventing oscillations on the supply lines. Resistors of 3 to 10 ohms work well and serve to ensure the stability of the OP-61 in such systems.

ADDITIONAL CAVEATS FOR HIGH-SPEED AMPLIFIERS INCLUDE:

1. Keep all leads as short as possible, using direct point-to-point wiring. Do not wire-wrap or use "plug-in" boards for prototyping circuits.
2. Op amp feedback networks should be placed in close proximity to the amplifiers inputs. This reduces stray capacitance that compromises stability margins.
3. Maintain low feedback and source resistance values. Impedance levels greater than several kilo-ohms may result in degrading the amplifier's overall bandwidth and stability.
4. The use of heavy ground planes reduces stray inductance, and provides a better return path for ground currents.
5. Decoupling capacitors must have short leads and be placed at the amplifier's supply pins. Use low equivalent series resistance (ESR) and low inductance chip capacitors wherever possible.
6. Evaluation of prototype circuits should be performed with a low input capacitance, X10 compensated oscilloscope probe. X1 uncompensated probes introduce excessive stray capacitance which alters circuit characteristics by introducing additional phase shifts.
7. Do not directly drive either large capacitive loads or coax cables with high-speed amplifiers (see DRIVING COAXIAL CABLES).
8. Watch out for parasitic capacitances at the +/– inputs to wideband noninverting op amp circuits. Since these nodes are not maintained at virtual ground as in the inverting amplifier configuration, parasitics may degrade bandwidth. Wideband noninverting amplifiers may require the ground plane trace removed from local proximity to the op amp's inputs.

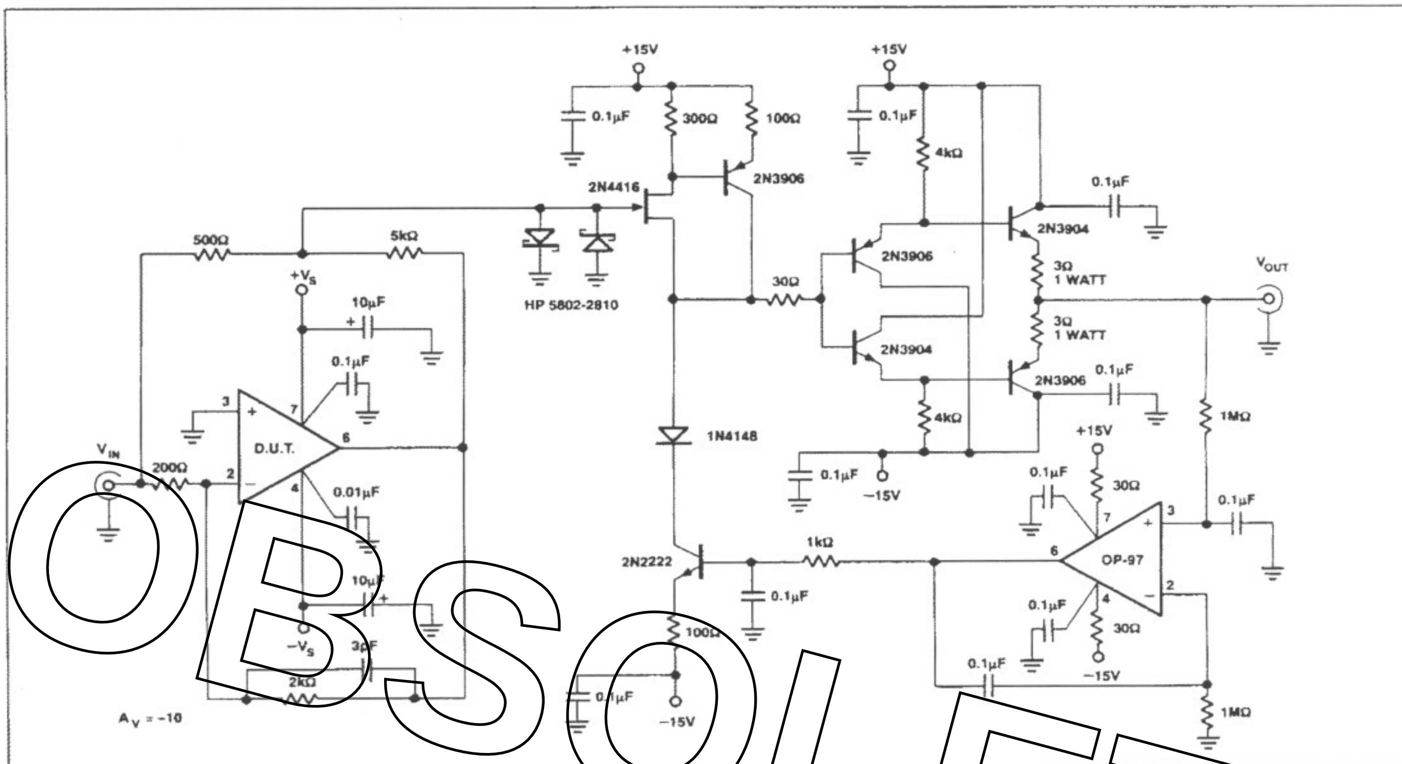


FIGURE 9: *High-Speed Settling Time Fixture (for 0.1 and 0.01%)*

SETTLING TIME

Settling time is the time between when the input signal begins to change and when the output permanently enters a prescribed error band. Figure 9 illustrates the artificial summing node test configuration, used to characterize the OP-61 settling time. The OP-61 is set in a gain of –10 with a 1.0V step input.The error bands on the output are 5mV and 0.5mV, respectively, for 0.1% and 0.01% accuracy.

The test circuit, built on a copper clad circuit board, has a FET input stage which maintains extremely low loading capacitance at the artificial sum node. Preceeding stages are complementary emitter follower stages, providing adequate drive current for a 50Ω oscilloscope input. The OP-97 establishes biasing for the input stage, and eliminates excessive offset voltage errors.

Figure 10 illustrates the OP-61's typical settling time of 330ns. Moreover, problems in settling response, such as thermal tails and long-term ringing are nonexistent. This performance of the OP-61 makes it a suberb choice for systems demanding both high sampling rates and high resolution.

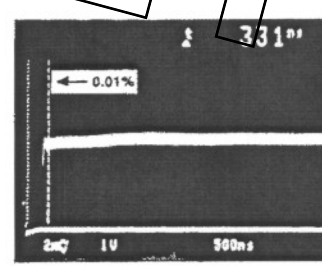


FIGURE 10: *Settling Characteristics of the OP-61 to 0.01%. No Thermal Settling Tail Appears as Part of the Settling Response.*

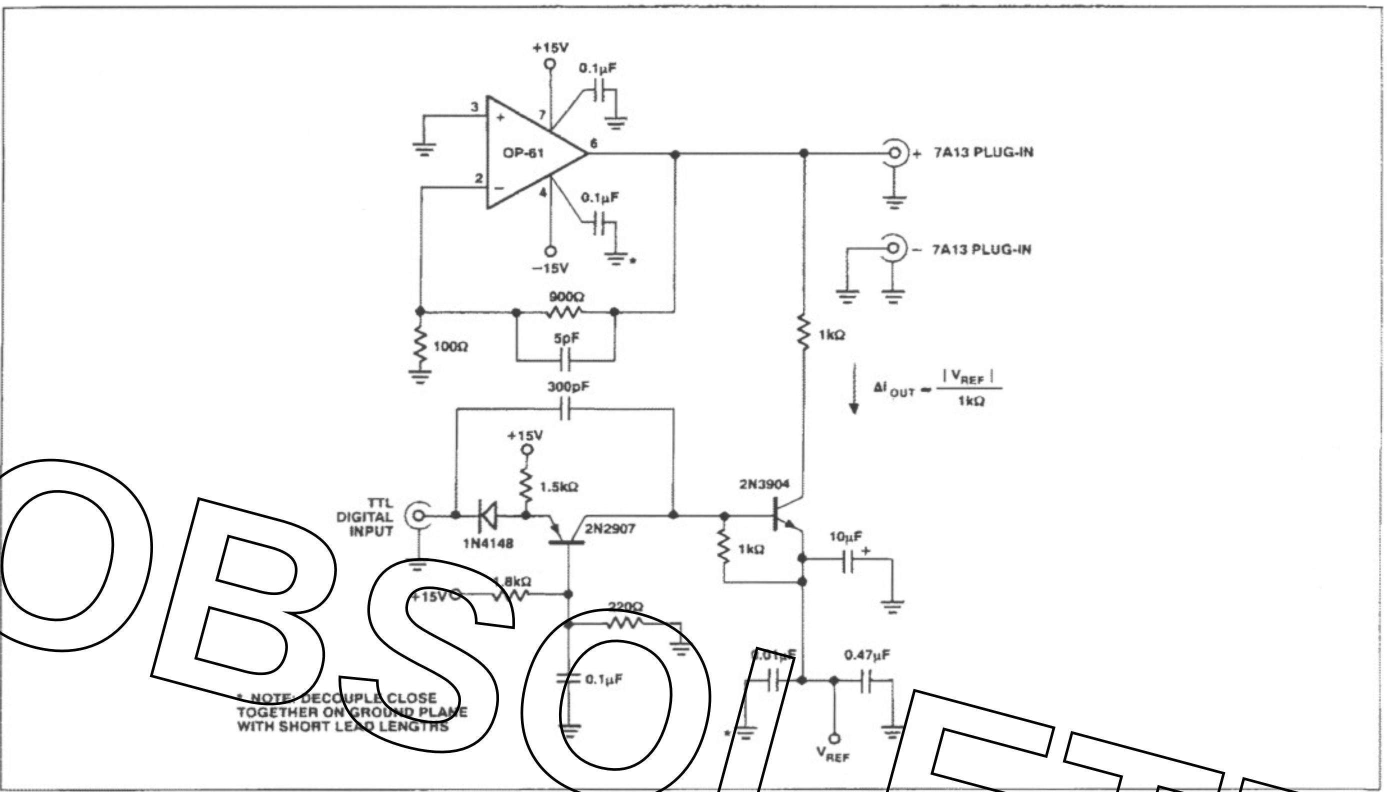


FIGURE 11: *Transient Output Impedance Test Fixture*

TRANSIENT OUTPUT IMPEDANCE

Settling characteristics of operational amplifiers also includes an amplifier's ability to recover, i.e., settle, from a transient current output load condition. An example of this includes an op amp driving the input from a SAR type A/D converter. Although the comparison point of the converter is usually diode clamped, the input swing of plus-and-minus a diode drop still gives rise to a significant modulation of input current. If the closed-loop output impedance is low enough and bandwidth of the amplifier is sufficiently large, the output will settle before the converter makes a comparison decision which will prevent linearity errors or missing codes.

Figure 11 shows a settling measurement circuit for evaluating recovery from an output current transient. An output disturbing current generator provides the transient change in output load current of 1mA. As seen in Figure 12, the OP-61 has extremely fast recovery of 180ns, (to 0.01%), for a 1mA load transient. The performance makes it an ideal amplifier for data acquisition systems.

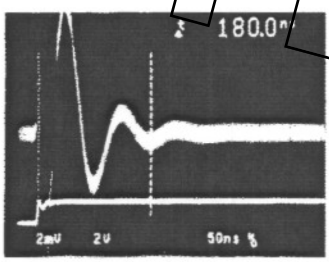


FIGURE 12: *OP-61's Extremely Fast Recovey Time from a 1mA Load Transient to 0.01%*

OP-61

DRIVING COAXIAL CABLES

The OP-61 amplifier, and a BUF-03 unity-gain buffer, make an excellent drive circuit for 75Ω or 50Ω coaxial cables. To maintain optimum pulse response, and minimum reflections, op amp circuits driving coaxial cables should be terminated at both ends. Unterminated cables can appear as a resonant load to the amplifier, degrading stability margins. Also, since coaxial cables represent a significant capacitive load shunting the driving amplifier, it is not possible to drive them directly from the op amp's output (RG-58 coax. typically has 33pF/foot of capacitance).

Figure 13 illustrates an OP-61 noninverting, gain of 10, amplifier stage, driving a double-matched coaxial cable. Since the double-matching of the cable results in voltage gain loss of 6dB, the composite voltage gain of the entire circuit is 5, or 14dB.

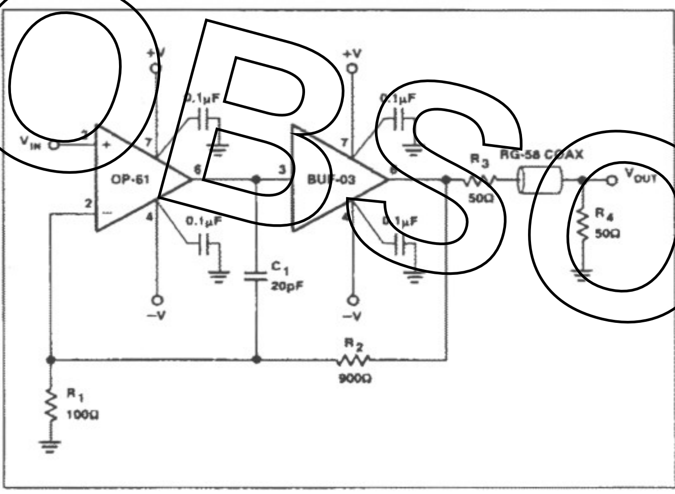


FIGURE 13: *OP-61 Noninverting Amplifier Driving Coaxial Cable, Composite Gain = 5 from V_{IN} to V_{OUT}. Adjust C_1 for Desired Pulse Response.*

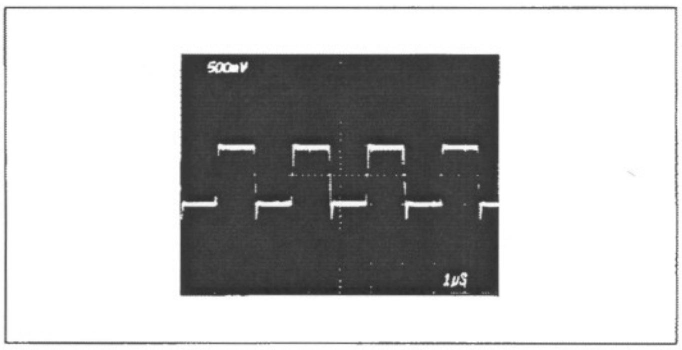


FIGURE 14: *Pulse Response from Amplifier Circuit in Figure 13, Driving 15 Ft. of RG-58 Coaxial Cable*

Resistors R_3 and R_4 serve to absorb reflections at both ends of the cable. The OP-61's wide bandwidth and fast symmetric slewing, results in a very clean pulse reponse, as can be seen in Figure 15. The BUF-03 serves to increase the output current capability to 70mA peak, and the ability to drive up to a 1µF capacitive load (or a longer cable). The value of C_1 may need to be slightly adjusted to provide an optimum value of phase lead, or pulse response. This capacitor serves to correct for the current buffers phase lag, internal to the OP-61's feedback loop.

NOISE MODEL AND DISCUSSION

The OP-61's exceptionally low voltage noise (e_n = 3.0nV/Hz, high open-loop gain, and wide bandwidth makes it ideal for accurately amplifying wideband low-level signals. Figure 15a shows the OP-61 cleanly amplifying a 5mVp-p, 1MHz sine wave, with inverting gain of 100. Noise or limited bandwidth prevents most amplifiers from achieving this performance.

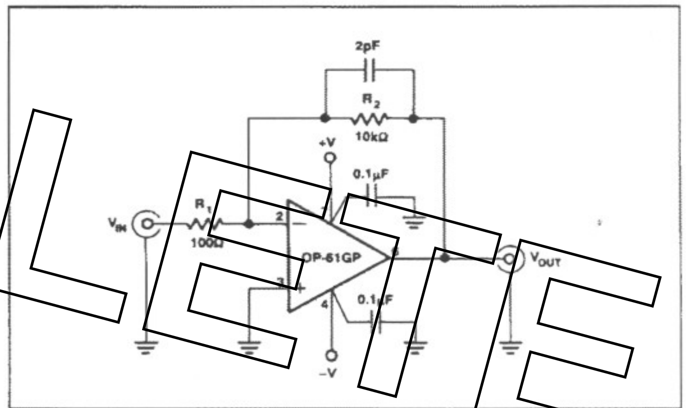


FIGURE 15a: *Example of Low Level Amplifier in an Inverting Configuration, Gain = V_{OUT}/V_{IN} = $-R_2/R_1$ = –100*

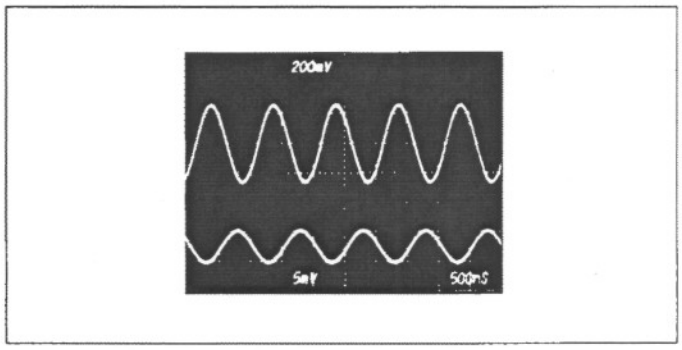


FIGURE 15b: *OP-61, Gain = –100.0, Wideband Amplifier, V_{IN} = 5mV_{p-p} Signal at 1MHz, V_{OUT} = 500mV_{p-p}*

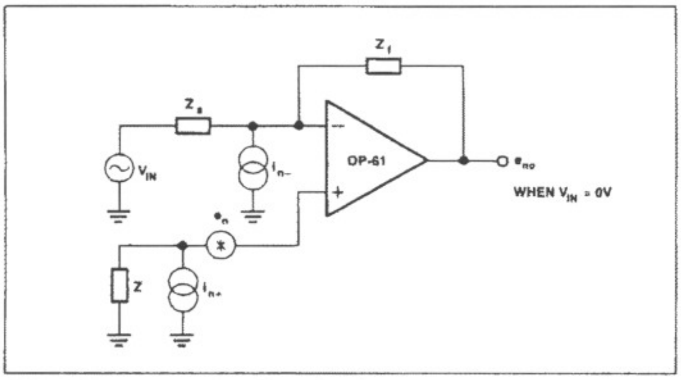


FIGURE 16: *Inverting Gain Configuration Noise Model for the OP-61*

The inverting amplifier model, seen in Figure 16, can be used to calculate the equivalent input noise, e_{ni}. e_{ni} is the voltage noise, modeled as part of the input signal. It represents all the current and voltage noise sources lumped into one equivalent input voltage.

Typical values for the OP-61 noise parameters are:

$e_n = 3.4\text{nV}/\sqrt{\text{Hz}}$ @ 1kHz

$i_n = 1.7\text{pA}/\sqrt{\text{Hz}}$ @ 10kHz

(where it is assumed that $i_n = i_n- = i_n+$).

It can be defined from the model in Figure 16:

e_{ni} = total input referred spot voltage noise (all noise contributions lumped into one equivalent voltage noise source).

e_n = spot voltage noise of OP-61

i_n = spot current noise of OP-61

Z_S = total input impedance

Z = impedance at OP-61 + input node

A_{VCL} = closed-loop gain for inverting amplifier

N.G. = 1 + $|A_{VCL}|$ = noise gain for inverting amplifier

i_{ZS} = spot noise current generated by Z_s. If $Z_s = R_s$, then $i_{ZS} = i_{RS} = 0.129\sqrt{(1/R_S)}$ nV/$\sqrt{\text{Hz}}$.

e_{Zf} = spot voltage noise generated by Z_f. If $Z_f = R_f$, then $e_{Zf} = e_{Rf} = 0.129\sqrt{R_f}$ nV/$\sqrt{\text{Hz}}$.

Note: Equation is derived from Johnson noise relationship of resistor R:

$e_R = \sqrt{4kTR} = \sqrt{4kT}\sqrt{R} = 0.129\sqrt{R}$ nV/$\sqrt{\text{Hz}}$. R is in ohms.

The equivalent input voltage noise, referred to the output, can be found by adding all the noise sources in a sum-of-square fashion:

$$e_{no}^2 = e_n^2\,(\text{N.G.})^2 + i_n^2\,|Z|^2\,(\text{N.G.})^2 + i_n^2\,|Z_f|^2 + i_{ZS}^2\,|Z_f|^2 + e_{Zf}^2$$

Referred back to the amplifiers input:

$$e_{ni} = \frac{e_{no}}{|A_{VCL}|} = \frac{\sqrt{\left(e_n^2\,(\text{N.G.})^2 + i_n^2\,|Z|^2\,(\text{N.G.})^2 + i_n^2\,|Z_f|^2 + i_{ZS}^2\,|Z_f|^2 + e_{Zf}^2\right)}}{|A_{VCL}|}$$

To capitalize on the low voltage performance of the OP-61, Z, Z_f and especially Z_S must be as low impedance as possible. With low impedance values of Z_f and Z_S:

$$e_{ni} \approx \frac{\sqrt{e_n^2\,(1 + |A_{VCL}|)^2}}{|A_{VCL}|} \quad \text{or,} \quad e_{ni} \approx \frac{e_n\ (\text{N.G.})}{(\text{N.G.}) - 1}$$

All noise contributions are now easily modelled as a signal equivalent noise voltage source, e_{ni} (see Figure 17).

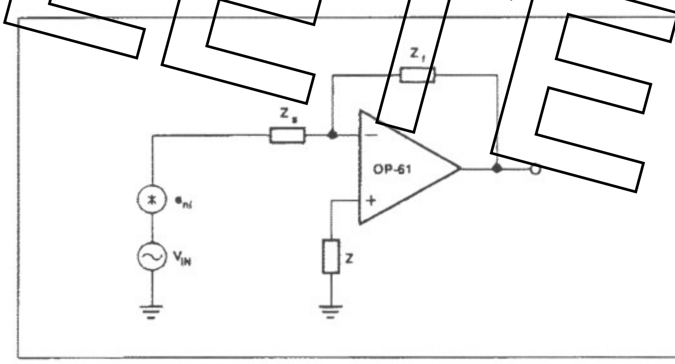


FIGURE 17: *Equivalent Noise Model, Where All Noise Contributions are Lumped Into e_{ni}*

OP-61 SPICE MACROMODEL

Figures 18 and 19 show the node and net list for a SPICE macromodel of the OP-61. The model is a simplified version of the actual device and simulates important DC parameters such as V_{OS}, I_{OS}, I_B, A_{VO}, CMR, V_O and I_{SY}. AC parameters such as slew rate, gain and phase reponse and CMR change with frequency are also simulated by the model.

The model uses typical parameters for the OP-61. The poles and zeros in the model were determined from the actual open and closed-loop gain and phase reponse of the OP-61. In this way the model presents an accurate AC representation of the actual device. The model assumes an ambient temperature of 25°C (see following pages).

OP-61

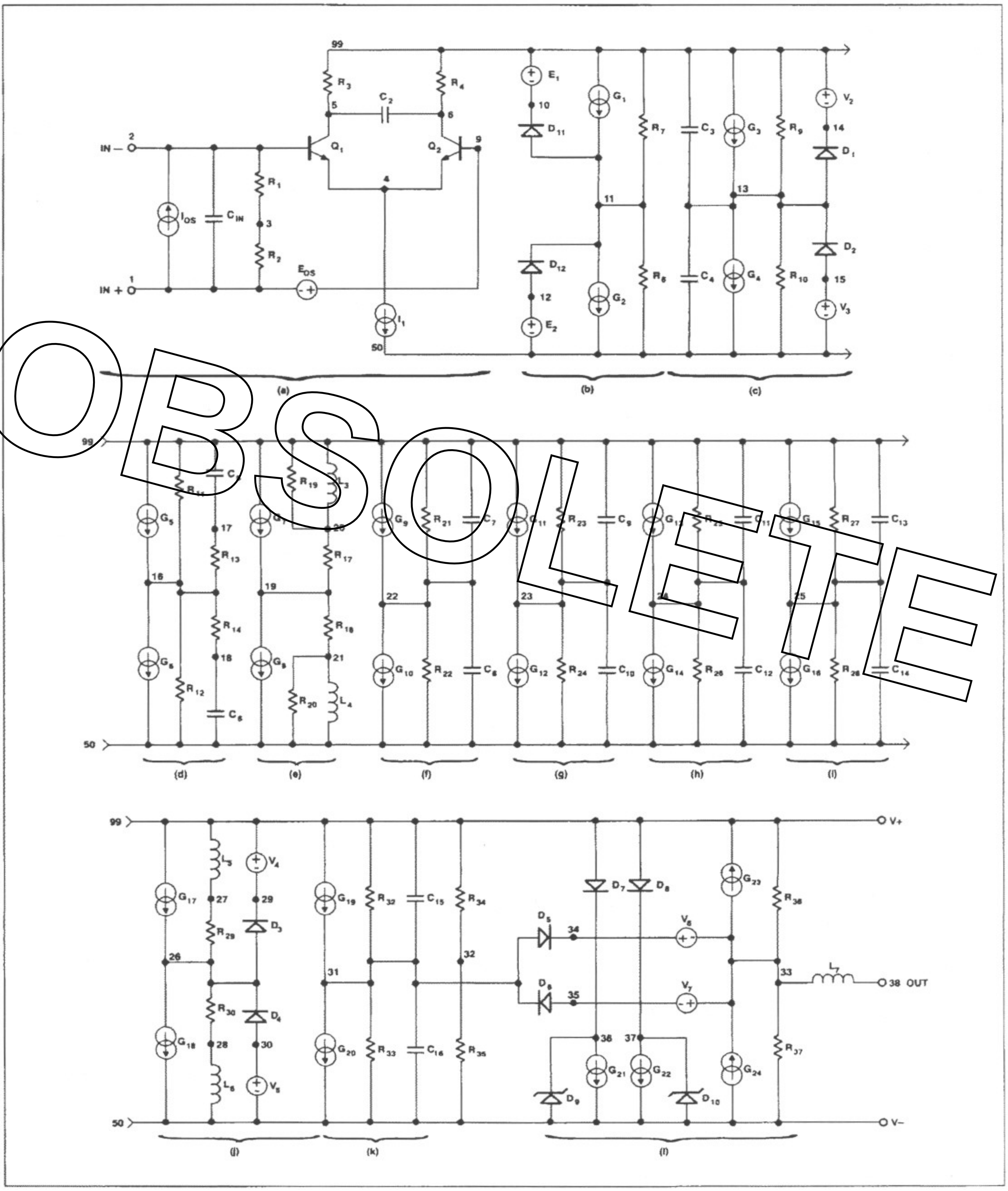


FIGURE 18: *OP-61 SPICE Macro-Model Schematic and Node List*

```
OP-61 MACROMODEL AND TEST CIRCUIT © ADI 1990
*
• subckt OP-61 1  2 38 99 50
*
* INPUT STAGE & POLE AT 300 MHz
*
r1   2    3         5E11
r2   1    3         5E11
r3   5    99        51.6
r4   6    99        51.6
cin  1    2         5E-12
c2   5    6         5.141E-12
i1   4    50        1E-3
ios  1    2         2E-7
eos  9    1         poly(1) 26 32 400E-6 1
q1   5    2    4    qx
q2   6    9    4    qx
*
* FIRST GAIN STAGE
*
r7   11   99        1E6
r8   11   50        1E6
d11  11   10        dx
d12  12   11        dx
g1   99   11        5 6 2E-4
g2   11   50        6 5 2E-4
e1   99   10        poly(1) 99 32 –4.4 1
e2   12   50        poly(1) 32 50 –4.4 1
*
* SECOND GAIN STAGE & POLE AT 2.5kHz
*
r9   13   99        5.1598E6
r10  13   50        5.1598E6
c3   13   99        12.338E-12
c4   13   50        12.338E-12
g3   99   13        poly(1) 11 32 4.24E-3 9.69E-5
g4   13   50        poly(1) 32 11 4.24E-3 9.69E-5
v2   99   14        2.3
v3   15   50        2.3
d1   13   14        dx
d2   15   13        dx
*
* POLE-ZERO PAIR AT 4MHz / 8MHz
*
r11  16   99        1E6
r12  16   50        1E6
r13  16   17        1E6
r14  16   18        1E6
c5   17   99        19.89E-15
c6   18   50        19.89E-15
g5   99   16        13 32 1E-6
g6   16   50        32 13 1E-6
*
* ZERO-POLE PAIR AT 85MHz / 300MHz
*
r17  19   20        1E6
r18  19   21        1E6
r19  20   99        2.529E6
r20  21   50        2.529E6
l3   20   99        1.342E-3
l4   21   50        1.342E-3
g7   99   19        16 32 1E-6
g8   19   50        32 16 1E-6
*
* POLE AT 40MHz
*
r21  22   99        1E6
r22  22   50        1E6
c7   22   99        3.979E-15
c8   22   50        3.979E-15
g9   99   22        19 32 1E-6
g10  22   50        32 19 1E-6
*
* POLE AT 200MHz
*
r23  23   99        1E6
r24  23   50        1E6
c9   23   99        .796E-15
c10  23   50        .796E-15
g11  99   23        22 32 1E-6
g12  23   50        32 22 1E-6
*
* POLE AT 200MHz
*
r25  24   99        1E6
26   24   50        1E6
c11  24   99        .796E-15
c12  24   50        .796E-15
g13  99   24        23 32 1E-6
g14  24   50        32 23 1E-6
*
* POLE AT 200MHz
*
r27  25   99        1E6
r28  25   50        1E6
c13  25   99        .796E-15
c14  25   50        .796E-15
g15  99   25        24 32 1E-6
g16  25   50        32 24 1E-6
*
* COMMON-MODE GAIN NETWORK WITH ZERO AT 40kHz
*
r29  26   27        1E6
r30  26   28        1E6
l5   27   99        3.979
l6   28   50        3.979
g17  99   26        3  32 1E-6
g18  26   50        32 3  1E-6
v4   99   29        2.5
v5   30   50        2.5
d3   26   29        dx
d4   30   26        dx
*
* POLE AT 300MHz
*
r32  31   99        1E6
r33  31   50        1E6
c15  31   99        .531E-15
c16  31   50        .531E-15
g19  99   31        25 32 1E-6
g20  31   50        32 25 1E-6
*
* OUTPUT STAGE
*
r34  32   99        20.0E3
r35  32   50        20.0E3
r36  33   99        30
r37  33   50        30
l7   33   38        1.65E-7
g21  36   50        31 33 33.3333333E-3
g22  37   50        33 31 33.3333333E-3
g23  33   99        99 31 33.3333333E-3
g24  50   33        31 50 33.3333333E-3
v6   34   33        .2
v7   33   35        .2
d5   31   34        dx
d6   35   31        dx
d7   99   36        dx
d8   99   37        dx
d9   50   36        dy
d10  50   37        dy
*
* MODELS USED
*
•model qx NPN(BF=1250)
•model dx  D(IS=1E-15)
•model dy  D(IS=1E-15 BV = 50)
•ends OP-61
```

FIGURE 19: *OP-61 SPICE Net List*

* PSpice is a registered trademark of MicroSim Corporation.
** HSPICE is a tradename of Meta-Software, Inc.