- **1.6 to 2.7 Gigabits Per Second (Gbps) Serializer/Deserializer**
- **Hot-Plug Protection**
- **High-Performance 64-Pin VQFP Thermally Enhanced Package (PowerPAD™)**
- **2.5-V Power Supply for Low Power Operation**
- **Programmable Voltage Output Swing on Serial Output**
- **Interfaces to Backplane, Copper Cables, or Optical Converters**
- **On-Chip 8-Bit/10-Bit Encoding/Decoding, Comma Detect**
- **On-Chip PLL Provides Clock Synthesis From Low-Speed Reference**
- **Receiver Differential Input Thresholds 200 mV Minimum**
- **Low Power: < 500 mW**
- **3 V Tolerance on Parallel Data Input Signals**
- **16-Bit Parallel TTL Compatible Data Interface**
- **Ideal for High-Speed Backplane Interconnect and Point-to-Point Data Link**
- **Industrial Temperature Range (−40°C to 85°C)**
- **Loss of Signal (LOS) Detection**

description

The TLK2701 is a member of the transceiver family of multigigabit transceivers, intended for use in ultrahigh-speed bidirectional point-to-point data transmission systems. The TLK2701 supports an effective serial interface speed of 1.6 Gbps to 2.7 Gbps, providing up to 2.16 Gbps of data bandwidth.

The primary application of this chip is to provide very high-speed I/O data channels for point-to-point baseband data transmission over controlled impedance media of approximately 50 Ω. The transmission media can be printed-circuit board, copper cables, or fiber-optic cable. The maximum rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.

This device can also be used to replace parallel data transmission architectures by providing a reduction in the number of traces, connector terminals, and transmit/receive terminals. Parallel data loaded into the transmitter is delivered to the receiver over a serial channel, which can be a coaxial copper cable, a controlled impedance backplane, or an optical link. It is then reconstructed into its original parallel format. It offers significant power and cost savings over current solutions, as well as scalability for higher data rate in the future.

The TLK2701 performs data conversion parallel-to-serial and serial-to-parallel. The clock extraction functions as a physical layer interface device. The serial transceiver interface operates at a maximum speed of 2.7 Gbps. The transmitter latches 16-bit parallel data at a rate based on the supplied reference clock (GTX_CLK). The 16-bit parallel data is internally encoded into 20 bits using an 8-bit/10-bit (8B/10B) encoding format. The resulting 20-bit word is then transmitted differentially at 20 times the reference clock (GTX_CLK) rate. The receiver section performs the serial-to-parallel conversion on the input data, synchronizing the resulting 20-bit wide parallel data to the extracted reference clock (RX_CLK). It then decodes the 20 bit wide data using 8-bit/10-bit decoding format resulting in 16 bits of parallel data at the receive data terminals (RXD0-15). The outcome is an effective data payload of 1.28 Gbps to 2.16 Gbps (16 bits data x the GTX_CLK frequency).

The TLK2701 is housed in a high performance, thermally enhanced, 64-pin VQFP PowerPAD package. Use of the PowerPAD package does not require any special considerations except to note that the PowerPAD, which is an exposed die pad on the bottom of the device, is a metallic thermal and electrical conductor. It is recommended that the TLK2701 PowerPAD be soldered to the thermal land on the board. All ac performance specifications in this data sheet are measured with the PowerPAD soldered to the test board.

The TLK2701 provides an internal loopback capability for self-test purposes. Serial data from the serializer is passed directly to the deserializer, allowing the protocol device a functional self-check of the physical interface.

description (continued)

The TLK2701 has a loss of signal detection circuit for conditions where the incoming signal no longer has a sufficient voltage amplitude to keep the clock recovery circuit in lock.

The TLK2701 allows users to implement redundant ports by connecting receive data bus terminals from two TLK2701 devices together. Asserting the LCKREFN to a low state will cause the receive data bus terminals, RXD[0:15], RX_CLK, and RKLSB, RKMSB/PRBS_PASS to go to a high-impedance state. This places the device in a transmit-only mode since the receiver is not tracking the data.

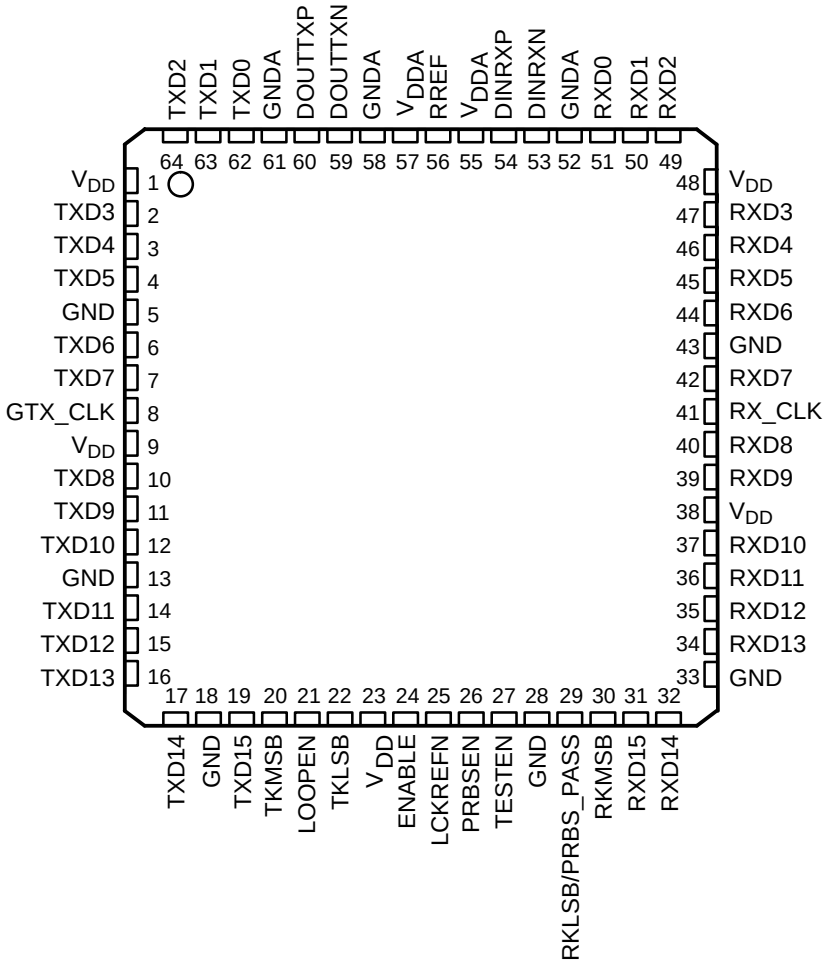
The TLK2701 uses a 2.5 V supply. The I/O section is 3 V compatible. With the 2.5-V supply the chipset is very power efficient consuming less than 350 mW typically. The TLK2701 is characterized for operation from −40°C to 85°C.

The TLK2701 is designed to be hot plug capable. An on-chip power-on reset circuit holds the RX_CLK low and goes to high impedance to the parallel side output signal terminals during power up as well as goes to DOUTTXP and DOUTTXN.

AVAILABLE OPTIONS

T_A	PACKAGE
	PowerPAD QUAD FLATPACK (VQFP)
−40°C to 85°C	TLK2701IRCP

RCP PACKAGE
(TOP VIEW)



block diagram

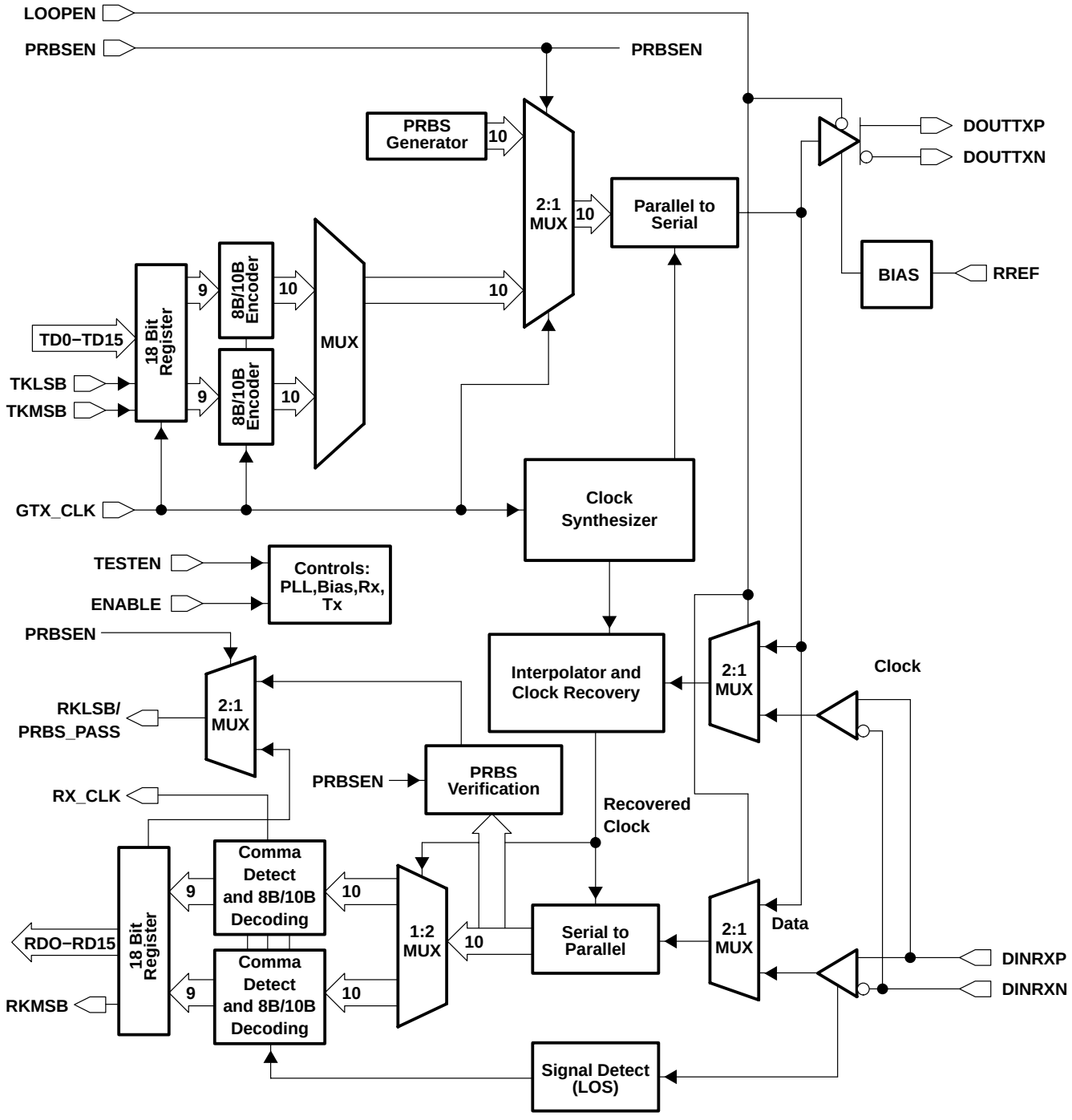


Figure 1. TLK2701 Block Diagram

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
DINRXN DINRXP	53 54	I	Serial receive inputs. DINRXP and DINRXN together are the differential serial input interface from a copper or an optical I/F module.
DOUTTXN DOUTTXP	59 60	O	Serial transmit outputs. DOUTTXP and DOUTTXN are differential serial outputs that interface to copper or an optical I/F module. These terminals transmit NRZ data at a rate of 20 times the GTX_CLK value. DOUTTXP and DOUTTXN are put in a high-impedance state when LOOPEN is high and are active when LOOPEN is low. During power-on reset these terminals are high impedance.
ENABLE	24	I	Device enable. When this terminal is held low, the device is placed in power-down mode. Only the signal detect circuit on the serial receive pair is active. When asserted high while the device is in power-down mode, the transceiver will go into power-on reset before beginning normal operation.
GND	5, 13, 18, 28, 33, 43		Digital logic ground. Provides a ground for the logic circuits and digital I/O buffers.
GNDA	52, 58, 61		Analog ground. GNDA provides a ground reference for the high-speed analog circuits, RX and TX.
GTX_CLK	8	I	Reference clock. GTX_CLK is a continuous external input clock that synchronizes the transmitter interface signals TKMSB, TKLSB and TXD. The frequency range of GTX_CLK is 80 MHz to 135 MHz. The transmitter uses the rising edge of this clock to register the 16-bit input data (TXD) for serialization.
LCKREFN	25	I	Lock to reference. When LCKREFN is low, the receiver clock is frequency locked to GTX_CLK. This places the device in a transmit only mode since the receiver is not tracking the data. When LCKREFN is asserted low, the receive data bus terminals, RXD[0:15], RX_CLK and RKLSB, RKMSB/LOS are in a high-impedance state. When LCKREFN is deasserted high, the receiver is locked to the received data stream.
LOOPEN	21	I	Loop enable. When LOOPEN is active high, the internal loop-back path is activated. The transmitted serial data is directly routed internally to the inputs of the receiver. This provides a self-test capability in conjunction with the protocol device. The DOUTTXP and DOUTTXN outputs are held in a high-impedance state during the loop-back test. LOOPEN is held low during standard operational state with external serial outputs and inputs active.
PRBSEN	26	I	PRBS test enable. When asserted high results of pseudo random bit stream (PRBS) tests can be monitored on the RKLSB/PRBS_PASS terminal. A high on PRBS_PASS indicates that valid PRBS is being received.
RREF	56	I	Reference resistor. The RREF terminal is used to connect to an external reference resistor. The other side of the resistor is connected to analog V_{DD}. The resistor is used to provide an accurate current reference to the transmitter circuitry.
RXD0 RXD1 RXD2 RXD3 RXD4 RXD5 RXD6 RXD7 RXD8 RXD9 RXD10 RXD11 RXD12 RXD13 RXD14 RXD15	51 50 49 47 46 45 44 42 40 39 37 36 35 34 32 31	O	Receive data bus. These outputs carry 16-bit parallel data output from the transceiver to the protocol device, synchronized to RX_CLK. The data is valid on the rising edge of RX_CLK as shown in Figure 11. These terminals are in high-impedance state during power-on reset.

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
RX_CLK	41	O	Recovered clock. Output clock that is synchronized to RXD, RKLSB, RKMSB/LOS. RX_CLK is the recovered serial data rate clock divided by 20. RX_CLK is held low during power-on reset.
RKLSB/ PRBS_PASS	29	O	K-Code indicator/PRBS test results. When RKLSB is active, an 8-bit/10-bit K code was received and is indicated by data bits RXD0 −RXD7. When RKLSB is inactive an 8-bit/10-bit D code is received and is presented on data bits RXD0 − RXD7. When PRBSEN is asserted high then this pin is used to indicate status of the PRBS test results (high = pass).
RKMSB	30	O	K-code indicator. When RKMSB is active an 8-bit/10-bit K code was received and is indicated by data bits RXD8 −RXD15. When RKMSB is inactive an 8-bit/10-bit D code was received and is presented on data bits RXD8 − RXD15.
TESTEN	27	I	Test mode enable. This terminal should be left unconnected or tied low.
TXD0 TXD1 TXD2 TXD3 TXD4 TXD5 TXD6 TXD7 TXD8 TXD9 TXD10 TXD11 TXD12 TXD13 TXD14 TXD15	62 63 64 2 3 4 6 7 10 11 12 14 15 16 17 19	I	Transmit data bus. These inputs carry the 16-bit parallel data output from a protocol device to the transceiver for encoding, serialization, and transmission. This 16-bit parallel data is clocked into the transceiver on the rising edge of GTX_CLK as shown in Figure 10.
TKMSB	20	I	K-code generator (MSB). When TKMSB is active an 8-bit/10-bit K code is transmitted as controlled by data bits TXD8 −TXD15. When TKMSB is inactive an 8-bit/10-bit D code is transmitted as controlled by data bits TXD8 − TXD15.
TKLSB	22	I	K-code generator (LSB). When TKLSB is active an 8-bit/10-bit K code is transmitted as controlled by data bits TXD0 −TXD7. When TKLSB is inactive an8-bit/10-bit D code is transmitted as controlled by data bits TXD0 − TXD7.
V_{DD}	1, 9, 23, 38, 48		Digital logic power. Provides power for all digital circuitry and digital I/O buffers.
V_{DDA}	55, 57		Analog power. V_{DDA} provides a supply reference for the high-speed analog circuits, receiver and transmitter

detailed description

transmit interface

The transmitter portion registers valid incoming 16-bit wide data (TXD[0:15]) on the rising edge of the GTX_CLK. The data is then 8-bit/10-bit encoded, serialized, and transmitted sequentially over the differential high-speed I/O channel. The clock multiplier multiplies the reference clock (GTX_CLK) by a factor of 10 times, creating a bit clock. This internal bit clock is fed to the parallel-to-serial shift register which transmits data on both the rising and falling edges of the bit clock, providing a serial data rate that is 20 times the reference clock. Data is transmitted LSB (D0) first.

detailed description (continued)

transmit data bus

The transmit bus interface accepts 16-bit single-ended TTL parallel data at the TXD[0:15] terminals. Data and k-code control is valid on the rising edge of the GTX_CLK. The GTX_CLK is used as the word clock. The data, k-code, and clock signals must be properly aligned as shown in Figure 2. Detailed timing information can be found in the electrical characteristics table**.**

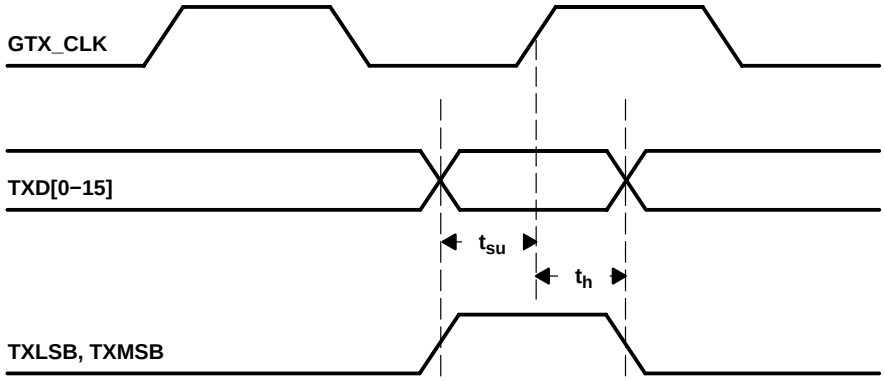


Figure 2. Transmit Timing Waveform

transmission latency

The data transmission latency of the TLK2701 is defined as the delay from the initial 16-bit word load to the serial transmission of bit 0. The transmit latency is fixed once the link is established. However, due to silicon process variations and implementation variables such as supply voltage and temperature, the exact delay will vary slightly. The minimum transmit latency ($T_{latency}$) is 34 bit times; the maximum is 38 bit times. Figure 3 illustrates the timing relationship between the transmit data bus, the GTX_CLK and serial transmit terminals.

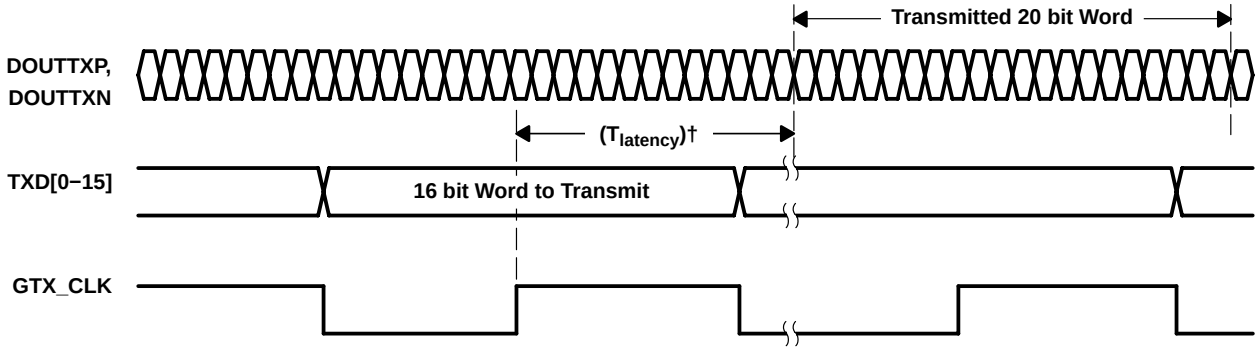


Figure 3. Transmitter Latency

8-bit/10-bit encoder

All true serial interfaces require a method of encoding to insure minimum transition density so that the receiving PLL has a minimal number of transitions to stay locked on. The encoding scheme maintains the signal dc balance by keeping the number of ones and zeros the same. This provides good transition density for clock recovery and improves error checking. The TLK2701 uses the 8-bit/10-bit encoding algorithm that is used by fibre channel and gigabit ethernet. This is transparent to the user, as the TLK2701 internally encodes and decodes the data such that the user reads and writes actual 16-bit data.

8-bit/10-bit encoder (continued)

The 8-bit/10-bit encoder converts 8-bit wide data to a 10-bit wide encoded data character to improve its transmission characteristics. Since the TLK2701 is a 16-bit wide interface, the data is split into two 8-bit wide bytes for encoding. Each byte is fed into a separate encoder. The encoding is dependant upon two additional input signals, the TKMSB and TKLSB.

Table 1. Transmit Data Controls

TKLSB	TKMSB	DECODED 20 BIT OUTPUT	
0	0	Valid data on TXD(0−7),	Valid data TXD(8−15)
0	1	Valid data on TXD(0−7),	K code on TXD(8−15)
1	0	K code on TXD(0−7),	Valid data on TXD(8−15)
1	1	K code on TXD(0−7),	K code on TXD(8−15)

PRBS generator

The TLK2701 has a built-in 2^7-1 PRBS (pseudorandom bit stream) function. When the PRBSEN terminal is forced high, the PRBS test is enabled. A PRBS is generated and fed into the 10-bit parallel-to-serial converter input register. Data from the normal input source is ignored during the PRBS mode. The PRBS pattern is then fed through the transmit circuitry as if it were normal data and sent out to the transmitter. The output can be sent to a BERT (bit error rate tester), the receiver of another TLK2701, or can be looped back to the receive input. Since the PRBS is not really random but a predetermined sequence of ones and zeroes, the data can be captured and checked for errors by a BERT.

parallel-to-serial

The parallel-to-serial shift register takes in the 20-bit wide data word multiplexed from the two parallel 8-bit/10-bit encoders and converts it to a serial stream. The shift register is clocked on both the rising and falling edge of the internally generated bit clock, which is 10 times the GTX_CLK input frequency. The LSB (D0) is transmitted first.

high-speed data output

The high-speed data output driver consists of a current-mode logic (CML) differential pair that can be optimized for a particular transmission line impedance and length. The line can be directly-coupled or ac-coupled. Refer to Figure 15 and Figure 16 for termination details.

receive interface

The receiver portion of the TLK2701 accepts 8-bit/10-bit encoded differential serial data. The interpolator and clock recovery circuit will lock to the data stream and extract the bit rate clock. This recovered clock is used to retime the input data stream. The serial data is then aligned to two separate 10-bit word boundaries, 8-bit/10-bit decoded and output on a 16-bit wide parallel bus synchronized to the extracted receive clock.

detailed description (continued)

receive data bus

The receive bus interface drives 16-bit wide single-ended TTL parallel data at the RXD[0:15] terminals. Data is valid on the rising edge of the RX_CLK The RX_CLK is used as the recovered word clock. The data, enable, and clock signals are aligned as shown in Figure 4. Detailed timing information can be found in the switching characteristics table**.**

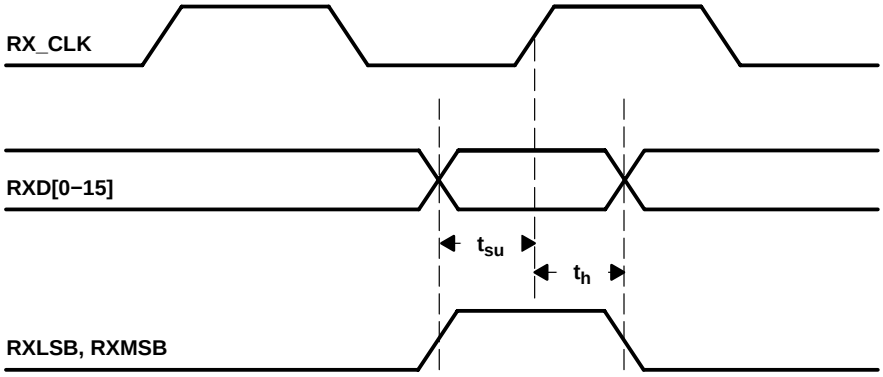


Figure 4. Receive Timing Waveform

data reception latency

The serial-to-parallel data receive latency is the time from when the first bit arrives at the receiver until it is output in the aligned parallel word with RXD0 received as first bit. The receive latency is fixed once the link is established. However, due to silicon process variations and implementation variables such as supply voltage and temperature, the exact delay will vary slightly. The minimum receive latency ($R_{latency}$) is 76 bit times; the maximum is 107 bit times. Figure 5 illustrates the timing relationship between the serial receive terminals, the recovered word clock (RX_CLK), and the receive data bus.

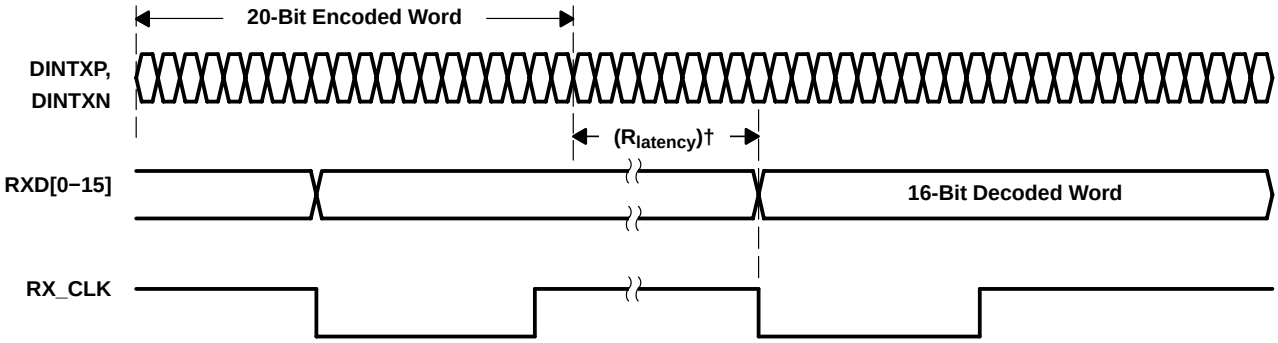


Figure 5. Receiver Latency

serial-to-parallel

Serial data is received on the DINRXP and DINRXN terminals. The interpolator and clock recovery circuit will lock to the data stream if the clock to be recovered is within 200 PPM of the internally generated bit rate clock. The recovered clock is used to retime the input data stream. The serial data is then clocked into the serial-to-parallel shift registers. The 10-bit wide parallel data is then multiplexed and fed into two separate 8-bit/10-bit decoders where the data is then synchronized to the incoming data steam word boundary by detection of the comma 8-bit/10-bit synchronization pattern.

detailed description (continued)

comma detect and 8-bit/10-bit decoding

The TLK2701 has two parallel 8-bit/10-bit decode circuits. Each 8-bit/10-bit decoder converts 10 bit encoded data (half of the 20 bit received word) back into 8-bits. The comma detect circuit is designed to provide for byte synchronization to an 8-bit/10-bit transmission code. When parallel data is clocked into a parallel to serial converter, the byte boundary that was associated with the parallel data is now lost in the serialization of the data. When the serial data is received and converted to parallel format again, a way is needed to recognize the byte boundary. Generally this is accomplished through the use of a synchronization pattern. This is generally a unique pattern of 1s and 0s that either cannot occur as part of valid data or is a pattern that repeats at defined intervals. The 8-bit/10-bit encoding contains a character called the comma (b0011111 or b1100000), which is used by the comma detect circuit on the TLK2701 to align the received serial data back to its original byte boundary. The decoder detects the comma, generating a synchronization signal aligning the data to their 10-bit boundaries for decoding; the comma is mapped into the LSB. It then converts the data back into 8-bit data. The output from the two decoders is latched into the 16-bit register synchronized to the recovered parallel data clock (RX_CLK) and output valid on the rising edge of the RX_CLK.

NOTE:

The TLK2701 only achieves byte alignment on the 0011111 comma.

Decoding provides two additional status signals, RKLSB and RKMSB. When RKLSB is asserted , an 8-bit/10-bit K code was received and the specific K code is presented on the data bits RXD0 − RXD7, else an 8-bit/10-bit D code was received. When TKMSB is asserted, an 8-bit/10-bit K code was received and the specific K code is presented on data bits RXD8 − RXD15, else an 8-bit/10-bit D code was received. The valid K codes the TLK2701 will decode are provided in Table 3. An error detected on either byte, including K codes not in Table 3, will cause that byte only to indicate a K0.0 code on the RK×SB and associated data pins, where K0.0 is known to be an invalid 8-bit/10-bit code. A loss of input signal will cause a K31.7 code to be presented on both bytes, where K31.7 is also known to be an invalid 8-bit/10-bit code.

Table 2. Receive Status Signals

RKLSB	RKMSB	DECODED 20 BIT OUTPUT	
0	0	Valid data on RXD(0−7),	Valid data RXD(8−15)
0	1	Valid data on RXD(0−7),	K code on RXD(8−15)
1	0	K code on RXD(0−7),	Valid data on RXD(8−15)
1	1	K code on RXD(0−7),	K code on RXD(8−15)

Table 3. Valid K Characters

K CHARACTER	RECEIVE DATA BUS (RXD[7−0]) OR (RXD[15−8])
K28.0	000 11100
K28.1	001 11100
K28.2	010 11100
K28.3	011 11100
K28.4	100 11100
K28.5	101 11100
K28.6	110 11100
K28.7	111 11100
K23.7	111 10111
K27.7	111 11011
K29.7	111 11101
K30.7	111 11110

detailed description (continued)

power down mode

When the ENABLE pin is deasserted low, the TLK2701 will go into a power down mode. In the power down mode, the serial transmit pins (DOUTTXP, DOUTTXN), the receive data bus pins (RXD[0:15]), and RKLSB will go into a high-impedance state. In the power down condition, the signal detection circuit draws less than 15 mW. When the TLK2701 is in the power-down mode, the clock signal on the GTX_CLK terminal must be provided.

loss of signal detection

The TLK2701 has a loss of signal detection circuit for conditions where the incoming signal no longer has a sufficient voltage level to keep the clock recovery circuit in lock. The signal detection circuit is intended to be an indication of gross signal error conditions, such as a detached cable or no signal being transmitted, and not an indication of signal coding health. The TLK2701 reports this condition by asserting, the RKMSB/LOS, RKLSB and RXD[0:15] all to a high state. As long as the signal is above 200 mV in differential magnitude, the LOS circuit will not signal an error condition.

PRBS verification

The TLK2701 also has a built-in BERT function in the receiver side that is enabled by the PRBSEN. It can check for errors and report the errors by forcing the RKLSB/PRBSPASS terminal low.

reference clock input

The reference clock (GTX_CLK) is an external input clock that synchronizes the transmitter interface. The reference clock is then multiplied in frequency 10 times to produce the internal serialization bit clock. The internal serialization bit clock is frequency-locked to the reference clock and used to clock out the serial transmit data on both its rising and falling edge clock, providing a serial data rate that is 20 times the reference clock.

operating frequency range

The TLK2701 may operate at a serial data rate between 1.6 Gbps to 2.7 Gbps. The GTX_CLK must be within ±100 PPM of the desired parallel data rate clock.

testability

The TLK2701 has a comprehensive suite of built-in self-tests. The loopback function provides for at-speed testing of the transmit/receive portions of the circuitry. The enable terminal allows for all circuitry to be disabled so that an I_{DDQ} test can be performed. The PRBS function allows for a BIST (built-in self-test).

loopback testing

The transceiver can provide a self-test function by enabling (LOOPEN) the internal loop-back path. Enabling this terminal will cause serial-transmitted data to be routed internally to the receiver. The parallel data output can be compared to the parallel input data for functional verification. (The external differential output is held in a high-impedance state during the loopback testing.)

built-in self-test (BIST)

The TLK2701 has a BIST function. By combining PRBS with loopback, an effective self-test of all the circuitry running at full speed can be realized. The successful completion of the BIST is reported on the RKLSB/ PRBS_PASS terminal.

power-on reset

Upon application of minimum valid power, the TLK2701 generates a power-on reset. During the power-on reset the RXD, RKLSB, and RKMSB/LOS signal terminals go to a high-impedance state. The RX_CLK is held low. The length of the power-on reset cycle is dependent upon the REFCLK frequency, but is less than 1 ms.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) . . . . . −0.3 to 3 V
Voltage range at TXD, ENABLE, GTX_CLK, TKLMSB, TKLLSB, LOOPEN, PRBS_PASS . . . . . −0.3 to 4 V
Voltage range at any other terminal except above . . . . . −0.3 to V_{DD}+0.3 V
Package power dissipation, P_D . . . . . See Dissipation Rating Table
Storage temperature, T_{stg} . . . . . −65°C to 150°C
Electrostatic discharge . . . . . HBM:2 kV, CDM:1 kV
Characterized free-air operating temperature range, T_A . . . . . −40°C to 85°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential I/O bus voltages, are with respect to network ground.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR‡ ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
RCP64§	5.25 W	46.58 mW/°C	2.89 W
RCP64¶	3.17 W	23.70 mW/°C	1.74 W
RCP64#	2.01 W	13.19 mW/°C	1.11 W

‡ This is the inverse of the traditional junction-to-ambient thermal resistance ($R_{\theta JA}$).
§ 2 oz. Trace and copper pad with solder.
¶ 2 oz. Trace and copper pad without solder.
# Standard JEDEC High-K board.

For more information, refer to TI application note *PowerPAD Thermally Enhanced Package,* TI literature number SLMA002.

electrical characteristics over recommended operating conditions

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		2.3	2.5	2.7	V
Supply current, I_{CC}	Frequency = 1.6 Gbps, PRBS pattern		105		mA
	Frequency = 2.7 Gbps, PRBS pattern		156		
Power dissipation, P_D	Frequency = 1.6 Gbps, PRBS pattern		262		mW
	Frequency = 2.7 Gbps, PRBS pattern		390		mW
	Frequency = 2.7 Gbps, worst case pattern‖			500	mW
Shutdown current	Enable = 0, V_{DDA}, V_{DD} terminals, V_{DD} = MAX		3		mA
PLL startup lock time	V_{DD},V_{DDC} = 2.3V		0.1	0.4	ms
Operating free-air temperature, T_A		−40		85	°C

‖ Worst case pattern is a pattern that creates a maximum transition density on the serial transceiver.

reference clock (GTX_CLK) timing requirements over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency	Minimum data rate	Typ−0.01%	80	Typ+0.01%	MHz
Frequency	Maximum data rate	Typ−0.01%	135	Typ+0.01%	MHz
Frequency tolerance		−100		100	ppm
Duty cycle		40%	50%	60%	
Jitter	Peak-to-peak			40	ps

TTL input electrical characteristics over recommended operating conditions (unless otherwise noted), TTL signals: TXDO−TXD15, GTX_CLK, LOOPEN, LCKREFN, PRBS_PASS, TKLSB, TKMSB

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
V_{IH}	High-level input voltage	See Figure 10	2		3.6	V
V_{IL}	Low-level input voltage	See Figure 10			0.80	V
I_{IL}	Input high current	V_{DD} = MAX, V_{IN} = 2 V			40	μA
I_{IH}	Input low current	V_{DD} = MAX, V_{IN} = 0.4 V	−40			μA
C_I	Receiver input capacitance				4	pF
t_r	Rise time, GTX_CLK, TKMSB, TKLSB, TXD	0.7 V to 1.9 V, C = 5 pF, See Figure 10		1		ns
t_f	Fall time, GTX_CLK, TKMSB, TKLSB, TXD	1.9 V to 0.7 V, C = 5 pF, See Figure 10		1		ns
t_{su}	TXD, TKMSB, TKLSB setup to ↑ GTX_CLK	See Figure 10	1.5			ns
t_h	TXD, TKMSB, TKLSB hold to ↑ GTX_CLK	See Figure 10	0.4			ns

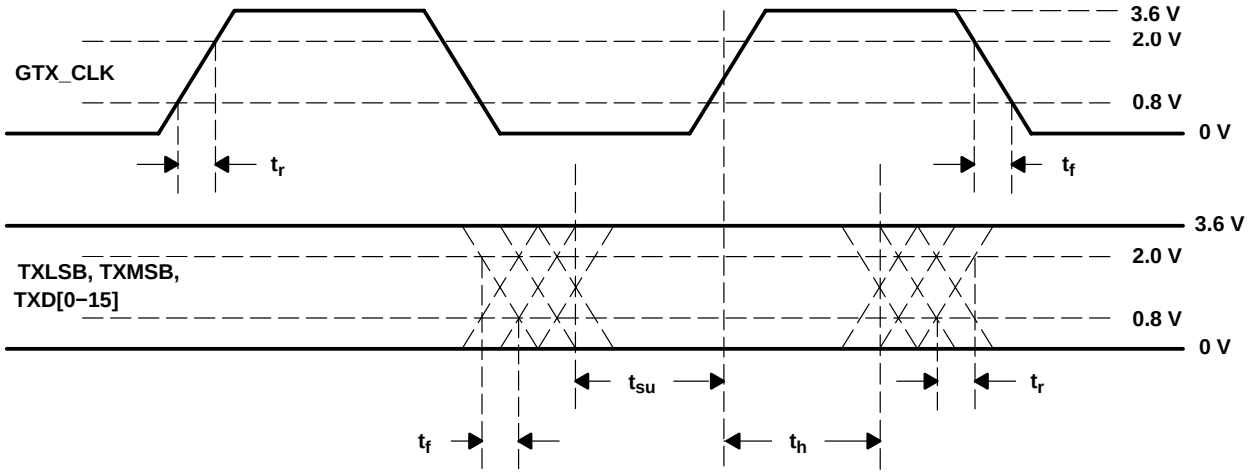


Figure 6. TTL Data Input Valid Levels for AC Measurements

TTL output switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −1 mA, V_{DD} = MIN	1.7	2.3		V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA, V_{DD} = MIN	GND	0.25	0.5	V
$t_{r(slew)}$	Slew rate (rising), magnitude of RX_CLK, RKLSB, RKMSB/LOS, RXD	0.8 V to 2 V, C = 5 pF, See Figure 11	0.5			V/ns
$t_{f(slew)}$	Slew rate (falling), magnitude of RX_CLK, RKLSB, RKMSB/LOS, RXD	0.8 V to 2 V, C = 5 pF, See Figure 11	0.5			V/ns
t_{su}	RXD, RKMSB/LOS, RKLSB setup to ↑ RX_CLK	50% voltage swing, GTX_CLK = 80 MHz, See Figure 11,	5.4			ns
		50% voltage swing, GTX_CLK = 135 MHz, See Figure 11,	2.7			ns
t_h	RXD, RKMSB/LOS, RKLSB hold to ↑ RX_CLK	50% voltage swing, GTX_CLK = 80 MHz, See Figure 11,	5.4			ns
		50% voltage swing, GTX_CLK = 135 MHz, See Figure 11,	2.7			ns

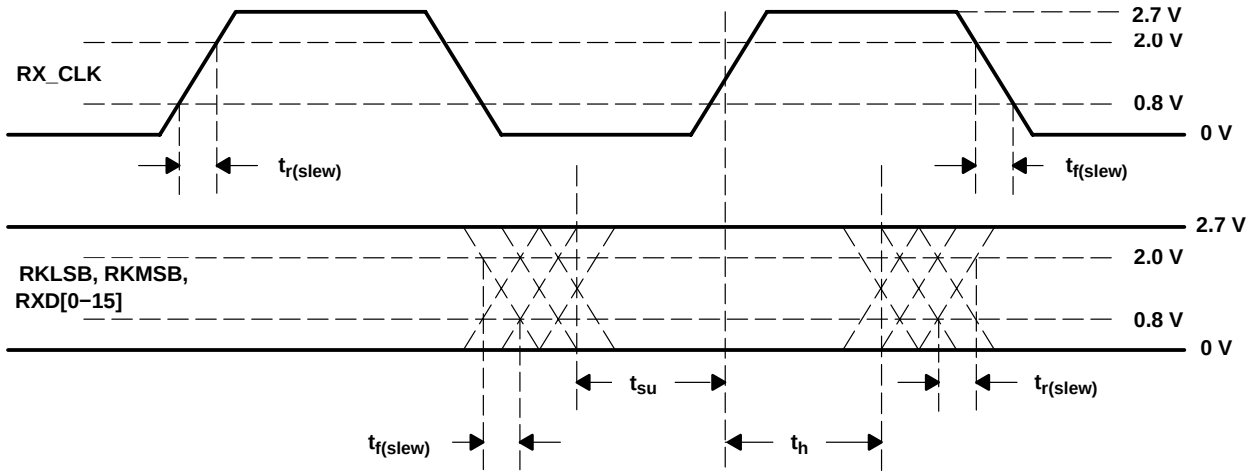


Figure 7. TTL Data Output Valid Levels for AC Measurements

transmitter/receiver characteristics

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$V_{(odp)}$	$V_{(odp)}$ = |VTXP−VTXN|, Preemphasis V_{OD}, direct	R_t = 50 Ω, RREF = 200 Ω, dc-coupled, See Figure 8	840	1050	1260	mV
$V_{(odd)}$	$V_{(odd)}$ = |VTXP−VTXN|, De-emphasis V_{OD}, direct	R_t = 50 Ω, RREF= 200 Ω, dc-coupled, See Figure 8	760	950	1140	mV
$V_{(term)}$	Transmit termination voltage range	R_t = 50 Ω, dc-coupled, See Figure 11			V_{DD}	mV
		R_t = 50 Ω, ac-coupled, See Figure 12	1500		$V_{DD}-V_{ID/2}$	
$V_{(ID)}$	Receiver input voltage requirement, V_{ID}=|RXP – RXN|		200			mV
$V_{(cmv)}$	Receiver common mode voltage range, (VRXP + VRXN)/2		1500		$V_{DD}-V_{ID/2}$	mV
$I_{lkg(R)}$	Receiver input leakage		−10		10	µA
C_I	Receiver input capacitance				2	pF
t_{TJ}	Serial data total jitter (peak-to-peak)	Differential output jitter at 2.7 Gbps, random + deterministic, PRBS pattern		0.15		UI
t_{TJ}	Serial data total jitter (peak-to-peak)	Differential output jitter at 1.6 Gbps, random + deterministic, PRBS pattern		0.15		UI
t_r, t_f	Differential output signal rise, fall time (20% to 80%)	R_L = 50 Ω, C_L = 5 pF, See Figure 12	100	150		ps
	Jitter tolerance	Differential input jitter, random + determinisitc, PRBS pattern at zero crossing	0.60			UI
$T_{(latency)}$	Tx latency		34		38	bits
$R_{(latency)}$	Rx latency		76		107	bits

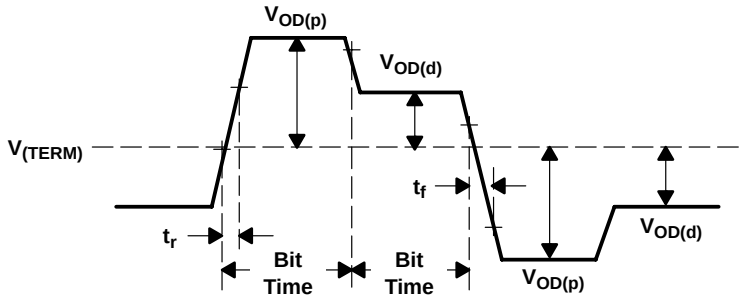


Figure 8. Differential and Common-Mode Output Voltage Definitions

THERMAL INFORMATION

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-free-air thermal resistance	Board-mounted, no air flow, high conductivity TI recommended test board, chip soldered or greased to thermal land		21.47		°C/W
$R_{\theta JC}$	Junction-to-case-thermal resistance			0.38		
$R_{\theta JA}$	Junction-to-free-air thermal resistance	Board-mounted, no air flow, high conductivity TI recommended test board with thermal land but no solder or grease thermal connection to thermal land		42.20		°C/W
$R_{\theta JC}$	Junction-to-case-thermal resistance			0.38		
$R_{\theta JA}$	Junction-to-free-air thermal resistance	Board-mounted, no air flow, JEDEC test board		75.83		°C/W
$R_{\theta JC}$	Junction-to-case-thermal resistance			7.8		

APPLICATION INFORMATION

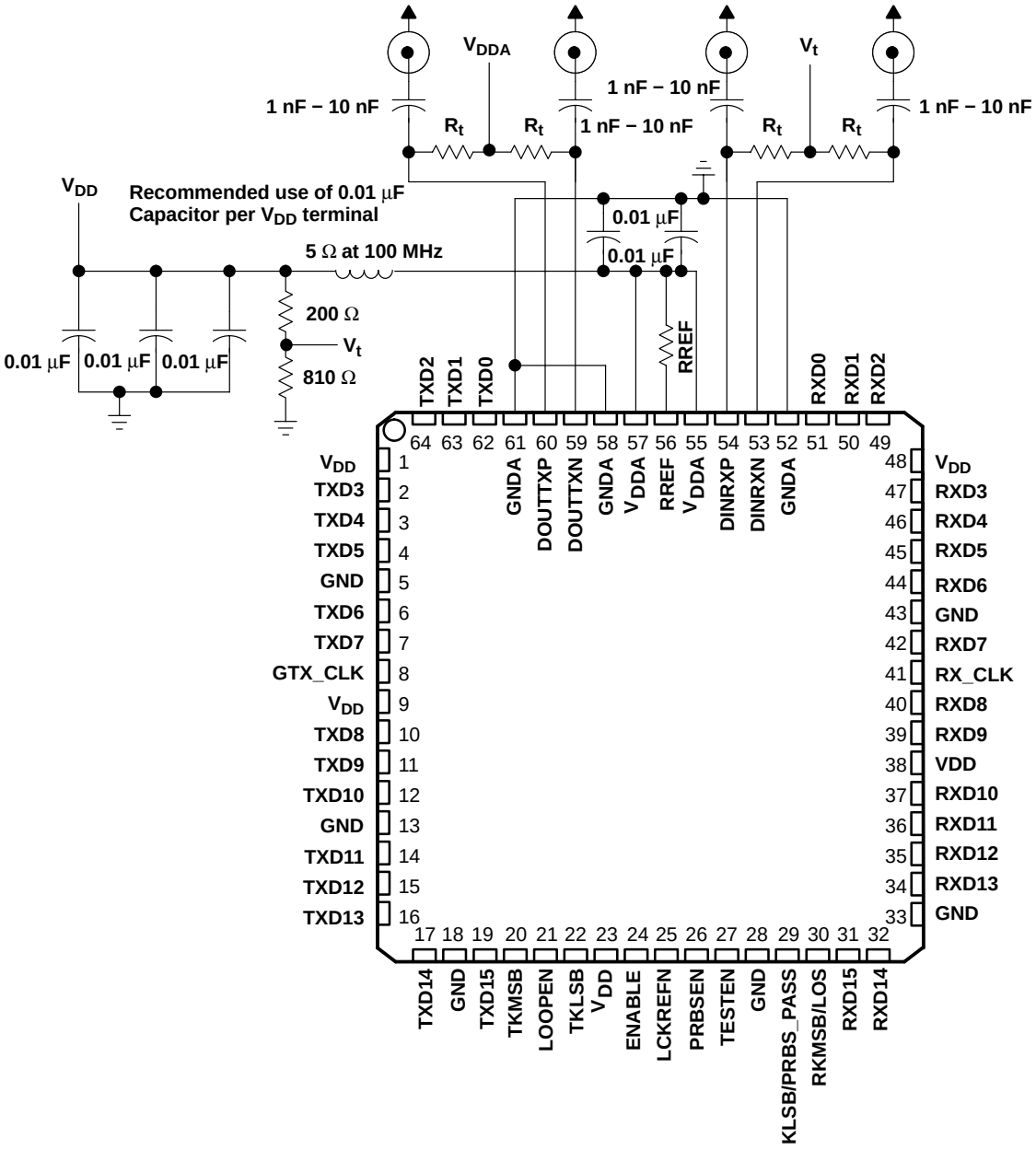


Figure 9. External Component Interconnection

APPLICATION INFORMATION

recommended values of external resistors (1% tolerance)

PARAMETER	TEST CONDITIONS	RECOMMENDED	UNIT
$R_{(t)}$, Termination resistor	50 Ω environment	50	Ω
	75 Ω environment	75	
$R_{(REF)}$, Reference resistor	50 Ω environment	200	Ω
	75 Ω environment	300	

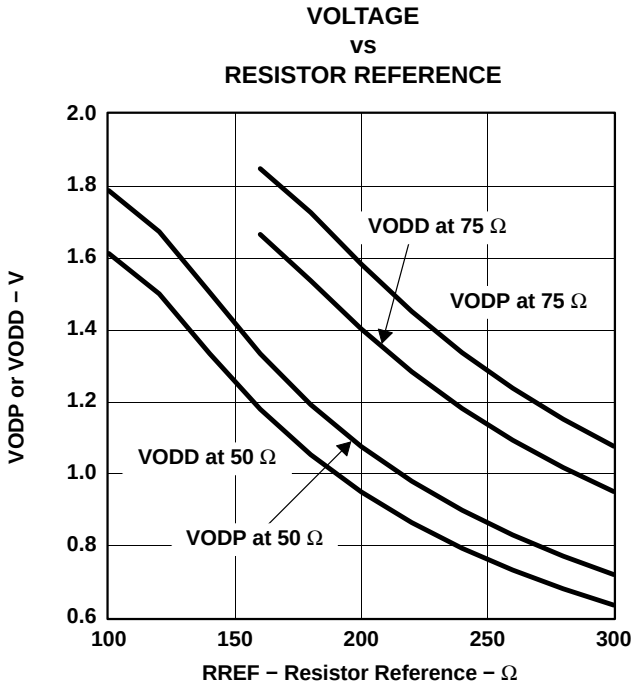
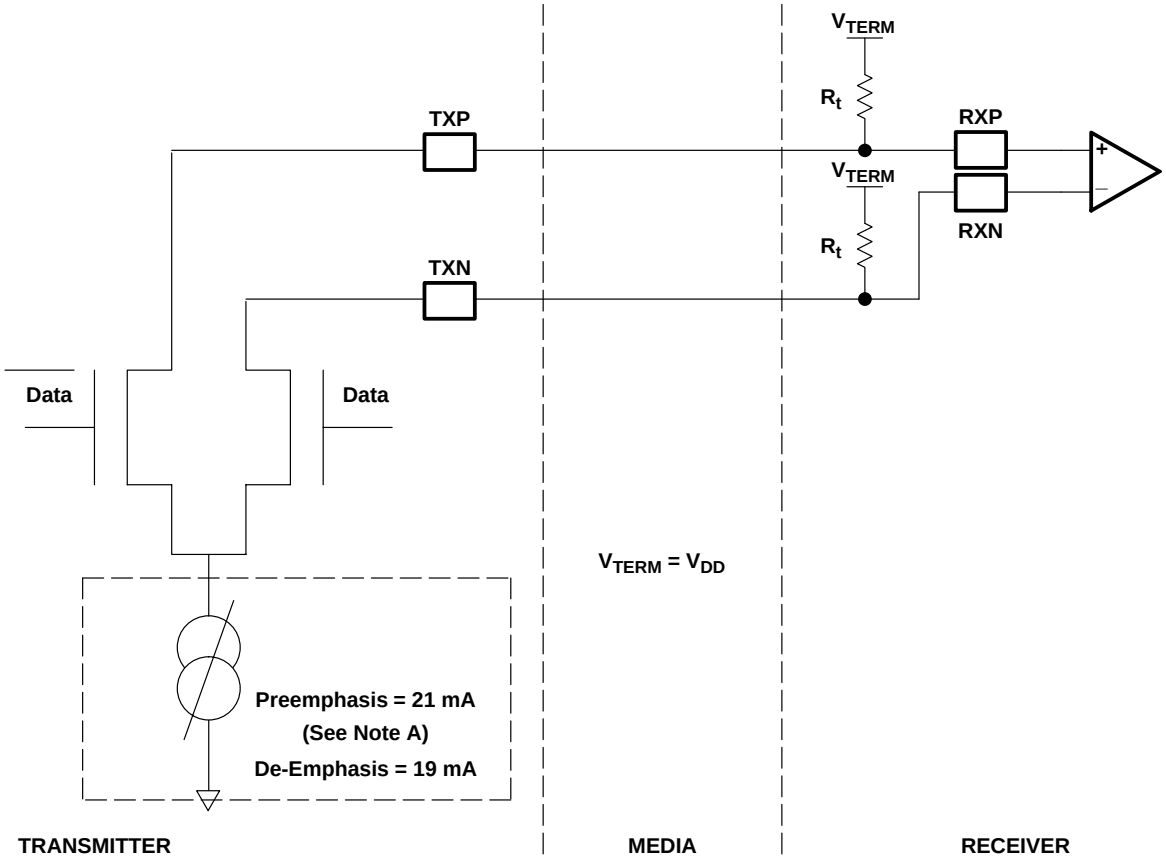


Figure 10. Differential Transmitter Voltage

choosing RREF resistor values

TLK2701 offers the flexibility to customize the voltage swing and transmission line termination by adjusting the reference resistor, RREF, and termination resistor, R_t. By choosing particular resistor values, the system can be optimized for a particular transmission line impedance, length, and controlling the output swing for EMI and attenuation concerns. Refer to Figure 10 to determine the nominal voltage swing and driver current as a function of resistor values. It is recommended that 1% tolerance resistors be used. Refer to Figure 11 for high-speed I/O directly coupled mode and Figure 12 for high-speed I/O ac-coupled mode.

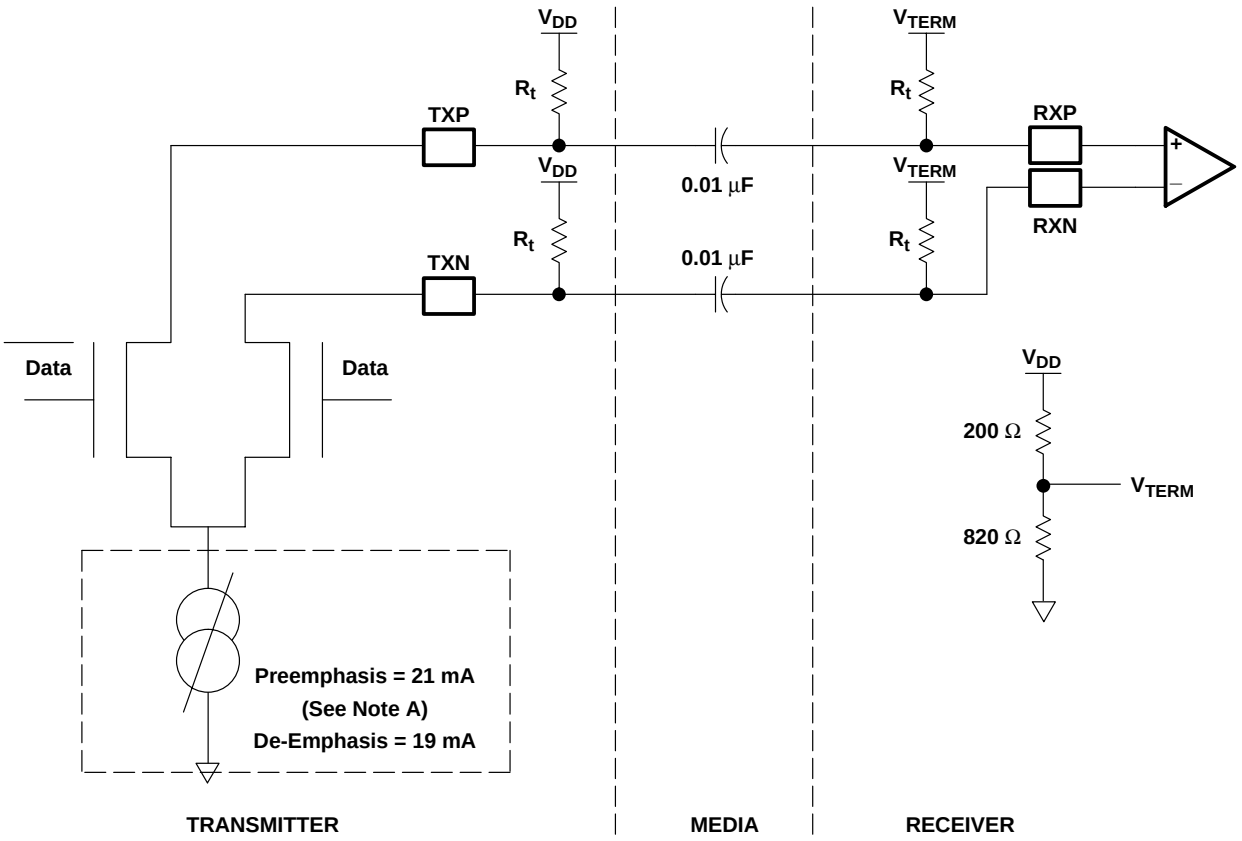
APPLICATION INFORMATION



NOTE A: This assumes RREF = 200 Ω and termination resistance = 50 Ω. See Figure 10 and section *choosing RREF resistor values* for more information.

Figure 11. High-Speed I/O Directly-Coupled Mode

APPLICATION INFORMATION



NOTE A: This assumes RREF = 200 Ω and termination resistance = 50 Ω. See Figure 10 and section *choosing RREF resistor values* for more information.

Figure 12. High-Speed I/O AC-Coupled Mode

APPLICATION INFORMATION

designing with PowerPAD

The TLK2701 is housed in a high-performance, thermally enhanced, 64-pin VQFP (RCP64) PowerPAD package. Use of the PowerPAD package does not require any special considerations except to note that the PowerPAD, which is an exposed die pad on the bottom of the device, is a metallic thermal and electrical conductor. Therefore, if not implementing PowerPAD PCB features, the use of solder masks (or other assembly techniques) may be required to prevent any inadvertent shorting by the exposed PowerPAD of connection etches or vias under the package. It is strongly recommended that the PowerPAD be soldered to the thermal land. The recommended convention, however, is to not run any etches or signal vias under the device, but to have only a grounded thermal land as explained below. Although the actual size of the exposed die pad may vary, the minimum size required for the keep-out area for the 64-pin PFP PowerPAD package is 8 mm X 8 mm.

It is recommended that there be a thermal land, which is an area of solder-tinned-copper, underneath the PowerPAD package. The thermal land will vary in size depending on the PowerPAD package being used, the PCB construction, and the amount of heat that needs to be removed. In addition, the thermal land may or may not contain numerous thermal vias depending on PCB construction.

Other requirements for thermal lands and thermal vias are detailed in the TI application note *PowerPAD Thermally Enhanced Package Application Report*, TI literature number SLMA002, available via the TI Web pages beginning at URL: http://www.ti.com.

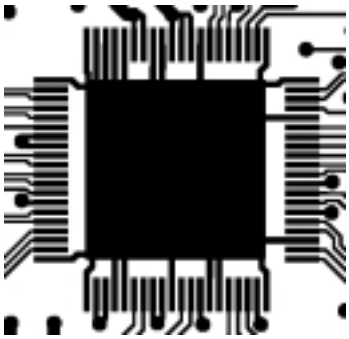


Figure 13. Example of a Thermal Land

For the TLK2701, this thermal land should be grounded to the low-impedance ground plane of the device. This improves not only thermal performance but also the electrical grounding of the device. It is also recommended that the device ground terminal landing pads be connected directly to the grounded thermal land. The land size should be as large as possible without shorting device signal terminals. The thermal land may be soldered to the exposed PowerPAD using standard reflow soldering techniques.

While the thermal land may be electrically floated and configured to remove heat to an external heat sink, it is recommended that the thermal land be connected to the low impedance ground plane for the device. More information may be obtained from the TI application note *PHY Layout*, TI literature number SLLA020.

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