M21204/M21214

SD and HD Cable Equalizers

Rev V2

Applications

- SMPTE Coaxial Cable Interface
- Studio video applications
- Broadcast video applications
- Distribution video applications

Standards Compliance

- SMPTE 259M, SMPTE 292M, SMPTE 344M (at appropriate data rates)
- DVB-ASI (270 Mbps)

Features

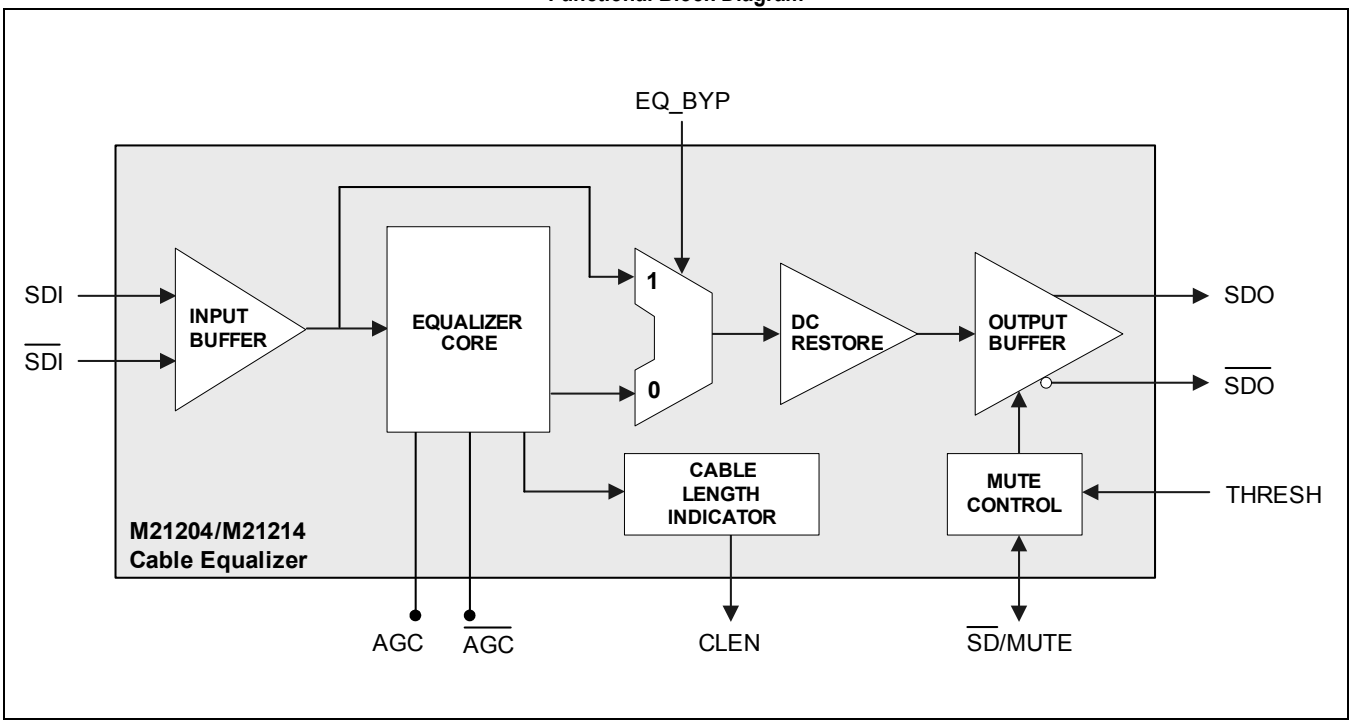
- SMPTE/DVB-ASI compliant at SD and HD (M21214)
- SMPTE/DVB-ASI compliant at SD (M21204)
- Pin for Pin and functionally compatible with GS1524 (M21214)
- Pin for Pin and functionally compatible with GS9064 (M21204)
- Interchangeable PCB footprint for all three devices
- 2.5V or 3.3V Supply
- Low Power (175 mW @ 2.5V, 230 mW @ 3.3V)
- 25 dB typical input return loss with existing matching circuit
- Extended Temperature range: –10 to 85 °C

The M21204/M21214 are high-speed, low-power, adaptive co-axial cable equalizers designed to increase the maximum low-jitter transmission distance of serial digital interface (SDI) video signals and DVB-ASI across commonly used bandwidth-limiting 75Ω coaxial cable. These devices automatically optimize their transfer function based on the bit rate and cable length to minimize the inter-symbol interference (ISI) jitter caused by the cable and to remove the DC offset components introduced with the pathological test pattern and AC coupling in systems.

The M21214 is designed to support at SD and HD data rates from 143 Mbps and 1485 Mbps. The M21204 is designed to support SD data rates between 143 Mbps and 540 Mbps. The low-noise, high-gain equalizer allows for low jitter HD transmissions up to a length of 200m (Belden 1694A) and 120m (Belden 8281). For SD data rates, cable lengths up to 400m (Belden 1694A) and 300m (Belden 8281) are supported.

The M21214 is designed to be a pin-for-pin compatible drop-in replacement for the legacy GS1524, while the M21204 is a pin-for-pin compatible drop-in replacement for the legacy GS9064. These devices offer lower power dissipation, a choice of a 2.5V or 3.3V power supply, for new designs, and increased typical input return loss of 25 dB, depending on installed input BNC connector.

Functional Block Diagram



Ordering Information

Part Number	Package	Operating Data Rate	Operating Temperature
M21204G-xx*	16-pin SOIC (RoHS compliant)	143–540 Mbps	–10 °C to 85 °C
M21214G-xx*	16-pin SOIC (RoHS compliant)	143–1485 Mbps	–10 °C to 85 °C

* Consult the price list for exact part number when ordering.

* The letter 'G' designator after the part number indicates a RoHS-compliant package.

Revision History

Revision	Level	Date	Description
V2	Release	May 2015	Updated logos and page layout. No content changes.
B (V1)	Release	April 2007	Production release. Specification changes to Tables 1-3, 1-5, and 1-6.
A	Preliminary	February 2007	Combined M21204 and M21214 Data Sheets. (replaces 21204-DSH-001-C and 21214-DSH-001-F). Removed 1.8V operation. Removed CLI and MUTE threshold specification.

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1.0 Product Specification

1.1 General Specifications

Table 1-1. Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Units
AV_{DD}	Digital I/O Power	AV_{SS} – 0.5	AV_{SS} + 3.6	V
—	High-speed signal pins	AV_{SS} – 0.5	AV_{SS} + 3.6	V
—	Control/Interface Pins	AV_{SS} – 0.5	AV_{SS} + 3.6	V
T_{STORE}	Storage Temperature	–65	+150	°C
ESD_{HBML}	Human Body Model (low-speed)	2000	—	V
ESD_{HBMH}	Human Body Model (high-speed)	2000	—	V
ESD_{CDM}	Charge Device Model	500	—	V

NOTE:

No Damage.

Table 1-2. Recommended Operating Conditions

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
AV_{DD}	Power	1	–5%	2.5/3.3	+5%	V
T_A	Ambient Temperature	—	–10	—	+85	°C
θ_{JA}	Junction to Ambient Thermal Resistance	—	—	90	—	°C/W

NOTES:

1. Mounted on multi layer board (≥ 4 layers).
2. Airflow = 0.0 m/s.

Table 1-3. Power DC Electrical Specifications

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
Total I_{DD}	Supply Current	1	—	70	90	mA
$P_{DISS2.5V}$	Total Power Dissipation (@2.5V)	1, 2, 3	—	175	236	mW
$P_{DISS3.3V}$	Total Power Dissipation (@3.3V)	1, 2, 3	—	230	312	mW

NOTES:

1. Specified at recommended operating conditions—see Table 1-2.
2. Includes on-chip power dissipation as well as off-chip power dissipated by termination resistors.
3. Typical calculated at nominal supply voltage, maximum calculated at nominal supply voltage + 5%.

1.2 Input/Output Level Specifications

Table 1-4. CMOS Input Electrical Specifications (Logic Signals Only)

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
V_{IH}	Input Logic High Voltage	1	0.75 x AV_{DD}	—	AV_{DD} + 0.3	V
V_{IL}	Input Logic Low Voltage	1	0	—	0.25 x AV_{DD}	V
I_{IH}	Input Current (logic high)	1	–100	—	100	µA
I_{IL}	Input Current (logic low)	1	–100	—	100	µA

NOTE:

1. Specified at recommended operating conditions—see Table 1-2. Spec is for a max load of 20 pF.

Table 1-5. High Speed Input Electrical Specifications

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
DR_{IN}	Input Bit Rate (M21204)	1	143	—	540	Mbps
	Input Bit Rate (M21214)	1	143	—	1485	Mbps
V_{ID}	Input Voltage Range with 0m of cable, p-p, A_{VDD} = 2.5 or 3.3V	1, 5	700	800	1200	mV
V_{ICM}	Input Common-Mode Voltage (AV_{DD} = 3.3V)	1, 4	—	2.75	—	V
	Input Common-Mode Voltage (AV_{DD} = 2.5V)	1, 4	—	1.95	—	V
C_{IN}	Input capacitance	1, 4	—	0.5	—	pF
R_{IN}	Input resistance	1, 4	—	1.6	—	kΩ
S_{11}	Input Return Loss (5 MHz to 1.5 GHz)	1, 2, 3	20	30	—	dB

NOTES:

1. Specified at recommended operation conditions—see Table 1-2.
2. Using the recommended input termination shown in Figure 2-1.
3. Measured single ended.
4. Guaranteed by design.
5. This is also the recommended cable launch level (far end).

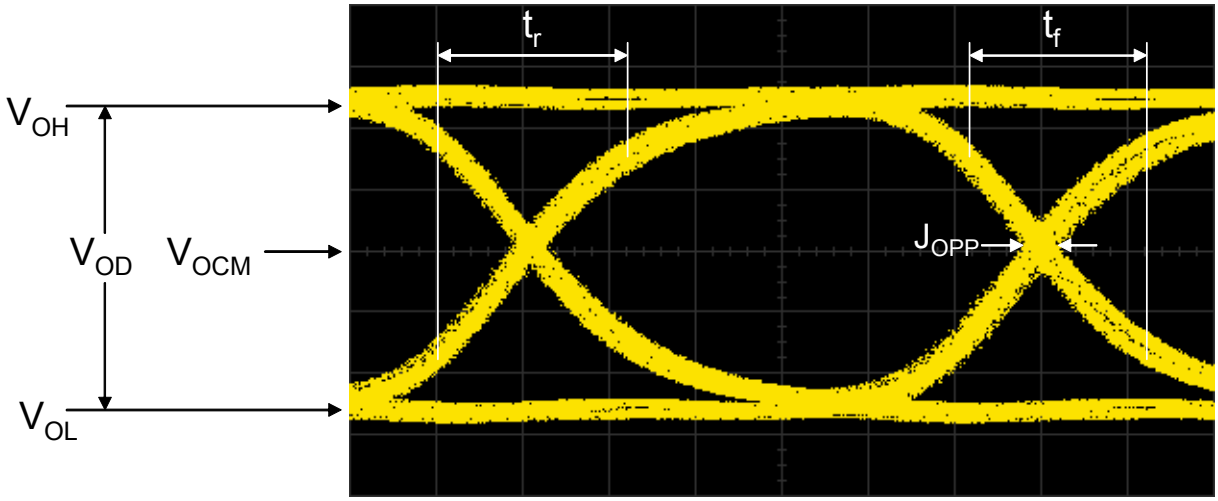
Table 1-6. High Speed Output Electrical Specifications

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
t_r/t_f	Rise/Fall Time (20%–80%), M21204	1, 2, 7	—	500	675	ps
	Rise/Fall Time (20%–80%), M21214	1, 2, 7	—	100	120	ps
t_r/t_{fmm}	Rise/Fall Time Mismatch, M21204	1, 2, 7	—	0	70	ps
	Rise/Fall Time Mismatch, M21214	1, 2, 7	—	0	30	ps
DCD_O	Duty Cycle Distortion (DCD), M21204	1, 2, 5, 6	—	0	50	ps
	Duty Cycle Distortion (DCD), M21214	1, 2, 5, 6	—	0	15	ps
V_{OD}	Differential Output Voltage p-p HiSwEn = 0 (750mV)	1, 3	600	750	950	mV
V_{OCM}	Common mode Voltage HiSwEn = 0 (750mV)	1, 3, 4	—	AV_{DD} – 0.205	—	V
V_{OD}	Differential Output Voltage p-p HiSwEn = 1 (1050mV)	1, 3	850	1050	1270	mV
V_{OCM}	Common mode Voltage HiSwEn = 1 (1050mV)	1, 3, 4	—	AV_{DD} – 0.290	—	V
Z_O	Internal Output Termination Resistance to AV_{DD}	1	40	50	60	Ω

NOTES:

1. Specified at recommended operation conditions—see Table 1-2.
2. With 100Ω differential termination.
3. With 50Ω to AV_{DD} termination.
4. Outputs DC-coupled.
5. Duty Cycle Distortion (DCD) is defined as the difference in the intrinsic jitter at the 50% voltage level and the intrinsic jitter at the rising/falling edge crossing point. If the rising/falling edge crossing point is at the 50% voltage level, then DCD = 0.
6. Measured with a 1010 pattern.
7. Measured with a PRBS23 pattern.

Figure 1-1. Output Symbols Definition



V_{OH}: Average voltage high level
V_{OL}: Average voltage low level
V_{OD}: (VOH) – (VOL)
V_{OCM}: Common Mode Voltage
J_{OPP}: Output Jitter Peak-Peak
t_r: 20-80% Rise Time
t_f: 80-20% Fall Time

NOTE: Waveform above is differential.

1.3 EQ Specifications

Table 1-7. Cable Equalizer Distance Specifications

Symbol	Parameter	Conditions	Notes	Minimum	Typical	Maximum	Units
LEN_{SD}	Max Cable Length	Belden 1694A	1, 3	—	400	—	m
	Max Cable Length	Belden 8281	1, 3	—	300	—	m
LEN_{HD}	Max Cable Length	Belden 1694A	2, 5	—	200	—	m
	Max Cable Length	Belden1694A	2, 4	—	140	—	m
	Max Cable Length	Belden 8281	2, 4	—	120	—	m

NOTES:

Entire table specified at recommended operating conditions—see Table 1-2.

1. Data Rate = 270 Mbps.
2. Data Rate = 1485 Mbps.
3. Error Free with timing Jitter typically = 0.2 UI, pathological pattern.
4. Error Free with alignment Jitter typically = 0.25 UI, pathological pattern.
5. Error Free with alignment jitter typically = 0.3 UI, pathological pattern.

Table 1-8. $\overline{SD}$/MUTE Specifications

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
V_{MUT_LO}	Output voltage when input signal detected	1	—	0.16 x AV_{DD}	—	V
V_{MUT_HI}	Output voltage when input signal not detected	1	—	0.95 x AV_{DD}	—	V

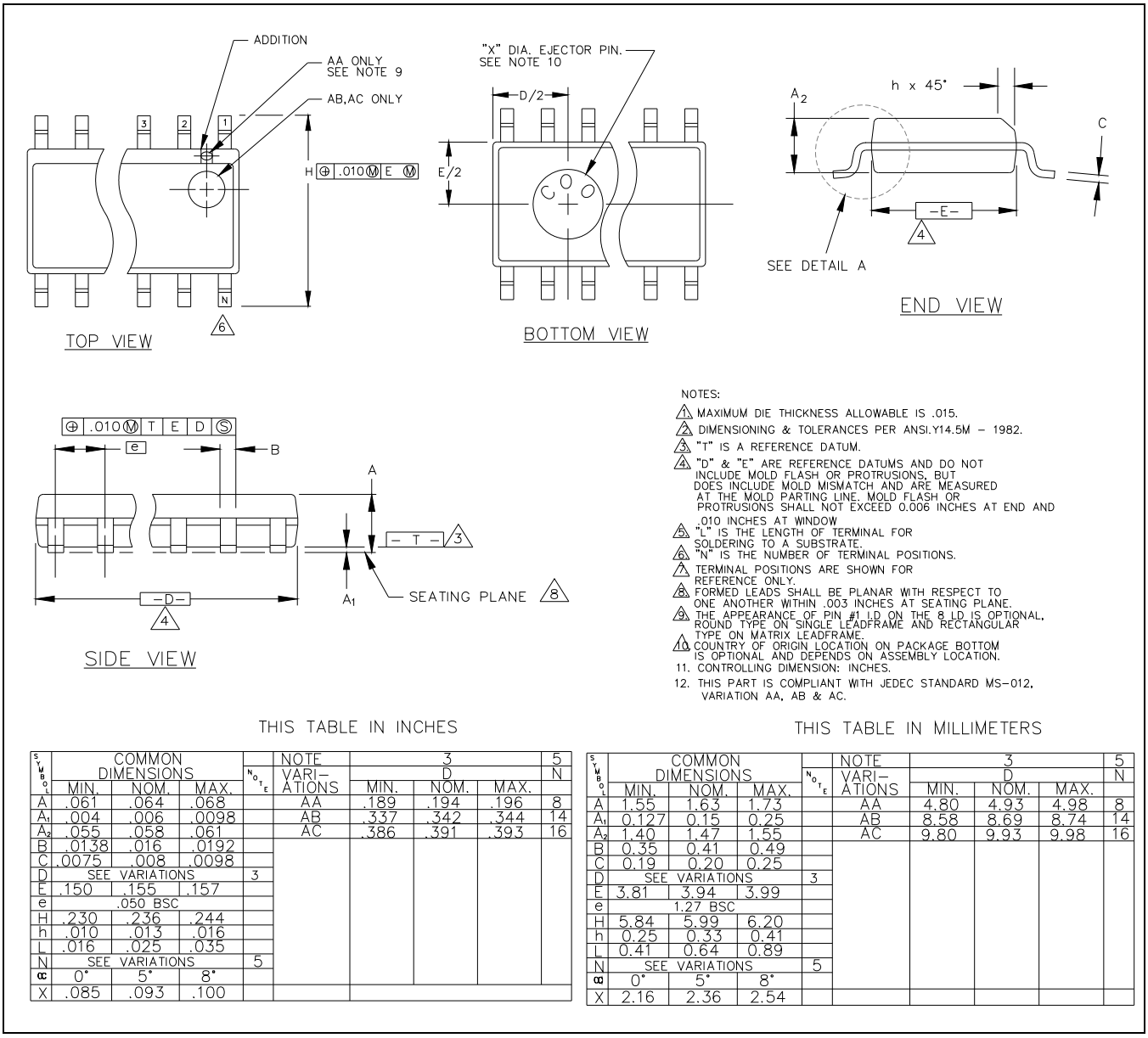
NOTE:

1. Specified at recommended operating condition—see Table 1-2.

1.4 Package Specification

The M21204/M21214 are available in a standard Pb-type package or in a RoHS compliant package. The RoHS package is compliant with standard reflow profiles for Pb-type packages. The package is illustrated in Figure 1-2 below.

Figure 1-2. M21204/M21214 Packaging Details



THIS TABLE IN INCHES

SYMBOL	COMMON DIMENSIONS MIN.	NOM.	MAX.	NOTE	VARIATIONS	D MIN.	D NOM.	D MAX.	N
A	.061	.064	.068		AA	.189	.194	.196	8
A_1	.004	.006	.0098		AB	.337	.342	.344	14
A_2	.055	.058	.061		AC	.386	.391	.393	16
B	.0138	.016	.0192						
C	.0075	.008	.0098						
D	SEE VARIATIONS			3					
E	.150	.155	.157						
e	.050 BSC								
H	.230	.236	.244						
h	.010	.013	.016						
L	.016	.025	.035						
N	SEE VARIATIONS			5					
α	0°	5°	8°						
X	.085	.093	.100						

THIS TABLE IN MILLIMETERS

SYMBOL	COMMON DIMENSIONS MIN.	NOM.	MAX.	NOTE	VARIATIONS	D MIN.	D NOM.	D MAX.	N
A	1.55	1.63	1.73		AA	4.80	4.93	4.98	8
A_1	0.127	0.15	0.25		AB	8.58	8.69	8.74	14
A_2	1.40	1.47	1.55		AC	9.80	9.93	9.98	16
B	0.35	0.41	0.49						
C	0.19	0.20	0.25						
D	SEE VARIATIONS			3					
E	3.81	3.94	3.99						
e	1.27 BSC								
H	5.84	5.99	6.20						
h	0.25	0.33	0.41						
L	0.41	0.64	0.89						
N	SEE VARIATIONS			5					
α	0°	5°	8°						
X	2.16	2.36	2.54						

1.5 Manufactureability

The values shown in this section may change; however, these are standard requirements.

1.5.1 Electrostatic Discharge

Tested per JESD22-A114. This device passes 2000V of ESD Human Body Model (HBM) testing.
Tested per JESD22-C101. This device passes 500V of ESD Charged Device Model (CDM) testing.
Tested per EIA/JESD78. This device passes 150mA of trigger current at 85°C during Latchup testing.

1.5.2 Peak Reflow Temperature

M21204G/M21214G (RoHS compliant package): Peak reflow temperature is 260°C per JEDEC standards.

1.5.3 Moisture Sensitivity Level (MSL)

All versions of this device (Std Pb-type and RoHS compliant packages) are Moisture Sensitivity Level (MSL) 3 per J-STD-020B and J-STD-033.

1.6 Design Considerations

For drop-in compatible applications the M21204/M21214 will be constrained to operate within an existing PCB layout. For new designs, the M21204/M21214 may use the existing legacy layout or it may be operated with 2.5V power supply rails.

See Digital Video Interfacing Application Note (212xx-APP-001-A) for guidance on the following:

- Component Placement and Layout
- Routing Considerations

1.6.1 Thermal Considerations

The M21204/M21214 consume less power than the legacy GS9064/GS1524 devices, therefore for existing designs, the M21204/M21214 will contribute less thermal energy and should result in a lower operating temperature.

2.0 Functional Description

2.1 Pin Descriptions

2.1.1 General Nomenclature

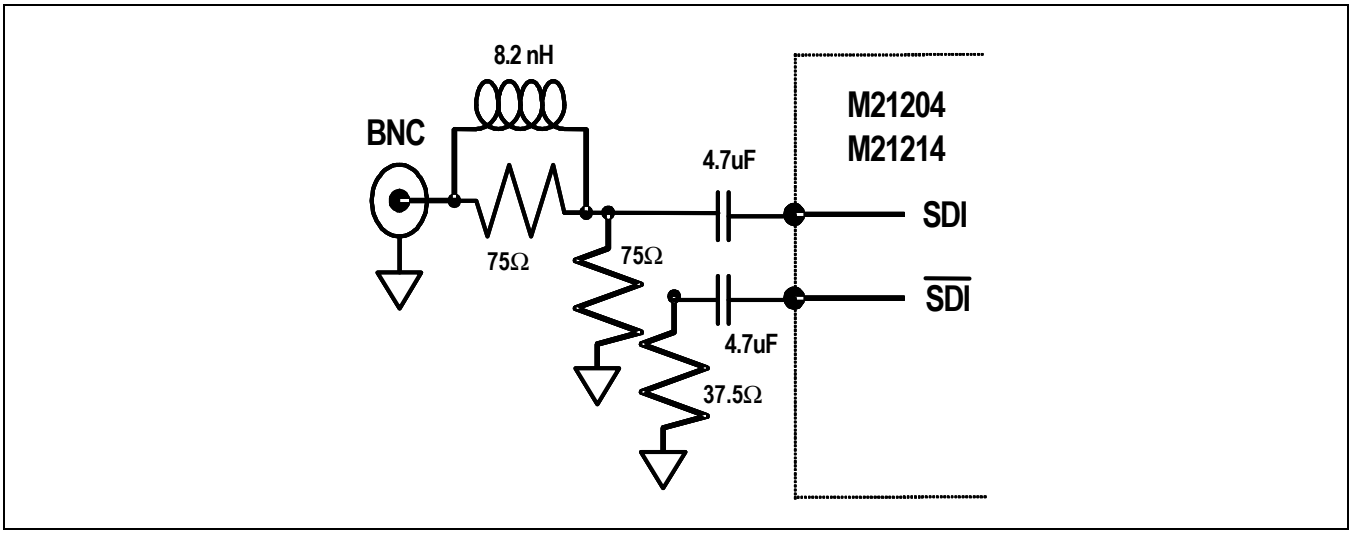
Through out this data sheet, physical pins will be denoted in **BOLD** print. An array of pins can be called by each individual pin name (e.g. **MF0, MF1, MF2, MF3**, and **MF6**) or as an array (e.g. **MF[6, 5..0]** or **MF[6:0]**).

2.1.2 High-Speed Input

Digital video coaxial cables are AC coupled to the high-speed low-noise inputs, **SDI/$\overline{\text{SDI}}$**, which, are designed to operate in both the single-ended or differential mode. The typical application is single-ended into the non-inverting **SDI** input with the inverting **SDI** input biased to match the bias on the used input.

For GS9064/GS1524 drop-in compatibility, the M21204/M21214 do not contain any internal input terminations and require both external input termination as well as the matching circuit to exceed the SMPTE input return loss specifications. The package and IC design of the M21204/M21214 have been optimized for high-speed performance allowing them to exceed the SMPTE return loss spec by 5dB to 10dB using the recommended external matching/termination network and commonly employed through-hole, or vertical mount 75Ω BNC connectors. For non-inverting single-ended operation, the recommended input circuit is shown in Figure 2-1. For differential operation, the matching/termination circuit on **SDI** should be duplicated on **$\overline{\text{SDI}}$**. The internal pull ups automatically bias **SDI/$\overline{\text{SDI}}$** to 0.72 x **AV_{DD}** for proper AC coupled operation.

Figure 2-1. Single-ended Typical Input Matching/Termination Network



2.1.3 High-Speed Output

The high-speed differential outputs after equalization are made available on the **SDO/$\overline{\text{SDO}}$** pins. The M21204/M21214 support power supply voltages of 2.5V or 3.3V. For backwards compatibility with a 3.3V power supply, the M21204/M21214 output swing and common-mode is compatible with the GS9064 and GS1524, respectively.

2.1.4 Adaptive Equalization Selection

In typical operation, the adaptive equalization is enabled with **EQ_BYP** = Low, however, with **EQ_BYP** = High, the adaptive equalization and DC restore circuits are bypassed and the input is fed directly to the output.

2.1.5 Cable Length Indicator

When the adaptive equalization is enabled (EQ_BYP = Low), an analog voltage inversely proportional to the cable length is made available on CLEN. The same transfer function applies to all bit rates. When the adaptive equalization is disabled (EQ_BYP = High), the voltage falls to its highest value (this indicates 0m cable length). During an LOS (Loss Of input Signal) event, the voltage falls to its lowest value.

2.1.6 Output Mute and Signal Detect

When configured as an input by forcing a voltage on **$\overline{\text{SD}}$/MUTE** = High (Vdd), the output of the M21204/M21214 will be inhibited at logic low (outputs muted). When **SD/MUTE** = Low (Vss), the output is never muted and the programmable cable length based mute function is disabled.

When tied to a high-impedance input or left floating, the programmable inhibit based on cable length is enabled and the pin is defined as an LOS output (logic). In the event of an LOS, the output is muted. The inhibit threshold is set with an analog voltage applied to the **THRESH** input pin, this threshold will depend on cable type (e.g. Belden 1694A or 8281).

2.1.7 Equalizer Detailed Description

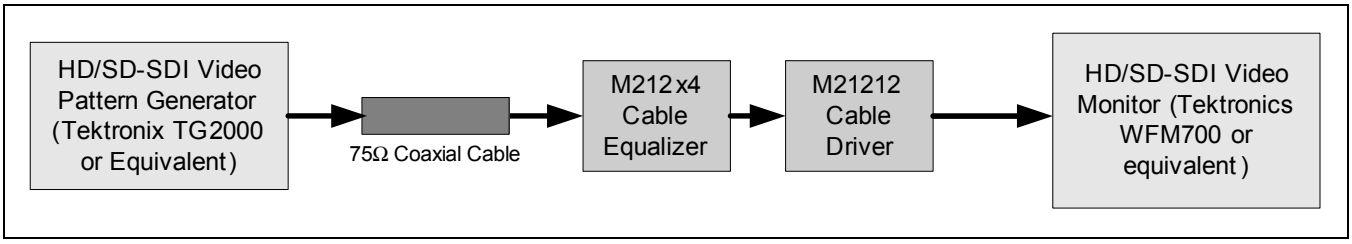
The basic equalizer design consists of interlaced stages of gain and equalization to maximize both the overall equalization gain as well as the input sensitivity for maximum performance with minimum jitter. In order to achieve maximum cable distances, the equalizer has over 50 dB of broadband signal boost and maintains an input sensitivity of approximately 10 mV. Using a high-performance silicon process, high gain-bandwidth products are achieved allowing for high-performance, wide dynamic range design with minimum power dissipation.

Since 270 Mbps and 1.485 Gbps signals are launched with different SMPTE specified rise and fall times which can vary substantially (especially at the receive end after going though a wide dynamic range of valid cable lengths) the M21204/M21214 equalization routine determines both the bit rate and the resultant signal HF attenuation as opposed to just looking at the launch edge rates. By determining both sets of conditions, it is possible to optimize the equalizer for both HD and SD performance. Therefore, the M21204/M21214 maintain the same maximum cable length as optimized SD only equalizers. For example, a SD signal through a short cable can have the same edge rate as a HD signal through a long cable; yet, both conditions require different levels of equalization as well as different optimized inverse-transfer functions. The advanced equalization technology can make the distinction between the two cases for optimal performance. This also leads to proper mute threshold (**THRESH**) and cable length indicator (**CLEN**) operation that is independent of the bit rate.

In order to accommodate both the SMPTE worst case equalizer pathological patterns as well as some customer derived worst case DC offset patterns, a high-gain slicer is included in the signal path to correct for any eye-crossing wander due to AC coupling of the input.

Figure 2-2 shows the test setup used by MACOM to evaluate the performance of the M21204/M21214 cable equalizers.

Figure 2-2. Test Setup Diagram for M21204/M21214 Cable Equalizer Evaluation



2.2 M21204/M21214 Common Signals by Interface Group

Table 2-1. Power Pins

Pin Name	Pin Number	Function	Type
AV_{SS}	3, 6, 11, 14	Ground	Power
AV_{DD}	2, 15	Positive Supply	Power

Table 2-2. High-speed Signal Pins

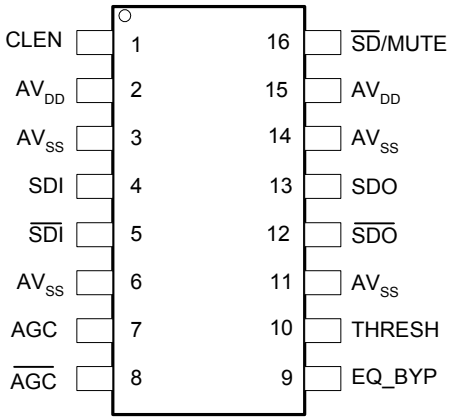
Pin Name	Pin Number	Function	Default	Type
SDI/$\overline{\text{SDI}}$	4, 5	Non-inverting and Inverting Serial Data Input to the adaptive equalizer	GS9064/GS1524 compatible at 3.3V and external termination required.	I—AC coupled high speed
SDO/$\overline{\text{SDO}}$	13, 12	Non-inverting and Inverting Serial Data Output	GS9064/GS1524 compatible at 3.3V	O—high speed CML

2.2.1 M21204/M21214 Pins

Table 2-3. M21204/M21214 Control/Interface Pins

Pin Name	Pin Number	Function	Default	Type
CLEN	1	Cable length Indicator output	—	Analog
THRESH	10	Input control signal. Programmable cable length forced mute threshold. This function is disabled if **$\overline{\text{SD}}$/MUTE** = Low.	Internal pull down	Analog
$\overline{\text{SD}}$/MUTE	16	Bi-directional Signal that can be used as an input control signal or as an output status indicator. When configured as an input by forcing a voltage on **$\overline{\text{SD}}$/MUTE** = High (a voltage greater that 1.2V), the SDO outputs will be inhibited at logic low (outputs muted). When **$\overline{\text{SD}}$/MUTE** = Low, the output is never muted and the programmable cable length based mute function is disabled. When configured as an output (tied to a high-impedance input) or left floating, the programmable inhibit based on cable length is enabled. Configured as Output: Low = Input signal detect High = Loss of signal Configured as Input: Low = Never mute High = Force Mute	—	I/O
EQ_BYP	9	Input control signal that when enabled (High) bypasses the inputs directly to the output stage. Low = Normal operation High = Disables EQ and bypasses input to output	Internal pull down	I—CMOS
AGC/$\overline{\text{AGC}}$	7, 8	External AGC (Automatic Gain Control) capacitor connection points. Use 1.0uF capacitor.	Internal pull up	Analog
NOTE: Internal pull-up/pull-down is 100 kΩ				

Figure 2-3. M21204/M21214 Pin Assignments



Appendix

A.1 Glossary of Terms/Acronyms

ASIC	Application Specific Integrated Circuit
DTV	Digital Television
DVB	Digital Video Broadcast
EQ	Equalizer or Equalization
HD	High Definition
SD	Standard Definition
SDI	Serial Digital Interface
SMPTE	Society of Motion Picture and Television Engineers

A.2 Reference Documents

A.2.1 External

Society of Motion Picture and Television Engineers

SMPTE 292M Bit-Serial Digital Interface for High-Definition Television Systems

SMPTE 259M 10-Bit 4:2:2 Component and $4f_{SC}$ Composite Digital Signals—Serial Digital Interface

SMPTE 344M 540Mb/s Serial Digital Interface

DVB Digital Video Broadcast