FAIRCHILD SEMICONDUCTOR®

July 2009

FSA2357 — Low R_{ON} 3:1 Analog Switch

Features

- 10µA Maximum I_{CCT} Current Over an Expanded Control Voltage Range: V_{IN}=2.6V, V_{CC}=4.5V
- On Capacitance (C_{ON}): 70pF Typical
- 0.55Ω Typical On Resistance (R_{ON})
- -3db Bandwidth: > 120MHz
- Low Power Consumption (1µA maximum)
- Packaged in Pb-Free 14-Pin TSSOP and DQFN
- Priority Enable Control Circuitry

Applications

- HDMI 5V Power Routing, LCD Monitor, TV, and Set-Top Box
- Cell Phone, PDA, Digital Camera, and Notebook

Description

The FSA2357 is a Double-Pole, Triple Throw (DP3T) multiplexer that routes three dual-channel sources of data or audio under the control of three select pins. The FSA2357 features very low quiescent current, which allows mobile handset applications direct interface with the baseband processor general-purpose I/Os. Typical applications involve switching in portables and consumer applications, such as cell phones, digital cameras, and notebooks with hubs or controllers.

IMPORTANT NOTE:

For additional information, please contact analogswitch@fairchildsemi.com.

Ordering Information

Part Number	Top Mark	Eco Status	Packing Description
FSA2357BQX	2357	Green	14-Terminal Depopulated very thin Quad Flat-pack No leads (DQFN) 2.5 x 3.0mm, JEDEC MO-241
FSA2357MTCX	FSA2357	RoHS	14-Lead Thin Shrink Small Outline Package (TSSOP) 4.4mm wide, JEDEC MO-153

For Fairchild's definition of Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

Analog Symbol

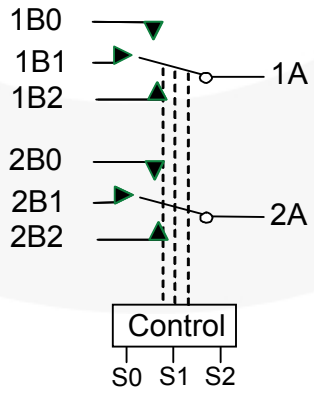


Figure 1. Analog Symbol

Pin Configurations

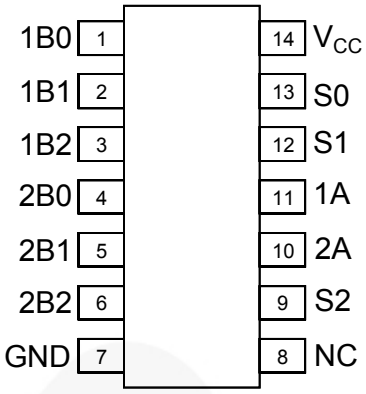


Figure 2. TSSOP-14 (Top Through View)

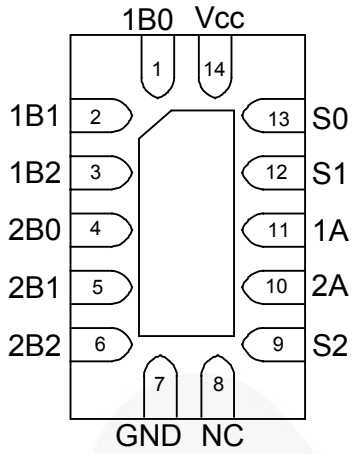


Figure 3. DQFN-14 (Top Through View)

Pin Descriptions

Name	Description
S0, S1, S2	Switch Control Selects
1A, 2A	A Data Bus (Common)
1Bn, 2Bn	Multiplexed Source inputs

Truth Table

S0	S1	S2	Function
HIGH	X	X	1B0 = 1A; 2B0 = 2A
LOW	HIGH	X	1B1 = 1A; 2B1 = 2A
LOW	LOW	HIGH	1B2 = 1A; 2B2 = 2A
LOW	LOW	LOW	Disconnected (Hi-Z)

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	Supply Voltage		-0.5	6.0	V
V_{SW}	Switch I/O Voltage[1]	1Bn, 2Bn Pins	-0.5	V_{CC} + 0.3	V
V_{CNTRL}	Control Input Voltage[1]	S0, S1 Pins	-0.5	6.0	V
I_{IK}	Input Clamp Diode Current		-50		mA
I_{SW}	Switch I/O Current (Continuous)			350	mA
I_{SWPEAK}	Peak Switch Current (Pulsed at 1ms Duration, <10% Duty Cycle)			500	mA
P_D	Power Dissipation at 85°C	DQFN-14		2.5	µW
		TSSOP-14		2.5	
T_{STG}	Storage Temperature Range		-65	+150	°C
T_J	Maximum Junction Temperature			+150	°C
T_L	Lead Temperature (Soldering, 10 Seconds)			+260	°C
ESD	Human Body Model, JEDEC: JESD22-A114	All Pins		5500	kV
		I/O to GND		8000	
		V_{CC} to GND		8000	
	Charged Device Model, JEDEC-JESD22-C101			2000	

Note:
1. The input and output negative ratings may be exceeded if the input and output diode current ratings are observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	Supply Voltage		2.7	5.5	V
V_{CNTRL}	Control Input Voltage ($V_{S0:S1}$)		0	V_{CC}	V
V_{SW}	Switch I/O Voltage		0	V_{CC}	V
T_A	Operating Temperature		-40	+85	°C
θ_{JA}	Thermal Resistance (Free Air)	DQFN-14		145	°C/W
		TSSOP-14			

DC Electrical Characteristics

All typical values are at 25ºC unless otherwise specified.

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = - 40°C to +85°C			Unit
				Min.	Typ.	Max.	
	Analog Signal Range			V_{CC} -5.5		V_{CC}	V
V_{IK}	Clamp Diode Voltage					1.2	V
V_{IH}	Control Input Voltage HIGH		2.7 to 3.6	1.2			V
			3.6 to 4.5	1.5			
V_{IL}	Control Input Voltage LOW		2.7 to 3.6			0.5	
			3.6 to 4.5			0.7	
I_{IN}	Control Input Leakage	V_{IN} = 0 to V_{CC}	4.5			±1	µA
$I_{NO(0FF)}$	Off-Leakage Current of Port (1Bn, 2Bn)	1Bn, 2Bn or 1A, 2A = 0.3V, V_{CC} -0.3V, or Floating	5.5	-100	10	100	nA
$I_{NC(0N)}$	On-Leakage Current of Port 1Bn, 2Bn	1Bn, 2Bn or 1A, 2A = 0.3V, V_{CC} -0.3V, or Floating	5.5	-100	10	100	nA
R_{ON}	Switch On Resistance[2]	1Bn or 2Bn = 0V, 0.7V, 2.0V, 2.7V; I_{ON} = -100mA Figure 4	2.7		0.75	2.00	Ω
			4.5		0.55	0.90	
ΔR_{ON}	Delta On Resistance[3]	1Bn or 2Bn = 0.7V, V_{CC}, I_{ON} = -100mA	2.7		0.50		Ω
			4.5		0.30		
$R_{FLAT(ON)}$	On Resistance Flatness[4]	1Bn or 2Bn = 0V, 0.7V, 2.0V, 2.7V; I_{ON} = -100mA Figure 4	2.7 to 4.5		0.23	0.40	Ω
I_{CC}	Quiescent Supply Current	V_{SW} = 0 or V_{CC}-0.3 I_{OUT} = 0	5.5		22	500	µA
I_{CCT}	Increase in Quiescent Supply Current per Control Voltage and V_{CC}	V_{CNTRL} = 3.3V	5.5		5	20	µA

Notes:

2. R_{ON} measured by the voltage drop between 1Bn (2Bn) and 1A (2A) pins at identical current through the switch. R_{ON} is determined by the lower of the voltage on the two pins.
3. Guaranteed by characterization; not production tested.
4. Flatness is defined as the difference between the maximum and minimum values of on resistance over the specified range of conditions.

AC Electrical Characteristics

All typical values are for V_{CC} = 3.3V at 25ºC unless otherwise specified.

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = - 40°C to +85°C			Unit
				Min.	Typ.	Max.	
t_{ON}	Turn-On Time S[0:1] to Output	V_{Bn} = 1.5V, R_L = 50Ω, C_L = 35pF Figure 8	2.7 to 4.5		30	60	ns
t_{OFF}	Turn-Off Time S[0:1] to Output	V_{Bn} = 1.5V, R_L = 50Ω, C_L = 35pF Figure 8	2.7 to 4.5		38	80	ns
t_{PD}	Propagation Delay(5)	R_L = 50Ω, C_L = 5pF Figure 9	3.6		0.25		ns
t_{BBM}	Break-Before-Make(5)	R_L = 50Ω, C_L = 5pF V_{IN1} = V_{IN2} = V_{IN3} = 1.5V	2.7 to 4.5	1.0	6.0		ns
Q	Charge Injection	R_{GEN} = 0Ω, C_L = 100pF, R_L = OPEN Figure 10	2.7 to 4.5		9		pC
O_{IRR}	Off-Isolation	f = 100kHz, R_L = 50Ω Figure 12	2.7 to 4.5		-68		dB
Xtalk	Non-Adjacent Channel Crosstalk	f = 100kHz, R_L = 50Ω Figure 13	2.7 to 4.5		-60		dB
THD	Total Harmonic Distortion	f = 20Hz to 20kHz, R_L = 600Ω,V_{SW} = 0.5V_{pp} Figure 16	2.7 to 4.5		0.01		%
BW	-3db Bandwidth	R_L = 50Ω, C_L = 0, 5pF Figure 11	2.7 to 4.5		90		MHz

Note:

5. Guaranteed by characterization; not production tested.

Capacitance

Symbol	Parameter	Conditions	T_A = - 40°C to +85°C	Unit
			Typical	
C_{IN}	Control Pin Input Capacitance	V_{CC} = 0V	2.75	pF
C_{ON}	A/B On Capacitance	V_{CC} = 3.3V, S[0:1] = 01, 10, 11, f = 1MHz Figure 15	70	pF
C_{OFFA}	Port 1A, 2A Off Capacitance	V_{CC} = 3.3V, S[0:1] = 00 Figure 14	42	pF
C_{OFFB}	Port 1Bn, 2Bn Off Capacitance	V_{CC} = 3.3V, S[0:1] = 00 Figure 14	20	pF

Test Diagrams

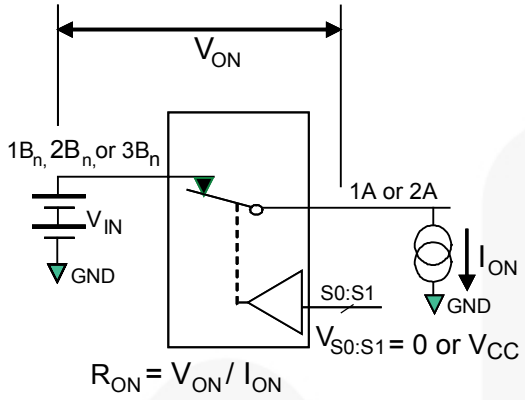


Figure 4. On Resistance

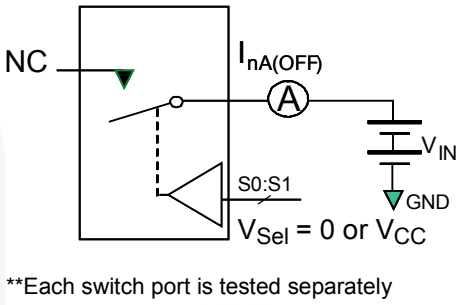
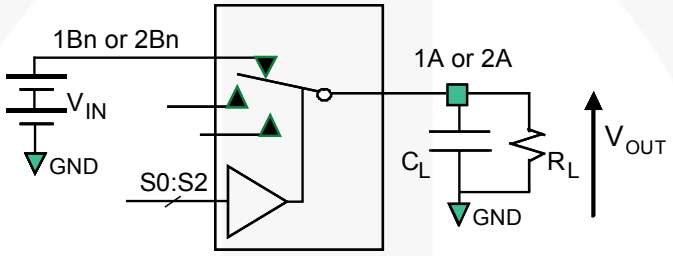
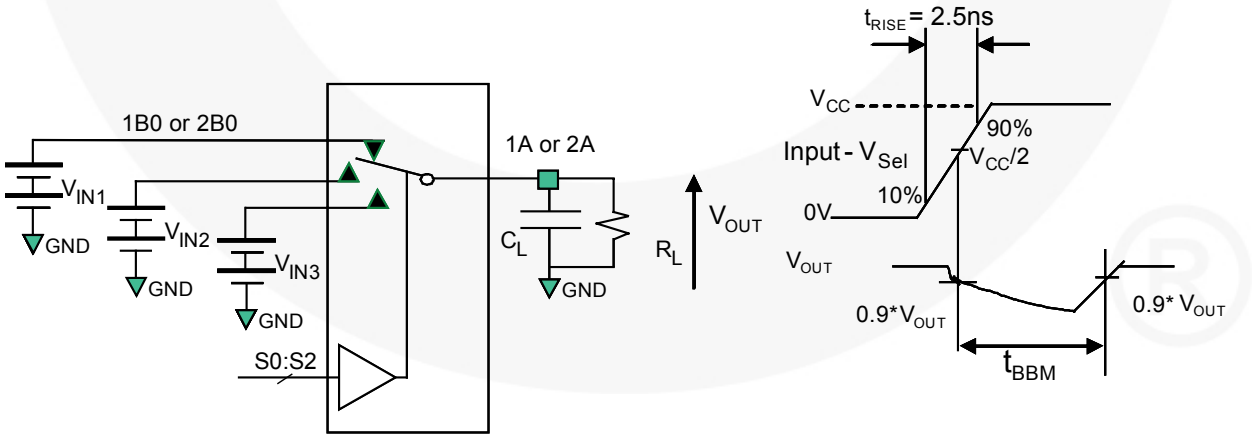


Figure 5. Off Leakage



R_L and C_L are functions of the application environment (see tables for specific values).
C_L includes test fixture and stray capacitance.

Figure 6. AC Test Circuit Load



R_L and C_L are functions of the application environment (see tables for specific values).
C_L includes test fixture and stray capacitance.

Figure 7. Break-Before-Make Timing

Test Diagrams (Continued)

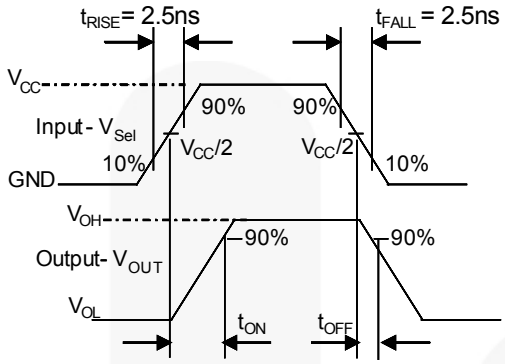


Figure 8. Turn-On / Turn-Off Waveforms

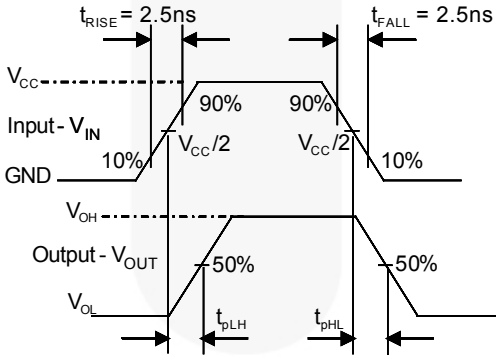


Figure 9. Switch Propagation Delay Waveforms

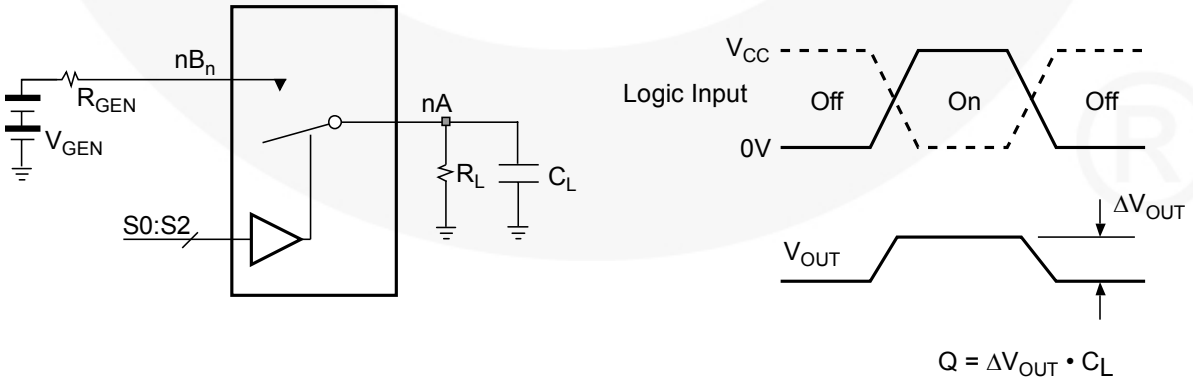
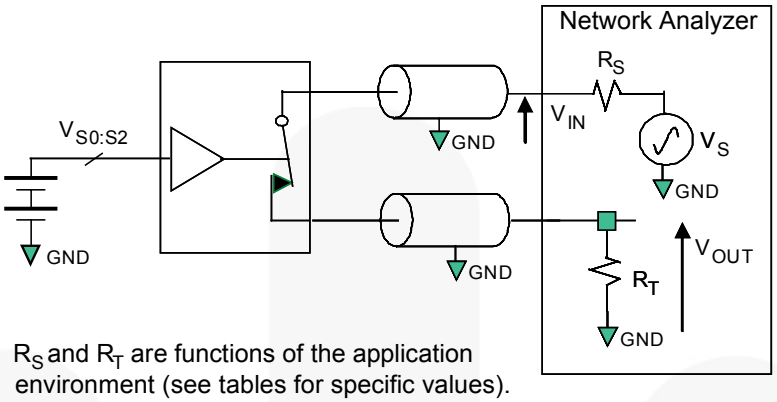


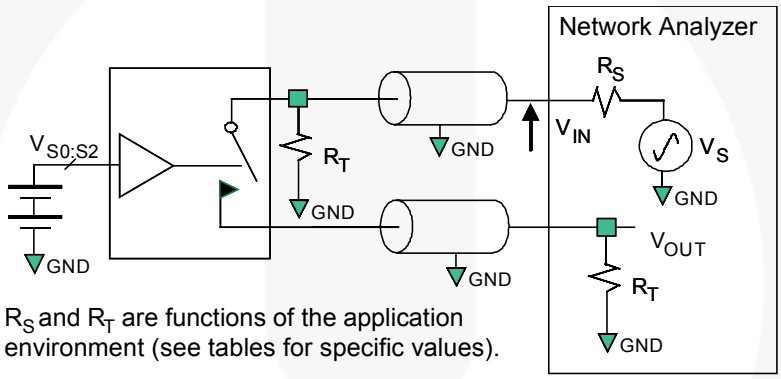
Figure 10. Charge Injection Test

Test Diagrams (Continued)



R_S and R_T are functions of the application environment (see tables for specific values).

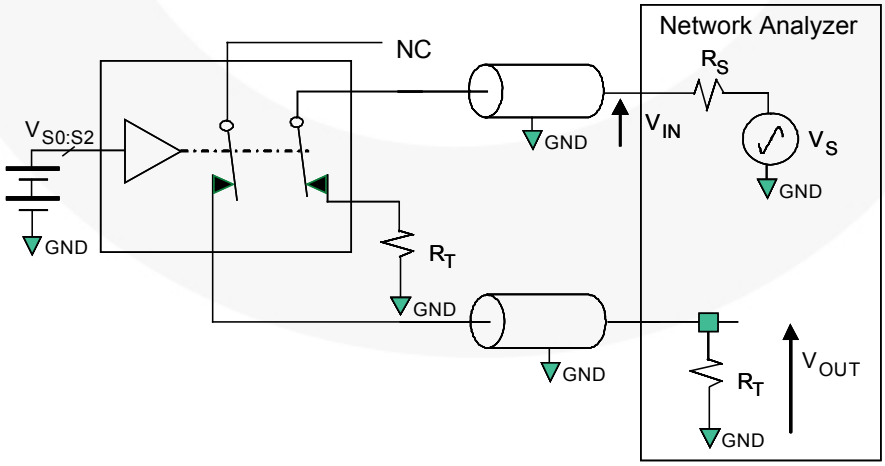
Figure 11. Bandwidth



R_S and R_T are functions of the application environment (see tables for specific values).

Off-Isolation = 20 Log (V_{OUT} / V_{IN})

Figure 12. Channel Off Isolation



CROSSTALK = 20 Log (V_{OUT}/ V_{IN})

Figure 13. Non-Adjacent Channel-to-Channel Crosstalk

Test Diagrams (Continued)

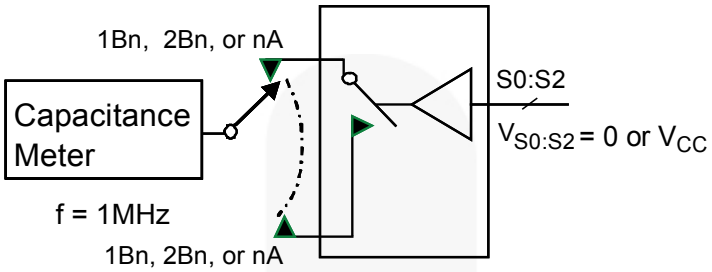


Figure 14. Channel Off Capacitance

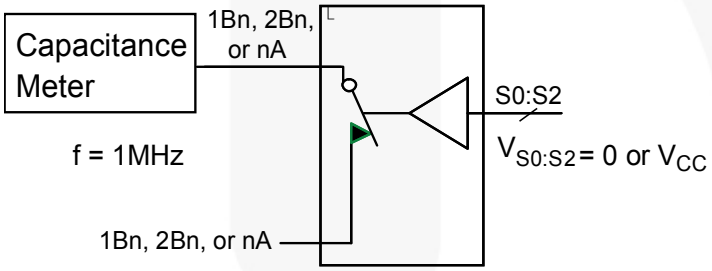


Figure 15. Channel On Capacitance

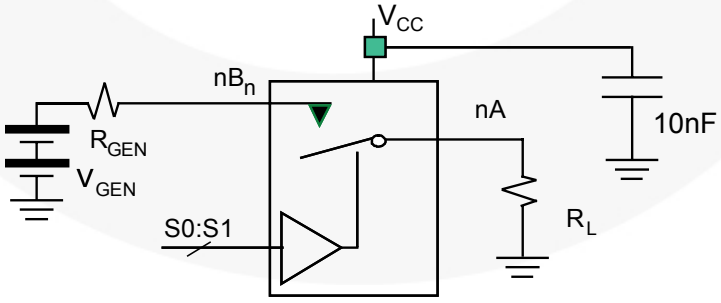
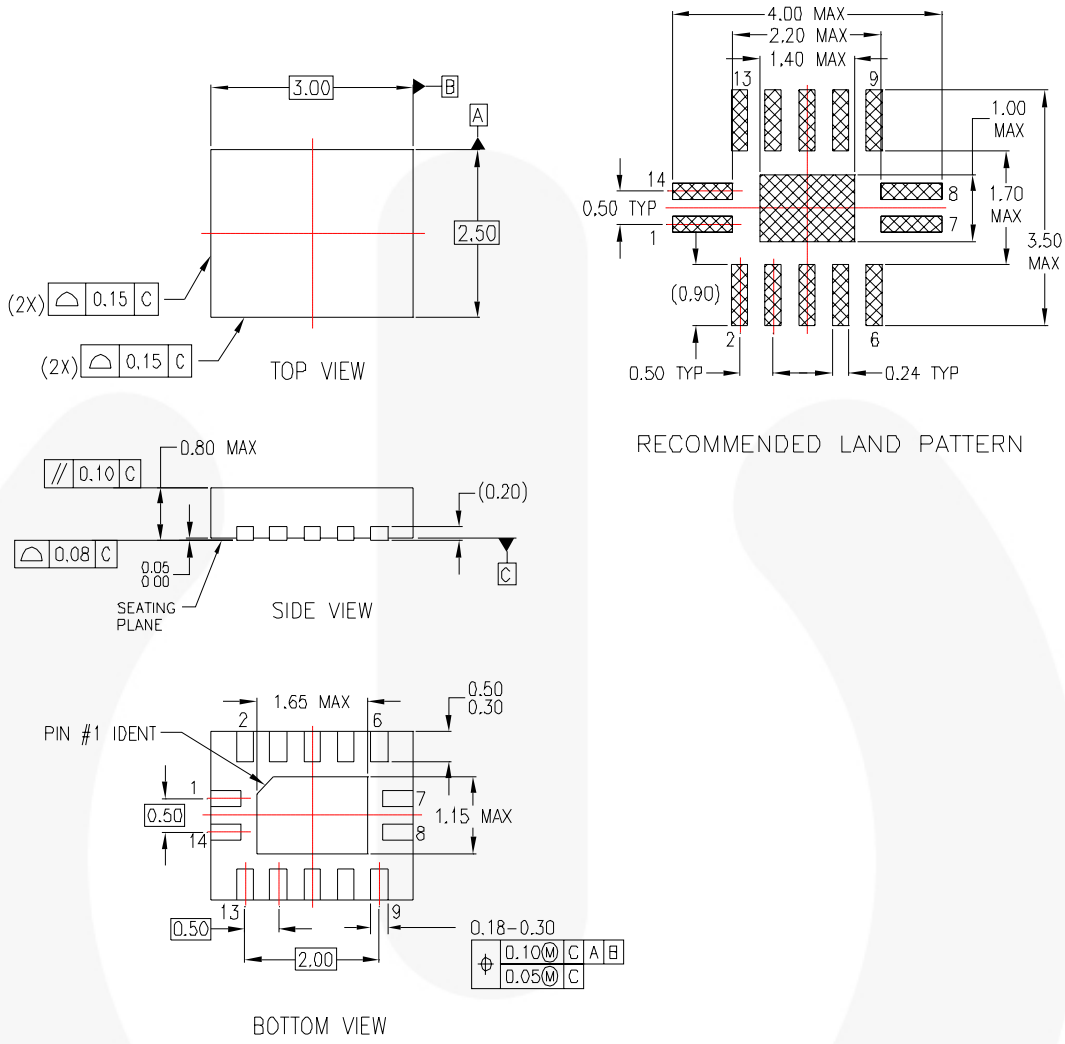


Figure 16. Total Harmonic Distortion

Physical Dimensions



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-241, VARIATION AA

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

MLP14ArevA

Figure 17. 14-Terminal Depopulated Very Thin Quad Flat-Pack, No leads (DQFN)

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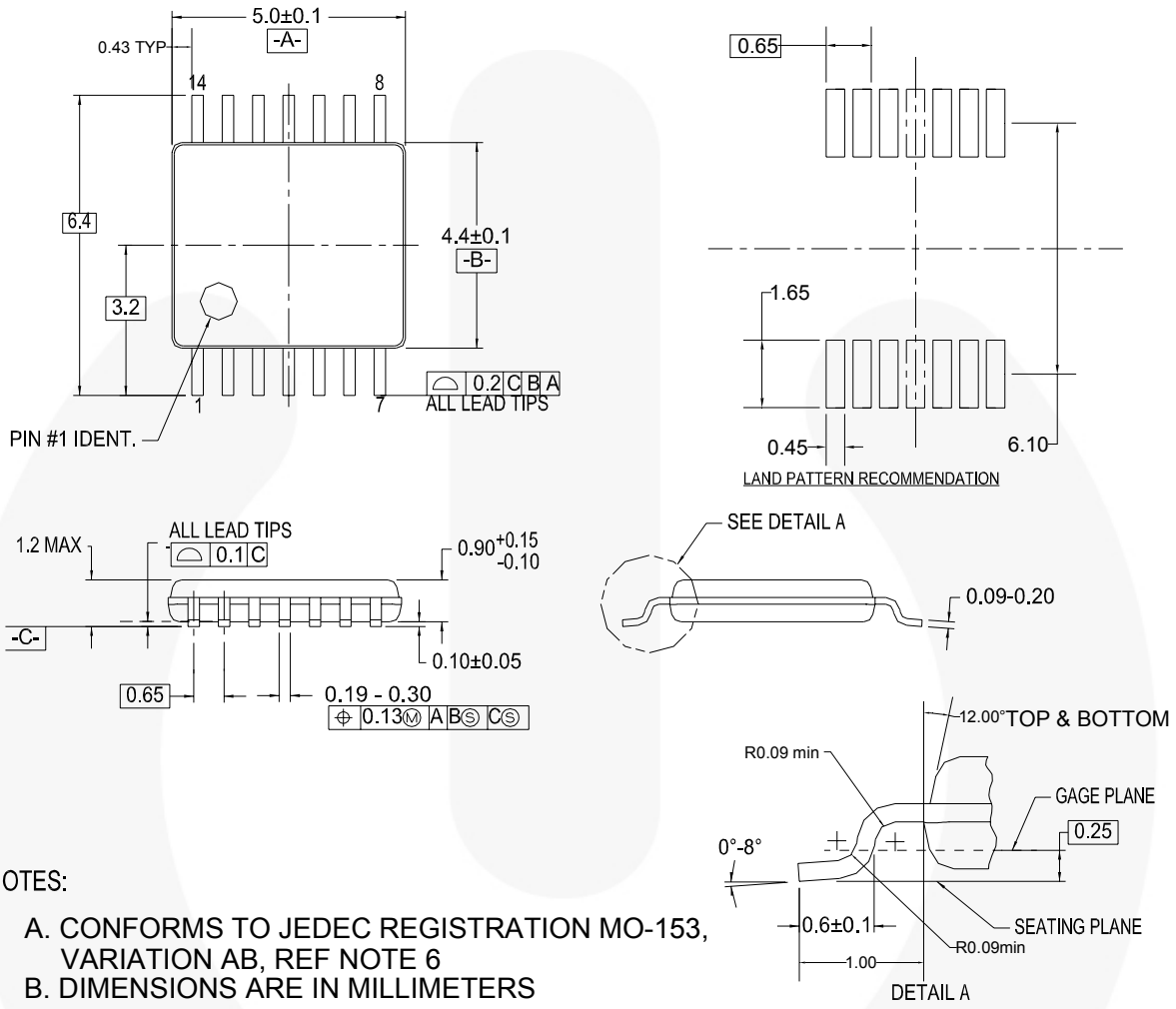
Physical Dimensions



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6

B. DIMENSIONS ARE IN MILLIMETERS

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS

D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982

E. LANDPATTERN STANDARD: SOP65P640X110-14M

F. DRAWING FILE NAME: MTC14REV6

Figure 18. 14-Lead Thin Shrink Small Outline Package (TSSOP)

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Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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