# Silicon SPDT Switch, Nonreflective, 9 kHz to 44 GHz

Data Sheet **ADRF5027**

## FEATURES

**Ultrawideband frequency range: 9 kHz to 44 GHz**
**Nonreflective design**
**Low insertion loss**
- **1.1 dB to 18 GHz**
- **1.5 dB to 26 GHz**
- **2.2 dB to 40 GHz**
- **3.8 dB to 44 GHz**

**High isolation**
- **53 dB to 18 GHz**
- **48 dB to 26 GHz**
- **48 dB to 40 GHz**
- **43 dB to 44 GHz**

**High input linearity**
- **P1dB: 26 dBm typical**
- **IP3: 54 dBm typical**

**High power handling**
- **24 dBm insertion loss path**
- **24 dBm isolation path**

**All off state control**
**No low frequency spurious signals**
**0.1 dB RF settling time: 6.0 µs typical**
**20-terminal, 3 mm × 3 mm LGA package**
**Pin compatible with ADRF5026, fast switching version**

## APPLICATIONS

**Industrial scanners**
**Test and instrumentation**
**Cellular infrastructure: 5G mmWave**
**Military radios, radars, electronic counter measures (ECMs)**
**Microwave radios and very small aperture terminals (VSATs)**

## FUNCTIONAL BLOCK DIAGRAM

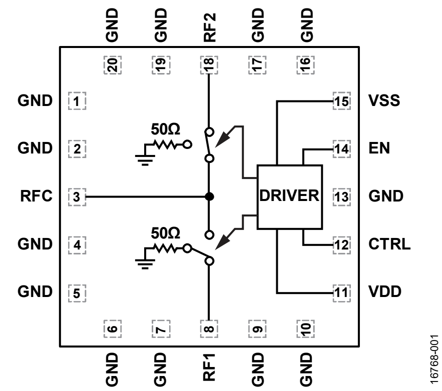


*Figure 1.*

## GENERAL DESCRIPTION

The ADRF5027 is a nonreflective, single-pole, double-throw (SPDT) radio frequency (RF) switch manufactured in a silicon process.

The ADRF5027 operates from 9 kHz to 44 GHz with better than 3.8 dB of insertion loss and 43 dB of isolation. The ADRF5027 features an all off control, where both RF ports are in an isolation state. The ADRF5027 has a nonreflective design and both of the RF ports are internally terminated to 50 Ω.

The ADRF5027 requires a dual-supply voltage of +3.3 V and −3.3 V. The device employs complimentary metal-oxide semiconductor/low-voltage transistor-transistor logic (CMOS/LVTTL) logic-compatible controls.

The ADRF5027 is pin compatible with the ADRF5026 fast switching version, which operates from 100 MHz to 44 GHz.

The ADRF5027 RF ports are designed to match a characteristic impedance of 50 Ω. For ultrawideband products, impedance matching on the RF transmission lines can further optimize high frequency insertion loss and return loss characteristics. Refer to the Narrow-Band Impedance Matching section for an example of a matched circuit that achieves a low insertion loss response of 2.2 dB from 28 GHz to 43 GHz.

The ADRF5027 comes in a 20-terminal, 3 mm × 3 mm, RoHS-compliant, land grid array (LGA) package and can operate from −40°C to +105°C.

**Rev. A** Document Feedback


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## REVISION HISTORY

**9/2020—Rev. 0 to Rev. A**

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**7/2018—Revision 0: Initial Version**

# SPECIFICATIONS

## ELECTRICAL SPECIFICATIONS

VDD = 3.3 V, VSS = −3.3 V, $V_{CTRL}/V_{EN}$ = 0 V or VDD, and $T_{CASE}$ = 25°C in a 50 Ω system, unless otherwise noted.

**Table 1.**

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| FREQUENCY RANGE | | | 0.009 | | 44,000 | MHz |
| INSERTION LOSS | IL | | | | | |
| Between RFC and RF1/RF2 | | 9 kHz to 18 GHz | | 1.1 | | dB |
| | | 18 GHz to 26 GHz | | 1.5 | | dB |
| | | 26 GHz to 35 GHz | | 1.9 | | dB |
| | | 35 GHz to 40 GHz | | 2.2 | | dB |
| | | 40 GHz to 44 GHz[1] | | 3.8 | | dB |
| RETURN LOSS | RL | | | | | |
| RFC and RF1/RF2 (On) | | 9 kHz to 18 GHz | | 18 | | dB |
| | | 18 GHz to 26 GHz | | 14 | | dB |
| | | 26 GHz to 35 GHz | | 14 | | dB |
| | | 35 GHz to 40 GHz | | 12 | | dB |
| | | 40 GHz to 44 GHz[1] | | 7 | | dB |
| RF1/RF2 (Off) | | 9 kHz to 18 GHz | | 28 | | dB |
| | | 18 GHz to 26 GHz | | 28 | | dB |
| | | 26 GHz to 35 GHz | | 17 | | dB |
| | | 35 GHz to 40 GHz | | 13 | | dB |
| | | 40 GHz to 44 GHz[1] | | 10 | | dB |
| ISOLATION | | | | | | |
| Between RFC and RF1/RF2 | | 9 kHz to 18 GHz | | 53 | | dB |
| | | 18 GHz to 26 GHz | | 48 | | dB |
| | | 26 GHz to 35 GHz | | 48 | | dB |
| | | 35 GHz to 40 GHz | | 48 | | dB |
| | | 40 GHz to 44 GHz | | 43 | | dB |
| Between RF1 and RF2 | | 9 kHz to 18 GHz | | 60 | | dB |
| | | 18 GHz to 26 GHz | | 60 | | dB |
| | | 26 GHz to 35 GHz | | 60 | | dB |
| | | 35 GHz to 40 GHz | | 60 | | dB |
| | | 40 GHz to 44 GHz | | 50 | | dB |
| SWITCHING CHARACTERISTICS | | | | | | |
| Rise and Fall Time | $t_{RISE}$, $t_{FALL}$ | 10% to 90% of RF output | | 1.3 | | μs |
| On and Off Time | $t_{ON}$, $t_{OFF}$ | 50% of triggered $V_{CTRL}$ to 90% of RF output | | 3.6 | | μs |
| RF Settling Time | | | | | | |
| 0.1 dB | | 50% of triggered $V_{CTRL}$ to 0.1 dB of final RF output | | 6.0 | | μs |
| 0.05 dB | | 50% of triggered $V_{CTRL}$ to 0.05 dB of final RF output | | 7.5 | | μs |
| INPUT LINEARITY[2] | | 200 kHz to 40 GHz | | | | |
| 1 dB Compression | P1dB | | | 26 | | dBm |
| Third-Order Intercept | IP3 | Two-tone input power = 12 dBm each tone, Δf = 1 MHz | | 54 | | dBm |
| SUPPLY CURRENT | | VDD and VSS pins | | | | |
| Positive | $I_{DD}$ | | | 2 | | μA |
| Negative | $I_{SS}$ | | | 100 | | μA |
| DIGITAL CONTROL INPUTS | | CTRL and EN pins | | | | |
| Voltage | | | | | | |
| Low | $V_{INL}$ | | 0 | | 0.8 | V |
| High | $V_{INH}$ | | 1.2 | | 3.3 | V |
| Current | | | | | | |
| Low and High Current | $I_{INL}$, $I_{INH}$ | | | <1 | | μA |

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| RECOMMENDED OPERATING CONDITONS | | | | | | |
| Supply Voltage | | | | | | |
| Positive | $V_{DD}$ | | 3.15 | | 3.45 | V |
| Negative | $V_{SS}$ | | −3.45 | | −3.15 | V |
| Digital Control Voltage | $V_{CTRL}$, $V_{EN}$ | | 0 | | $V_{DD}$ | V |
| RF Input Power[3] | $P_{IN}$ | f = 200 kHz to 40 GHz, $T_{CASE}$ = 85°C[4] | | | | |
| Insertion Loss Path | | RF signal is applied to the RFC or through connected RF1/RF2 | | | 24 | dBm |
| Isolation Path | | RF signal is applied to terminated RF1/RF2 | | | 24 | dBm |
| Hot Switching | | RF signal is present at the RFC while switching between RF1 and RF2 | | | 24 | dBm |
| Case Temperature | $T_{CASE}$ | | −40 | | +105 | °C |

[1] Impendence matching on RF transmission lines improves high frequency performance. Refer to the Applications Information section for more information.
[2] For input linearity performance vs. frequency, see Figure 11 and Figure 13.
[3] For power derating vs. frequency, see Figure 2 and Figure 3. This power derating is applicable for insertion loss path, isolation path, and hot switching power specifications.
[4] For 105°C operation, the power handling degrades from the $T_{CASE}$ = 85°C specification by 3 dB.

# ABSOLUTE MAXIMUM RATINGS

For recommended operating conditions, see Table 1.

**Table 2.**

| Parameter | Rating |
|---|---|
| Positive Supply Voltage | −0.3 V to +3.6 V |
| Negative Supply Voltage | −3.6 V to +0.3 V |
| Digital Control Inputs | |
| Voltage | −0.3 V to VDD +0.3 V |
| Current | 3 mA |
| RF Input Power[1] (200 kHz to 40 GHz at $T_{CASE}$ = 85°C[2]) | |
| Insertion Loss Path | 26 dBm |
| Isolation Path | 25 dBm |
| Hot Switching | 25 dBm |
| RF Input Power Under Unbiased Condition ($V_{DD}$, $V_{SS}$ = 0 V) | 20 dBm |
| Temperature | |
| Junction, $T_J$ | 135°C |
| Storage Range | −65°C to +150°C |
| Reflow | 260°C |
| Electrostatic Discharge (ESD) Sensitivity | |
| Human Body Model (HBM) | |
| RFC, RF1, RF2 Pins | 1500 V |
| Digital Pins | 2000 V |
| Charged Device Model (CDM) | 1250 V |

[1] For power derating vs. frequency, see Figure 2 and Figure 3. This power derating is applicable for insertion loss path, isolation path, and hot switching power specifications.
[2] For 105°C operation, the power handling degrades from the $T_{CASE}$ = 85°C specification by 3 dB.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

## THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

$\theta_{JC}$ is the junction to case bottom (channel to package bottom) thermal resistance.

**Table 3. Thermal Resistance**

| Package Type | $\theta_{JC}$ | Unit |
|---|---|---|
| CC-20-3 | | |
| Through Path | 423 | °C/W |
| Terminated Path | 241 | °C/W |

## POWER DERATING CURVES

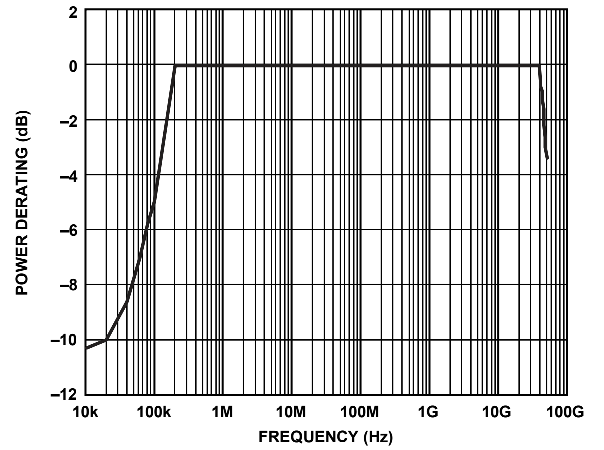



*Figure 2. Power Derating vs. Frequency, Low Frequency Detail, $T_{CASE}$ = 85°C*

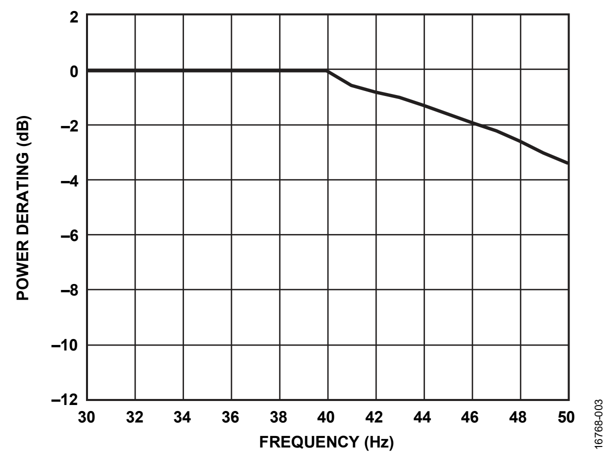
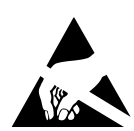



*Figure 3. Power Derating vs. Frequency, High Frequency Detail, $T_{CASE}$ = 85°C*

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

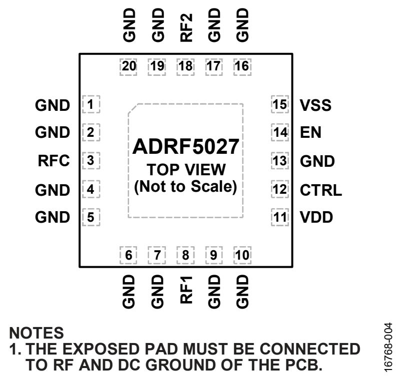



*Figure 4. Pin Configuration*

**Table 4. Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1, 2, 4, 5, 6, 7, 9, 10, 13, 16, 17, 19, 20 | GND | Ground. These pins must be connected to the RF and dc ground of the PCB. |
| 3 | RFC | RF Common Port. This pin is dc-coupled to 0 V and ac matched to 50 Ω. No dc blocking capacitor is necessary when the RF line potential is equal to 0 V dc. See Figure 5 for the interface schematic. |
| 8 | RF1 | RF1 Port. This pin is dc-coupled to 0 V and ac matched to 50 Ω. No dc blocking capacitor is necessary when the RF line potential is equal to 0 V dc. See Figure 5 for the interface schematic. |
| 11 | VDD | Positive Supply Voltage. |
| 12 | CTRL | Control Input Voltage. See Table 5 for the truth table. See Figure 6 for the interface schematic. |
| 14 | EN | Enable Input Voltage. See Table 5 for the truth table. See Figure 6 for the interface schematic. |
| 15 | VSS | Negative Supply Voltage. |
| 18 | RF2 | RF2 Port. This pin is dc-coupled to 0 V and ac matched to 50 Ω. No dc blocking capacitor is necessary when the RF line potential is equal to 0 V dc. See Figure 5 for the interface schematic. |
| | EPAD | Exposed Pad. The exposed pad must be connected to the RF and dc ground of the PCB. |

## INTERFACE SCHEMATICS

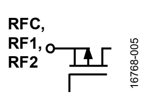



*Figure 5. RFC, RF1, RF2 Interface Schematic*

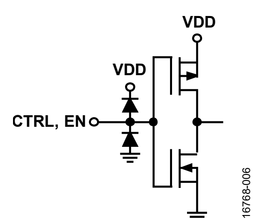



*Figure 6. CTRL, EN Interface Schematic*

# TYPICAL PERFORMANCE CHARACTERISTICS

## INSERTION LOSS, RETURN LOSS, AND ISOLATION

VDD = 3.3 V, VSS = −3.3 V, $V_{CTRL}/V_{EN}$ = 0 V or VDD, and $T_{CASE}$ = 25°C in a 50 Ω system, unless otherwise noted.

Insertion loss and return loss are measured on the probe matrix board using ground-signal-ground (GSG) probes close to the RFx pins. Signal coupling between the probes limits the isolation performance of ADRF5027. Isolation is measured on the ADRF5027-EVALZ evaluation board. See the Applications Information section for details on the ADRF5027-EVALZ evaluation board and probe matrix board.

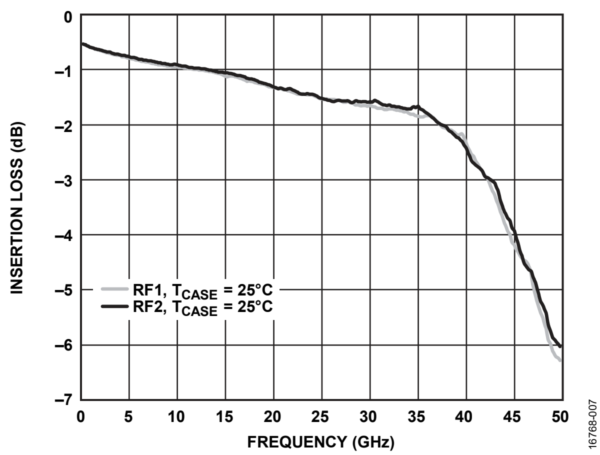



Figure 7. Insertion Loss vs. Frequency at Room Temperature for RF1 and RF2

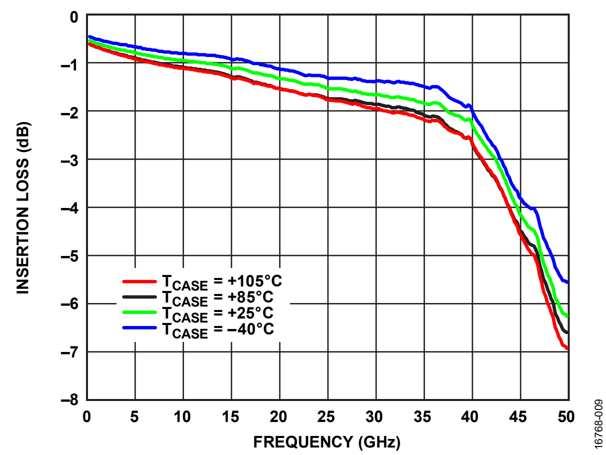



Figure 9. Insertion Loss vs. Frequency over Temperature

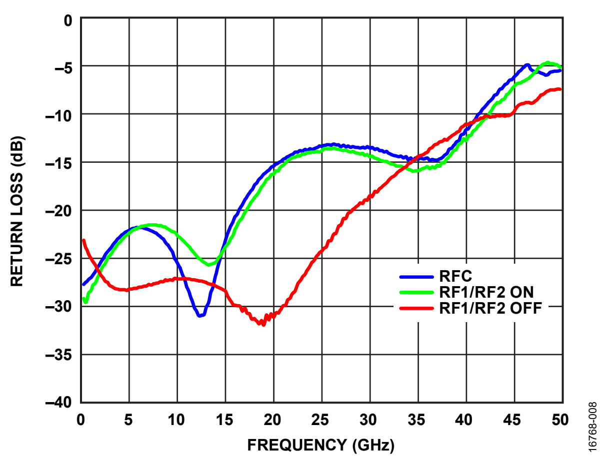



Figure 8. Return Loss vs. Frequency

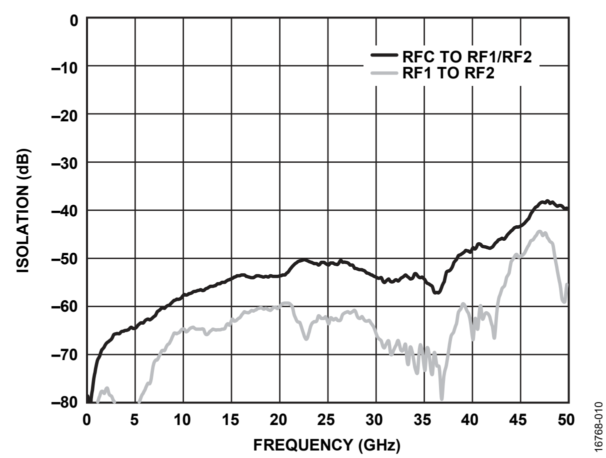



Figure 10. Isolation vs. Frequency

## INPUT POWER COMPRESSIONS AND THIRD-ORDER INTERCEPT

VDD = 3.3 V, VSS = −3.3 V, $V_{CTRL}$/$V_{EN}$ = 0 V or VDD, and $T_{CASE}$ = 25°C in a 50 Ω system, unless otherwise noted. All of the large signal performance parameters are measured on the ADRF5027-EVALZ evaluation board.

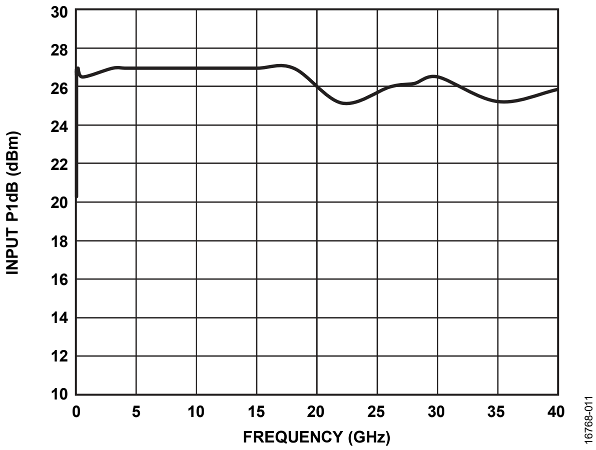



*Figure 11. Input P1dB vs. Frequency*

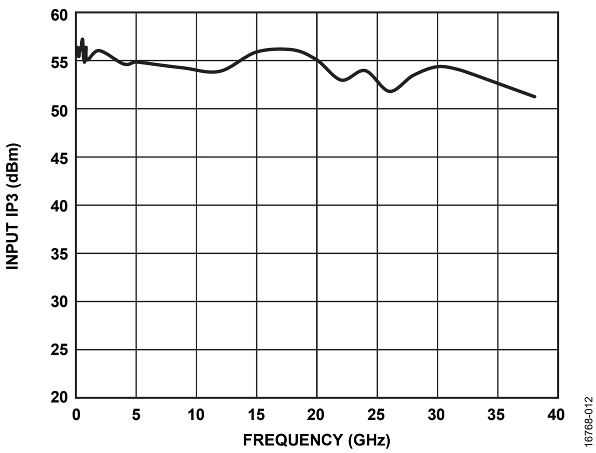



*Figure 12. Input IP3 vs. Frequency*

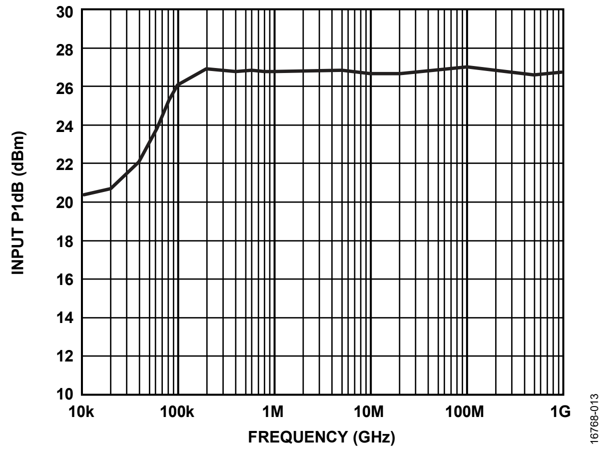



*Figure 13. Input P1dB vs. Frequency (Low Frequency Detail)*

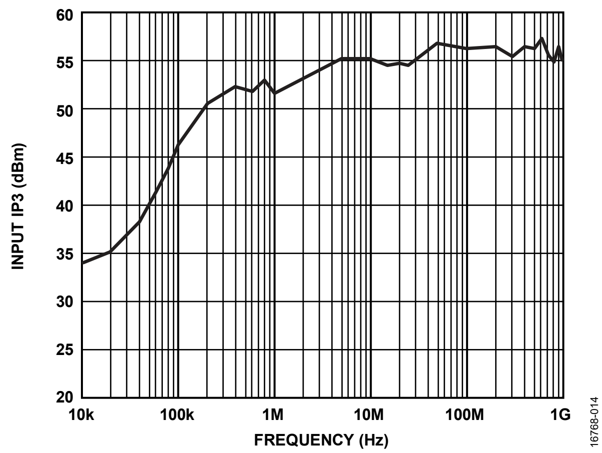



*Figure 14. Input IP3 vs. Frequency (Low Frequency Detail)*

# THEORY OF OPERATION

The ADRF5027 requires a positive supply voltage applied to the VDD pin and a negative supply voltage applied to the VSS pin. Bypassing capacitors are recommended on the supply lines to filter high frequency noise.

All of the RF ports (RFC, RF1, and RF2) are dc-coupled to 0 V, and no dc blocking capacitors are required at the RF ports when the RF potential is equal to 0 V.

The RF ports are internally matched to 50 Ω. Therefore, external matching networks are not required. Impedance matching on the RF transmission lines can improve insertion loss and return loss performance at high frequencies.

The ADRF5027 integrates a driver to perform logic function internally and to provide the advantage of a simplified control interface. The driver features two digital control input pins, CTRL and EN. When the EN pin is logic low, the logic level applied to the CTRL pin determines which RF port is in insertion loss state and which RF port is in isolation state.

The ADRF5027 supports an all off state control. When the EN pin is logic high, both the RF1 to RFC path and the RF2 to RFC path are in an isolation state, regardless of the logic state of the CTRL pin. The RF1 and RF2 ports are terminated to internal 50 Ω resistors, and the RFC port becomes open reflective (see Table 5).

The ADRF5027 design is bidirectional with equal power handling capabilities. An RF input signal ($RF_{IN}$) can be applied to the RFC port or the RF1 or RF2 port. The isolation path provides high loss between the unselected RFx port and the insertion loss path.

The ideal power-up sequence is as follows:

1. Connect GND.
2. Power up VDD and VSS. Power up VSS after VDD to avoid current transients on VDD during ramp-up.
3. Apply the digital control inputs. The relative order of the digital control inputs is not important. However, powering the digital control inputs before the VDD supply may inadvertently forward bias and damage the internal ESD protection structures. To avoid this damage, use a series 1 kΩ resistor to limit the current flowing in to the control pin. Use pull-up or pull-down resistors if the controller output is in a high impedance state after VDD is powered up and the control pins are not driven to a valid logic state.
4. Apply an RF input signal to RFC, RF1, or RF2.

The ideal power-down sequence is the reverse order of the power-up sequence.

**Table 5. Control Voltage Truth Table**

| Digital Control Input | | RF Paths | |
|---|---|---|---|
| **EN** | **CTRL** | **RF1 to RFC** | **RF2 to RFC** |
| Low | Low | Isolation (off) | Insertion loss (on) |
| Low | High | Insertion loss (on) | Isolation (off) |
| High | Low | Isolation (off) | Isolation (off) |
| High | High | Isolation (off) | Isolation (off) |

# APPLICATIONS INFORMATION

## EVALUATION BOARD

The ADRF5027-EVALZ evaluation board is a 4-layer evaluation board. The outer copper (Cu) layers are 0.5 oz (0.7 mil) plated to 1.5 oz (2.2 mil) and are separated by dielectric materials. Figure 15 shows the ADRF5027-EVALZ evaluation board stack up.

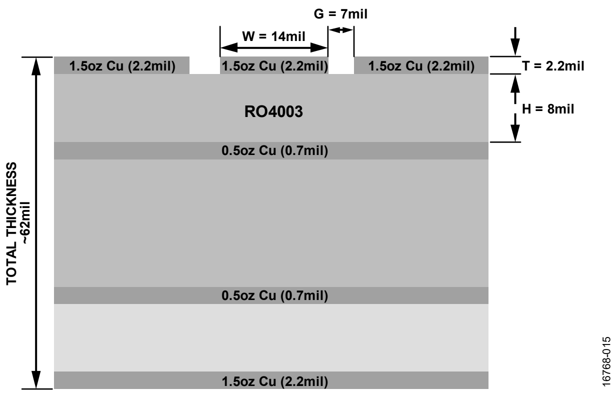



Figure 15. Evaluation Board Stack Up

All RF and dc traces are routed on the top copper layer, whereas the inner and bottom layers are ground planes that provide a solid ground for the RF transmission lines. The top dielectric material is 8 mil Rogers RO4003, which offers optimal high frequency performance. The middle and bottom dielectric materials provide mechanical strength. The overall board thickness is 62 mil, which allows 2.4 mm RF launchers to be connected at the board edges.


Figure 16. Evaluation Board Layout

The RF transmission lines are designed using a coplanar waveguide (CPWG) model with a width of 14 mil and a ground spacing of 7 mil, and have a characteristic impedance of 50 Ω. For optimal RF and thermal grounding, as many plated through vias as possible are arranged around transmission lines and under the exposed pad of the package.

The RF input and output ports (RFC, RF1, and RF2) are connected through 50 Ω transmission lines to the 2.4 mm launchers (J1, J2, and J3, respectively). These high frequency RF launchers are connected by contact and are not soldered to the board.

The thru calibration line, THRU CAL, can calibrate out the board loss effects from the ADRF5027-EVALZ evaluation board measurements to determine the device performance at the pins of the IC. Figure 17 shows the typical board loss for the ADRF5027-EVALZ evaluation board at room temperature, the embedded insertion loss, and the de-embedded insertion loss for the ADRF5027.

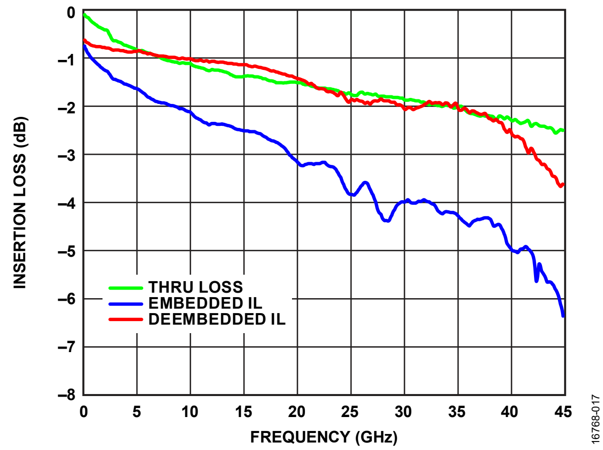



Figure 17. Insertion Loss vs. Frequency

Two power supply ports are connected to the VDD and VSS test points, and the ground reference is connected to the GND test point. On the supply traces, VDD and VSS, a 100 pF bypass capacitor filters high frequency noise. Additionally, unpopulated component positions are available for applying extra bypass capacitors.

Two control ports are connected to the EN and CTRL test points. There are provisions for the resistor capacitor (RC) filter to eliminate dc-coupled noise, if needed by the application.

The ADRF5027-EVALZ evaluation board schematic is shown in Figure 18.

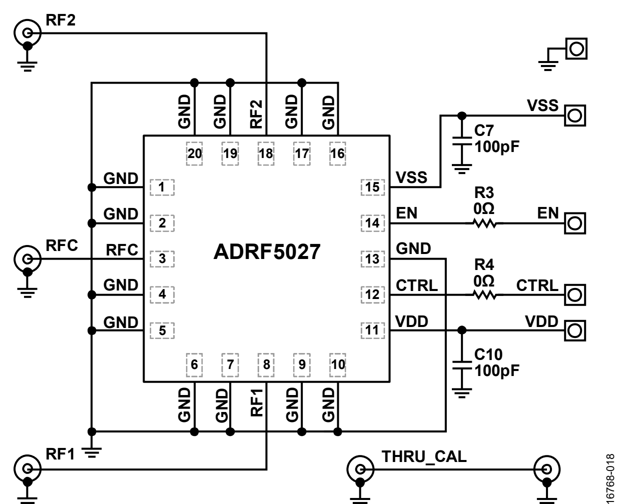



Figure 18. Simplified Evaluation Board Schematic

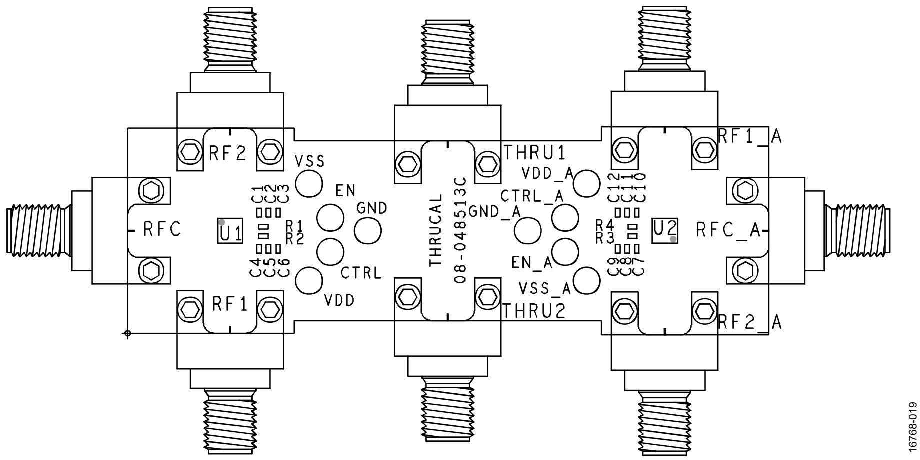



*Figure 19. Evaluation Board Component Placement*

**Table 6. Evaluation Board Components**

| Component | Description |
|---|---|
| RF1_A, RFC_A, RF2_A | End launch connectors, 2.4 mm |
| VDD_A, VSS_A, CTRL_A, EN_A, GND_A | Through-hole mount test points |
| C7, C10 | 100 pF capacitors, 0402 package |
| R3, R4 | 0 Ω resistors, 0402 package |
| U2 | ADRF5027 SPDT switch |

## PROBE MATRIX BOARD

The probe matrix board is a 4-layer board. This board also uses an 8 mil Rogers RO4003 dielectric. The outer copper layers are 0.5 oz (0.7 mil) plated to 1.5 oz (2.2 mil). The RF transmission lines were designed using a CPWG model with a width of 14 mil and a ground spacing of 7 mil to have a characteristic impedance of 50 Ω.

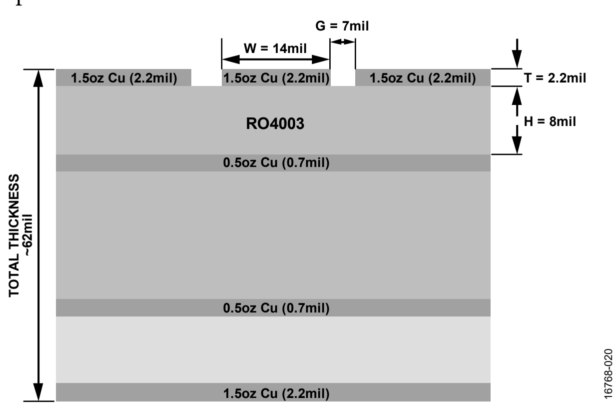



*Figure 20. Probe Matrix Board Stack Up*

Figure 20 and Figure 21 show the stack up and the layout, respectively, of the probe matrix board. Measurements are made using GSG probes at close proximity to the RF pins. Probing reduces the reflections caused by mismatch arising from connectors, cables, and board layout, resulting in a more accurate measurement of insertion loss and return loss. Signal coupling between the RF probes limits the isolation measurement. The ADRF5027-EVALZ evaluation board is used for making isolation measurements.

RF traces for a through-reflect-line (TRL) calibration are designed on the probe matrix board. Board loss is compensated for by using a nonzero line length at calibration. The actual board duplicates the same layout in matrix form, which allows multiple devices to assemble at once. Insertion loss and return loss measurements are made on this board, while isolation measurements are made on the ADRF5027-EVALZ evaluation board.

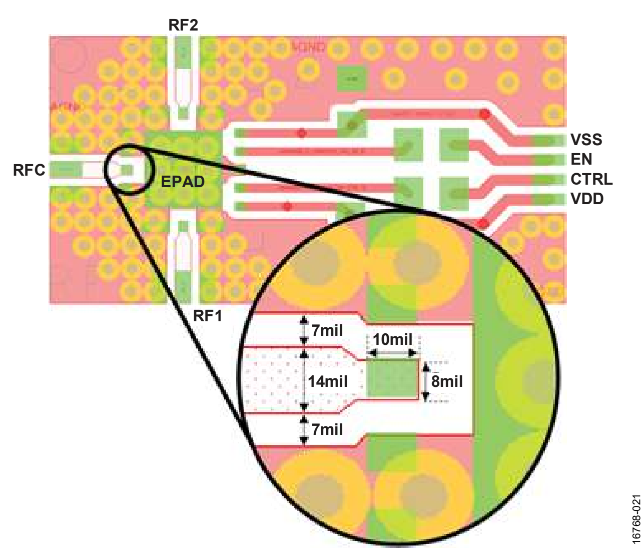



*Figure 21. Probe Matrix Board Layout*

### *Narrow-Band Impedance Matching*

#### 5G mmWave Frequencies

Narrow-band impedance matching on the RF transmission lines can improve return loss and insertion loss for a targeted frequency range. The impedance matched circuit, highlighted in Figure 22, achieves a low insertion loss response of 2.2 dB from 28 GHz to 43 GHz (see Figure 23). The dimensions of the 50 Ω lines are 14 mil trace width and a 7 mil gap. To implement this impedance matched circuit, an 8 mil trace with a width of 5 mil is inserted between the pin pad and the 50 Ω trace.

Table 7, Figure 23, Figure 24, and Figure 25 show the measured performance of ADRF5027 on the impedance matched circuit on the probe matrix board.

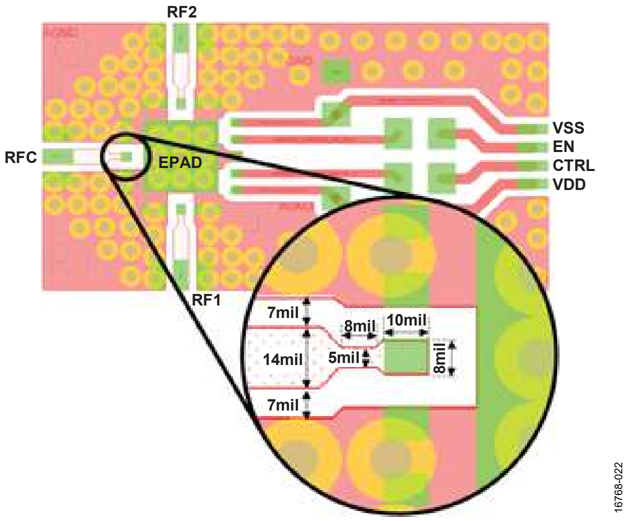



*Figure 22. Impedance Matched Circuit*

**Table 7. Impedance Matched Parameters**

| Parameter | Test Condition | Typ | Unit |
|---|---|---|---|
| Insertion Loss | See Figure 23 | | |
| Between RFC and RF1/RF2 | 9 kHz to 18 GHz | 1.1 | dB |
| | 18 GHz to 26 GHz | 1.8 | dB |
| | 26 GHz to 35 GHz | 2.3 | dB |
| | 35 GHz to 40 GHz | 2.2 | dB |
| | 40 GHz to 44 GHz | 2.7 | dB |
| Return Loss | See Figure 24 | | |
| RFC and RF1/RF2 (On) | 9 kHz to 18 GHz | 20 | dB |
| | 18 GHz to 26 GHz | 8 | dB |
| | 26 GHz to 35 GHz | 7 | dB |
| | 35 GHz to 40 GHz | 10 | dB |
| | 40 GHz to 44 GHz | 14 | dB |
| RF1/RF2 (Off) | See Figure 24 | | |
| | 9 kHz to 18 GHz | 25 | dB |
| | 18 GHz to 26 GHz | 23 | dB |
| | 26 GHz to 35 GHz | 17 | dB |
| | 35 GHz to 40 GHz | 11 | dB |
| | 40 GHz to 44 GHz | 7 | dB |

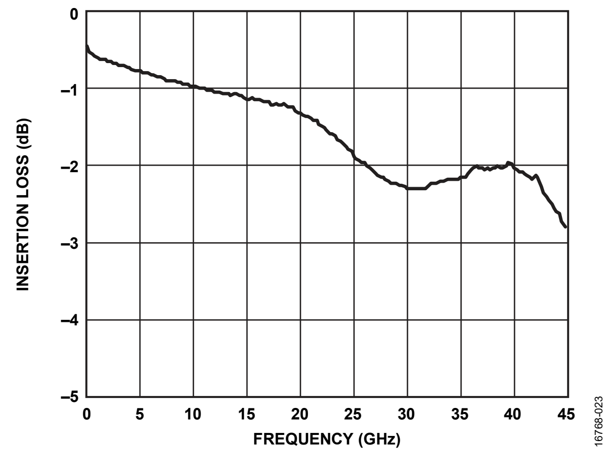



*Figure 23. Insertion Loss vs. Frequency, with Impedance Matching*

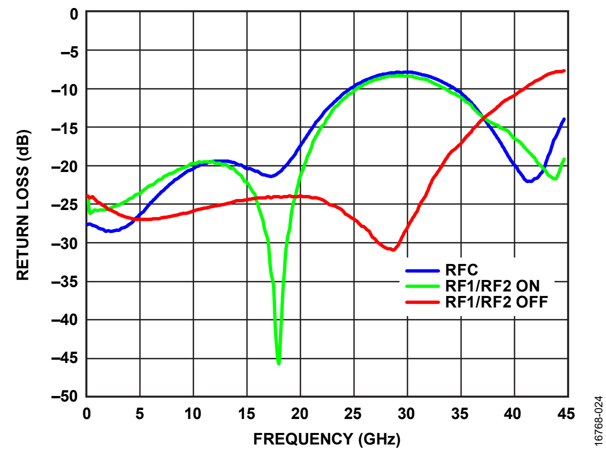



*Figure 24. Return Loss vs. Frequency, with Impedance Matching*

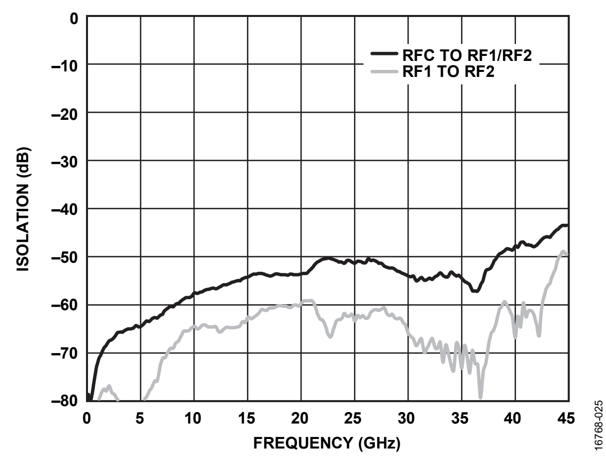



*Figure 25. Isolation vs. Frequency, with Impedance Matching*

# OUTLINE DIMENSIONS

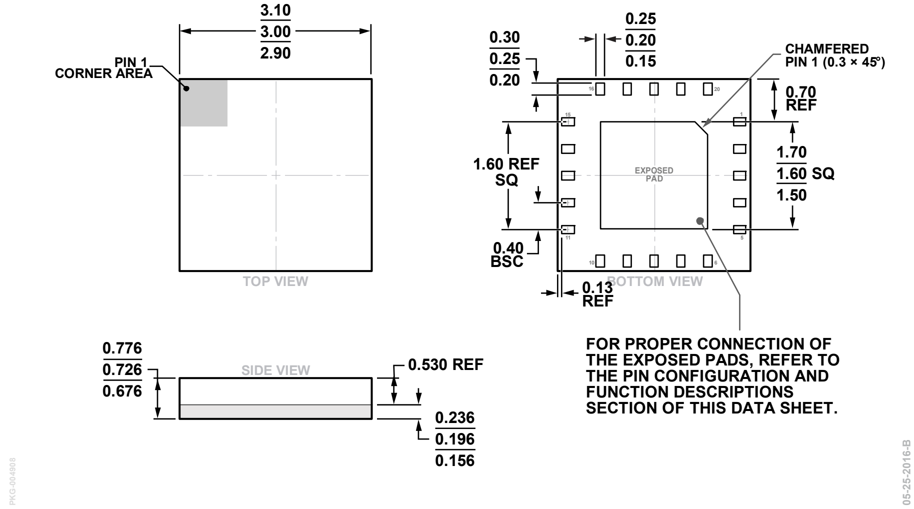



*Figure 26. 20-Terminal Land Grid Array [LGA]*
*3 mm × 3 mm Body and 0.726 mm Package Height*
*(CC-20-3)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model[1] | Temperature Range | Package Description | Package Option | Marking Code |
|---|---|---|---|---|
| ADRF5027BCCZN | −40°C to +105°C | 20-Terminal Land Grid Array [LGA] | CC-20-3 | 027 |
| ADRF5027BCCZN-R7 | −40°C to +105°C | 20-Terminal Land Grid Array [LGA] | CC-20-3 | 027 |
| ADRF5027-EVALZ-292 | | Evaluation Board with 2.92 mm connectors | | |
| ADRF5027-EVALZ-240 | | Evaluation Board with 2.40 mm connectors | | |

[1] Z = RoHS Compliant Part.