MIC23650

6A Step-Down Converter with HyperLight Load™ and Output Voltage Select

Features

- 2.4V to 5.5V Input Voltage Range
- 6A (Pulsed) Output Current
- Pin Strapping Voltage Selection:
  - Three-State pins (nine voltage options)
  - 0.6V, 0.8V, 0.9V, 1.0V, 1.2V, 1.5V, 1.8V, 2.5V or 3.3V output voltage
- Reduced Component Count (No Feedback Resistors)
- High Efficiency (up to 95%)
- Output Discharge when Disabled
- Constant-ON-Time Control with High Switching Frequency:
  - 1.2 MHz typical at 1.0V output voltage
- ±1.5% Output Voltage Accuracy Over Line/Load/Temperature Range
- 0.8 ms/V Soft Start Speed
- Supports Safe Start-Up with Pre-Biased Output
- Typical 1.5 µA Shutdown Supply Current
- Low Dropout Operation (100% Duty Cycle)
- Ultra Fast Transient Response
- Latch-Off Thermal Shutdown Protection
- Latch-Off Current Limit Protection
- Power Good (PG) Open-Drain Output

Applications

- Solid State Drives (SSD)
- FPGAs, DSP and Low-Voltage ASIC Power

General Description

The MIC23650 is a high-efficiency, low-voltage, 6A peak synchronous step-down regulator. The Constant-ON-Time (COT) control architecture with HyperLight Load™ provides very high efficiency at light loads, while still having ultra fast transient response.

The MIC23650 output voltage is set by two V_{SEL} (Voltage Selection) pins, between nine different values. This method eliminates the need for an external feedback resistor divider and improves the output voltage setting accuracy.

The 2.4V to 5.5V input voltage range, low shutdown and quiescent currents make the MIC23650 ideal for single-cell Li-Ion battery-powered applications. The 100% duty cycle capability provides low dropout operation, extending operating range in portable systems.

The MIC23650 pinout is compatible with the MIC23656 I^2C-based programmable regulator version, such that applications can be easily converted. An open-drain Power Good output is provided to indicate when the output voltage is within 9% of regulation and facilitates the interface with an MCU, or power sequencing. If set in shutdown (EN=GND), the MIC23650 typically draws 1.5 µA, while the output is discharged through 10Ω pull-down.

The MIC23650 is available in a thermally efficient, 16 Lead 2.5 mm x 2.5 mm x 0.55 mm thin FTQFN package, with an operating junction temperature range from –40°C to +125°C.

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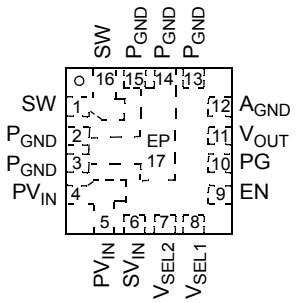
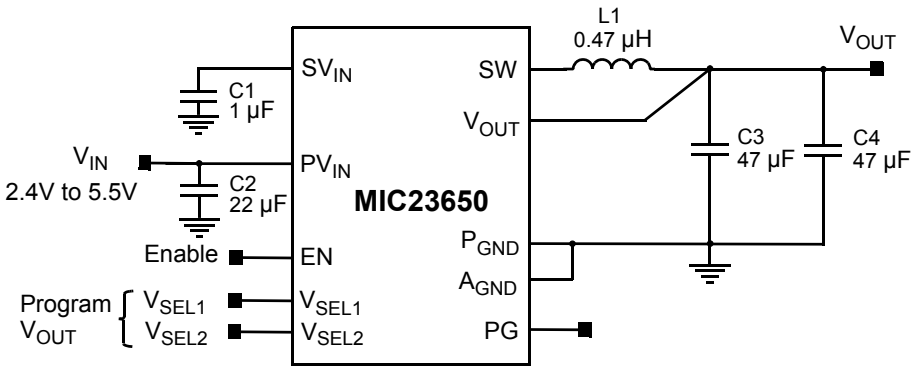
Package Type

MIC23650
16-pin FTQFN 2.5 mm x 2.5 mm



Top View

Typical Application



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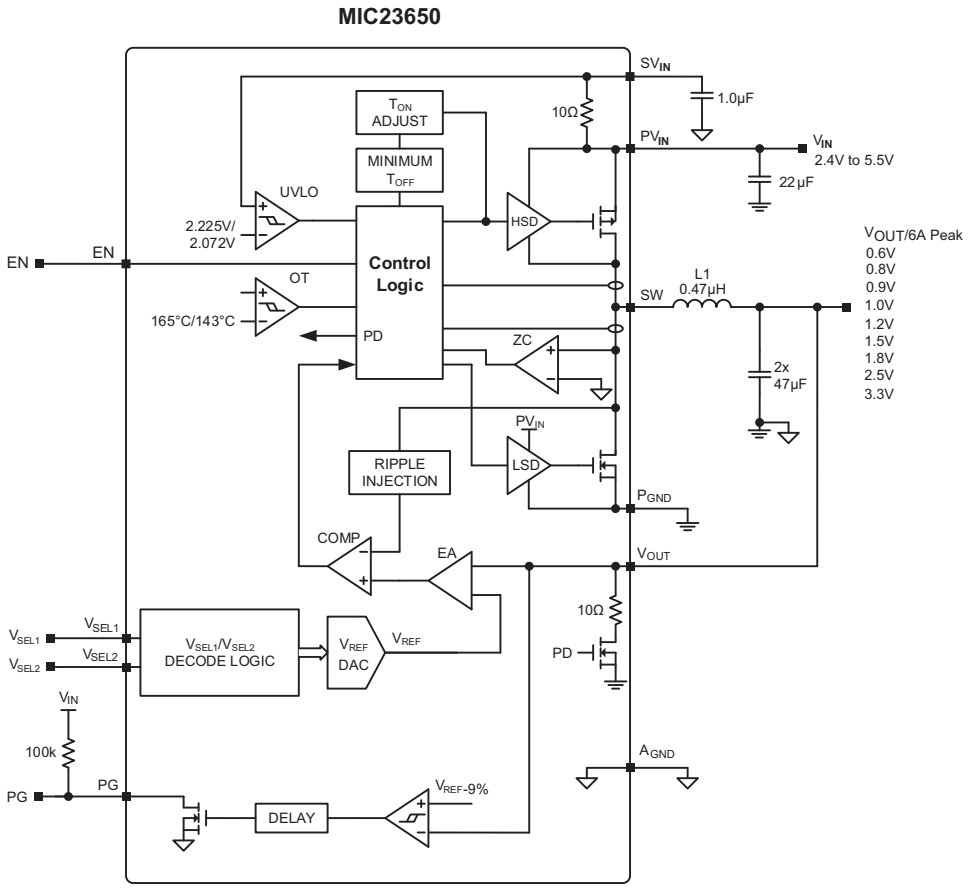
Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

SV_{IN}, PV_{IN} to A_{GND} ..... –0.3V to +6V
V_{SW} to A_{GND} ..... –0.3V to +6V
V_{EN} to A_{GND} ..... –0.3V to PV_{IN}
V_{PG} to A_{GND} ..... –0.3V to PV_{IN}
V_{VSEL1}, V_{VSEL2} to A_{GND} ..... –0.3V to PV_{IN}
PV_{IN} to SV_{IN} ..... –0.3V to +0.3V
A_{GND} to P_{GND} ..... –0.3V to +0.3V
Junction Temperature ..... +150°C
Storage Temperature (T_S) ..... –65°C to +150°C
Lead Temperature (soldering, 10s) ..... +260°C
ESD Rating (Note 1)
HBM 2000V
CDM 1500V
MM 200V

† Notice: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5 kΩ in series with 100 pF.

Operating Ratings[(1)]

Supply Voltage (PV_{IN}) ..... 2.4V to 5.5V
Enable Voltage (V_{EN}) ..... 0V to PV_{IN}
Power-Good Pull-Up Voltage (V_{PU_PG}) ..... 0V to 5.5V
Maximum Output Current 6A
Junction Temperature (T_J) ..... –40°C to +125°C

Note 1: The device is not ensured to function outside the operating range.

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ELECTRICAL CHARACTERISTICS (Note 1)

Electrical Specifications: unless otherwise specified, PV_{IN} = 5V; V_{OUT} = 1.0V, C_{OUT} = 2 x 47 µF, T_A = +25°C. **Boldface** values indicate -40°C ≤ T_J ≤ +125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
V_{IN} Supply						
Input Range	PV_{IN}	**2.4**	—	**5.5**	V	
Undervoltage Lockout Threshold	UVLO	**2.15**	2.225	**2.35**	V	SV_{IN} rising
Undervoltage Lockout Hysteresis	UVLO_H	—	153	—	mV	SV_{IN} falling
Operating Supply Current	I_{IN0}	—	60	**100**	µA	V_{OUT} = 1.2V, nonswitching
Shutdown Current	I_{SHDN}	—	1.5	10	µA	V_{EN} = 0V, PV_{IN} = SV_{IN} = 5.5V, V_{SW}=V_{SEL1}=V_{SEL2}=0V -40°C ≤T_J≤+105°C
		—		**20**	µA	V_{EN} = 0V, PV_{IN} = SV_{IN} = 5.5V, V_{SW}=V_{SEL1}=V_{SEL2}=0V -40°C ≤T_J≤+125°C
Output Voltage vs. $V_{SEL1/2}$						
Output Accuracy	V_{OUT_ACC}	**0.5910**	0.6	**0.6090**	V	V_{SEL2} = 0; V_{SEL1} = 0
		0.7880	0.8	**0.8120**	V	V_{SEL2} = 0; V_{SEL1} = Z
		0.8865	0.9	**0.9135**	V	V_{SEL2} = 0; V_{SEL1} = 1
		0.9850	1.0	**1.0150**	V	V_{SEL2} = Z; V_{SEL1} = 0
		1.1820	1.2	**1.2180**	V	V_{SEL2} = Z; V_{SEL1} = Z
		1.4775	1.5	**1.5225**	V	V_{SEL2} = Z; V_{SEL1} = 1
		1.7730	1.8	**1.8270**	V	V_{SEL2} = 1; V_{SEL1} = 0
		2.4625	2.5	**2.5375**	V	V_{SEL2} = 1; V_{SEL1} = Z
		3.2505	3.3	**3.3495**	V	V_{SEL2} = 1; V_{SEL1} = 1
Line Regulation		—	0.06	—	%	V_{OUT} = 1.0V V_{IN} = 2.5V to 5.5 V I_{OUT} = 300 mA
Load Regulation		—	0.2	—	%	V_{OUT} = 1.0V I_{OUT} = 0A to 6A
Enable Control						
EN Logic Level High	V_{EN_H}	**1.2**	—	—	V	V_{EN} rising, Regulator Enabled
EN Logic Level Low	V_{EN_L}	—	—	**0.4**	V	V_{EN} falling, Regulator Shutdown
EN Low-Input Current	I_{EN_L}	—	0.01	500	nA	V_{EN} = 0V
EN High-Input Current	I_{EN_H}	—	0.01	500	nA	V_{EN} = 5.5V
Enable Lockout Delay	—	0.15	0.25	0.4	ms	
V_{SEL} Logic Level Control						
$V_{SEL1,2}$ Logic Level High	V_{SEL_H}	1.2	—	—	V	$V_{SEL1,2}$ rising, Regulator Enabled
$V_{SEL1,2}$ Logic Level Low	V_{SEL_L}	—	—	0.4	V	$V_{SEL1,2}$ falling, Regulator Shutdown
$V_{SEL1,2}$ Logic Level Open	V_{SEL_O}	—	0.8	—	V	$V_{SEL1,2}$ falling, Regulator Shutdown
$V_{SEL1,2}$ Low-Input Current	I_{VSEL_L}	–1	0.01	1	µA	$V_{SEL1,2}$ = 0V
$V_{SEL1,2}$ High-Input Current	I_{VSEL_H}	–1	0.01	1	µA	$V_{SEL1,2}$ = 5.5V
T_{ON} Control/Switching Frequency						

Note 1: Specification for packaged product only.

2: Tested in open loop. The closed-loop current limit is affected by the inductance value.

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ELECTRICAL CHARACTERISTICS (Note 1) (CONTINUED)

Electrical Specifications: unless otherwise specified, PV_{IN} = 5V; V_{OUT} = 1.0V, C_{OUT} = 2 x 47 µF, T_A = +25°C. **Boldface** values indicate -40°C ≤ T_J ≤ +125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Switching ON Time	TON	—	180	—	ns	V_{IN} = 5V V_{OUT} = 1V
Switching Frequency	FREQ	—	1.2	—	MHz	V_{OUT} = 1.0V, I_{OUT} = 3A, L = XEL4030-471ME
		—	1.1	—		V_{OUT} = 3.3V, I_{OUT} = 3A, L = XEL4030-471
Maximum Duty Cycle	DCMAX	—	—	**100**	%	
Short-Circuit Protection						
High-Side MOSFET Forward Current Limit	I_{LIM_HS}	8	10	12	A	**Note 2**
Low-Side MOSFET Forward Current Limit	I_{LIM_LS}	—	8	—	A	**Note 2**
Low-Side MOSFET Negative Current Limit	I_{LIM_NEG}	–2	–3	–4	A	**Note 2**
N-Channel Zero-Crossing Threshold	I_{ZC_TH}	—	0.9	—	A	
Current Limit Events before Hiccup	HICCUP	—	8	—	Cycles	
Hiccup Period before Restart	—	—	1	—	ms	
Internal MOSFETs						
High-Side ON-Resistance	$R_{DS-ON-HS}$	—	30	60	mΩ	I_{SW} = 1A
Low-Side ON-Resistance	$R_{DS-ON-LS}$	—	16	40	mΩ	I_{SW} = –1A
Output Discharge Resistance	$R_{DS-ON-DSC}$	—	10	50	Ω	V_{EN} = 0V, V_{SW} = 5.5V, from V_{OUT} to P_{GND}
SW Leakage Current	I_{LEAK_SW}	—	1	**10**	µA	PV_{IN} = 5.5V, V_{SW} = 0V, V_{EN} = 0V, flowing out of SW pin
Power Good						
PG Threshold	PG_TH	87	91	95	$\%V_{OUT}$	V_{OUT} Rising (Good)
PG Hysteresis	PG_HYS	—	4	—	$\%V_{OUT}$	V_{OUT} Falling
PG Blanking Time	PG_BLANK	—	65	—	µs	
PG Output Leakage Current	PG_LEAK	—	30	300	nA	V_{OUT} = $V_{OUT(NOM)}$, V_{PG} = 5.5V
PG Sink Low Voltage	PG_SINKV	—	—	200	mV	V_{OUT} = 0V; I_{PG} = 10 mA
Thermal Shutdown						
Thermal Shutdown	T_{SHDN}	—	+165	—	°C	T_J rising
Thermal Shutdown Hysteresis	T_{SHDN_HYST}	—	+22	—	°C	T_J falling
Thermal Latch-Off Soft Start Cycles	TH_LATCH	—	4	—	Cycles	

Note 1: Specification for packaged product only.

2: Tested in open loop. The closed-loop current limit is affected by the inductance value.

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TEMPERATURE SPECIFICATIONS

Electrical Specifications: unless otherwise specified, SV_{IN} = PV_{IN} = 5V; V_{OUT} = 1.0V, C_{OUT} = 2 x 47 µF, T_A = +25°C.
Boldface values indicate –40°C ≤ T_J ≤ +125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Junction Temperature	T_J	–40	—	+125	°C	
Storage Temperature Range	T_A	–65	—	+150	°C	
Package Thermal Resistances						
Thermal Resistance, 16LD 2.5 mm x 2.5 mm thin FTQFN	θ_{JA}	—	+45	—	°C/W	

2.0 TYPICAL CHARACTERISTIC CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, PV_{IN} = 5V, L = 0.47 µH, T_A = +25°C.

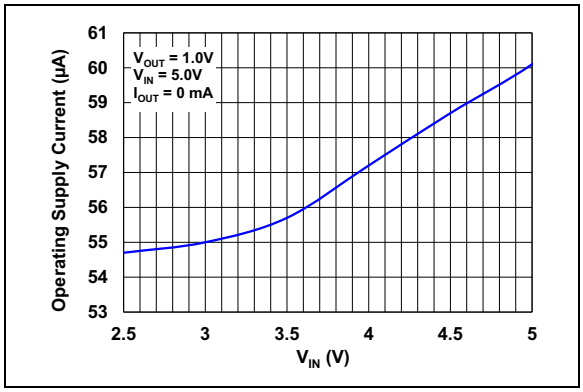

FIGURE 2-1: *Operating Supply Current vs. Input Voltage, Switching.*

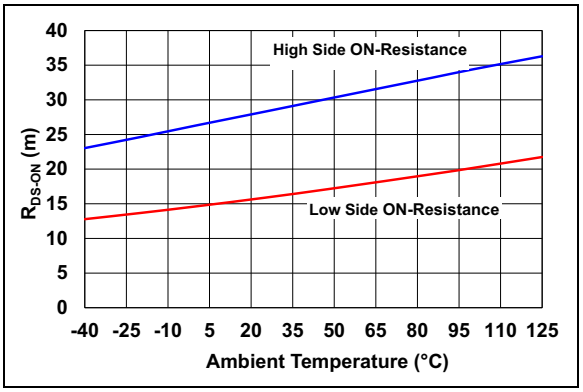

FIGURE 2-4: *R_{DS-ON} vs. Temperature.*

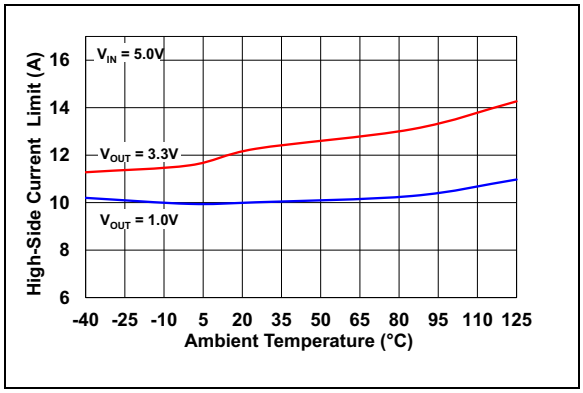

FIGURE 2-2: *High-Side Current Limit vs. Temperature (closed-loop).*

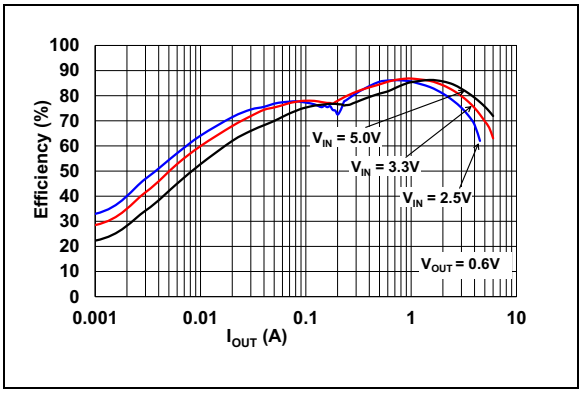

FIGURE 2-5: *Efficiency vs. Load Current.*

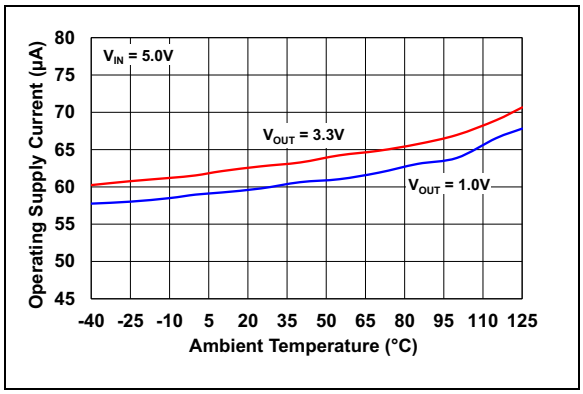

FIGURE 2-3: *Operating Supply Current vs. Temperature, Switching.*

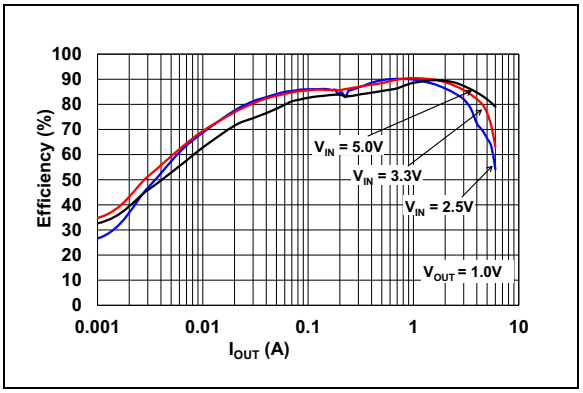

FIGURE 2-6: *Efficiency vs. Load Current.*

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Note: Unless otherwise indicated, PV_{IN} = 5V, L = 0.47 µH, T_A = +25°C.

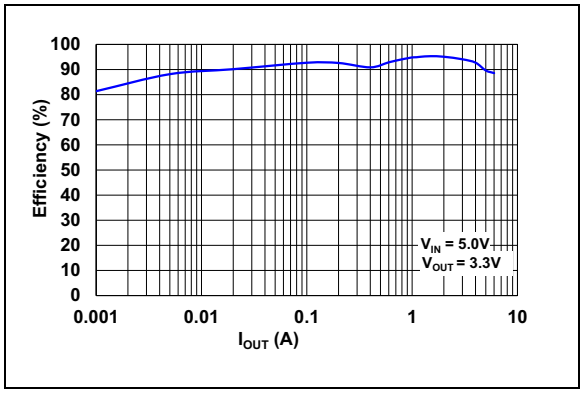

FIGURE 2-7: *Efficiency vs. Load Current.*

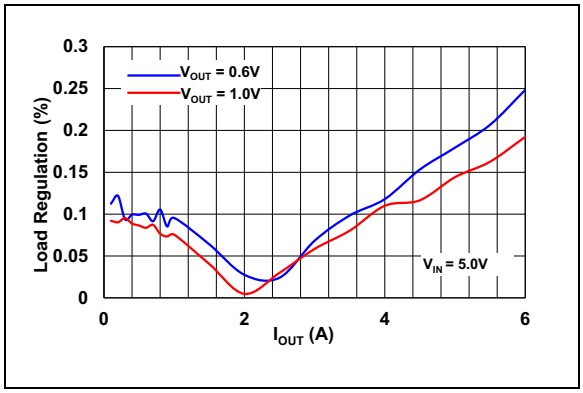

FIGURE 2-10: *Load Regulation: V_{OUT} Voltage Variation vs. I_{OUT}.*

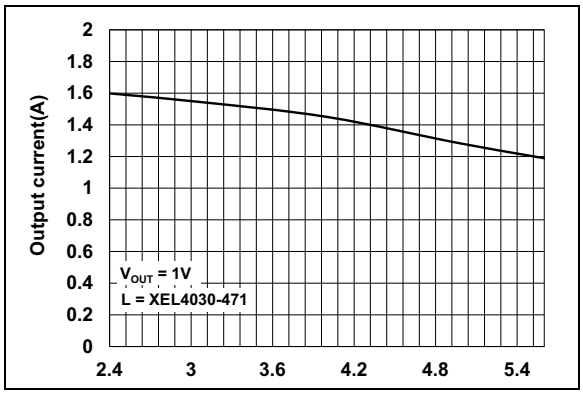

FIGURE 2-8: *DCM/FPWM I_{OUT} Threshold vs. V_{IN}.*

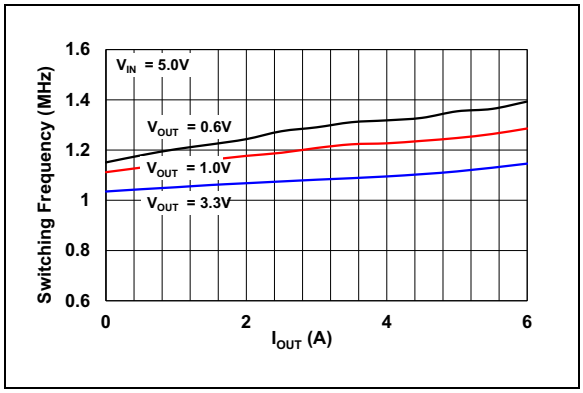

FIGURE 2-11: *Switching Frequency vs. Output Current.*

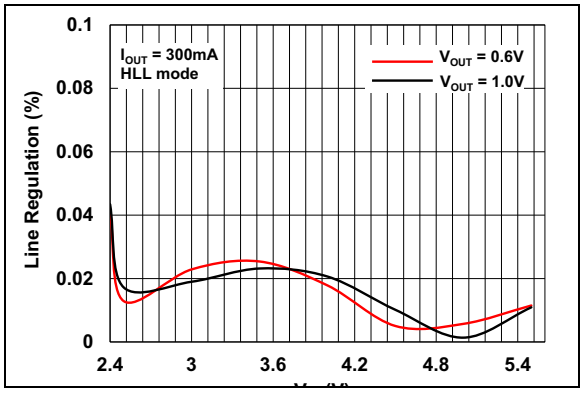

FIGURE 2-9: *Line Regulation: Output Voltage Variation vs. Input Voltage.*

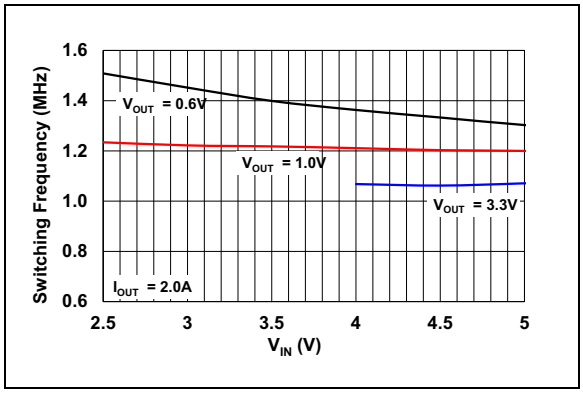

FIGURE 2-12: *Switching Frequency vs. Input Voltage.*

Note: Unless otherwise indicated, PV_{IN} = 5V, L = 0.47 µH, T_A = +25°C.

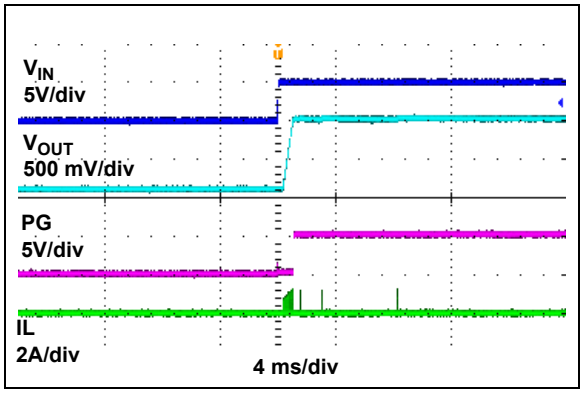

FIGURE 2-13: *V_{IN} Turn-On (EN = PV_{IN}).*

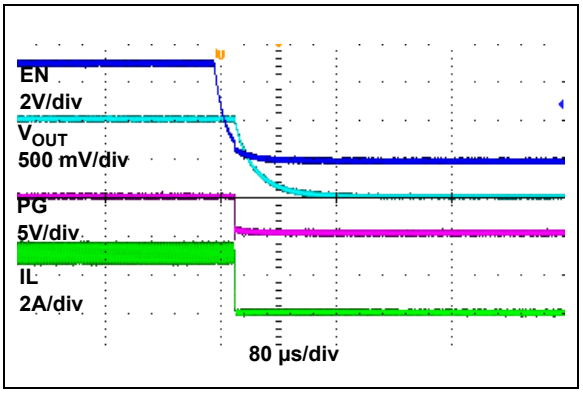

FIGURE 2-16: *EN Turn-Off, R_{LOAD} = 0.3Ω.*

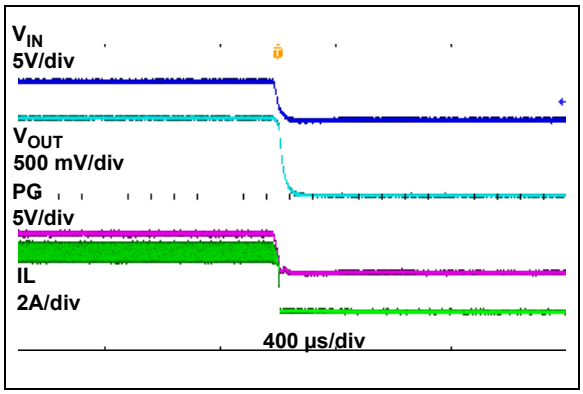

FIGURE 2-14: *V_{IN} Turn-Off (EN = PV_{IN}), R_{LOAD} = 0.3Ω.*

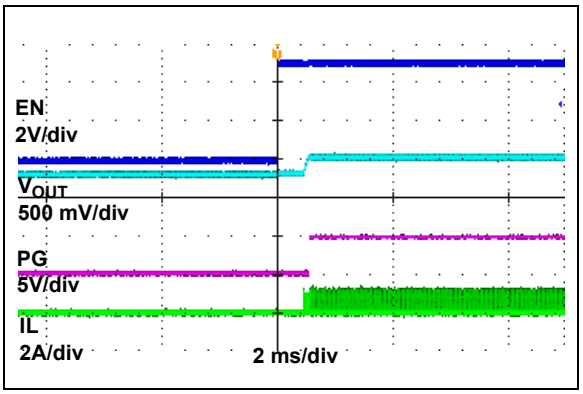

FIGURE 2-17: *EN Turn-On into Pre-Biased Output ($V_{pre\text{-}bias}$ = 0.8V).*

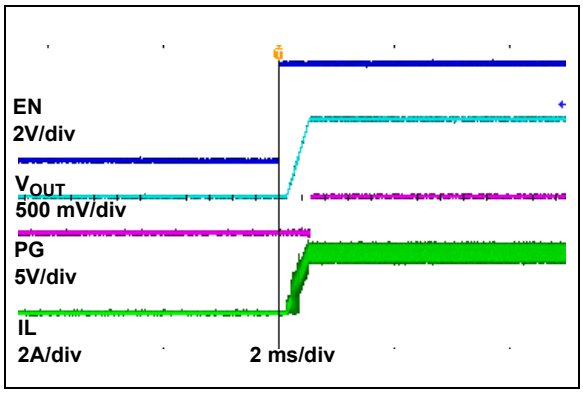

FIGURE 2-15: *EN Turn-On, R_{LOAD} = 0.3Ω.*

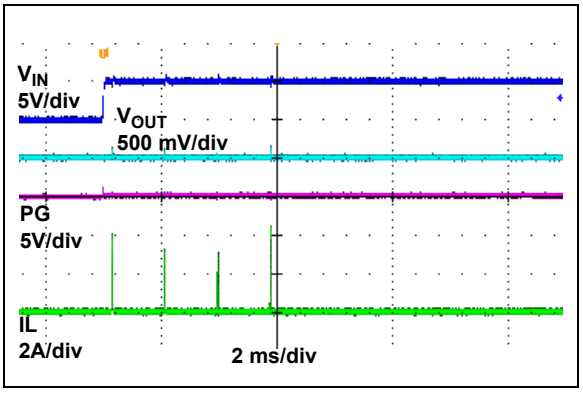

FIGURE 2-18: *Power-Up into Short-Circuit.*

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Note: Unless otherwise indicated, $SV_{IN} = PV_{IN} = 5V$, L = 0.47 µH, T_A = +25°C.

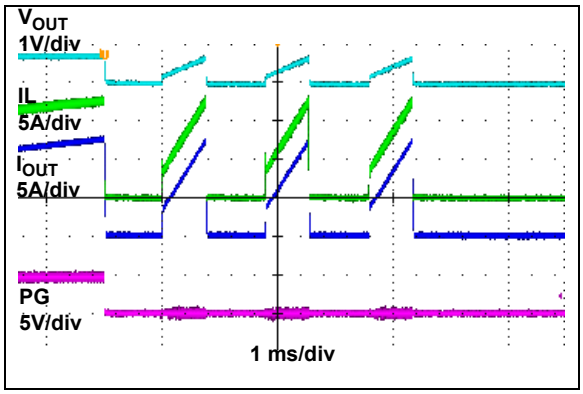

FIGURE 2-19: *Output Current Limit Threshold.*

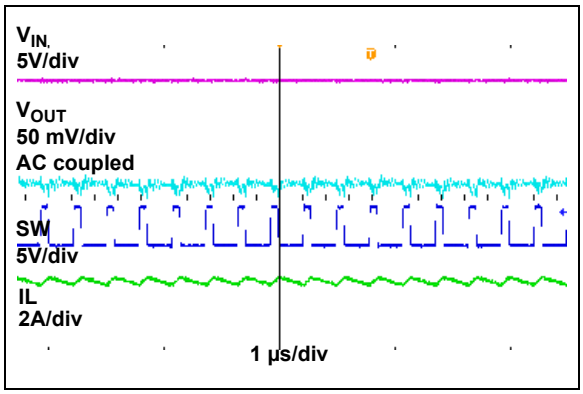

FIGURE 2-22: *Switching Waveforms, I_{OUT} = 6A.*

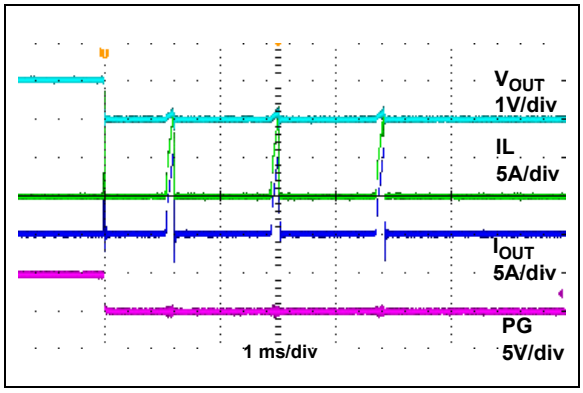

FIGURE 2-20: *Hiccup Mode Short-Circuit Current Limit Response.*

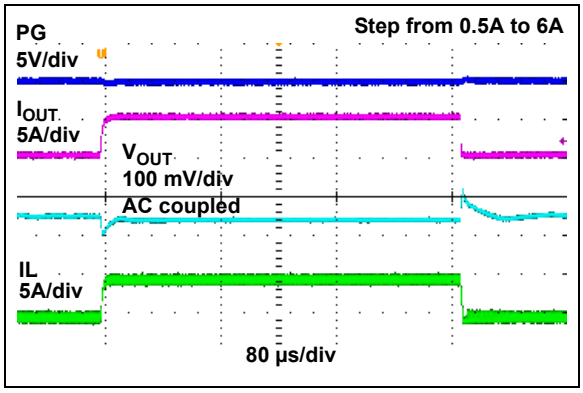

FIGURE 2-23: *Load Transient Response.*

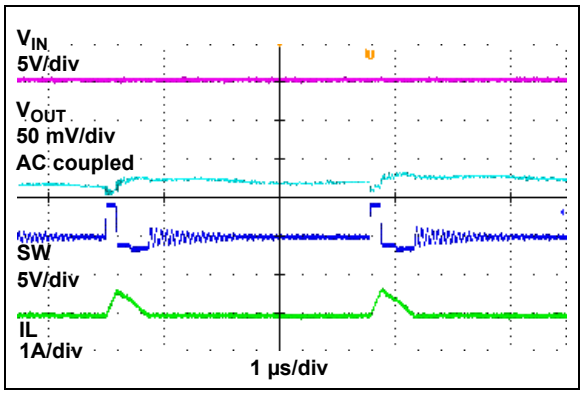

FIGURE 2-21: *Switching Waveforms, I_{OUT} = 50 mA.*

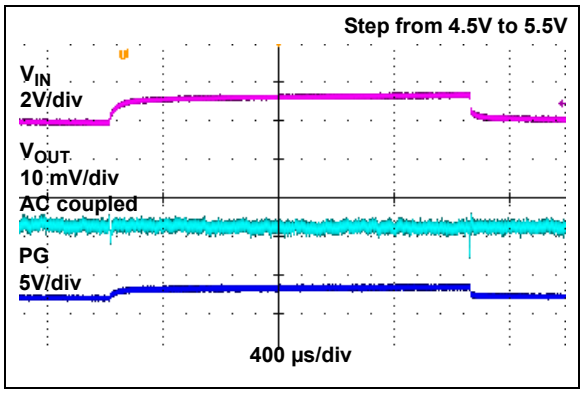

FIGURE 2-24: *Line Transient Response.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Symbol	Description
2, 3, 13, 14, 15	P_{GND}	Power Ground P_{GND} is the ground path for the MIC23650 buck converter power stage.
1, 16	SW	Switch Node pin
4, 5	PV_{IN}	Power Supply Voltage pin
6	SV_{IN}	Analog Voltage Input pin: the power to the internal reference and control sections of the MIC23650. A 1.0 µF ceramic capacitor from SV_{IN} to ground must be used. Internally connected to PV_{IN} through a 10Ω resistor.
7	V_{SEL2}	Output Voltage Selection Control 2 (Input) pin: the logic state of V_{SEL1} and V_{SEL2} selects the output voltage. This input has three digital states: High, Low and Floating.
8	V_{SEL1}	Output Voltage Selection Control 1 (Input) pin: the logic state of V_{SEL1} and V_{SEL2} selects the output voltage. This input has three digital states: High, Low and Floating.
9	EN	Enable (Input) pin: logic high enables the operation of the regulator. The EN pin should not be left open.
10	PG	Power Good (Output) pin: this is an open-drain output that indicates when the output voltage is higher than the 91% limit.
11	V_{OUT}	Output Voltage Sense (Input) pin: this pin is used to remote sense the output voltage. Connect V_{OUT} as close to the output capacitor as possible to sense the output voltage. Also provides the path to discharge the output through an internal 10Ω resistor when disabled.
12	A_{GND}	Analog Ground pin: internal signal ground for all low-power circuits
17	EP	Exposed Thermal pad, internally connected to P_{GND}

3.1 Power Ground Pin (P_{GND})

P_{GND} is the ground path for the MIC23650 buck converter power stage. The P_{GND} pin connects to the sources of low-side N-Channel MOSFETs, the negative terminals of input capacitors, and the negative terminals of output capacitors. The loop for the power ground should be as small as possible and separate from the analog ground (A_{GND}) loop.

3.2 Switch Node Pin (SW)

High-current output which connects to the internal MOSFETs. Connect the inductor to this pin. This is a high-frequency, high-power connection; therefore, traces should be kept as short and as wide as practical.

3.3 Input Voltage Pin (PV_{IN})

Input supply to the source of the internal high-side P-channel MOSFET. The PV_{IN} operating voltage range is from 2.4V to 5.5V. An input capacitor between PV_{IN} and the power ground P_{GND} pin is required and placed as close as possible to the IC.

3.4 Analog Voltage Input Pin (SV_{IN})

This pin is the power to the internal reference and control sections of the MIC23650. A 1.0 µF ceramic capacitor from SV_{IN} to ground must be used. It is internally connected to PV_{IN} through a 10Ω resistor.

3.5 Output Voltage Selection Control Pin 2 (V_{SEL2})

Output Voltage Selection Control 2 (Input). The logic state of the V_{SEL1} and V_{SEL2} selects the output voltage. This input has three digital states: High, Low and Floating. See Table 4-1.

3.6 Output Voltage Selection Control Pin 1 (V_{SEL1})

Output Voltage Selection Control 1 (Input). The logic state of V_{SEL1} and V_{SEL2} selects the output voltage. This input has three digital states: High, Low and Floating. See Table 4-1.

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3.7 Enable Pin (EN)

The logic high enables the operation of the regulator. Logic low shuts down the device. In the OFF state, the supply current of the device is greatly reduced (typically 1.5 µA). The EN pin should not be left open.

3.8 Power Good Pin (PG)

This is an open-drain output that indicates when the output voltage is higher than the 91% limit. There is a 4% hysteresis, therefore PG will return low when the falling output voltage falls below 87% of the target regulation voltage.

3.9 Output Voltage Sense Pin (V_{OUT})

This pin is used to remote sense the output voltage. Connect to V_{OUT} as close to the output capacitor as possible to sense the output voltage. It also provides the path to discharge the output through an internal 10Ω resistor when the device is disabled.

3.10 Analog Ground Pin (A_{GND})

Internal signal ground for all low power circuits. Connect to ground plane. For best load regulation, the connection path from A_{GND} to the output capacitor ground terminal should be free from parasitic voltage drops.

3.11 P_{GND} Exposed Pad (P_{GND})

It is electrically connected to P_{GND} pins. It must be connected with thermal vias to the ground plane to ensure adequate heat-sinking. See Section 6.0, Packaging Information.

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4.0 FUNCTIONAL DESCRIPTION

4.1 Device Overview

The MIC23650 is a high-efficiency, 6A peak current synchronous buck regulator with HyperLight Load mode. The COT control architecture with automatic HyperLight Load mode provides very high efficiency at light loads and ultra-fast transient response.

The MIC23650 output voltage is set by two V_{SEL} three-state logic pins that can set the output voltage to nine different values. See Table 4-1.

The 2.4V to 5.5V input voltage operating range makes the device ideal for single cell Li-Ion battery-powered applications. The 100% duty cycle capability provides low dropout operation, extending battery life in portable systems. The automatic HyperLight Load mode provides very high efficiency at light loads.

This device focuses on high output voltage accuracy. Total output error is less than 1.5% over line, load and temperature.

The MIC23650 buck regulator uses an adaptive COT control method. The adaptive on-time control scheme is employed to obtain a nearly constant switching frequency in Continuous Conduction mode. Overcurrent protection is implemented by sensing the current on both the low-side and high-side internal power MOSFETs. The device includes an internal soft start function which reduces the power supply input surge current at start-up by controlling the output voltage rise time.

4.2 HyperLight Load Mode (HLL)

HLL is a power saving mode. In HLL, the switching frequency is not constant over the operation current range, but its average value reduces proportionally to the load current. This reduces switching and drive losses and maintains high efficiency as the load current decreases.

4.3 Enable (EN)

When the EN pin is pulled LOW, the IC is in a Shutdown state with all internal circuits disabled with the PG output low. During shutdown, the part typically consumes .5 µA. When the EN pin is pulled HIGH, the start-up sequence is initiated.

4.4 Power Good (PG)

The PG output is generally used for power sequencing where the power good output is tied to the enable output of another regulator. This technique avoids all the regulators powering up at the same time, causing large inrush current.

The PG output is an open-drain output. During start-up when the output voltage is rising, the PG output goes high by means of an external pull-up resistor, when the output voltage reaches 91% of its set value. The PG threshold has 4% hysteresis so the PG output stays high until the output voltage falls below 87% of the set value. A built-in 65 µs blanking time is incorporated to prevent nuisance tripping.

The pull-up resistor can be connected to V_{IN}, V_{OUT} or an external source that is less than or equal to V_{IN}. The PG pin can be connected to another regulator's enable pin for outputs sequencing. The PG output is deasserted as soon as the enable pin is pulled low or an input undervoltage condition or any other Fault is detected.

4.5 Resistive Discharge (Soft-Discharge)

To ensure a known output condition when the device is turned off and then back on, the output is actively discharged to ground by means of an internal 10Ω resistor. This prevents the load from powering up starting from an undefined condition.

4.6 Output Voltage Setting

The MIC23650 V_{SEL1} and V_{SEL2} pins are used to choose among nine predefined voltage settings: 0.6V, 0.8V, 0.9V, 1.0V, 1.2V, 1.5V, 1.8V, 2.5V, 3.3V. These pins can be tied to V_{IN}, GND or left floating. The relation between V_{SEL1}/V_{SEL2} and the output voltage is shown in Table 4-1.

TABLE 4-1: OUTPUT VOLTAGE SETTINGS

V_{SEL2}	V_{SEL1}	V_{OUT}
GND	GND	0.6V
GND	OPEN	0.8V
GND	V_{IN}	0.9V
OPEN	GND	1.0V
OPEN	OPEN	1.2V
OPEN	V_{IN}	1.5V
V_{IN}	GND	1.8V
V_{IN}	OPEN	2.5V
V_{IN}	V_{IN}	3.3V

The output voltage sensing pin V_{OUT} should be connected to the desired point-of-load regulation, avoiding parasitic resistive drops. It is possible to fine tune the desired output voltage, by adding a series resistor on VOUT pin. This allows slightly higher output values programming, but should not exceed 5% deviation from the VSEL selected value.

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EQUATION 4-1:

$R_{VOUT} = 8.2k\Omega * TRIM$

Where:

RV_{OUT} = V_{OUT} series resistance needed for a TRIM% output voltage increase

4.7 Converter Stability, Output Capacitor

The MIC23650 utilizes an internal compensation network and it is designed to provide stable operation with output capacitors from 47 µF to 1000 µF. This greatly simplifies the design where the user can add supplementary output capacitance without having to worry about stability.

4.8 Soft Start

Excess bulk capacitance on the output can cause excessive input inrush current. The MIC23650 internal soft start feature forces the output voltage to rise gradually, keeping the inrush current at reasonable levels. This is particularly important in battery-powered applications. When the enable pin goes high, the output voltage starts to rise. Once the soft start period has finished, the PG comparator is enabled, and if the output voltage is above 91% of the nominal regulation voltage, then the PG output goes high.

The output voltage soft start time is determined by the soft start equation below. The soft-start time t_{SS} can be calculated by:

EQUATION 4-2:

$$t_{SS} = V_{OUT} \times t_{RAMP}$$

$$t_{SS} = 1.0V \times 800\mu s/V$$

$$t_{SS} = 800\mu s = 0.8ms$$

Where:

V_{OUT} = 1.0V

t_{RAMP} = 800 µs/V

4.9 Dropout Operation

As the input voltage approaches the output voltage, the minimum on-time limits the maximum duty cycle. To achieve a 100% duty cycle, the high-side switch is latched on when the duty cycle reaches around 92% and stays latched until the output voltage falls 4% below its regulated value. In dropout, the output voltage is determined by the input voltage minus the voltage drop across the high-side MOSFET.

4.10 Switching Frequency

The switching frequency of the MIC23650 is determined by the internal on-time (T_{ON}) calculation. For an input voltage of 5V and an output voltage of 1V, the typical value of T_{ON} is 180 ns.

The resulting switching frequency can be estimated by the following equation:

EQUATION 4-3:

$$f_{SW} = V_{OUT}/(V_{IN} \times T_{ON})$$

The above equation is only valid in Continuous Conduction mode and for a lossless converter. In practice, losses will cause an increase of the switching frequency with respect to the ideal case. As the load current increases, losses increase too and so does the switching frequency.

The on-time calculation is adaptive, in that the T_{ON} value is modulated based on the input voltage and on the target output voltage to stabilize the switching frequency against their variations. Losses are not accounted for.

TABLE 4-2: T_{ON} FOR TYPICAL APPLICATIONS

V_{IN} (V)	V_{OUT} (V)	T_{ON}
5	0.6	110
	1	180
	1.8	340
	2.5	490
	3.3	610
3.3	1	270

4.11 Undervoltage Protection (UVLO)

Undervoltage protection ensures that the IC has enough voltage to bias the internal circuitry properly and provide sufficient gate drive for the power MOSFETs. When the input voltage starts to rise, both power MOSFETs are off and the PG output is pulled low. The IC starts at typically 2.225V and has a typical 153 mV of hysteresis to prevent chattering between the UVLO High and Low states.

4.12 Overtemperature Fault

The MIC23650 monitors the die junction temperature to keep the IC operating properly. If the IC junction temperature exceeds +165°C, both power MOSFETs are immediately turned off. The IC is allowed to restart when the die temperature falls below +143°C.

During recovery from a thermal shutdown event, if the regulator hits another thermal shutdown event or a current limit event is causing hiccup before PG can be achieved, the controller resets again. If this happens four times in a row, the part will be in a latch-off state and the MOSFETs are permanently latched off. The MIC23650 will not restart unless the input power is cycled or the EN pin is set low and then high again. This latch-off feature eliminates the thermal stress on the MIC23650 during a persistent Fault event.

4.13 Safe Start-Up into a Pre-Biased Output

The MIC23650 is designed for safe start-up into a pre-biased output. This feature prevents high negative inductor current flow in a pre-bias condition which can damage the IC. This is achieved by not allowing PWM operation until the control loop commands 8 switching cycles. After 8 cycles, the low-side negative current limit is switched from 0A to -3A. The cycle counter is reset to zero if the enable pin is pulled low or an input undervoltage condition or any other Fault is detected.

4.14 Current Limiting

The MIC23650 regulator uses both high-side and low-side current sense for current limiting. When the high-side current sense threshold is reached, the high-side MOSFET is turned off and the low-side MOSFET is turned on. The low-side MOSFET stays on until the current falls to 80% of the high-side current threshold value then the high-side can be turned on again. If the overload condition lasts for more than seven cycles, the MIC23650 enters hiccup current limiting and both MOSFETs are turned off. There is a cool-off period before the MOSFETs are allowed to be turned on. If the regulator has another hiccup event before it reaches the power good threshold on restart it will again turn off both MOSFETs and wait for the cool-off period. If this happens more than three times in a row, then the part enters the latch-off state, which will permanently turn off both MOSFETs until the part is reset by cycling input power or by toggling the enable input.

4.15 Thermal Considerations

Although the MIC23650 is capable of delivering up to 6A under load, the package thermal resistance and the device internal power dissipation may dictate some limitations to the continuous output current.

As a reference, for V_{IN} = 5V, V_{OUT} = 1V, I_{OUT} = 5A, the evaluation board application shows a stable +40°C chip package self heating (ADM00885).

For V_{IN} = 5V, V_{OUT} = 3.3V, the same self heating is produced at about 4A.

If operated above the rated junction temperature, electrical parameters may drift beyond characterized specifications. The MIC23650 is protected under all circumstances by thermal shutdown.

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5.0 APPLICATION INFORMATION

5.1 Output Voltage Sensing

To achieve accurate output voltage regulation, the V_{OUT} pin (internal feedback divider top terminal) should be Kelvin-connected as close as possible to the point of regulation top terminal. Since both the internal reference and the internal feedback divider's bottom terminal refer to A_{GND}, it is important to minimize voltage drops between the A_{GND} and the point of regulation return terminal (typically the ground terminal of the output capacitor which is closest to the load).

5.2 Inductor Selection and Slope Compensation

When selecting an inductor, it is important to consider the following factors:

- Inductance
- Rated current value
- Size requirements
- DC Resistance (DCR)
- Core losses

Values for inductance, peak, and RMS currents are required to select the output inductor. The input and output voltages and the inductance value determine the peak-to-peak inductor ripple current. Generally, higher inductance values are used with higher input voltages. Larger peak-to-peak ripple currents increase the power dissipation in the inductor and MOSFETs. Larger output ripple currents also require more output capacitance to smooth out the larger ripple current. Smaller peak-to-peak ripple currents require a larger inductance value and therefore a larger and more expensive inductor. A good compromise between size, loss, and cost is to set the inductor ripple current to be equal to about 30% of the maximum output current. The inductance value is calculated by Equation 5-1.

EQUATION 5-1:

$$L = \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \times f_{SW} \times r \times I_{OUT(MAX)}}$$

Where:

f_{SW}	=	Switching Frequency
r	=	Ratio of AC Inductor Ripple Current to DC Output Current (typical 30%)
$V_{IN(MAX)}$	=	Maximum Power Stage Input Voltage

The switching frequency can be estimated from Figure 2-11 and Figure 2-12. The peak-to-peak inductor current ripple is:

EQUATION 5-2:

$$\Delta I_{L(PP)} = \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \times f_{SW} \times L}$$

The peak inductor current is equal to the average output current plus one half of the peak-to-peak inductor current ripple.

EQUATION 5-3:

$$I_{L(PK)} = I_{OUT(MAX)} + 0.5 \times \Delta I_{L(PP)}$$

The RMS inductor current is used to calculate the I^2R losses in the inductor.

EQUATION 5-4:

$$I_{L(RMS)} = \sqrt{I_{OUT(MAX)}^2 + \frac{\Delta I_{L(PP)}^2}{12}}$$

Maximizing efficiency requires the proper selection of core material while minimizing the winding resistance. The high-frequency operation of the MIC23650 requires the use of low-loss high-frequency magnetic materials for all but the most cost-sensitive applications. Lower cost iron powder cores may be used, but the increase in core loss will reduce the efficiency of the power supply. This is especially noticeable at low output power. The winding resistance decreases efficiency at the higher output current levels. The winding resistance must be minimized, although this usually comes at the expense of a larger inductor. The power dissipated in the inductor is equal to the sum of the core and copper losses. Core loss information is usually available from the magnetics vendor. Copper loss in the inductor is calculated by Equation 5-5.

EQUATION 5-5:

$$P_{INDUCTOR(CU)} = I_{L(RMS)}^2 \times R_{WINDING}$$

The resistance of the copper wire, $R_{WINDING}$, increases with the temperature. The value of the winding resistance should be at the operating temperature.

EQUATION 5-6:

$$P_{WINDING(HT)} = R_{WINDING(20C)} \times (1 + 0.0042 \times (T_H - T_{20C}))$$

Where:

T_H = Temperature of Wire Under Full Load

T_{20C} = Ambient Temperature

$R_{WINDING(20C)}$ = Room Temperature Winding Resistance (usually specified by the manufacturer)

5.3 Output Capacitor Selection

The type of output capacitor is usually determined by its equivalent series resistance (ESR). Voltage and RMS current capability are two other important factors for selecting the output capacitor. Recommended capacitor types are ceramic, OS–CON, and POSCAP. The output capacitor ESR is usually the main cause of the output ripple. The output capacitor ESR also affects the control loop from a stability point of view. The maximum value of ESR is calculated using Equation 5-7.

EQUATION 5-7:

$$ESR_{C_{OUT}} \leq \frac{\Delta V_{OUT(PP)}}{\Delta I_{L(PP)}}$$

Where:

$\Delta V_{OUT(PP)}$ = Peak-to-Peak Output Voltage Ripple

$\Delta I_{L(PP)}$ = Peak-to-Peak Inductor Current Ripple

The total output ripple is a combination of the ESR and output capacitance.The total ripple is calculated in Equation 5-8.

EQUATION 5-8:

$$\Delta V_{OUT(PP)} = \sqrt{\left(\frac{\Delta I_{L(PP)}}{C_{OUT} \times f_{SW} \times 8}\right)^2 + \left(\Delta I_{L(PP)} \times ESR_{C_{OUT}}\right)^2}$$

Where:

C_{OUT} = Output Capacitance Value

f_{SW} = Switching Frequency

The output capacitor RMS current is calculated in Equation 5-9.

EQUATION 5-9:

$$I_{C_{OUT(RMS)}} = \frac{\Delta I_{L(PP)}}{\sqrt{12}}$$

The power dissipated in the output capacitor is:

EQUATION 5-10:

$$P_{DISS(COUT)} = I_{COUT(RMS)}^2 \times ESR_{COUT}$$

5.4 Input Capacitor Selection

The input capacitor for the power stage input V_{IN} should be selected for ripple current rating and voltage rating. Due to the pulsed waveform of the buck stage input current, ceramic input capacitors with good high-frequency characteristics are mandatory and should be placed as close to the device as possible. Additional polarized capacitors can be used in parallel to the ceramic input capacitors. Tantalum input capacitors may fail when subjected to high inrush currents, caused by turning on the input supply. A tantalum input capacitor voltage rating should be at least two times the maximum input voltage to maximize reliability. Aluminum electrolytic, OS–CON, and multilayer polymer film capacitors can handle the higher inrush currents without voltage derating. The input voltage ripple will primarily depend on the input capacitor ESR. The peak input current is equal to the peak inductor current, so:

EQUATION 5-11:

$$\Delta V_{IN} = I_{L(PK)} \times ESR_{CIN}$$

The input capacitor must be rated for the input current ripple. The RMS value of input capacitor current is determined at the maximum output current. Assuming the peak-to-peak inductor current ripple is low:

EQUATION 5-12:

$$I_{CIN(RMS)} \approx I_{OUT(MAX)} \times \sqrt{D \times (1 - D)}$$

Where:

$D = V_{OUT}/V_{IN}$

The power dissipated in the input capacitor is:

EQUATION 5-13:

$$P_{DISS(CIN)} = I_{CIN(RMS)}^2 \times ESR_{CIN}$$

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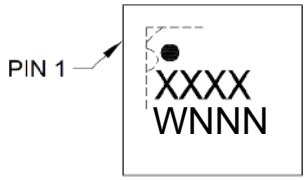
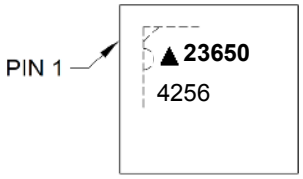
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

16-Lead FTQFN 2.5 mm x 2.5 mm



Example



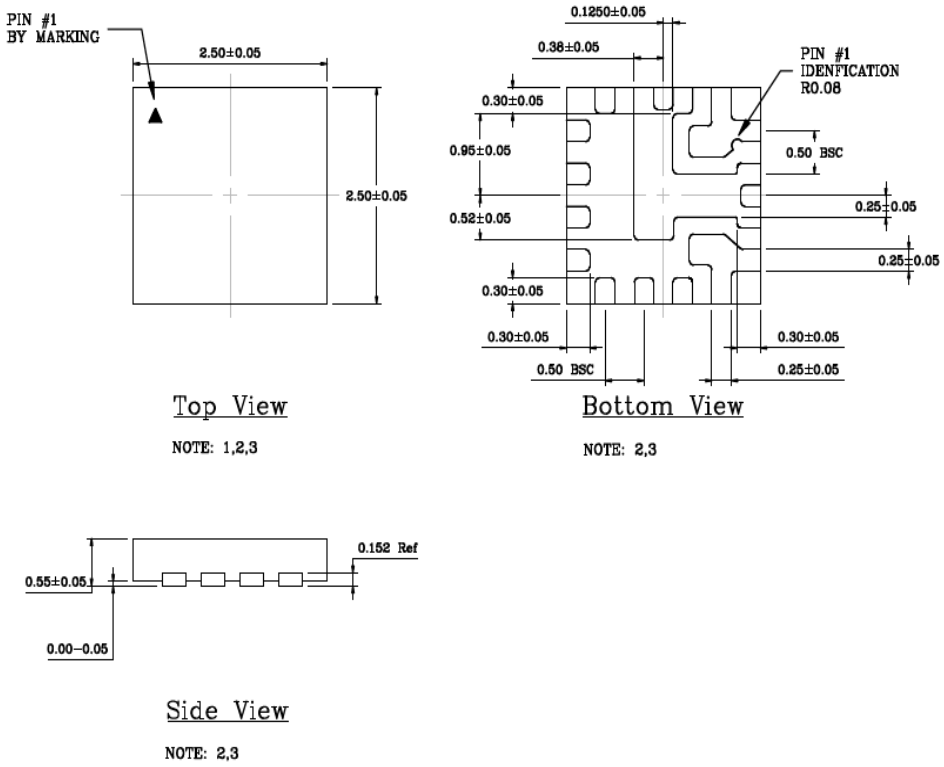
Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

TITLE

16 LEAD FTQFN 2.5x2.5 mm PACKAGE (Flip Chip) OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	FTQFN2525-16LD-PL-1	UNIT	MM



Top View

NOTE: 1,2,3

Bottom View

NOTE: 2,3

Side View

NOTE: 2,3

NOTES:

1. Top mark Pin #1 will be laser mark.
2. 0.05mm max package warpage.
3. Max allowable burr is 0.076mm in all directions.
4. Black, Blue and Red color pads represent different potential. Do not connect to GND.
5. Black color pads represent different IOs. Do not connect together.
6. Shaded rectangles (area) represents solder stencil opening on exposed metal trace.
7. Red Color circles are VIAs. 0.30mm diameter. Should be connected to ground for maximum thermal performance.
8. Thermal VIAs are optional.
9. Recommended Land Pattern Tolerance is ±0.020mm unless specified.
10. See recommended Land Pattern on page2.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

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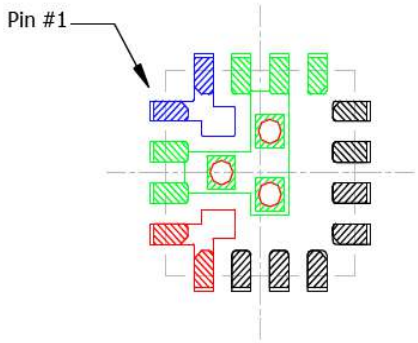
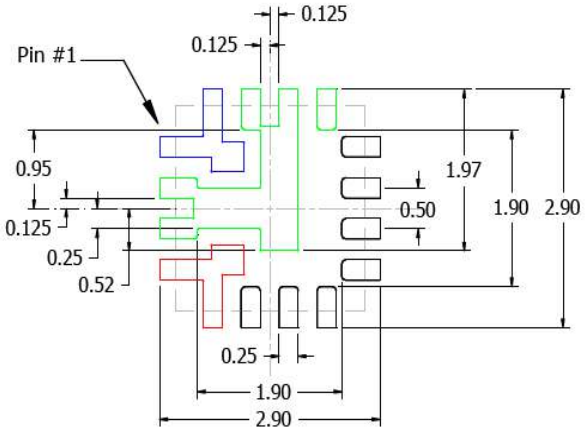
POD-Land Pattern Doc #: FTQFN2525-16LD-PL-1-A

Recommended Land Pattern

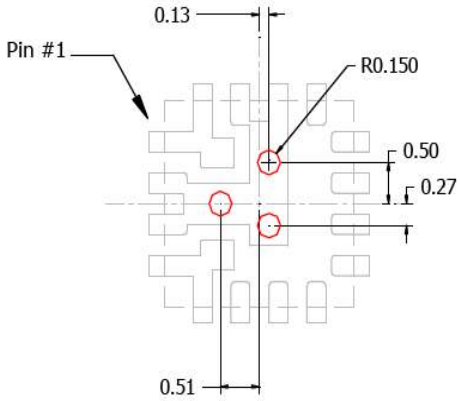
Note: 4,5,6,7,8, 9



Stack Up

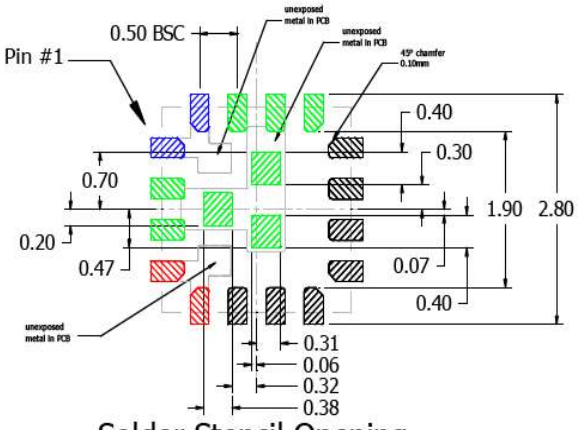


Exposed Metal



Thermal (Filled) VIA

optional



Solder Stencil Opening

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

NOTES:

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APPENDIX A: REVISION HISTORY

Revision B (February 2019)

- Updated Electrical Characteristics: supply current, shutdown current, line regulation and load regulation, TON, SW leakage current, PG hysteresis, PG output leakage, and PG sink low voltage
- Updated Figures 2, 14, 18, 20 and 24
- Updated Pin Function Table
- Updated Sections 3.3, 3.4, 3.5, 3.6, 3.7, 3.8, 4.1, 4.5, 4.10, 4.11, 4.15, 5.3, 5.4
- Updated Equation 5-1
- Other minor editorial updates

Revision A (October 2018)

- Original release of this document

NOTES:

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	XX	XX
Device	Temperature Range	Package	Tape and Reel Option

Device:	MIC23650	Step-Down Converter with HyperLight Load™
Temperature Range:	Y	= -40°C to+125°C Junction Temperature Range, PB-Free
Package:	FT	= 16-Lead FTQFN 2.5 x 2.5 mm
Tape and Reel Option:	TR	= Tape and Reel

Examples:

a) MIC23650YFT: Step-Down Converter with HyperLight Load, -40°C to+125°C Junction Temperature Range, 16-Lead FTQFN

b) MIC23650YFT-TR: Step-Down Converter with HyperLight Load, -40°C to +125°C Junction Temperature Range, 16-Lead FTQFN, Tape and Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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ISBN: 978-1-5224-4200-4

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