

## Evaluation Board for CS4362A

### Features

- ◆ Demonstrates recommended layout and grounding arrangements
- ◆ CS8416 receives S/PDIF, & EIAJ-340 compatible digital audio
- ◆ Headers for external audio input for either PCM or DSD®
- ◆ Requires only a digital signal source and Power supplies for a complete digital-to-analog converter system

### Description

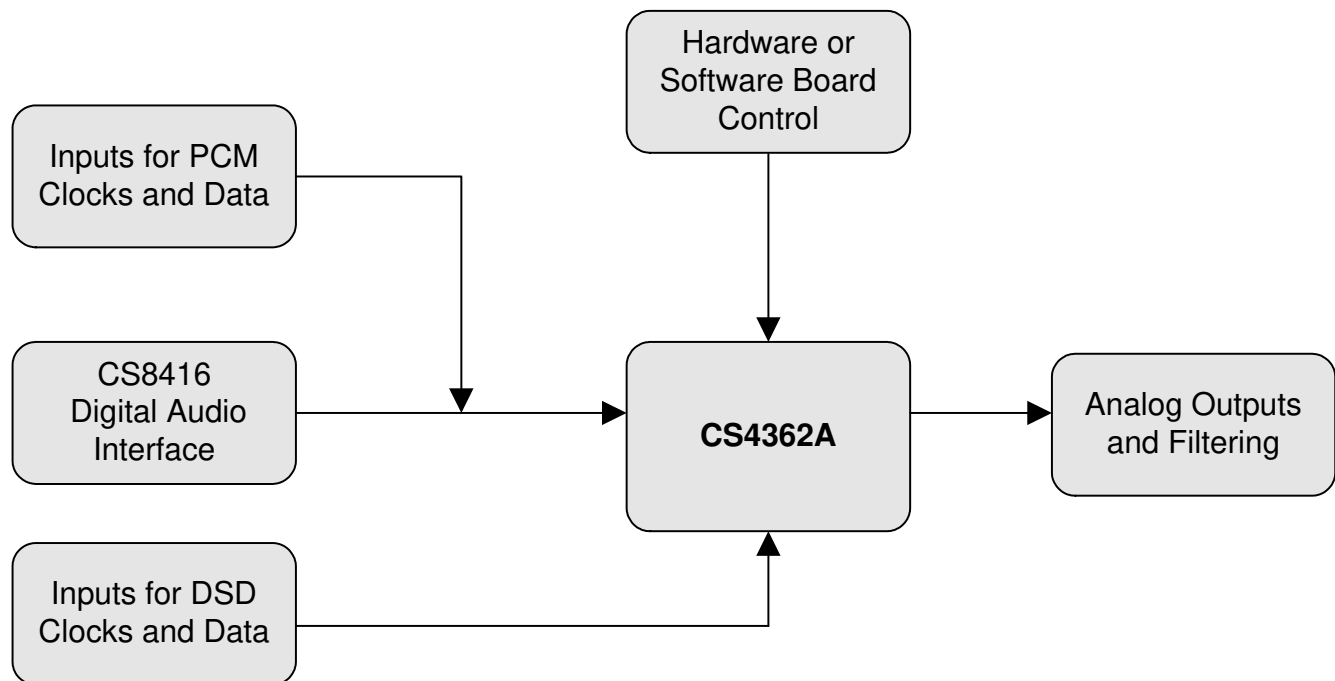
The CDB4362A evaluation board is an excellent means for quickly evaluating the CS4362A 24-bit, 48-pin, 6-channel D/A converter. Evaluation requires an analog signal analyzer, a digital signal source, a PC for controlling the CS4362A (only required for control port mode), and a power supply. Analog line-level outputs are provided via RCA phono jacks.

The CS8416 digital audio receiver IC provides the system timing necessary to operate the digital-to-analog converter and will accept S/PDIF and EIAJ-340-compatible audio data. The evaluation board may also be configured to accept external timing and data signals for operation in a user application during system development.

### ORDERING INFORMATION

CDB4362A

Evaluation Board



---

**TABLE OF CONTENTS**

<b>1. CS4362A DIGITAL-TO-ANALOG CONVERTER .....</b>	<b>4</b>
<b>2. CS8416 DIGITAL AUDIO RECEIVER .....</b>	<b>4</b>
<b>3. INPUT FOR CLOCKS AND DATA .....</b>	<b>4</b>
<b>4. INPUT FOR CONTROL DATA .....</b>	<b>5</b>
<b>5. POWER SUPPLY CIRCUITRY .....</b>	<b>5</b>
<b>6. GROUNDING AND POWER SUPPLY DECOUPLING .....</b>	<b>5</b>
<b>7. ANALOG OUTPUT FILTERING .....</b>	<b>5</b>
<b>8. PERFORMANCE PLOTS .....</b>	<b>7</b>
<b>9. CDB4362A SCHEMATICS .....</b>	<b>17</b>
<b>10. REVISION HISTORY .....</b>	<b>30</b>

**LIST OF FIGURES**

Figure 1.FFT (48 kHz, 0 dB) .....	7
Figure 2.FFT (48 kHz, -60 dB) .....	7
Figure 3.FFT (48 kHz, No Input) .....	7
Figure 4.FFT (48 kHz Out-of-Band, No Input) .....	7
Figure 5.FFT (48 kHz -60 dB Wideband) .....	8
Figure 6.FFT (IMD 48 kHz) .....	8
Figure 7.48 kHz, THD+N vs. Input Freq .....	8
Figure 8.48 kHz, THD+N vs. Level .....	8
Figure 9.48 kHz, Fade-to-Noise Linearity .....	8
Figure 10.48 kHz, Frequency Response .....	8
Figure 11.48 kHz, Crosstalk .....	9
Figure 12.48 kHz, Impulse Response .....	9
Figure 13.48 kHz, Impulse Prefilter .....	9
Figure 14.Dynamic Range 48 kHz .....	10
Figure 15.FFT (96 kHz, 0 dB) .....	10
Figure 16.FFT (96 kHz, -60 dB) .....	10
Figure 17.FFT (96 kHz, No Input) .....	11
Figure 18.FFT (96 kHz Out-of-Band, No Input) .....	11
Figure 19.FFT (96 kHz, -60 dB Wideband) .....	11
Figure 20.FFT (IMD 96 kHz) .....	11
Figure 21.96 kHz, THD+N vs. Input Freq .....	11
Figure 22.96 kHz, THD+N vs. Level .....	11
Figure 23.96 kHz, Fade-to-Noise Linearity .....	12
Figure 24.96 kHz, Frequency Response .....	12
Figure 25.96 kHz, Crosstalk .....	12
Figure 26.96 kHz, Impulse Response .....	12
Figure 27.96 kHz, Impulse Prefilter .....	12
Figure 28.Dynamic Range 96 kHz .....	13
Figure 29.FFT (192 kHz, 0 dB) .....	13
Figure 30.FFT (192 kHz, -60 dB) .....	13
Figure 31.FFT (192 kHz, No Input) .....	14
Figure 32.FFT (192 kHz Out-of-Band, No Input) .....	14
Figure 33.FFT (192 kHz, -60 dB Wideband) .....	14
Figure 34.FFT (IMD 192 kHz) .....	14
Figure 35.192 kHz, THD+N vs. Input Freq .....	14
Figure 36.192 kHz, THD+N vs. Level .....	14
Figure 37.192 kHz, Fade-to-Noise Linearity .....	15
Figure 38.192 kHz, Frequency Response .....	15
Figure 39.192 kHz, Crosstalk .....	15
Figure 40.192 kHz, Impulse Response .....	15

---

Figure 41. 192 kHz, Impulse Prefilter .....	15
Figure 42. Dynamic Range 192 kHz .....	16
Figure 43. System Block Diagram and Signal Flow .....	17
Figure 44. CS4362A .....	18
Figure 45. Analog Outputs A1 - B1 .....	19
Figure 46. Analog Outputs A2 - B2 .....	20
Figure 47. Analog Outputs A3 - B3 .....	21
Figure 48. CS8416 S/PDIF Input .....	22
Figure 49. PCM Input Header and Multiplexing .....	23
Figure 50. DSD Input Header .....	24
Figure 51. Control Input .....	25
Figure 52. Power Input .....	26
Figure 53. Silkscreen Top .....	27
Figure 54. Top Side .....	28
Figure 55. Bottom Side .....	29

## LIST OF TABLES

Table 1. System Connections .....	5
Table 2. CDB4362A Jumper Settings .....	6

---

## CDB4362A SYSTEM OVERVIEW

The CDB4362A evaluation board is an excellent means of quickly evaluating the CS4362A. The CS8416 digital audio interface receiver provides an easy interface to digital audio signal sources including the majority of digital audio test equipment. The evaluation board also allows the user to supply external PCM or DSD clocks and data through PCB headers for system development.

The CDB4362A uses the CDB4385 as a base PCB board. For this reason, there may be additional circuitry on board that is not populated because it has no function for this device.

The CDB4362A schematic has been partitioned into the nine schematics shown in [Figures 44](#) through [52](#). Each partitioned schematic is represented in the system diagram shown in [Figure 43](#). Notice that the system diagram also includes the interconnections between the partitioned schematics.

### 1. CS4362A DIGITAL-TO-ANALOG CONVERTER

A description of the CS4362A is included in the CS4362A datasheet.

### 2. CS8416 DIGITAL AUDIO RECEIVER

The system receives and decodes the standard S/PDIF data format using a CS8416 digital audio receiver ([Figure 48](#)). The outputs of the CS8416 include a serial bit clock, serial data, left-right clock, and a 128/256 Fs master clock. The CS8416 data format is fixed to I<sup>2</sup>S. The operation of the CS8416 and a discussion of the digital audio interface are included in the CS8416 datasheet.

The evaluation board has been designed such that the input can be either optical or coaxial (See [Figure 48](#)). However, both inputs cannot be driven simultaneously.

Switch position 7 of S1 sets the output MCLK-to-LRCK ratio of the CS8416. This switch should be set to 256 (closed) for inputs  $F_s \leq 96$  kHz and 128 (open) for  $F_s \geq 64$  kHz. The 8416 must be manually reset using 'HW RST' (S2) or through the software when this switch is changed.

### 3. INPUT FOR CLOCKS AND DATA

The evaluation board has been designed to allow interfacing to external systems via headers J11 and J7. Header J11 allows the evaluation board to accept externally generated PCM clocks and data. The schematic for the clock/data input is shown in [Figure 49](#). Switch position 6 of S1 selects the source as either CS8416 (open) or header J11 (closed).

Header J7 allows the evaluation board to accept externally generated DSD data and clocks. The schematic for the clock/data input is shown in [Figure 50](#). A synchronous MCLK must still be provided via Header J11. Switch position 8 of S1 selects either PCM (open) or DSD (closed).

Please see the CS4362A datasheet for more information.

## 4. INPUT FOR CONTROL DATA

The evaluation board can be run in either a stand-alone mode or with a PC. Stand-alone mode uses the CS4362A in hardware mode and the mode pins are configured using switch positions 1 through 5 of S1. PC mode uses software to set up the CS4362A through I<sup>2</sup>C® using the PC's serial or USB ports. PC mode is automatically selected when the serial or USB port is attached and the CDB4362A software is running.

Header J15 offers the option for external input of RST and SPI<sup>TM</sup>/I<sup>2</sup>C clocks and data. The board is set up at the factory to use the on-board microcontroller in conjunction with the supplied software. To use an external control source, remove the shunts on J15 and place a ribbon cable so the signal lines are on the center row and the grounds are on the right side. R116 and R119 should be populated with 2-kΩ resistors when using an external I<sup>2</sup>C source that does not already provide pull-ups.

## 5. POWER SUPPLY CIRCUITRY

Power is supplied to the evaluation board by four binding posts (GND, +5V, +12V, and -12V), see [Figure 53](#). The '+5V' terminal supplies VA and the rest of the +5-V circuitry on the board. The +3.3-V circuitry is powered from a regulator. The +2.5 volts required for VD is also provided from an on-board regulator. The +5-V supply should be set within the recommended values for VA stated in the CS4362A datasheet.

**WARNING:** Refer to the CS4362A datasheet for maximum allowable voltage levels. Operation outside this range can cause permanent damage to the device.

## 6. GROUNDING AND POWER SUPPLY DECOUPLING

As with any high-performance converter, the CS4362A requires careful attention to power supply and grounding arrangements to optimize performance. [Figure 44](#) details the connections to the CS4362A and [Figures 53, 54, and 55](#) show the component placement and top and bottom layout. The decoupling capacitors are located as close to the CS4362A as possible. Extensive use of ground-plane fill in the evaluation board yields large reductions in radiated noise.

## 7. ANALOG OUTPUT FILTERING

The analog output on the CDB4362A has been designed according to the CS4362A datasheet. This output circuit includes an active 2-pole, 50-kHz filter which uses the multiple-feedback topology.

CONNECTOR	INPUT/OUTPUT	SIGNAL PRESENT
+5V	Input	+ 5 V power
GND	Input	Ground connection from power supply
+12V	Input	+12 V positive supply for the on-board filtering
-12V	Input	-12 V negative supply for the on-board filtering
S/PDIF IN - J9	Input	Digital audio interface input via coax
S/PDIF IN - OPT1	Input	Digital audio interface input via optical
PCM INPUT - J11	Input	Input for master, serial, left/right clocks and serial data
DSD INPUT - J7	Input	Input for DSD serial clock and DSD data
OUTA1-B3	Output	RCA line level analog outputs

**Table 1. System Connections**

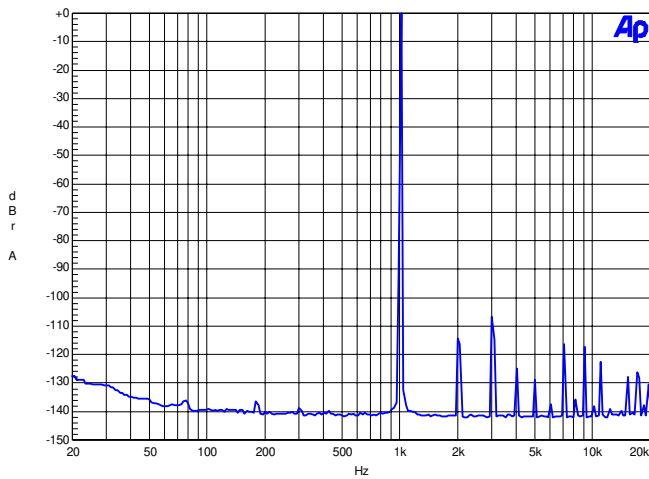
<b>JUMPER / SWITCH</b>	<b>PURPOSE</b>	<b>POSITION</b>	<b>FUNCTION SELECTED</b>
J15	Selects source of control data	*shunts on Left shunts removed	*Control from PC and on-board microcontroller External control input using center and right columns
J16	JTAG micro programming	-	Reserved for factory use only
S2	Resets CS8416 and CS4362A		The CS8416 must be reset if switch S1 is changed
S1	CS4362A mode settings M0-M4	1-5	Default: M0, M4 open (HI) M1, M2, M3 closed (LO)
	Sets clock source	6	Sets clock source for CS4362A *open = RX(CS8416), closed = $\overline{\text{EXT}}$ (J11)
	Sets MCLK ratio of CS8416	7	Selects 128x (open) or $\overline{256x}$ (*closed) MCLK/LRCK ratio output for CS8416
	Selects PCM or DSD mode	8	For PCM input set to *Open, for DSD set to Closed
*Default Factory Settings			

**Table 2. CDB4362A Jumper Settings**

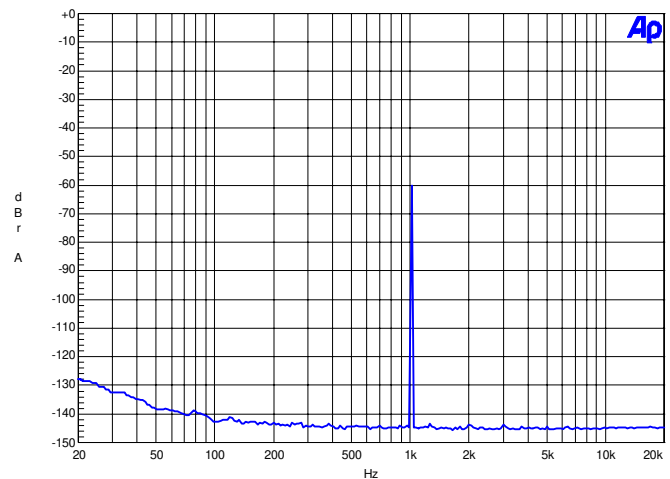
## 8. PERFORMANCE PLOTS

The plots in the following section were achieved using an Audio Precision System 2700 and a randomly chosen production CDB4362A. In some cases the performance may be limited by the CDB4362A. All measurements were taken at room temp using the standard AP filter options (20 Hz to 22 kHz) with default board settings and nominal datasheet voltages applied unless otherwise noted.

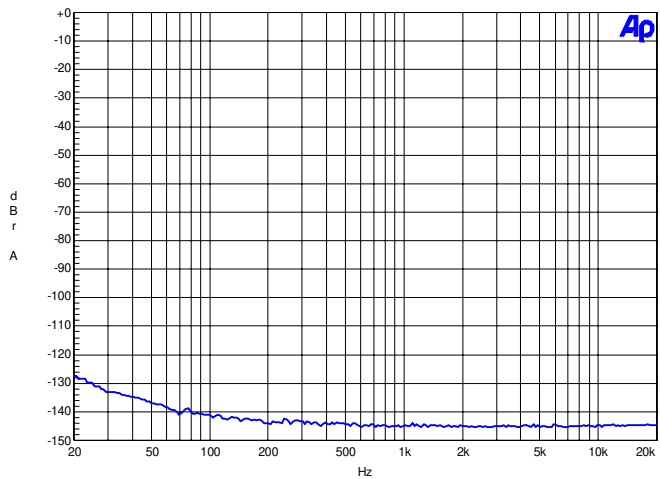
The impulse response plots were taken both pre-and post filtering as the off-chip filter was degrading the performance at higher sample rates. The pre-filter impulse response plots were taken directly at the output pins of the DAC (with the analog filter still connected) to show the effect of the CDB's analog filtering on the impulse response (as the analog filtering adds its own signature to the impulse response of the DAC, and in the case of the higher sampling rates it was band-limiting it).



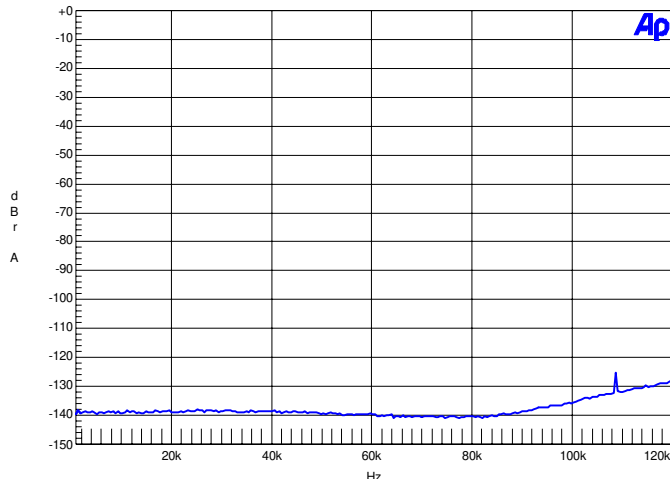
**Figure 1. FFT (48 kHz, 0 dB)**



**Figure 2. FFT (48 kHz, -60 dB)**



**Figure 3. FFT (48 kHz, No Input)**



**Figure 4. FFT (48 kHz Out-of-Band, No Input)**

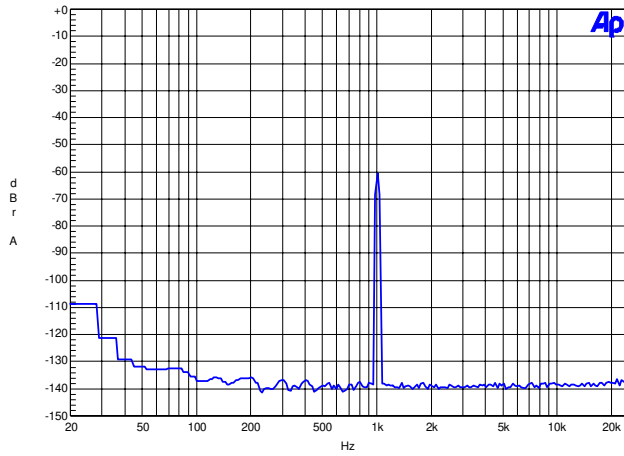


Figure 5. FFT (48 kHz -60 dB Wideband)

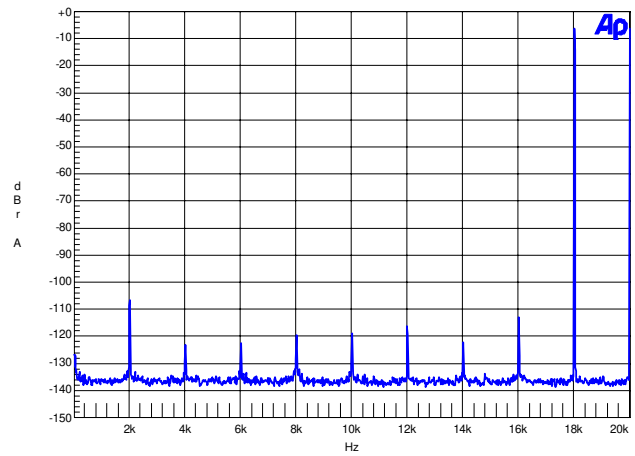


Figure 6. FFT (IMD 48 kHz)

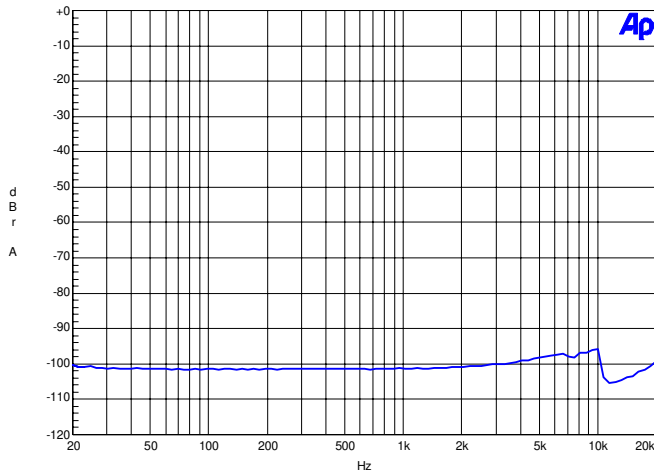


Figure 7. 48 kHz, THD+N vs. Input Freq

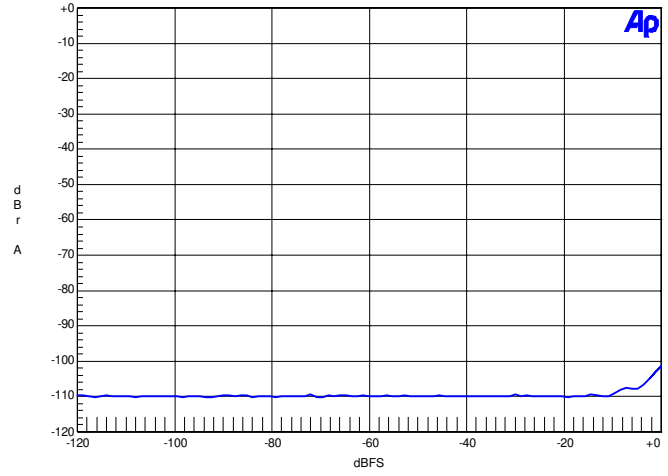


Figure 8. 48 kHz, THD+N vs. Level

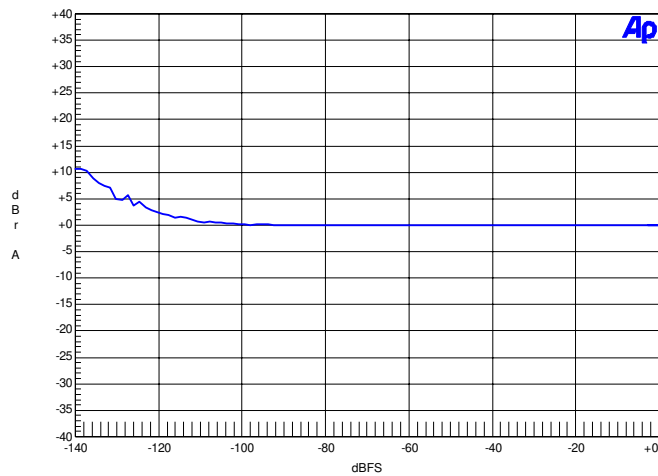


Figure 9. 48 kHz, Fade-to-Noise Linearity

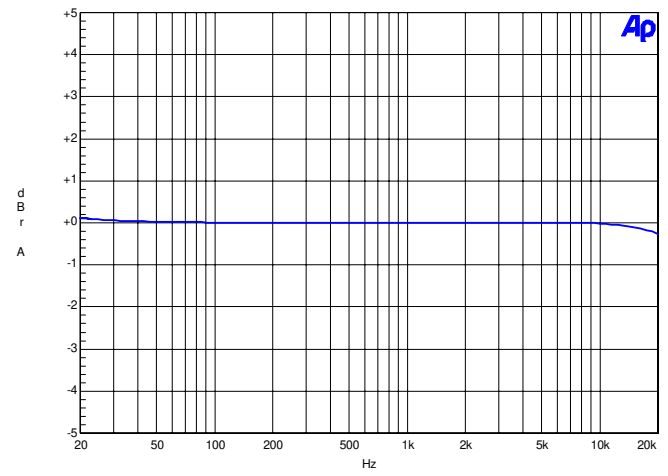


Figure 10. 48 kHz, Frequency Response



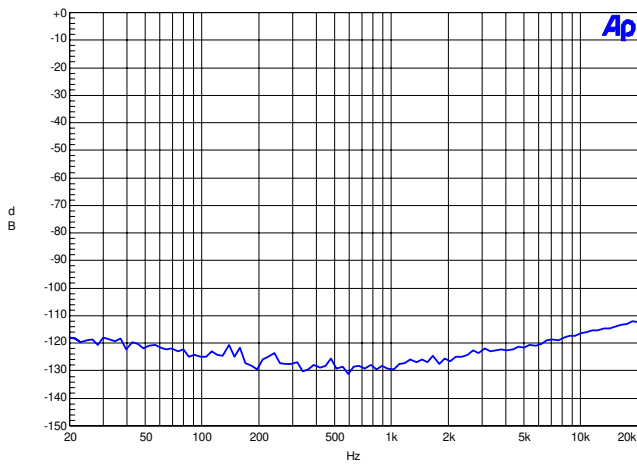


Figure 11. 48 kHz, Crosstalk

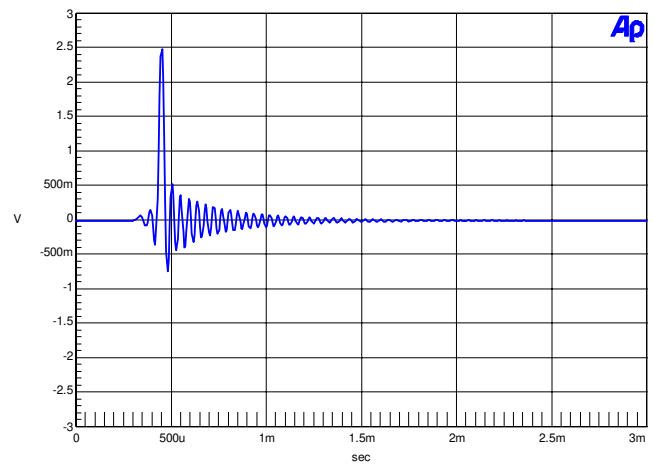


Figure 12. 48 kHz, Impulse Response

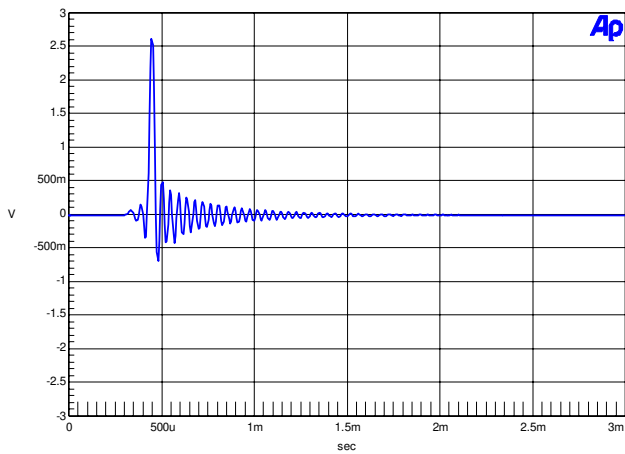
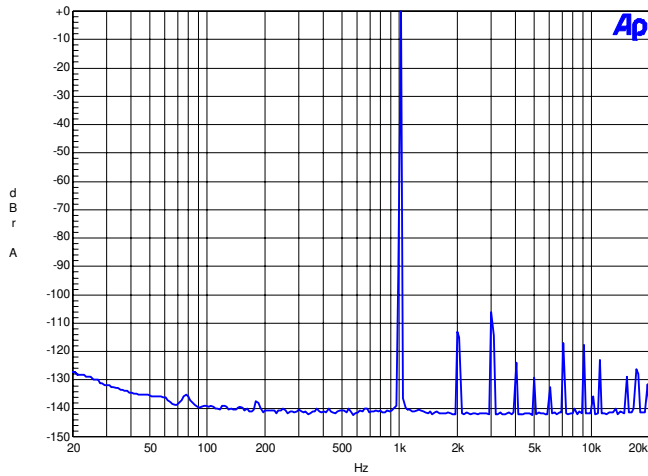
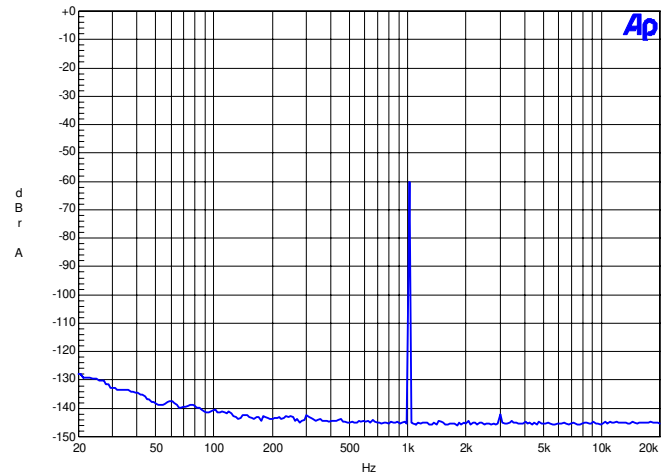
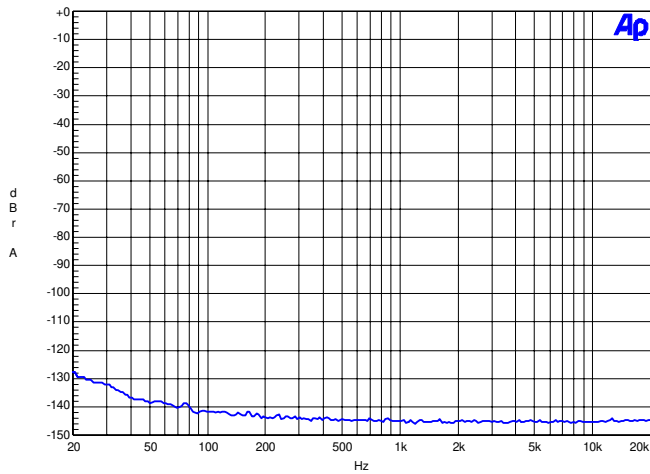
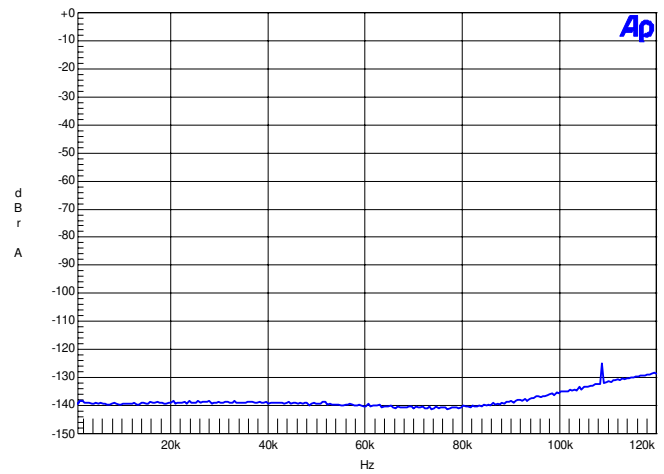
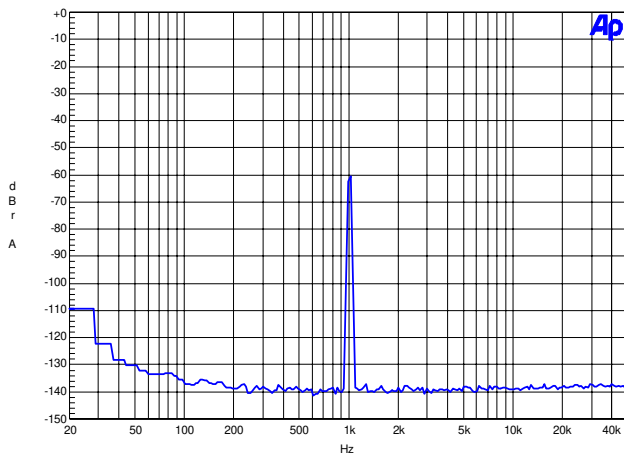
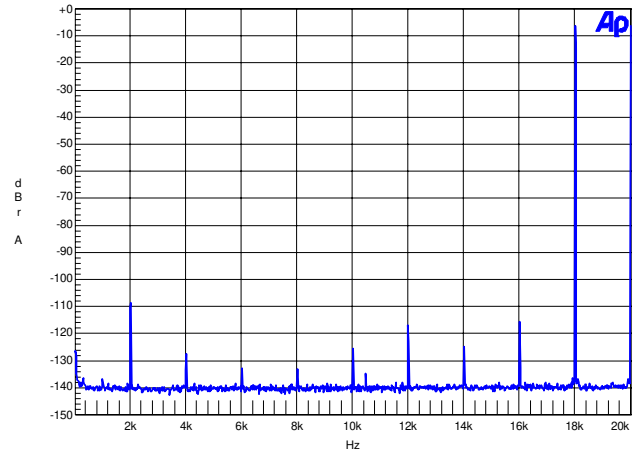
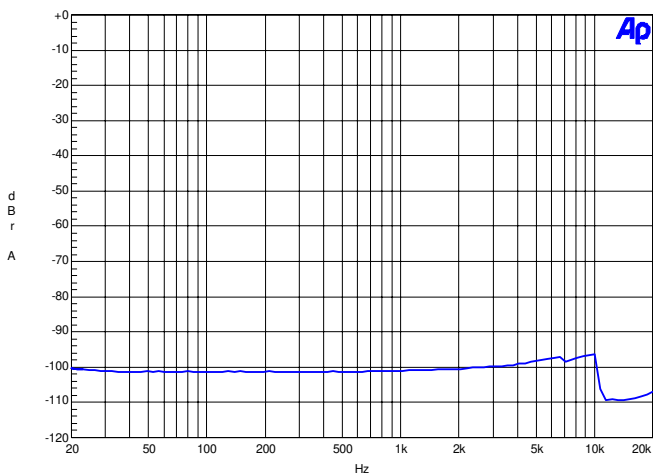
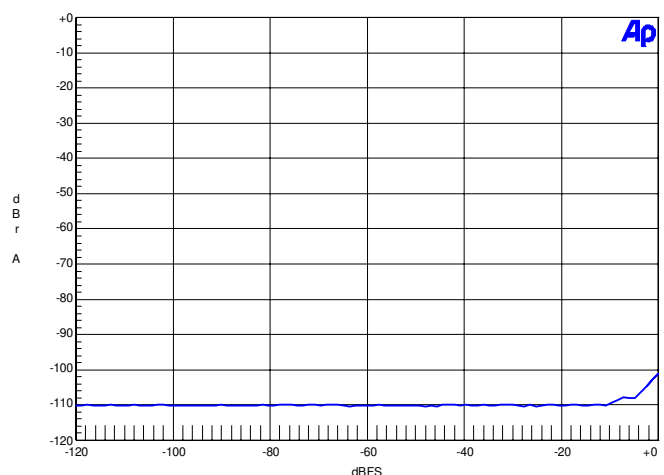


Figure 13. 48 kHz, Impulse Prefilter


**Figure 14. Dynamic Range 48 kHz**

**Figure 15. FFT (96 kHz, 0 dB)**

**Figure 16. FFT (96 kHz, -60 dB)**


**Figure 17. FFT (96 kHz, No Input)**

**Figure 18. FFT (96 kHz Out-of-Band, No Input)**

**Figure 19. FFT (96 kHz, -60 dB Wideband)**

**Figure 20. FFT (IMD 96 kHz)**

**Figure 21. 96 kHz, THD+N vs. Input Freq**

**Figure 22. 96 kHz, THD+N vs. Level**

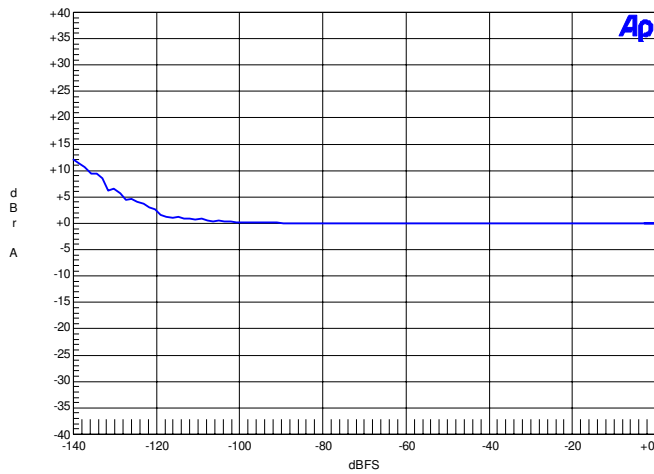


Figure 23. 96 kHz, Fade-to-Noise Linearity

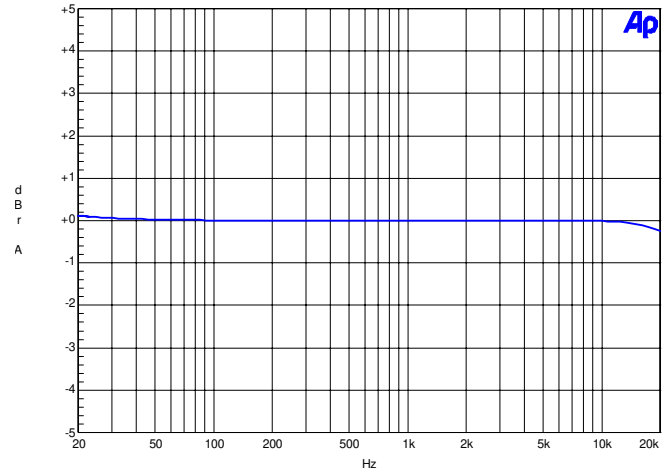


Figure 24. 96 kHz, Frequency Response

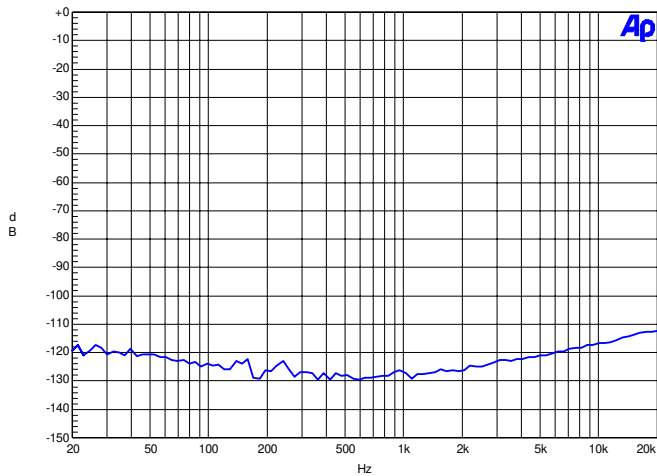


Figure 25. 96 kHz, Crosstalk

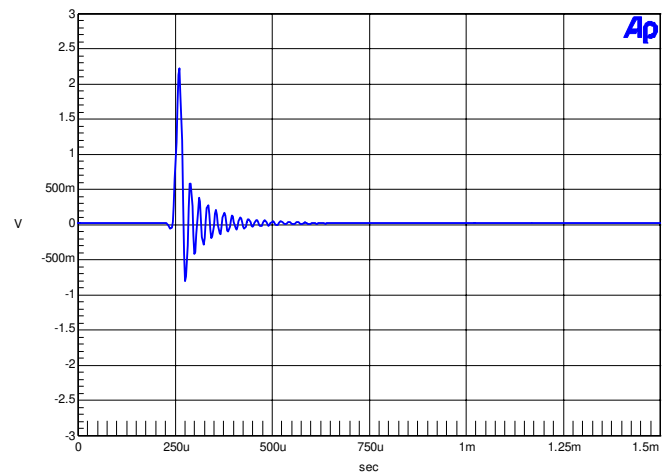


Figure 26. 96 kHz, Impulse Response

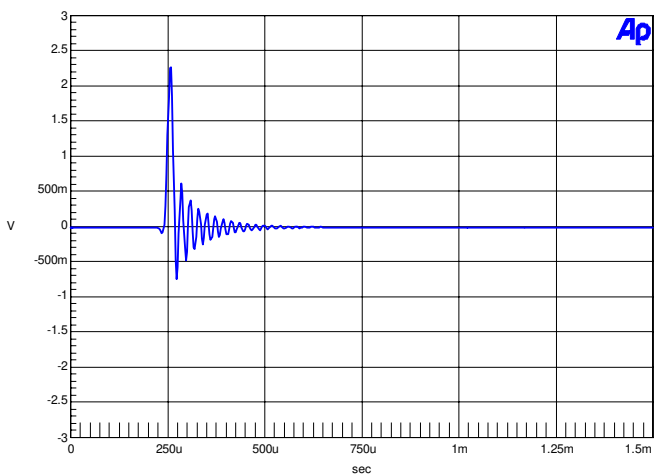
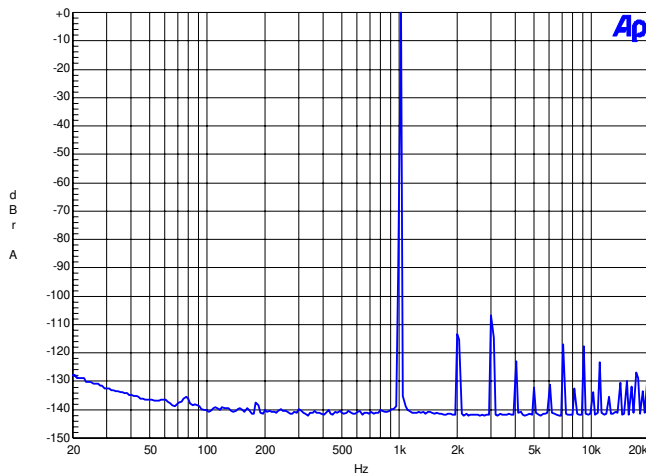
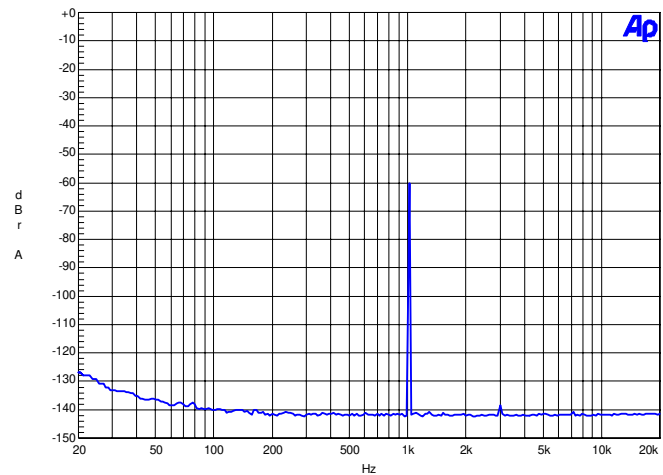
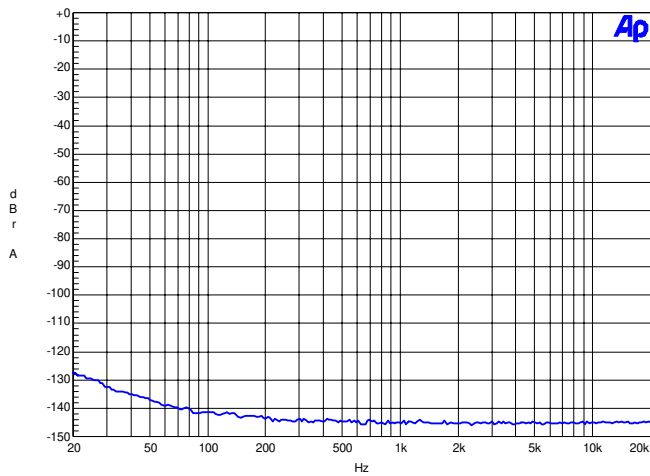
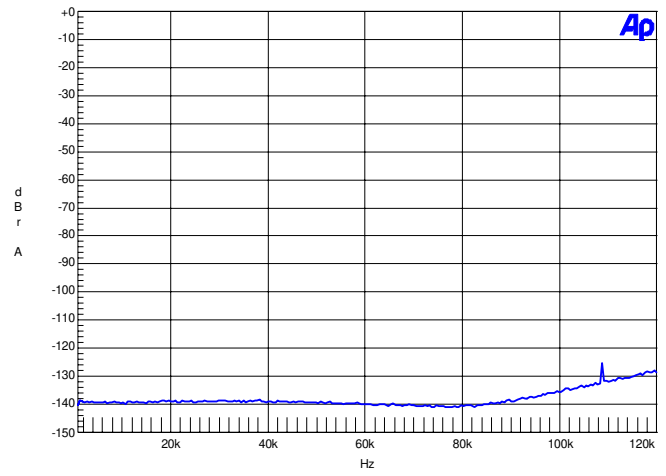
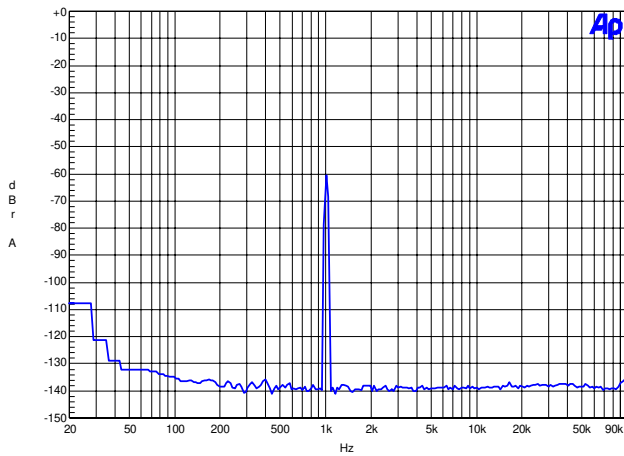
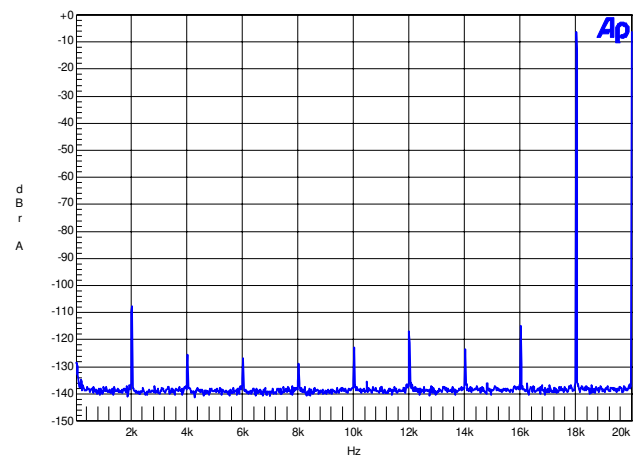
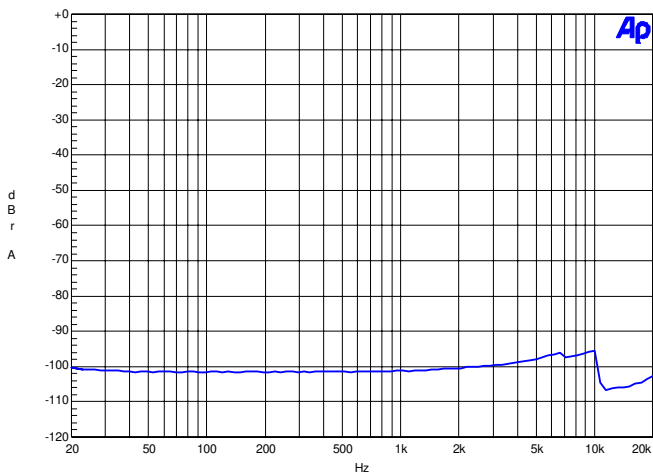
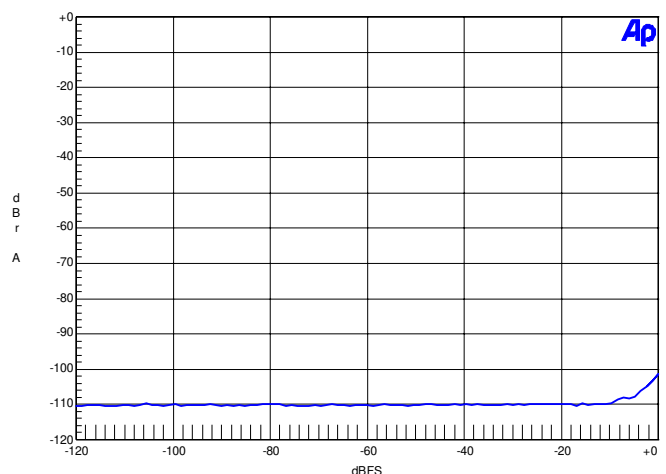
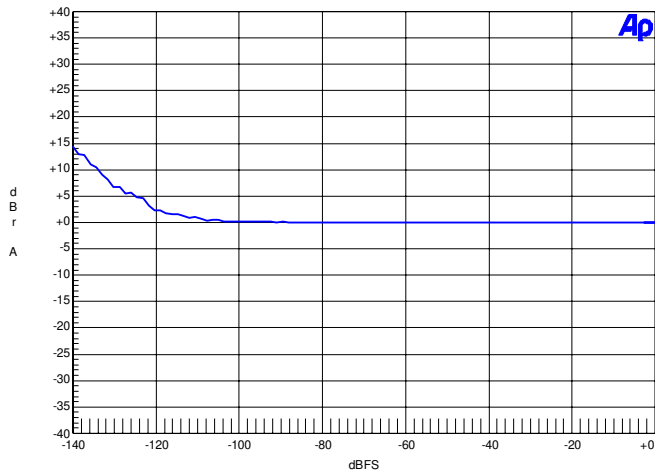
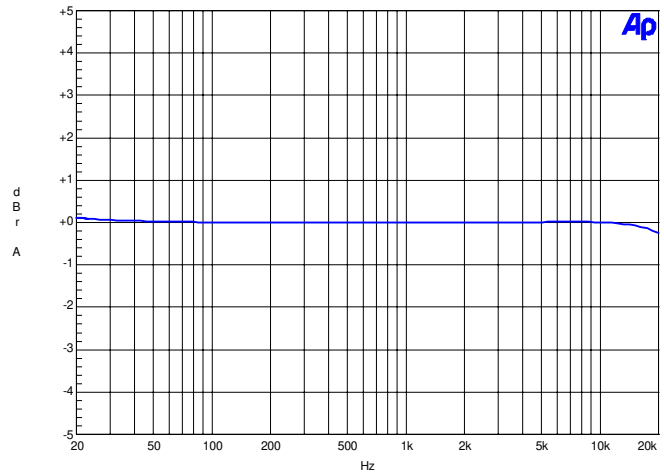
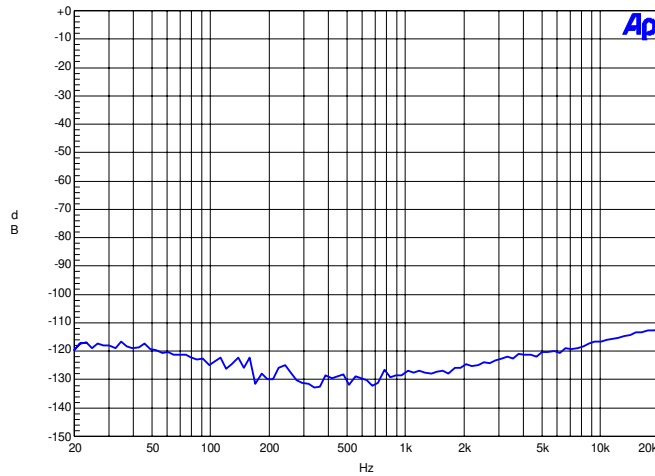
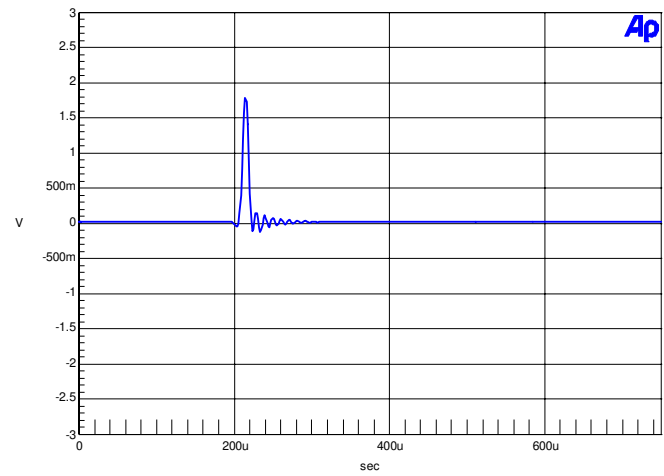
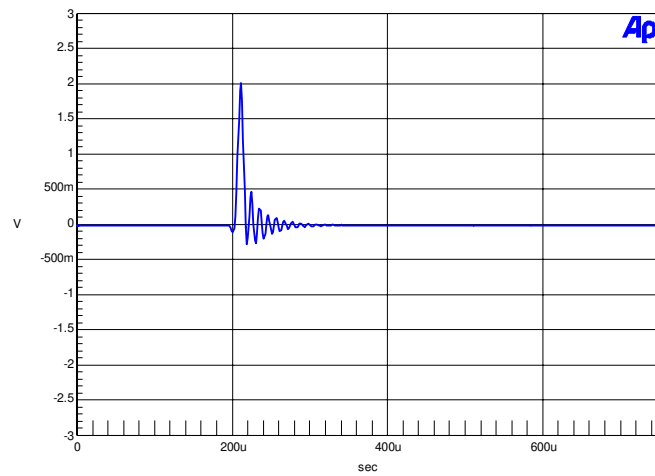
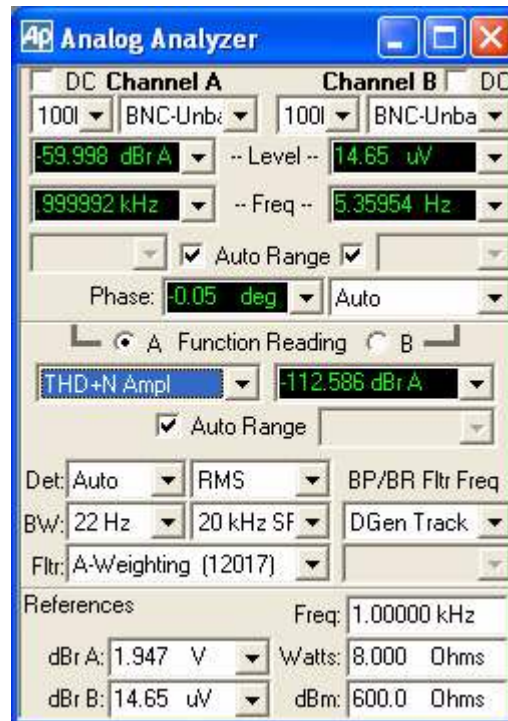


Figure 27. 96 kHz, Impulse Prefilter


**Figure 28. Dynamic Range 96 kHz**

**Figure 29. FFT (192 kHz, 0 dB)**

**Figure 30. FFT (192 kHz, -60 dB)**


**Figure 31. FFT (192 kHz, No Input)**

**Figure 32. FFT (192 kHz Out-of-Band, No Input)**

**Figure 33. FFT (192 kHz, -60 dB Wideband)**

**Figure 34. FFT (IMD 192 kHz)**

**Figure 35. 192 kHz, THD+N vs. Input Freq**

**Figure 36. 192 kHz, THD+N vs. Level**


**Figure 37. 192 kHz, Fade-to-Noise Linearity**

**Figure 38. 192 kHz, Frequency Response**

**Figure 39. 192 kHz, Crosstalk**

**Figure 40. 192 kHz, Impulse Response**

**Figure 41. 192 kHz, Impulse Prefilter**

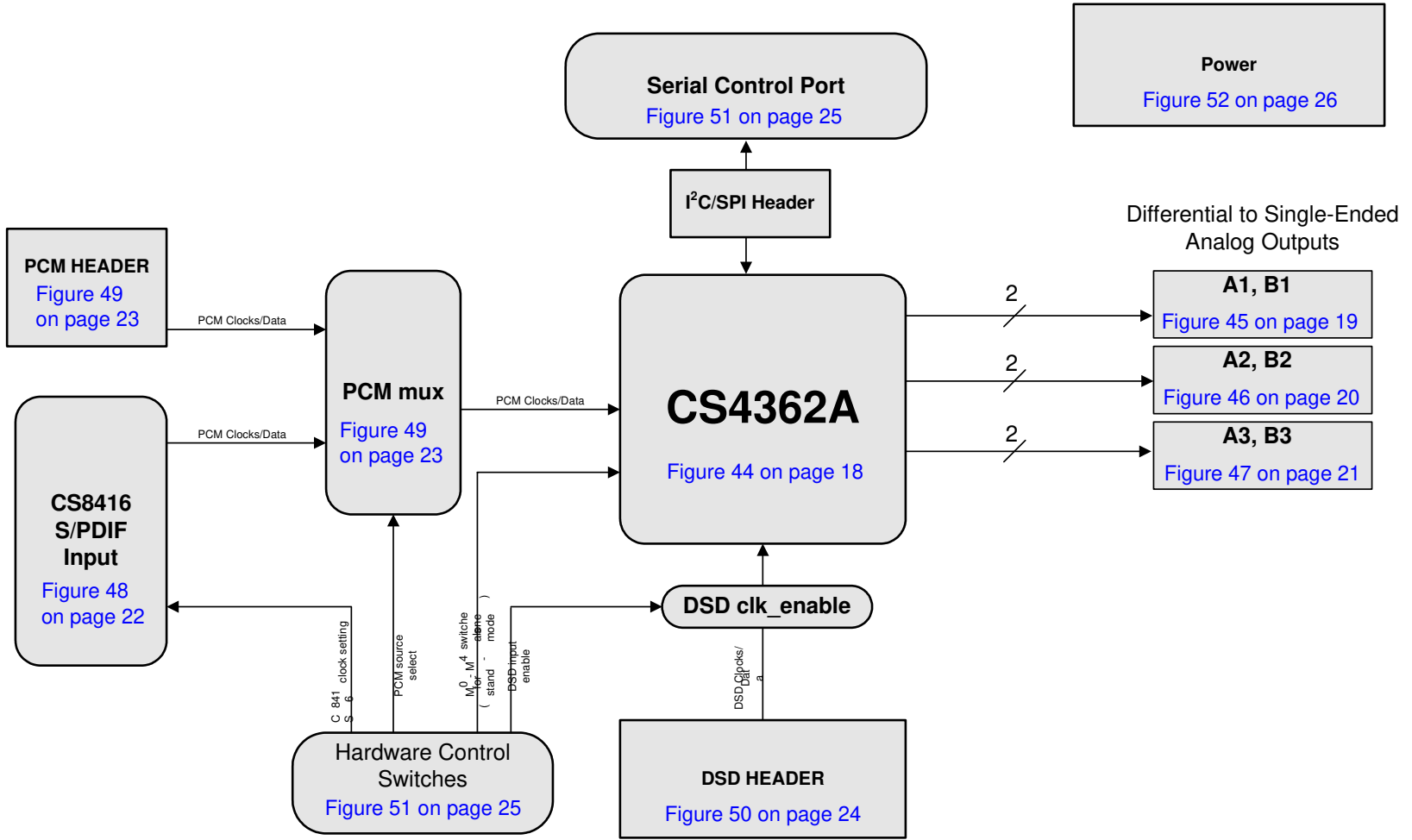


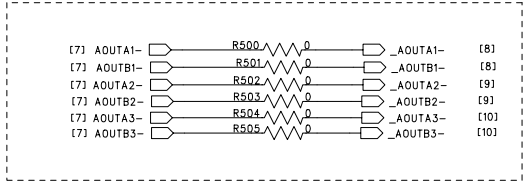
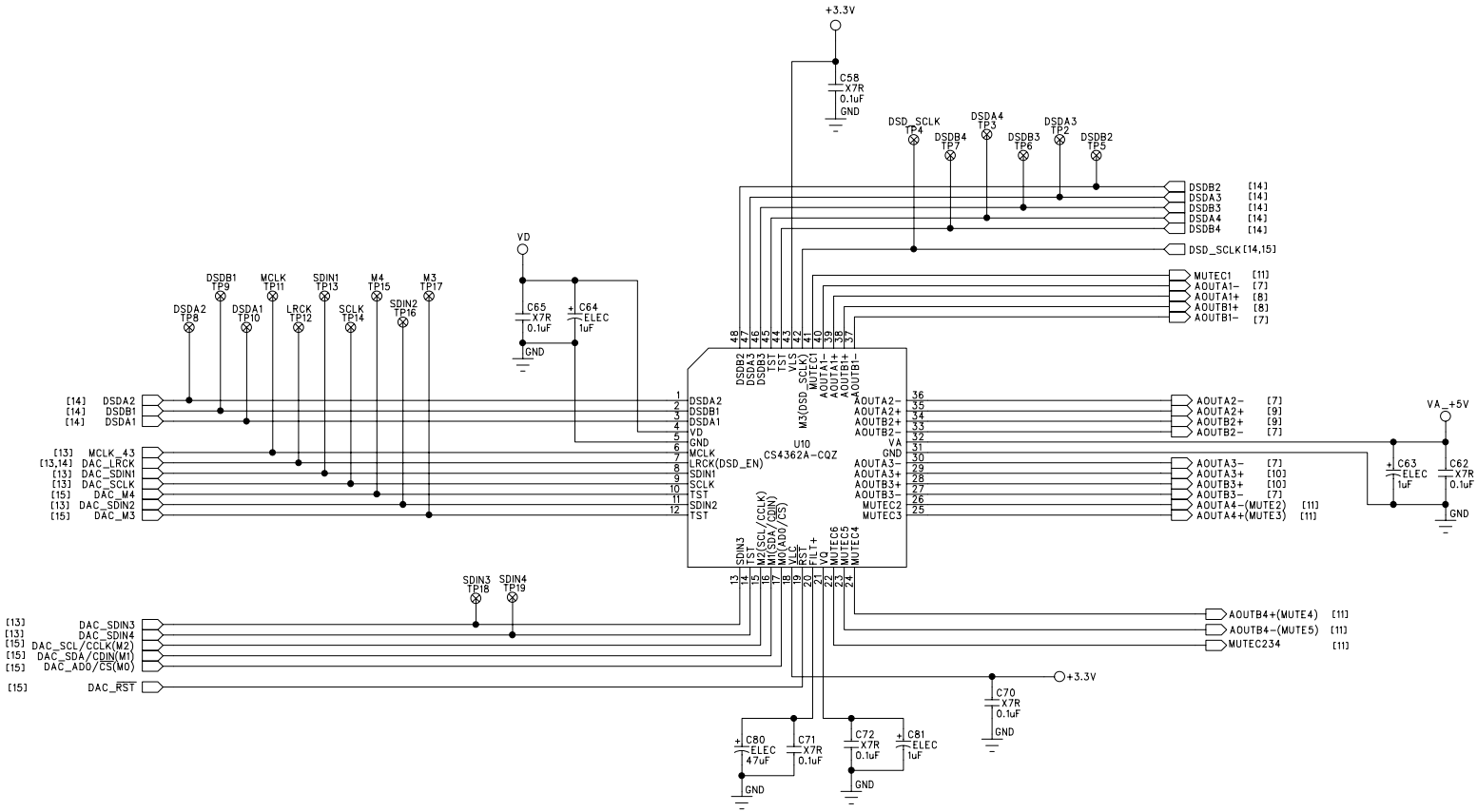
**Figure 42. Dynamic Range 192 kHz**



# 9. CDB4362A SCHEMATICS

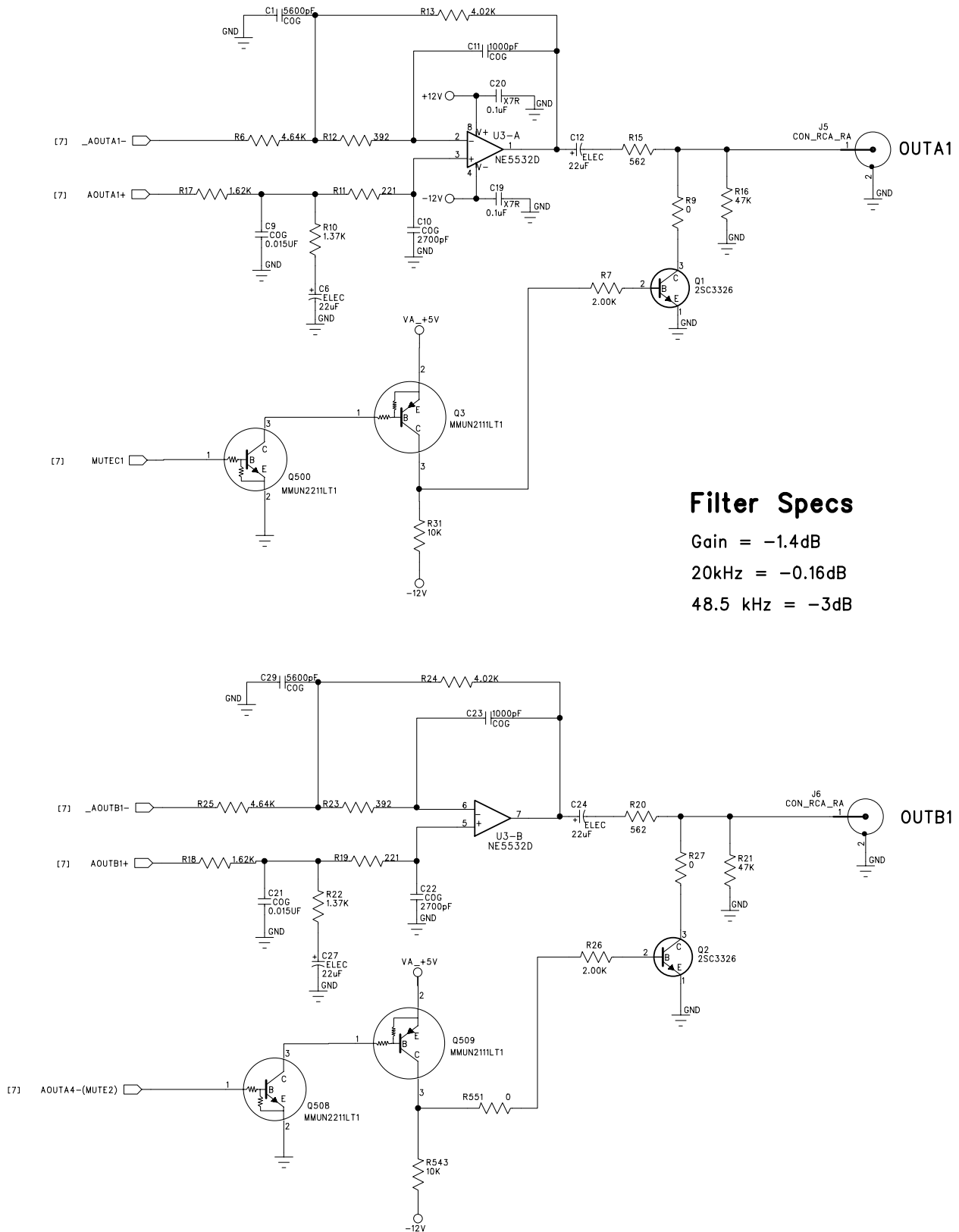
Figure 43. System Block Diagram and Signal Flow

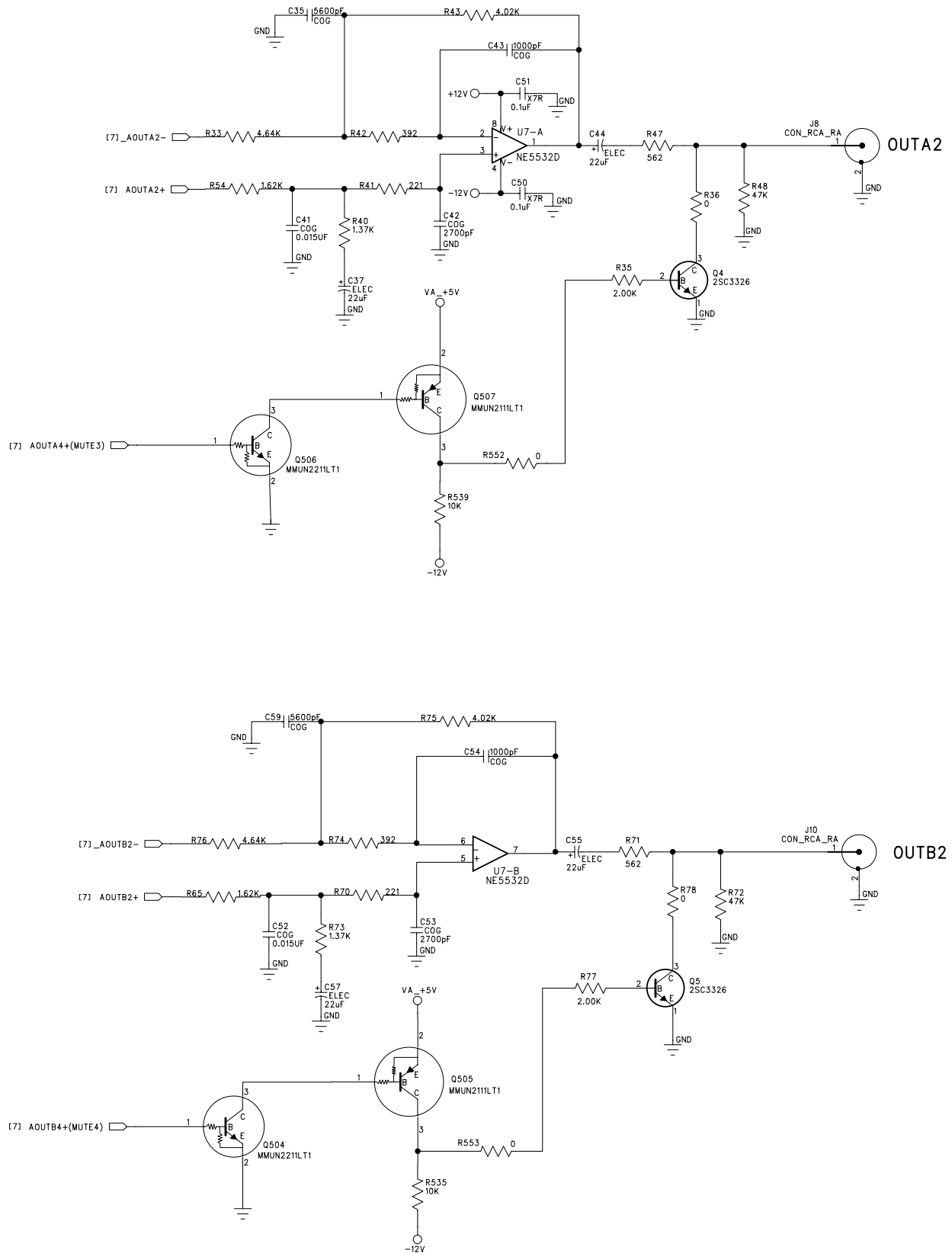


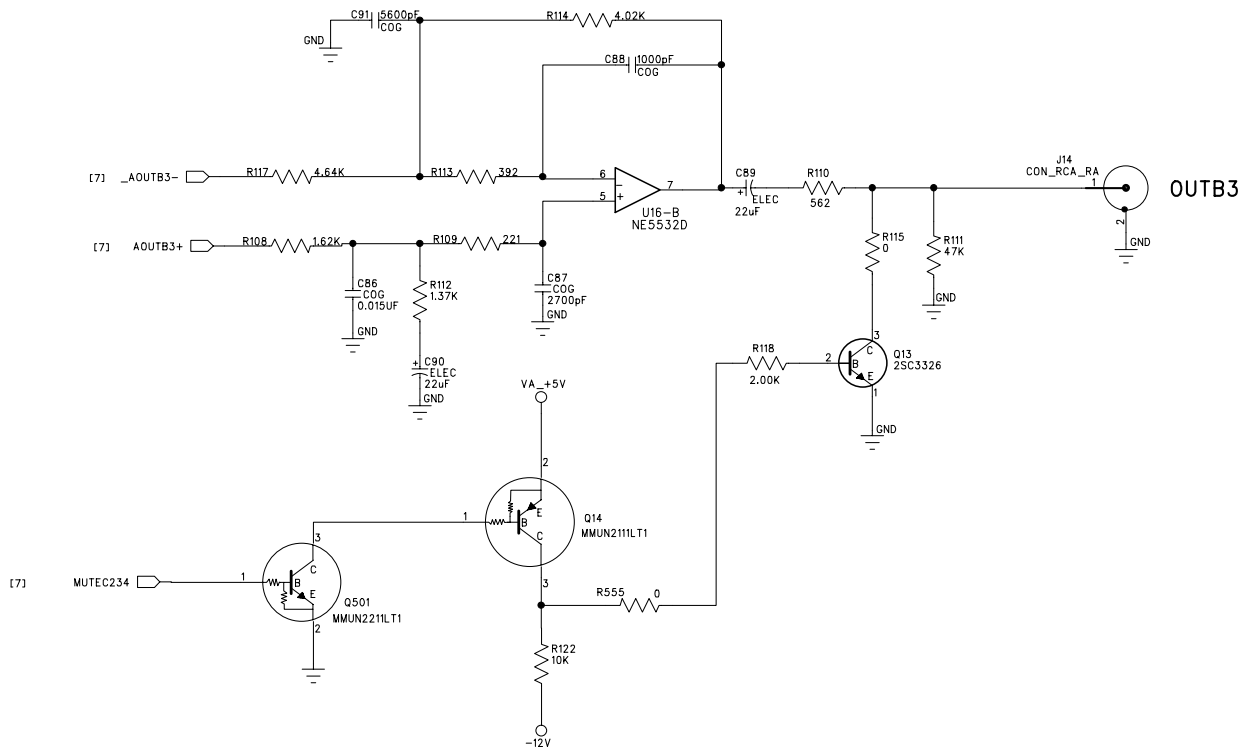
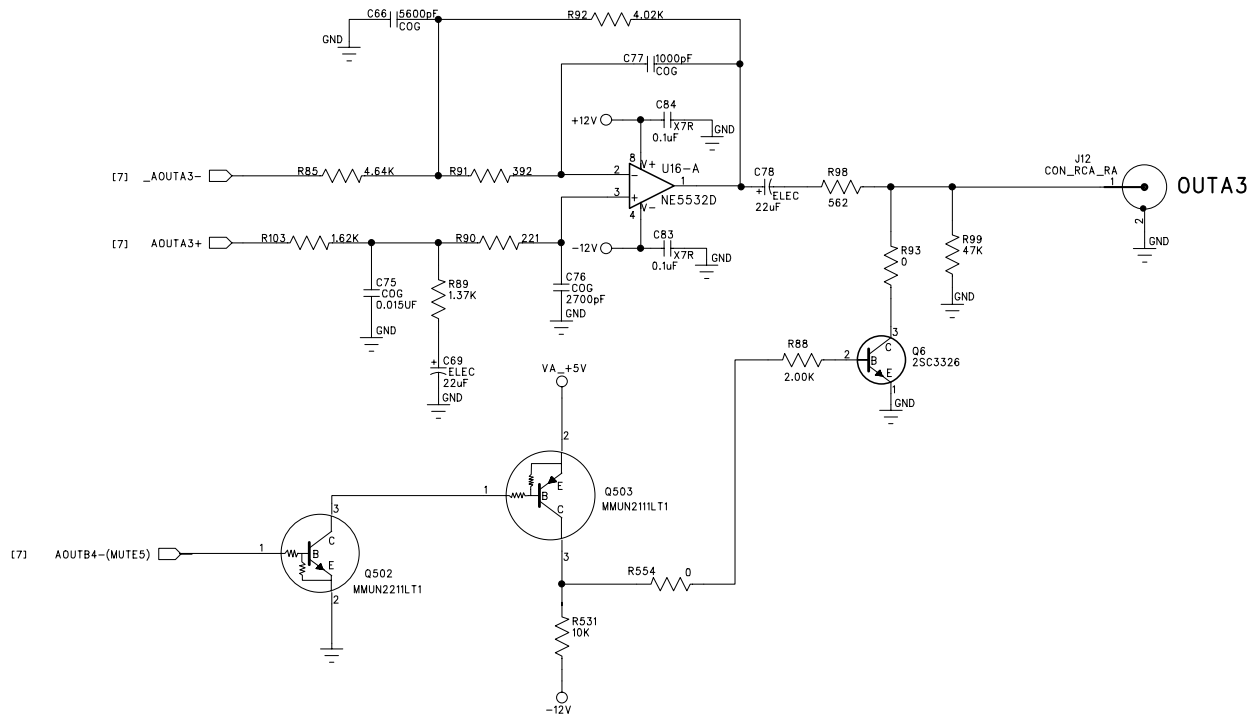


NOTE: ALL RESISTOR VALUES ARE IN OHMS UNLESS OTHERWISE SPECIFIED.

Figure 44. CS4362A


**Figure 45. Analog Outputs A1 - B1**


**Figure 46. Analog Outputs A2 - B2**


**Figure 47. Analog Outputs A3 - B3**

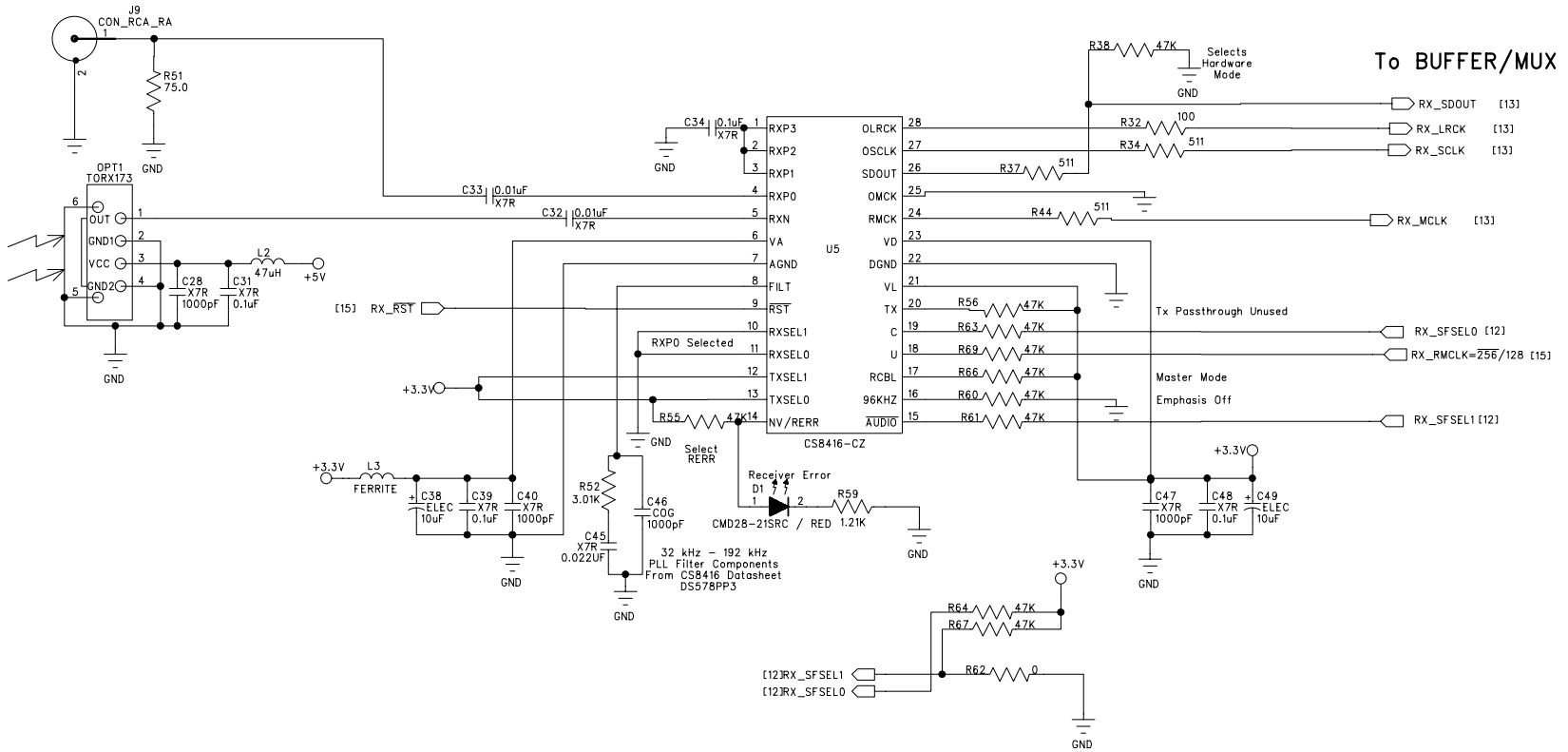


Figure 48. CS8416 S/PDIF Input

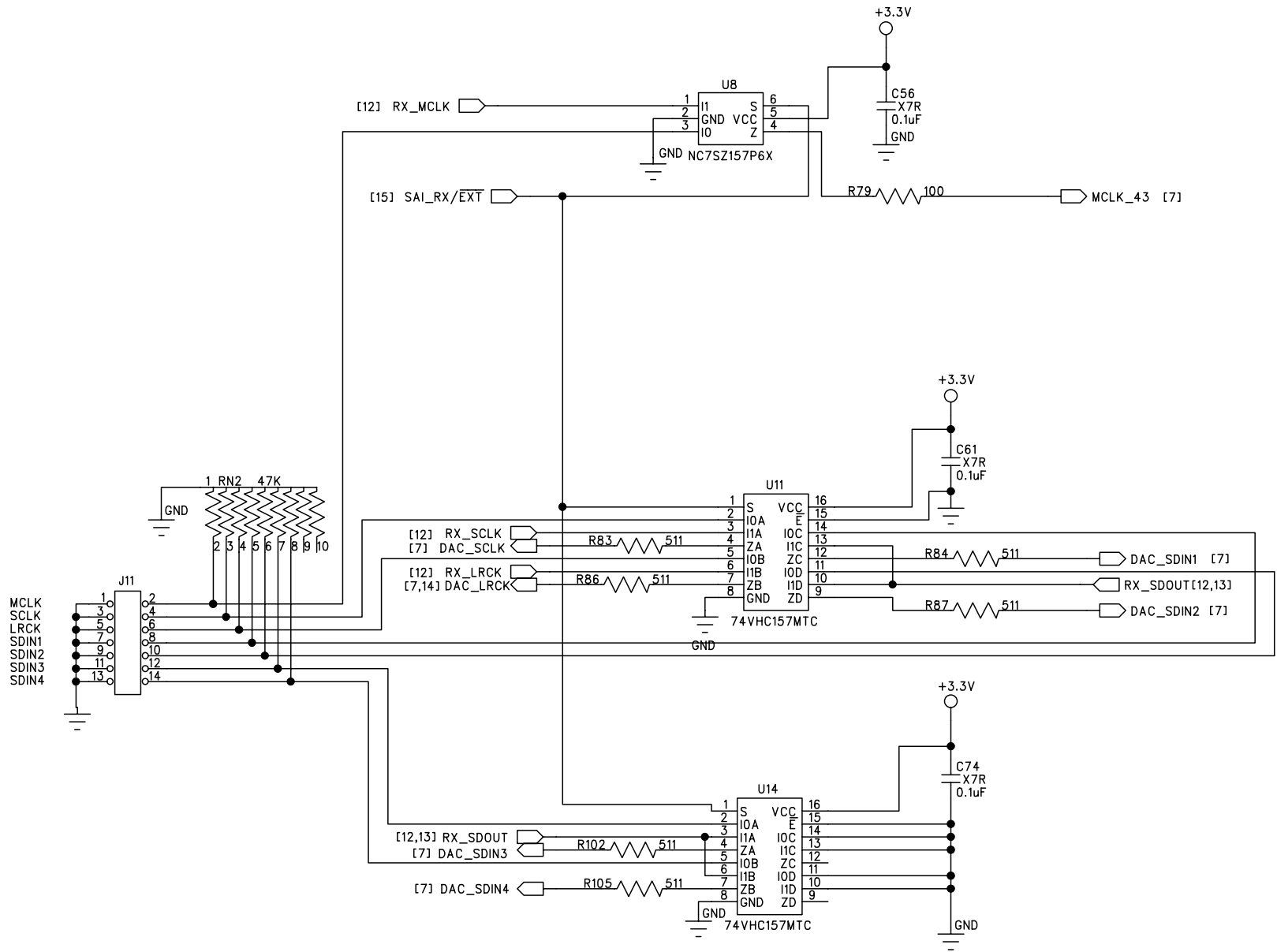


Figure 49. PCM Input Header and Multiplexing

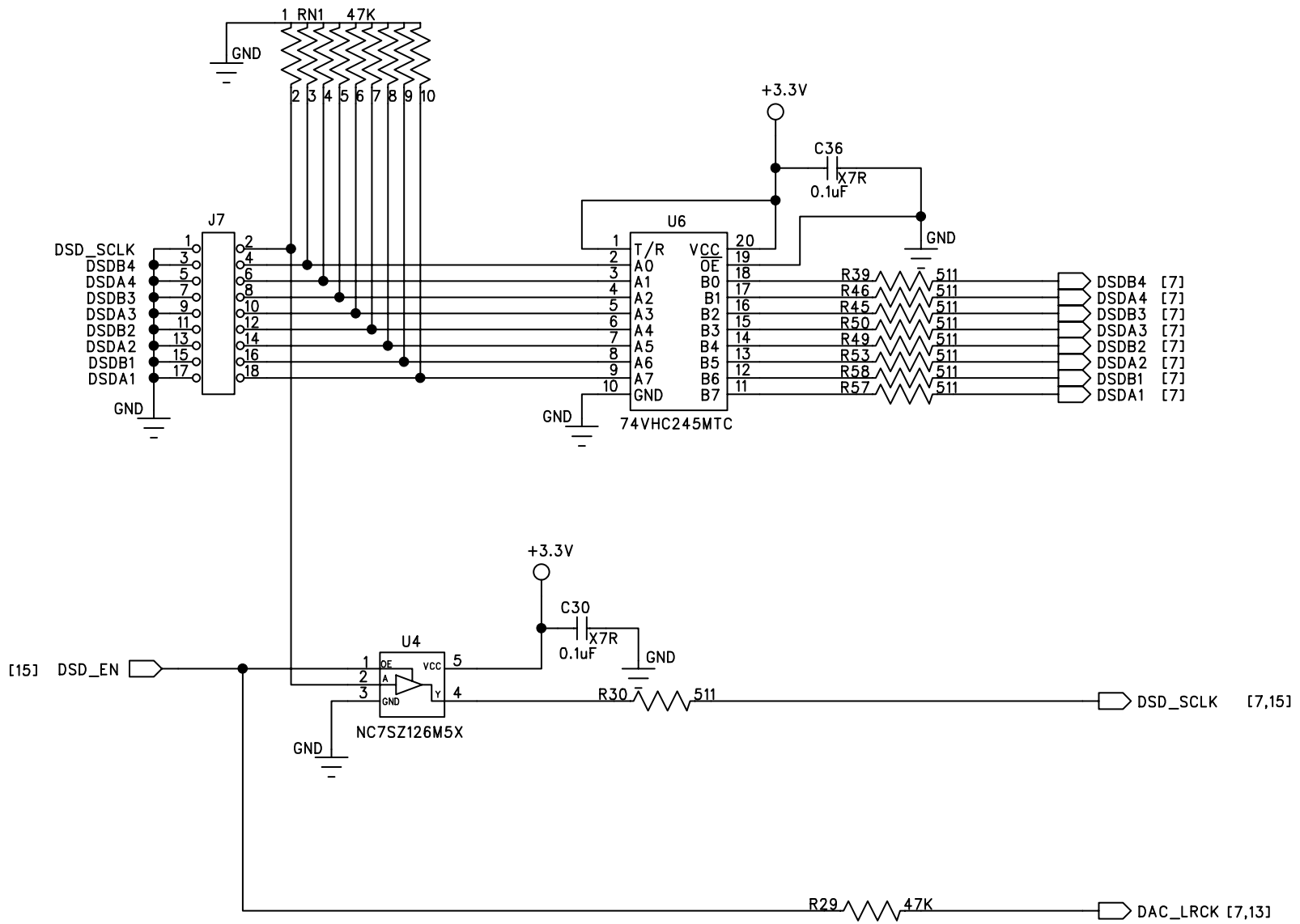


Figure 50. DSD Input Header





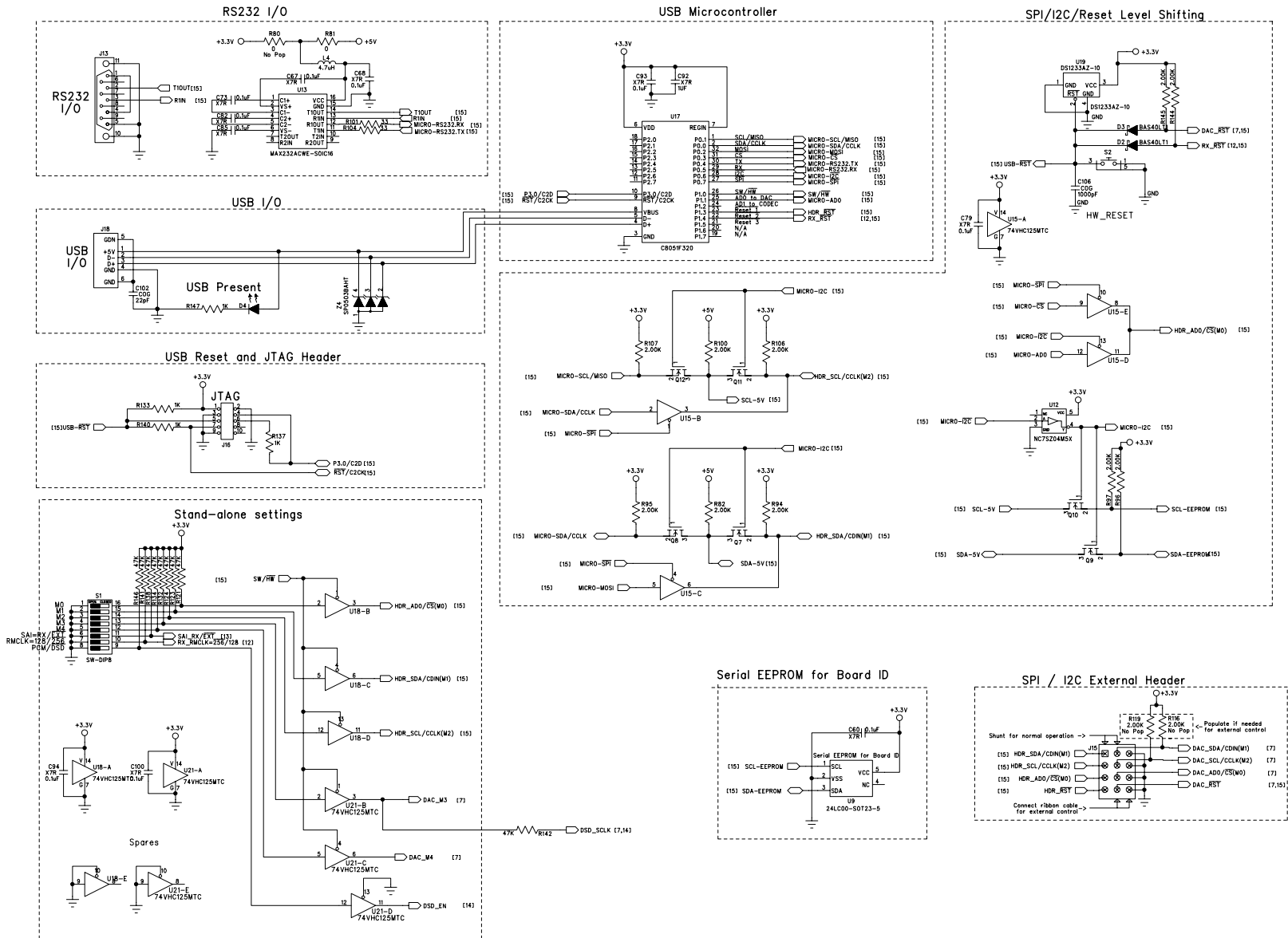


Figure 51. Control Input

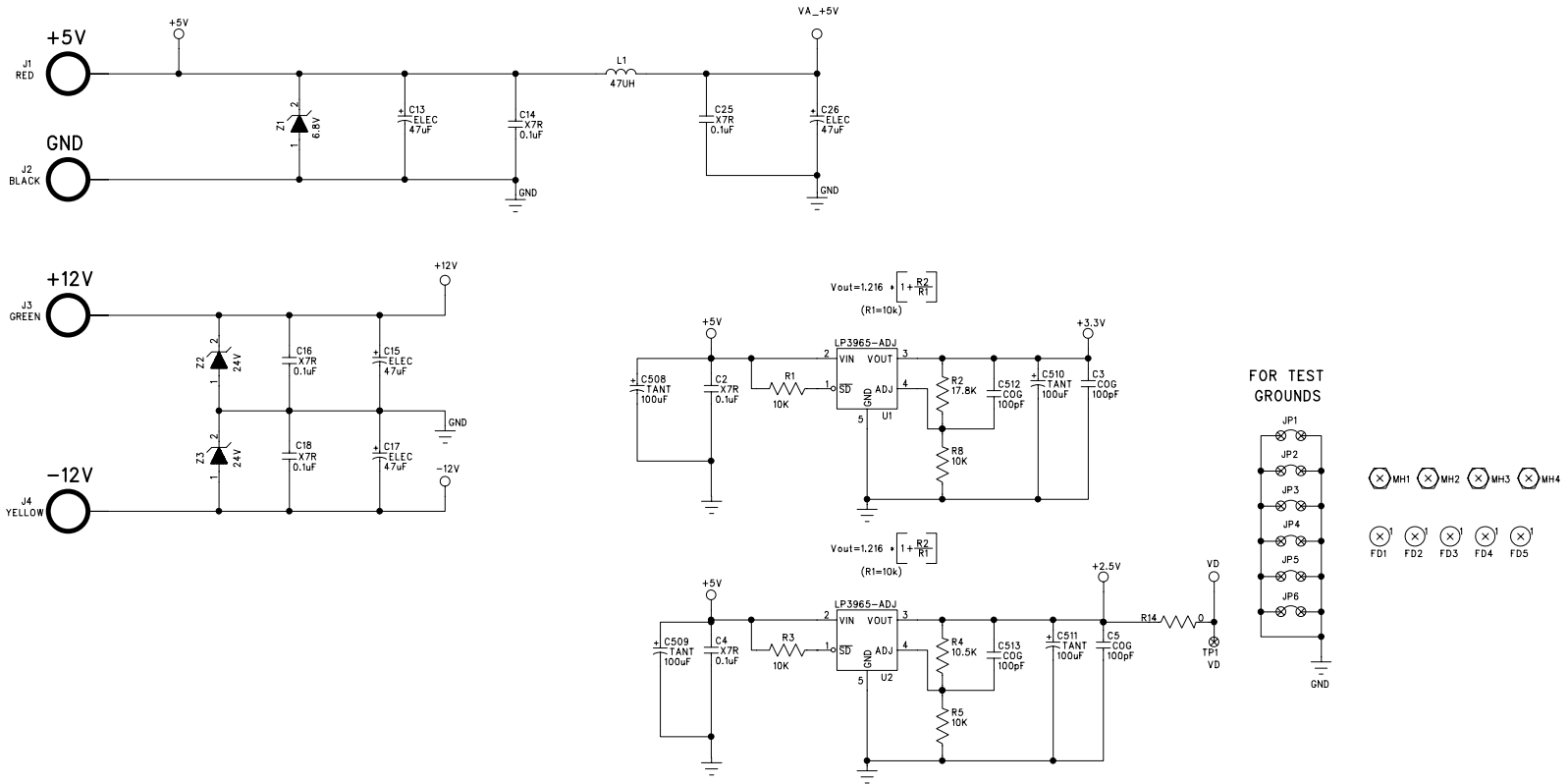
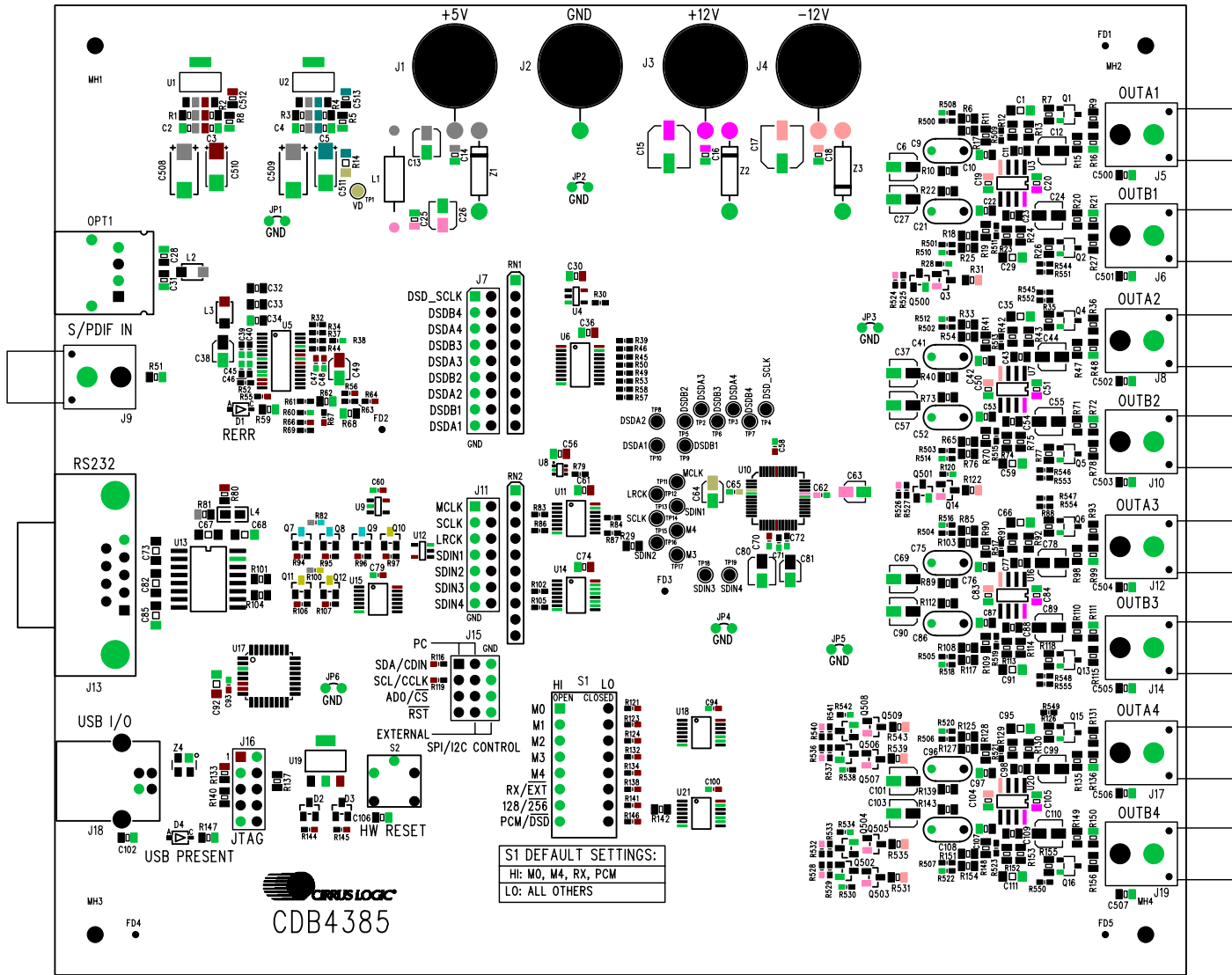


Figure 52. Power Input





CIRRUS LOGIC CDB4385 PCB 240-00123-01 Rev C

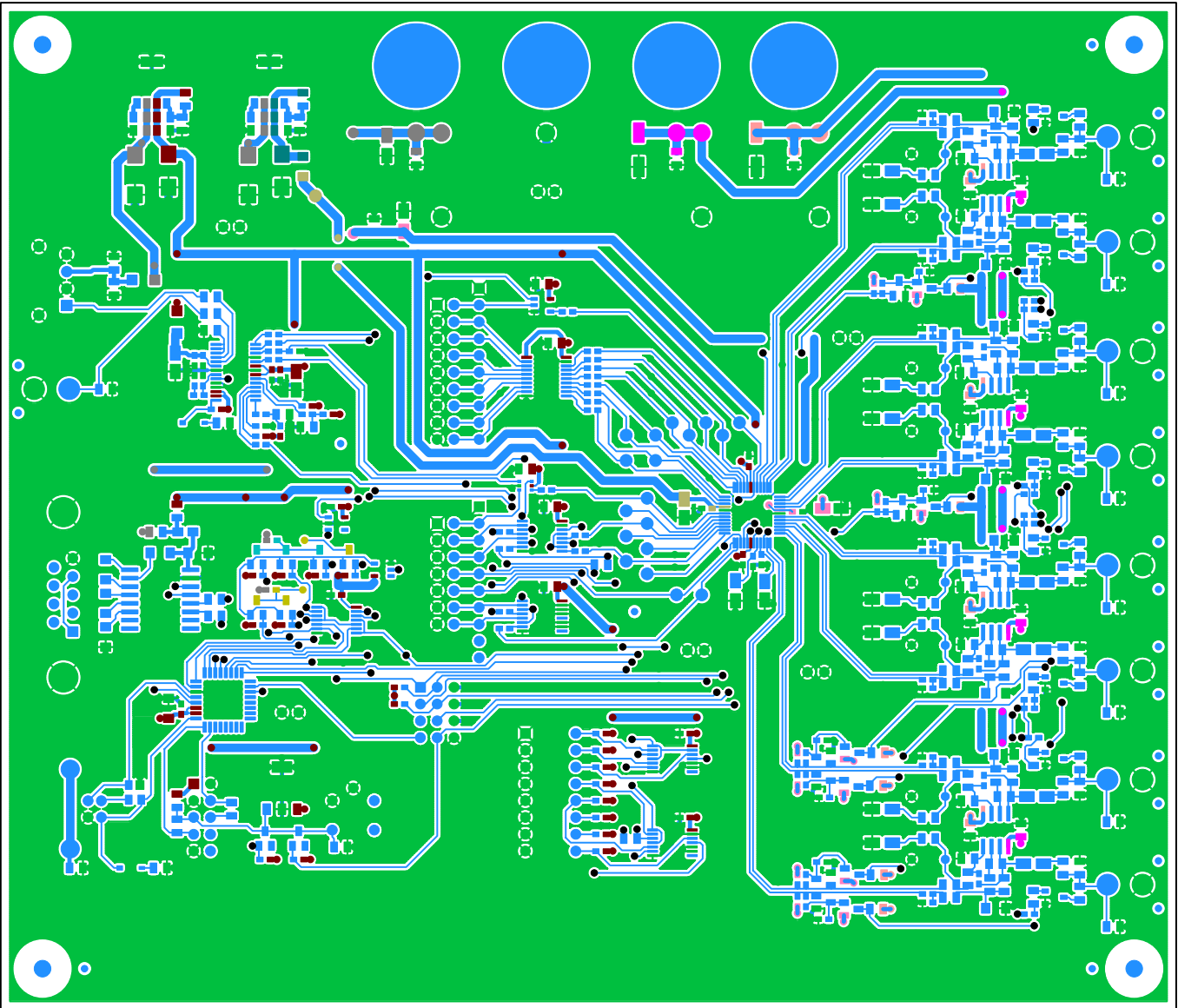
SILKSCREEN TOP

Figure 53. Silkscreen Top



CIRRUS

CDB4362A



CIRRUS LOGIC CDB4385 PCB 240-00123-01 Rev C

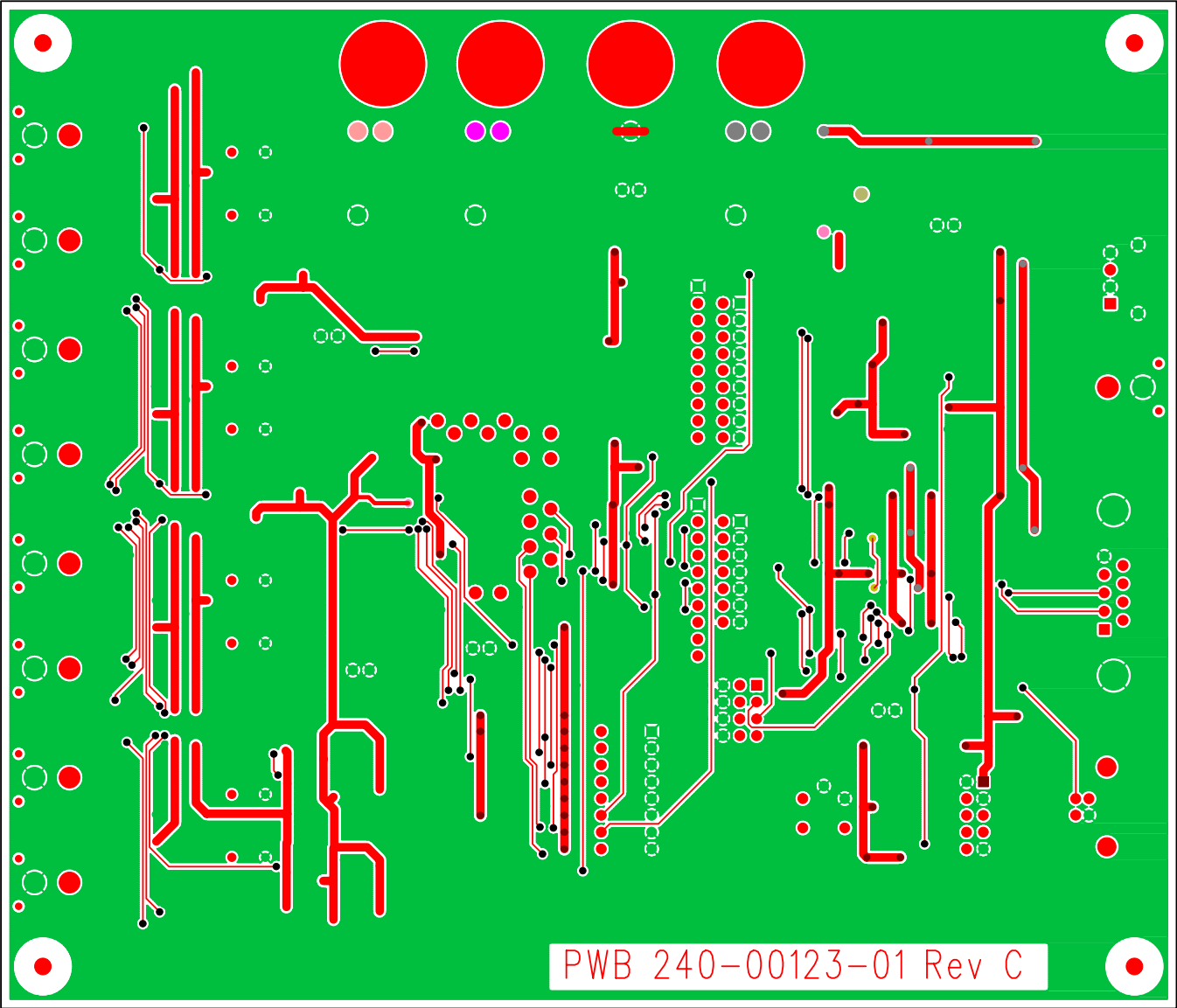
TOP SIDE

Figure 54. Top Side



CIRRUS

CDB4362A



CIRRUS LOGIC CDB4382 PCB 240-00123-01 Rev C

Figure 55. Bottom Side

---

## 10. REVISION HISTORY

Release	Changes
DB1	Initial Release
DB2	Added Performance Plots
DB3	Added USB support to <a href="#">Section 4. Input for Control Data</a>

---

### Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.

To find the one nearest to you, go to [www.cirrus.com](http://www.cirrus.com).

#### IMPORTANT NOTICE

Cirrus Logic, Inc. and its subsidiaries ("Cirrus") believe that the information contained in this document is accurate and reliable. However, the information is subject to change without notice and is provided "AS IS" without warranty of any kind (express or implied). Customers are advised to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, indemnification, and limitation of liability. No responsibility is assumed by Cirrus for the use of this information, including use of this information as the basis for manufacture or sale of any items, or for infringement of patents or other rights of third parties. This document is the property of Cirrus and by furnishing this information, Cirrus grants no license, express or implied under any patents, mask work rights, copyrights, trademarks, trade secrets or other intellectual property rights. Cirrus owns the copyrights associated with the information contained herein and gives consent for copies to be made of the information only for use within your organization with respect to Cirrus integrated circuits or other products of Cirrus. This consent does not extend to other copying such as copying for general distribution, advertising or promotional purposes, or for creating any work for resale.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). CIRRUS PRODUCTS ARE NOT DESIGNED, AUTHORIZED OR WARRANTED FOR USE IN PRODUCTS SURGICALLY IMPLANTED INTO THE BODY, AUTOMOTIVE SAFETY OR SECURITY DEVICES, LIFE SUPPORT PRODUCTS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF CIRRUS PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK AND CIRRUS DISCLAIMS AND MAKES NO WARRANTY, EXPRESS, STATUTORY OR IMPLIED, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR PARTICULAR PURPOSE, WITH REGARD TO ANY CIRRUS PRODUCT THAT IS USED IN SUCH A MANNER. IF THE CUSTOMER OR CUSTOMER'S CUSTOMER USES OR PERMITS THE USE OF CIRRUS PRODUCTS IN CRITICAL APPLICATIONS, CUSTOMER AGREES, BY SUCH USE, TO FULLY INDEMNIFY CIRRUS, ITS OFFICERS, DIRECTORS, EMPLOYEES, DISTRIBUTORS AND OTHER AGENTS FROM ANY AND ALL LIABILITY, INCLUDING ATTORNEYS' FEES AND COSTS, THAT MAY RESULT FROM OR ARISE IN CONNECTION WITH THESE USES.

Cirrus Logic, Cirrus, and the Cirrus Logic logo designs are trademarks of Cirrus Logic, Inc. All other brand and product names in this document may be trademarks or service marks of their respective owners.

DSD is a registered trademark of Sony Kabushiki Kaisha TA Sony Company.

®C is a registered trademark of Philips Semiconductor.

SPI is a trademark of Motorola, Inc.