

P-Channel 30 V (D-S) MOSFET



PRODUCT SUMMARY				
V _{DS} (V)	-30			
$R_{DS(on)}$ max. (Ω) at V_{GS} = -10 V	0.0150			
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -4.5 \text{ V}$	0.0260			
Q _g typ. (nC)	16			
I _D (A)	-13.6 °			
Configuration	Single			

FEATURES

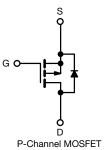
- TrenchFET® power MOSFET
- 100 % R_a and UIS tested
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>

Pb-free

ROHS COMPLIANT HALOGEN FREE

APPLICATIONS

- Notebook computers and mobile computing
- Adaptor switch / load switch
- Battery management
- Power management



ORDERING INFORMATION	
Package	SO-8
Lead (Pb)-free and halogen-free	Si4155DY-T1-GE3

PARAMETER	SYMBOL	LIMIT	UNIT		
Drain-source voltage		V _{DS}	-30	V	
Gate-source voltage		V_{GS}	± 25		
Continuous drain current (T _J = 150 °C)	T _C = 25 °C		-13.6		
	T _C = 70 °C	1 , 🗀	-10.9		
	T _A = 25 °C	I _D	-10.2 ^{a,b}		
	T _A = 70 °C		-8.2 ^{a,b}		
Pulsed drain current (t = 100 μs)		I _{DM}	-50	A	
Continuous source-drain diode current	T _C = 25 °C		3.7		
	T _A = 25 °C	l _s	-2.1 ^{a,b}		
Avalanche current	1 0411	I _{AS}	-14		
Single-pulse avalanche energy	L = 0.1 mH	E _{AS}	9.8	mJ	
Maximum power dissipation	T _C = 25 °C		4.5		
	T _C = 70 °C		2.9		
	T _A = 25 °C	P _D	2.5 ^{a,b}	W	
	T _A = 70 °C	1	1.6 ^{a,b}		
Operating junction and storage temperature range		T _J , T _{stq}	-50 to 150	°C	

Notes

- a. Surface mounted on 1" x 1" FR4 board
- b. t = 10 s
- c. $T_C = 25$ °C



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THERMAL RESISTANCE RATINGS						
PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT		
Maximum junction to ambient a,b	t ≤ 10 s	R _{thJA}	38	50	°C ///	
Maximum junction to case (drain)	Steady State	R _{thJC}	22	28	°C/W	

Notes

- a. Surface mounted on 1" x 1" FR4 board
- b. Maximum under steady state conditions is 85 °C/W

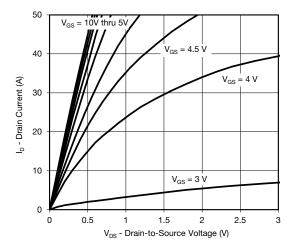
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V _{DS}	$V_{GS} = 0 \text{ V}, I_D = -250 \mu\text{A}$	-30	-	-	V
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$	J 0504	=.	-23	-	mV/°0
V _{GS(th)} temperature coefficient	$\Delta V_{GS(th)}/T_J$	- I _D = -250 μA	-	4.8	-	
Gate-source threshold voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	-1.2	-	-2.5	V
Gate-source leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 25 \text{ V}$	-	-	± 100	nA
Zara gata valtaga duain avuwant	,	$V_{DS} = -30 \text{ V}, V_{GS} = 0 \text{ V}$	-	-	-1	
Zero gate voltage drain current	I _{DSS}	V _{DS} = -30 V, V _{GS} = 0 V, T _J = 55 °C	-	-	-10	μA
Drain-source on-state resistance ^a	В	V _{GS} = -10 V, I _D = -7 A	-	0.0125	0.0150	Ω
	R _{DS(on)}	$V_{GS} = -4.5 \text{ V}, I_D = -3 \text{ A}$	-	0.0210	0.0260	
Forward transconductance ^a	9 _{fs}	$V_{DS} = -15 \text{ V}, I_D = -7 \text{ A}$	-	52	-	S
Dynamic ^b						
Input capacitance	C _{iss}	V _{DS} = -15 V, V _{GS} = 0 V, f = 1 MHz	-	1870	-	pF
Output capacitance	C _{oss}		-	245	-	
Reverse transfer capacitance	C _{rss}		-	212	-	
Tabel a standards		V _{DS} = -15 V, V _{GS} = -10 V, I _D = -12 A	-	33	50	nC
Total gate charge	Q_g		-	16	25	
Gate-source charge	Q_{gs}	$V_{DS} = -15 \text{ V}, V_{GS} = -4.5 \text{ V}, I_{D} = -12 \text{ A}$	-	5.6	-	
Gate-drain charge	Q_{gd}	1	-	5.5	-	
Gate resistance	R_{g}	f = 1 MHz	0.64	3.2	6.4	Ω
Turn-on delay time	t _{d(on)}		-	38	57	
Rise time	t _r	$V_{DD} = -15 \text{ V}, R_{L} = 1.6 \Omega$	-	34	51	
Turn-off delay time	t _{d(off)}	$I_D \cong -9.6 \text{ A}, V_{GEN} = -4.5 \text{ V}, R_g = 1 \Omega$	-	24	36	
Fall time	t _f	1	-	10	20	1
Turn-on delay time	t _{d(on)}		-	8	16	ns
Rise time	t _r	$V_{DD} = -15 \text{ V}, R_{L} = 1.6 \Omega$	-	9	18	
Turn-off delay time	t _{d(off)}	$I_D \cong -9.6 \text{ A}, V_{GEN} = -10 \text{ V}, R_g = 1 \Omega$	-	22	33	
Fall time	t _f		-	7	14	
Drain-Source Body Diode Characteris	tics					
Continuous source-drain diode current	I _S	T _C = 25 °C	-	-	-18 ^c	
Pulse diode forward current d	I _{SM}		-	-	-50	A
Body diode voltage	V _{SD}	I _F = -9.6 A	-	-0.8	-1.2	V
Body diode reverse recovery time	t _{rr}	I _F = -9.6 A, dl/dt = 100 A/μs, T _J = 25 °C	-	21	32	ns
Body diode reverse recovery charge	Q _{rr}		-	12	20	nC
Reverse recovery fall time	t _a		=	11	-	
Reverse recovery rise time	t _b	1	-	10	_	ns

Notes

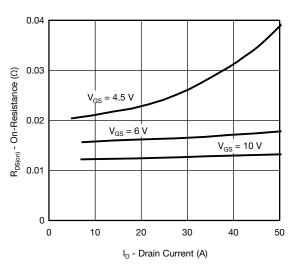
- a. Pulse test; pulse width $\leq 300~\mu s,~duty~cycle \leq 2~\%$
- b. Guaranteed by design, not subject to production testing
- c. Package limited
- d. $t = 100 \,\mu s$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

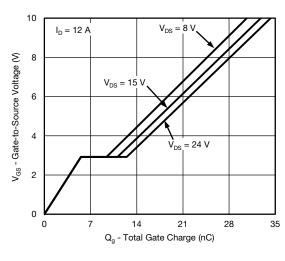




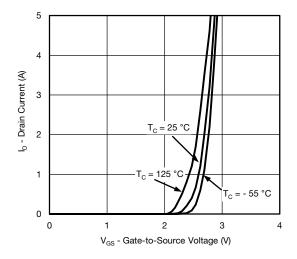
Output Characteristics



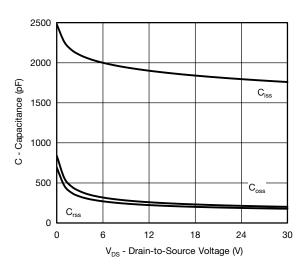
On-Resistance vs. Drain Current and Gate Voltage



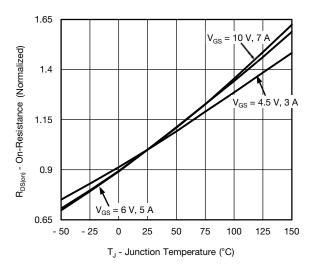
Gate Charge



Transfer Characteristics

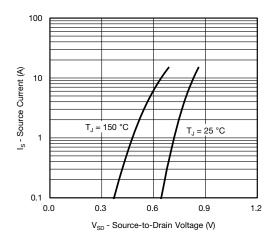


Capacitance

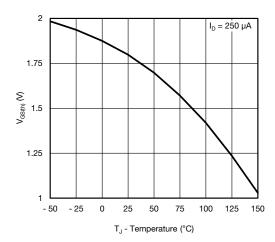


On-Resistance vs. Junction Temperature

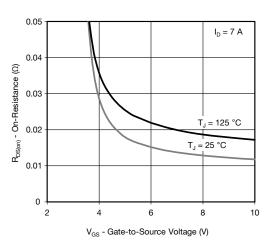




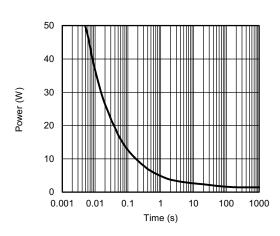
Source-Drain Diode Forward Voltage



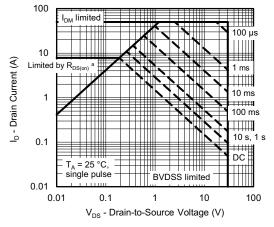
Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power, Junction-to-Ambient

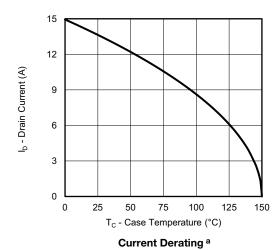


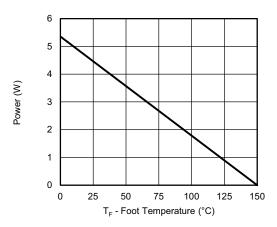
Safe Operating Area, Junction-to-Ambient

Note

a. V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified





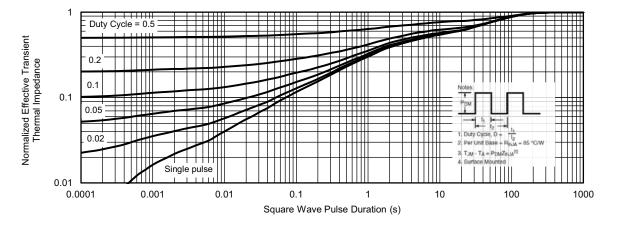


Power, Junction-to-Foot

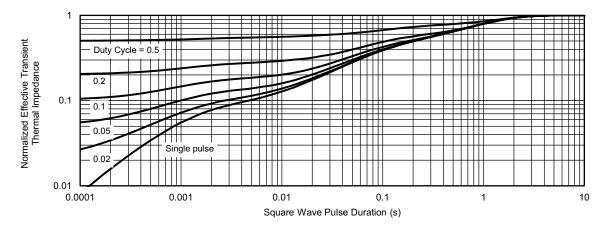
Note

a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit





Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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