

# TPS7B4254-Q1 Evaluation Module

This user's guide describes the TPS7B4254-Q1 EVM evaluation module (EVM) and includes setup instructions, board layouts, schematics, and the bill of materials (BOM).

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## 1 Introduction

TI's TPS7B4254EVM evaluation module (EVM) helps designers evaluate the operation and performance of the TPS7B4254-Q1 tracking LDO. For more information on the TPS7B4254-Q1 device, see the data sheet ([SLVSDI1](#)).

The EVM contains one linear regulator (see [Table 1](#)).

**Table 1. Device and Package Configurations**

Regulator	IC	Package
U1	TPS7B4254QDDARQ1	8-pin SO PowerPAD

## 2 Setup

This section describes the jumpers and connectors on the EVM as well as how to properly connect, set up, and use the TPS7B4254-Q1 EVM.

### 2.1 Input and Output (I/O) Connector Descriptions

**TP1/VIN** – This test point provides a power (VIN) connection for powering the EVM. The input voltage can be measured on this test point.

**TP2/ADJ** – This test point is a reference input voltage for the regulator, allowing the user to attach a reference voltage to the EVM and measure the input voltage of ADJ pin.

**TP3/VOUT** – This test point provides the output of the regulator allowing attachment of a load to the EVM. The output voltage can be measured on this test point.

**TP4/TP5/TP6/GND** – GND is the ground return for the regulator. The EVM provides three GND test points to power up the EVM, to connect the load, and to attach an oscilloscope ground lead.

**TP7/FB** – This test point is the feedback for the regulator allowing measurement of the voltage of the FB pin.

**J1/J2/Output voltage selection** – These two connectors provide the choice of two different output voltage modes:

1. **VOUT equals ADJ (default):** Connect pin 1 and 2 of J1, and leave J2 open. This connection sets the output voltage equal to ADJ with high accuracy.
2. **VOUT decided by resistor:** Connect pin 1 and 2 of J2, and leave J1 open. This connection sets the output voltage with [Equation 1](#). Output voltage can be modified by changing resistors R1 and R2. With the EVM default setup, output voltage should be 40 V when the reference input voltage ADJ is 5 V.

$$V_{OUT} = \left(1 + \frac{R_1}{R_2}\right) \times V_{FB} = \left(1 + \frac{R_1}{R_2}\right) \times V_{ADJ} \quad (1)$$

### 2.2 Bench Setup

The input voltage range for the tracking LDO TPS7B4254-Q1 is 4 V to 40 V. The EVM can support up to 150 mA of load current. Using the following steps to setup the test bench for the EVM:

1. Set the power supply for input VIN to 12 V and set current limit to 1.2 A.
2. Set the power supply for reference ADJ to 5 V and set current limit to 0.1 A.
3. Connect the input power supply positive lead to VIN and the negative lead to GND.
4. Connect the reference power supply positive lead to ADJ and the negative lead to GND.
5. Apply the load between VOUT and GND.

### 2.3 Operation

The TPS7B4254-Q1 powers up after the VIN voltage exceeds the UVLO rising threshold.

### 3 Board Layout

The PCB offers footprints for the TPS7B4254-Q1 device as shown in [Figure 1](#), [Figure 2](#), and [Figure 3](#).

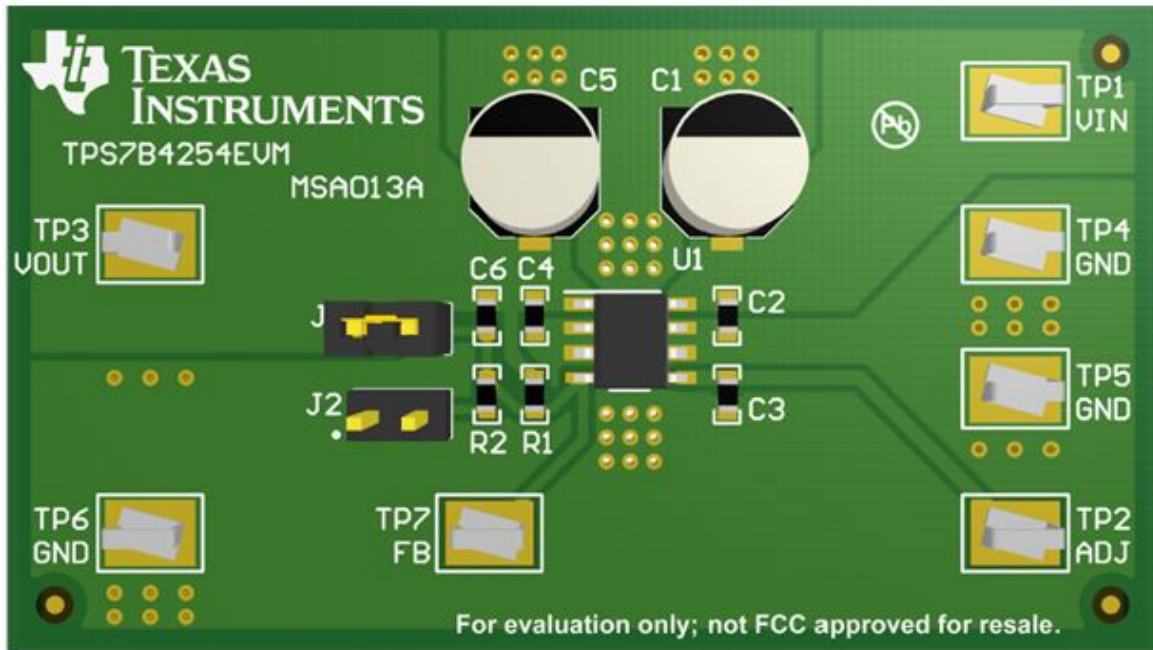


Figure 1. TPS7B4254EVM Component Placement (Assembly Top View)

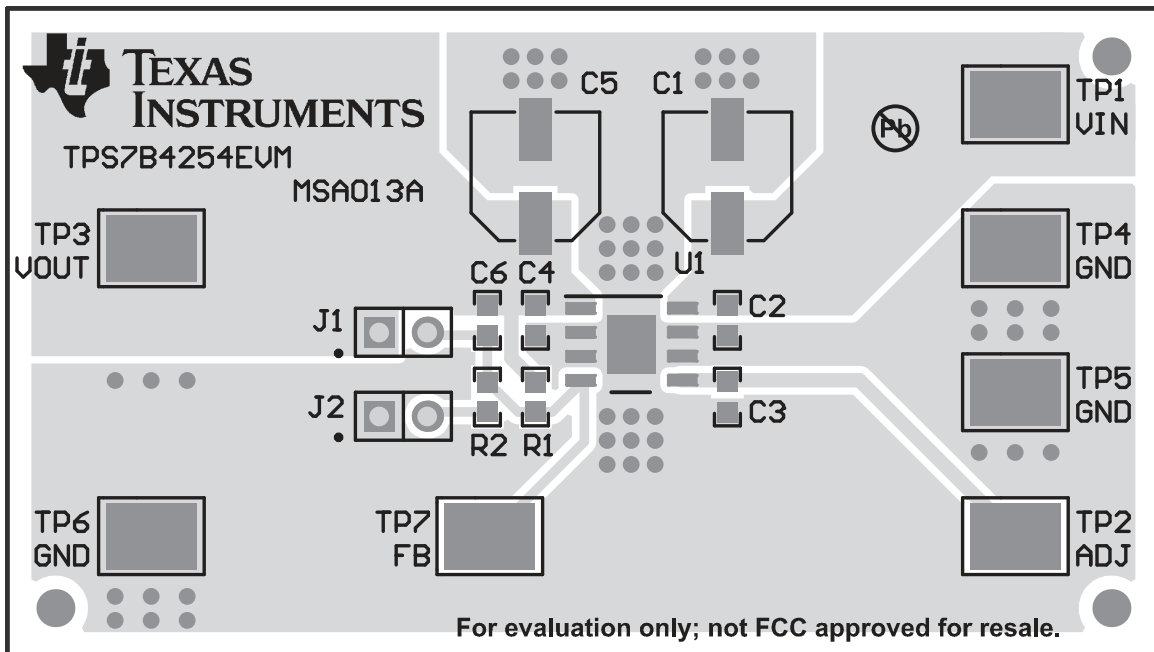


Figure 2. TPS7B4254EVM Top Layer Routing

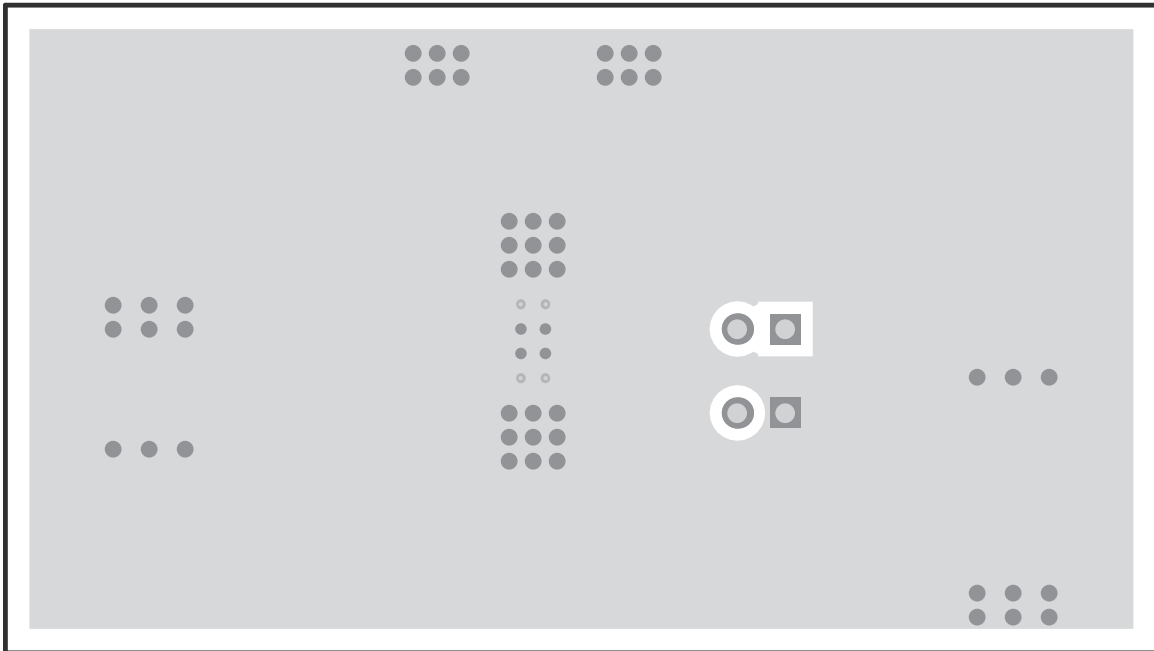
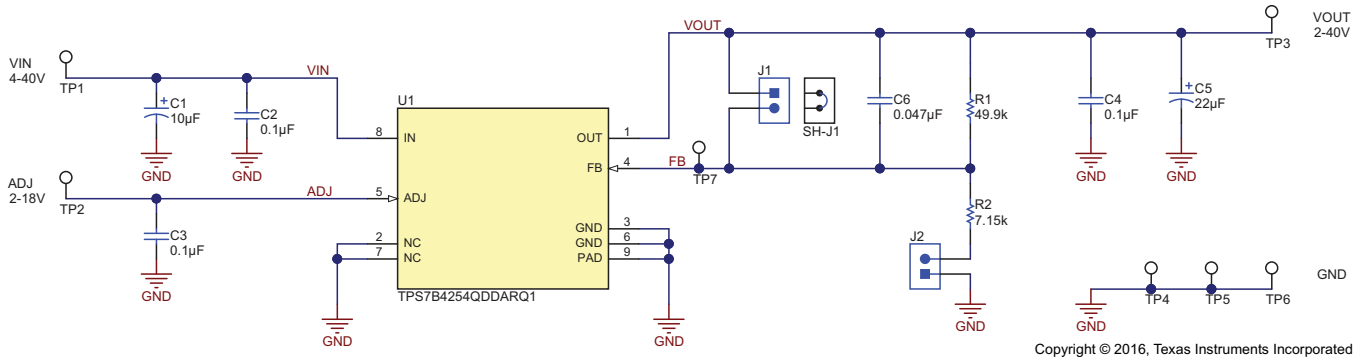


Figure 3. TPS7B4254EVM Bottom Layer Routing

## 4 Schematic and Bill of Materials

Figure 4 illustrates the EVM schematic.



**Figure 4. TPS7B4254QDDARQ1 EVM Schematic**

Table 2 lists the EVM BOM.

**Table 2. Bill of Materials**

Designator	QTY	Value	Description	Package Reference	Part Number	Manufacturer
C1	1	10µF	CAP, AL, 10 µF, 63 V, +/- 20%, 1.5 ohm, SMD	SMT Radial D	EEE-FK1J100P	Panasonic
C2, C3, C4	3	0.1µF	CAP, CERM, 0.1 µF, 50 V, +/- 10%, X7R, 0603	0603	GRM188R71H104KA93D	Murata
C5	1	22µF	CAP, AL, 22 µF, 50 V, +/- 20%, 0.88 ohm, SMD	SMT Radial D	EEE-FK1H220P	Panasonic
C6	1	0.047 µF	CAP, CERM, 0.047 µF, 50 V, +/- 10%, X7R, 0603	0603	GRM188R71H473KA61D	Murata
J1, J2	2		Header, 100mil, 2x1, Gold, TH	2x1 Header	TSW-102-07-G-S	Samtec
R1	1	49.9k	RES, 49.9 k, 1%, 0.1 W, 0603	0603	CRCW060349K9FKEA	Vishay-Dale
R2	1	7.15k	RES, 7.15 k, 1%, 0.1 W, 0603	0603	CRCW06037K15FKEA	Vishay-Dale
SH-J1	1	1x2	Shunt, 100mil, Gold plated, Black	Shunt	969102-0000-DA	3M
TP1, TP2, TP3, TP4, TP5, TP6, TP7	7	SMT	Test Point, Compact, SMT	Test point Keystone Compact	5016	Keystone
U1	1		150mA 40-V Low Dropout Voltage Tracking LDO with 4-mV Tracking Tolerance, DDA0008J	DDA0008J	TPS7B4254QDDARQ1	Texas Instruments

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- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
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3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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