DAC5687 EVM

User's Guide

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DAC5687 EVM

1 Overview

This user's guide document gives a general overview of the DAC5687 evaluation module (EVM) and provides a general description of the features and functions to be considered while using this module.

1.1 Purpose

The DAC5687 EVM provides a platform for evaluating the DAC5687 digital-to-analog converter (DAC) under various signal, reference, and supply conditions. This document should be used in combination with the EVM schematic diagram supplied.

1.2 EVM Basic Functions

Digital inputs to the DAC can be provided with CMOS level signals up to 250 MSPS (external clock mode) through two 34-pin headers. This enables the user to provide high-speed digital data to the DAC5687 device.

The analog outputs from the DAC are available via SMA connectors. Because of its flexible design the analog outputs of the DAC5687 device can be configured to drive a 50-Ω terminated cable using a 4:1 or 1:1 impedance ratio transformer, or single-ended referred to AVDD. The EVM also allows for an option to double the output power by summing the DAC A and DAC B outputs through a 1:1 transformer.

The EVM allows the user to input single-ended, TTL/CMOS level signals, to generate differential clock sources for both CLK1 and CLK2. See Section 4.1, *Input Clocks*, for proper configuration and operation.

Power connections to the EVM are via banana jack sockets.

In addition to the internal bandgap reference provided by the DAC5687 device, options on the EVM allow an external reference to be provided to the DAC.

The DAC5687 EVM allows the user to program the DAC5687 internal registers with the supplied computer parallel port cable and serial interface software. The interface allows read and write access to all registers that define the operation mode of the DAC5687 device.

1.3 Power Requirements

The demonstration board requires only two power supplies. 3.3 Vdc is required at banana jack J7, with the return connected to J9. 1.8 Vdc is required at banana jack J8, with the return to J10.

1.3.1 Voltage Limits

CAUTION

Exceeding the maximum input voltages can damage EVM components. Undervoltage may cause improper operation of some or all of the EVM components.

1.4 Software Installation

All necessary software to operate the serial interface is provided on the enclosed CD-ROM.

1. Insert the CD-ROM into the computer to be used to operate the serial interface.
2. Click on the zipped directory called DAC5687SPI_Installv2p2.zip. Extract all of the files into a new directory, called C:\temp, on the PC.
3. Go the following directory: C:\temp\Installer. Double click on the file called **setup.exe**.
4. The software will create a top level directory at the following location: **C:\Program Files\TI.fdr\DAC5687_SPI**. This directory will contain the required files as well as a labwindows-cvi runtime engine to run the software.
5. Once the installation is complete, the software is launched by running **DAC5687_SPI.exe**. See Chapter 2, DAC5687 EVM Operational Procedure, for instructions on operating the serial interface software.

1.5 Hardware Configuration

The DAC5687 EVM can be set up in a variety of configurations to accommodate a specific mode of operation. Before starting evaluation, the user should decide on the configuration and make the appropriate connections or changes. The demonstration board comes with the following factory-set configuration:

- Differential clock mode using transformers T3 and T4. Input single-ended clocks are required at J3 and J4.
- Transformer-coupled outputs using 4:1 transformers T1 and T2.
- The converter is set to operate with internal reference. Jumper W1 is installed between pins 2 and 3.
- Full-scale output current set to 20 mA through RBIAS resistor R1.
- The DAC5687 output is enabled (sleep mode disabled).
- TxENABLE is set high to enable the DAC5687 device to process data. A jumper is installed between pins 11 and 12 on J15.
- Internal PLL disabled. Jumper W3 is installed between pins 2 and 3.
- Input data level is set to +3.3VDC. Jumper W2 is installed between pins 1 and 2.

To prepare the DAC5687 EVM for evaluation, connect the following:

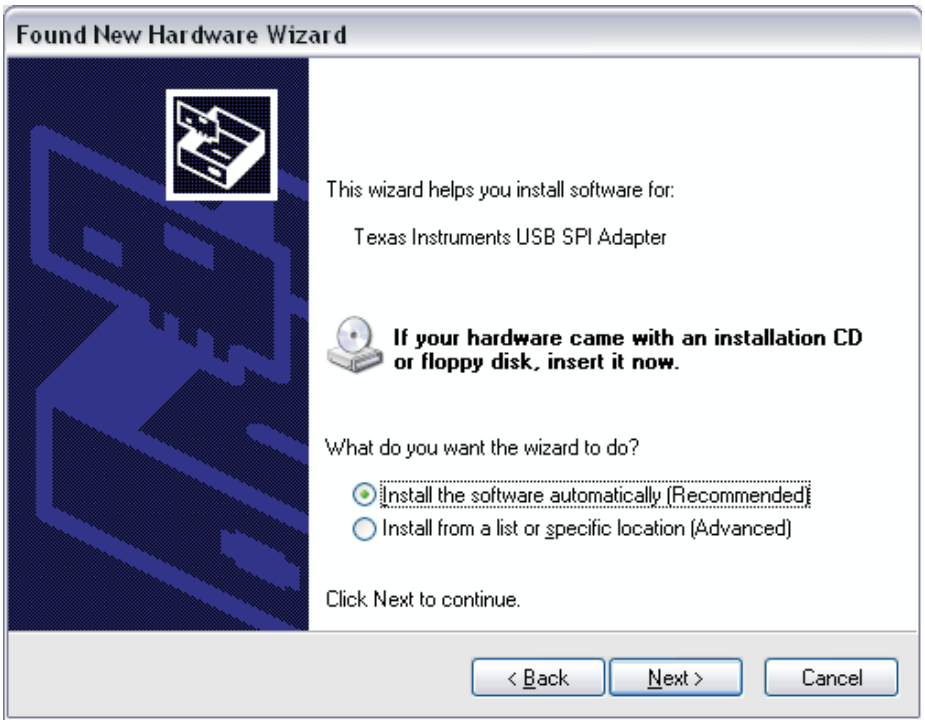
1. 3.3 V to J7 and the return to J9.
2. 1.8 V to J8 and the return to J10.
3. Provide a single-ended, 1-V_{PP}, 0-V offset sine-wave signal to SMA connector J3 (CLK1) if the internal PLL is to be used. Connect this signal to SMA connector J4 (CLK2) if the PLL is disabled. A second sine-wave source is required only for dual clock mode. In this mode, the signal on CLK1 is used to clock data into the DAC5687 and the signal on CLK2 is used to clock the internal DAC. CLK1 and CLK2 must be phase-aligned for this option to work properly. In order to preserve the specified performance of the DAC5687 converter, the clock sources must feature very low jitter. Using a clock with a 50% duty cycle gives optimum dynamic performance.
4. Use a digital test pattern generator with 50-Ω outputs to provide 3.3-V CMOS logic level inputs to connectors J13 and J14. Adjust the digital inputs to provide the proper voltage levels and setup and hold times at the DAC5687 inputs. See the DAC5687 data sheet (SLWS164) for timing information. Another solution is to use the TSW1400 pattern generator card as explained in Section 2.3
5. Connect one end of the supplied serial interface cable to the parallel port of a PC. Connect the other end of the cable to J1 on the EVM. The user can also use the provided USB to SPI adapter, setup is explained in Section 2.
6. The DAC5687 outputs can be monitored using SMA connector J5 for IOUTA and SMA connector J19 for IOUTB.

2 DAC5687 EVM Operational Procedure

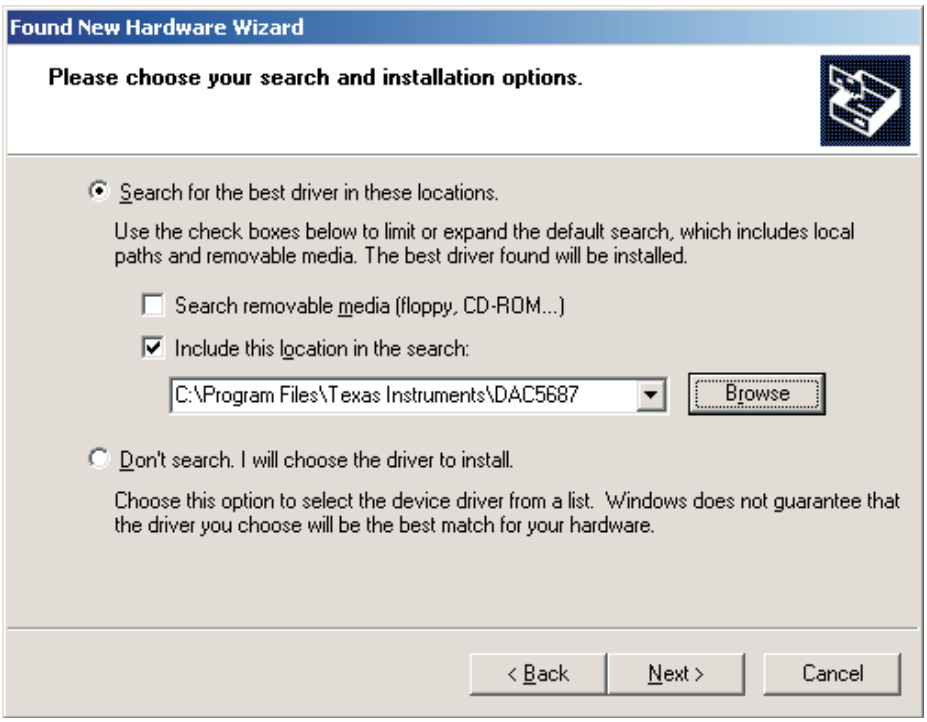
To prepare the DAC5687 EVM for operation, follow these steps:

1. *Parallel Port Interface:* Connect one end of the supplied serial interface cable to the parallel port of a PC and the other end of the cable to J1 on the EVM and skip steps 2 to 7.
2. *USB Interface:* Connect the provided USB to SPI adapter board to the parallel port connector on the EVM and to a spare USB port on the host PC using the supplied USB cable. The Windows Found New Hardware Wizard should open; if this is not the case make sure the cable is connected properly. Select “No, not this time” from the options available and then click “Next” to proceed with the installation.

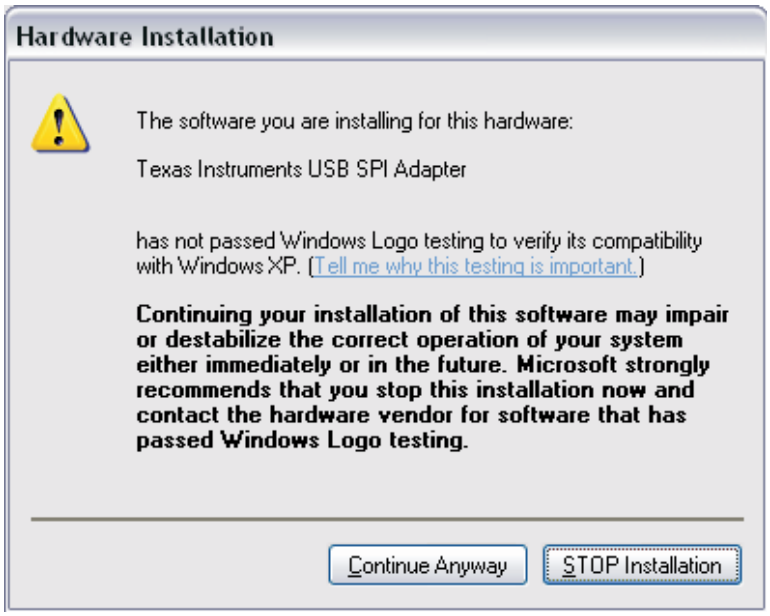
3. Select "Install the software automatically (recommended)" as shown below and then click "Next".



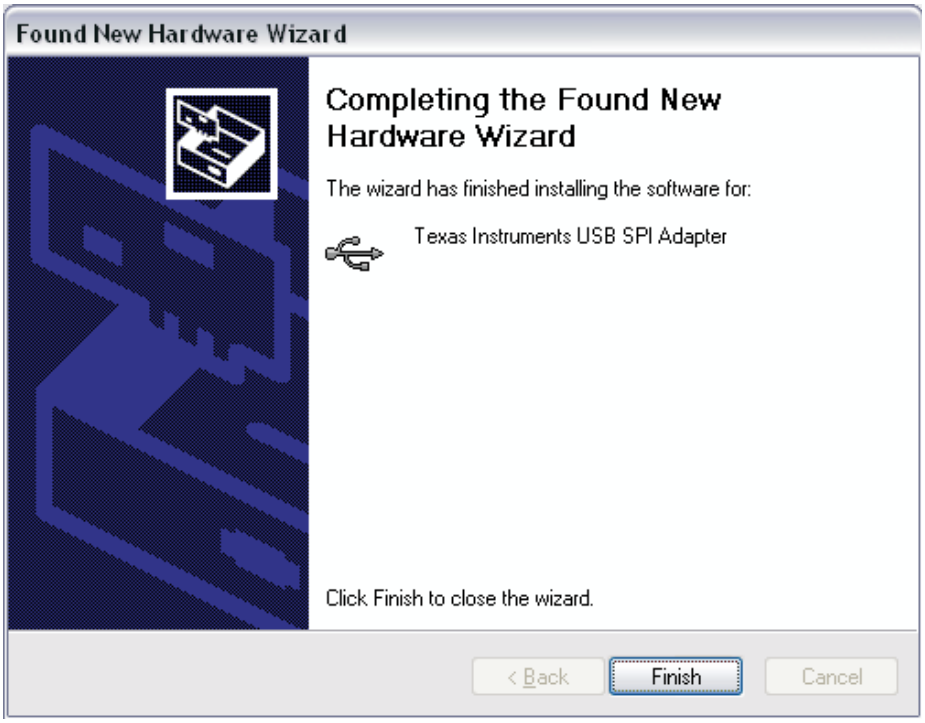
4. If Windows is not able to find the appropriate USB drivers press “Back” and select “Install from a list or specific location (advanced)”. Click “Next”.
5. Select "Search for the best driver in these locations" and browse for the folder where the DAC5687 program was installed (the default location is C:\Program Files\Texas Instruments\DAC5687). Once the file path has been selected, click “Next” to proceed.



6. If Windows XP is configured to warn when unsigned (non-WHQL certified) drivers are about to be installed, the following screen is displayed unless installing a Microsoft WHQL certified driver. Click on "Continue Anyway" to continue with the installation. If Windows XP is configured to ignore file signature warnings, no message will appear.



7. Windows should then display a message indicating that the installation was successful. Click "Finish" to complete the installation.



2.1 Starting the Serial Interface Program

Power up the EVM. After power up, depress switch S1 to reset the DAC5687. Start the software by running the following executable:

C:\Program Files\TI.fdr\DAC5687_SPI\ DAC5687_SPI.exe.

If the EVM is powered on with the parallel port connected properly, then the GUI shown in Figure 1 is displayed with the default settings read from the device. If using the USB interface card, change mode to USB in the upper right corner window. The hardware and software are now ready for testing. For serial interface operation, simply click on the switches, up/down arrows, etc., to select the desired settings of the DAC5687. If there is a problem with the communication, such as the EVM is not powered on or the parallel port cable is not connected, an error message will be displayed instructing the user to correct the problem. Once corrected, hit the "Read All" button, located in the lower right corner of the GUI, to read the default settings of the device.

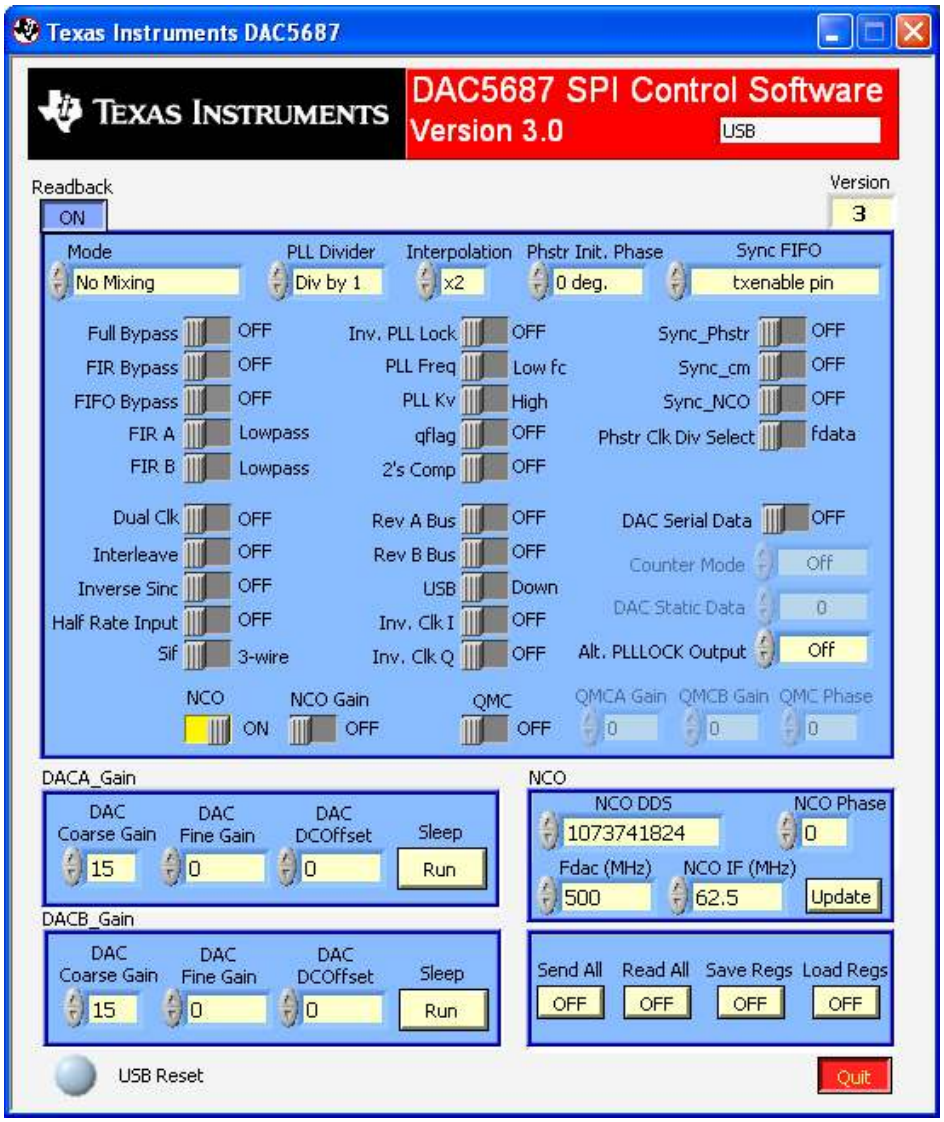


Figure 1. Serial Interface GUI

For normal operation, the user needs only to select values and switches as desired. The values are automatically sent to the device and read back to verify their configuration.

2.2 DAC5687 Initial Setup Tests

There are several initial tests with the DAC5687 that can be done without any input data. The following setup steps are suggested to familiarize the user with the DAC5687 and EVM software and verify that the DAC5687 is functioning properly.

1. Provide a CLK2 input if the PLL is disabled or a CLK1 input if the PLL is enabled (W3). Do not provide parallel input data.
2. Power up EVM with 1.8V DVDD and 3.3V AVDD
3. Start DAC5687_SPI software.
4. Click on the "Load Regs" button on the GUI. A new directory window will open. Click on the file called "User Guide Test.reg5687". Click on "OK". This will load a test setting for the DAC, corresponding to $F_{NCO}/12.5$ = 20 MHz for CLK2 = 500 MSPS ($F_{NCO} = F_{DAC}/2$ for X4L mode). The GUI should now look as shown in Figure 2.

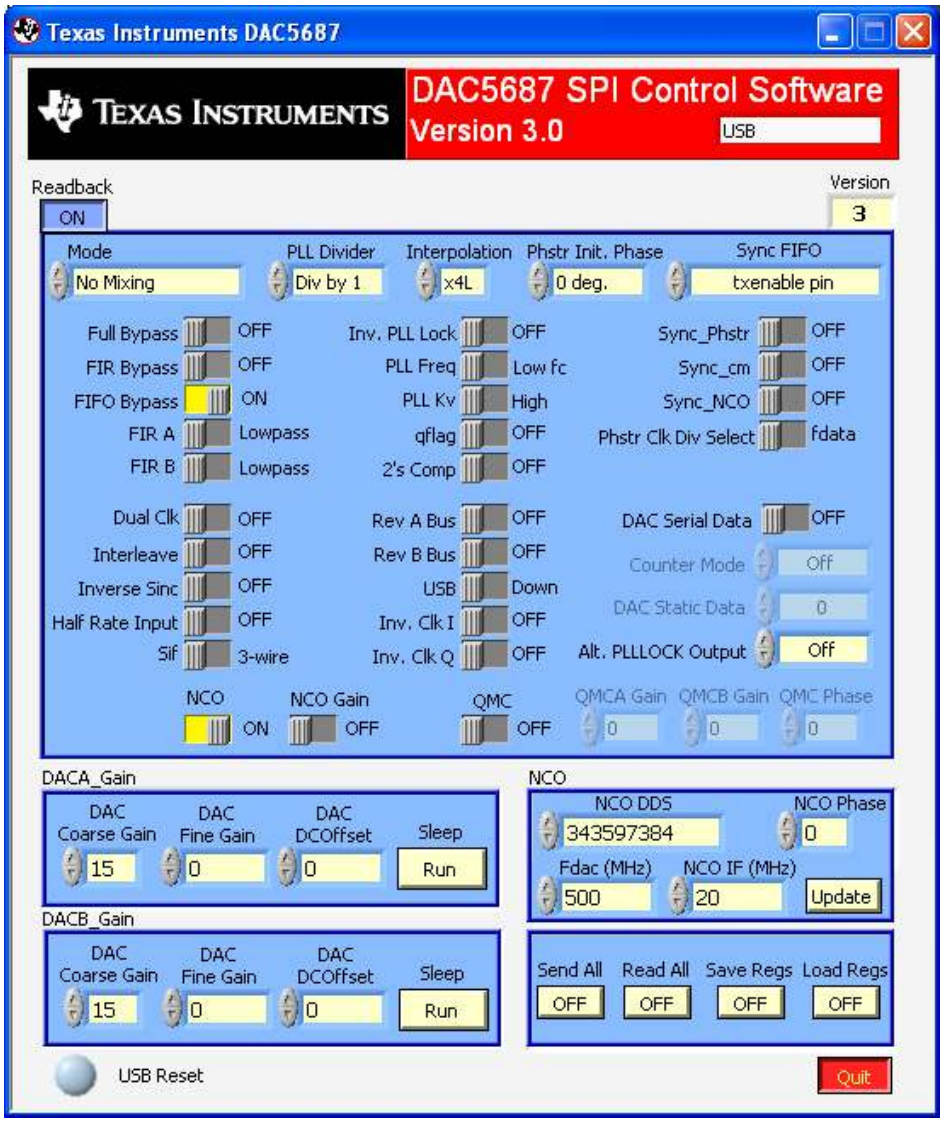


Figure 2. DAC5687 Setup for X4L Mode and NCO Tone at $F_{DAC}/25$

This tone is being generated by the DAC5687 NCO. With no input data provided to connectors J13 and J14, the Channel A and B data bus inputs will all be zeros, or a full scale negative value in the default offset binary format. In the X4L mode, after the first 2x interpolation, the full scale DC input signal at a clock rate of 250 MSPS is mixed with the NCO running at the setting of $F_{NCO}/12.5$ (343597383) to generate a tone at 20 MHz. After a second 2x interpolation, a 20 MHz tone is output from the DAC sampling at 500 MSPS. The output spectrum should be similar to Figure 3.

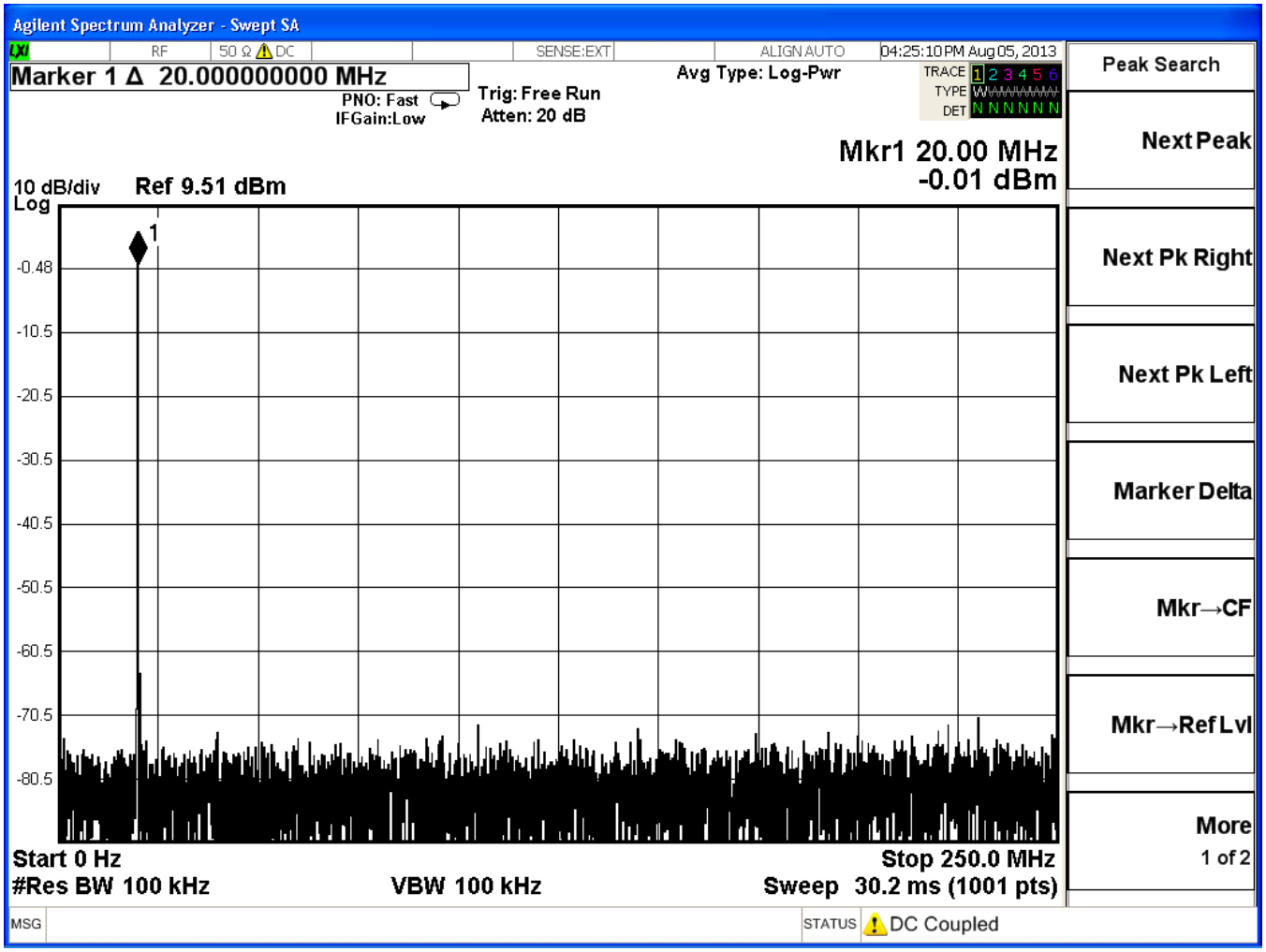


Figure 3. Spectrum with CLK2 = 500 MHz, X4L Interpolation and NCO Frequency = 343597383

5. Change the Mode to *1000 $F_{DAC}/4$ (+,+)*, corresponding to $F_{DAC}/4$ (see data sheet). This will increase the output by $F_{DAC}/4$ to 20 MHz + 125 MHz = 145 MHz.
6. Changing the NCO DDS to 3951369913 (2^{32} x (1-20/250)) will now result in an output tone at 125 MHz - 20 MHz = 105 MHz.
7. Change the interpolation to X4, and the mode to *No Mixing*, the NCO DDC to 286331153 ($F_{NCO}/15$) and reduce the CLK2 frequency to < 320 MSPS. The GUI should look as shown in Figure 4. The NCO is now running at the DAC update rate (= CLK2). For CLK2 = 300 MSPS, the result is an output tone at 20 MHz.

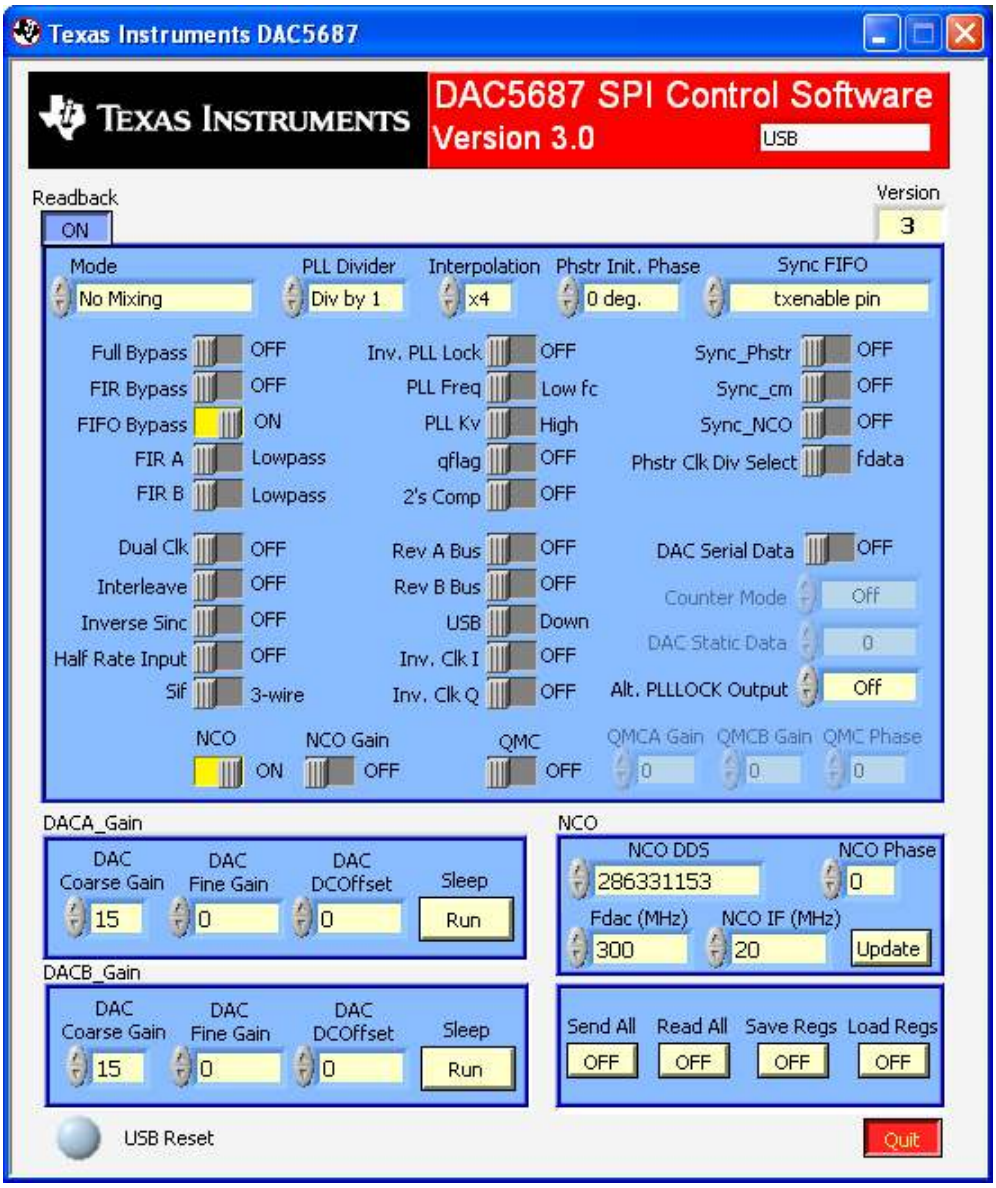


Figure 4. DAC5687 Setup for X4 Mode and NCO Tone at $F_{DAC}/15$

2.3 Basic Test Procedure with TSW1400

This section outlines the basic test procedure for testing the EVM with the TSW1400.

2.3.1 TSW1400 Overview

The TSW1400 is a high speed data capture and pattern generator board. For more detailed explanation of the TSW1400 setup and operation, see the TSW1400 user's guide (SLWU079). This document assumes that the High Speed Data Converter Pro software (available to download here: http://www.ti.com/tool/tsw1400evm) is installed and functioning properly.

2.3.2 Test Block Diagrams for TSW1400

As described in Figure 5, the first steps consist in connecting boards together through CMOS interface, connecting USB interfaces to a PC and connecting a source clock to CLK2 and one output to a signal analyzer.

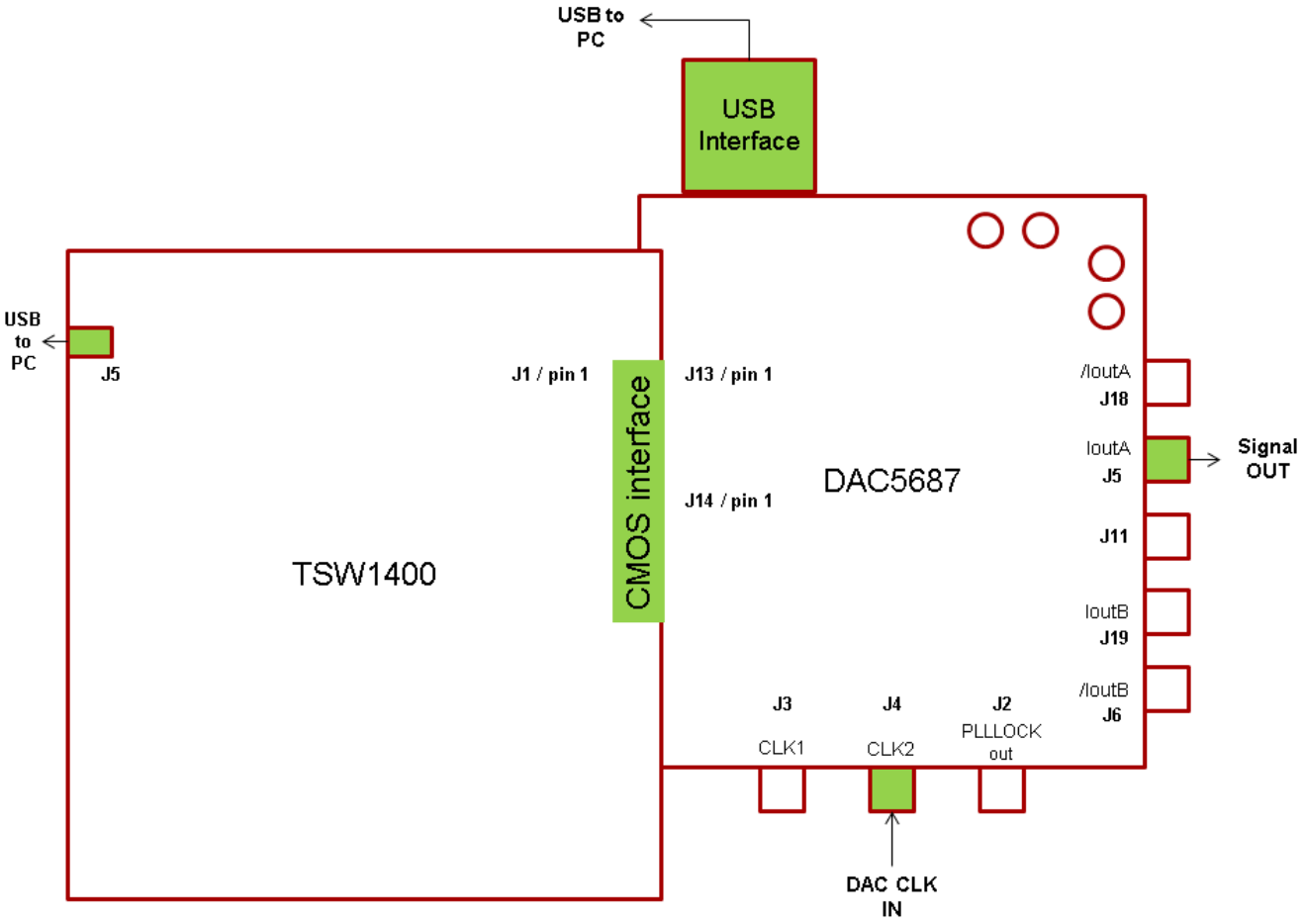


Figure 5. Connecting TSW1400 and DAC5687 Together

Next, as shown in Figure 6, it is important to connect the PLL output of the DAC5687 “PLLLOCK out” to the “CMOS CLK” input of the TSW1400 in order to synchronize the data rates. Finally, supply the DAC5687 with 1.8V and 3.3V, and supplying the TSW with a 5V jack.

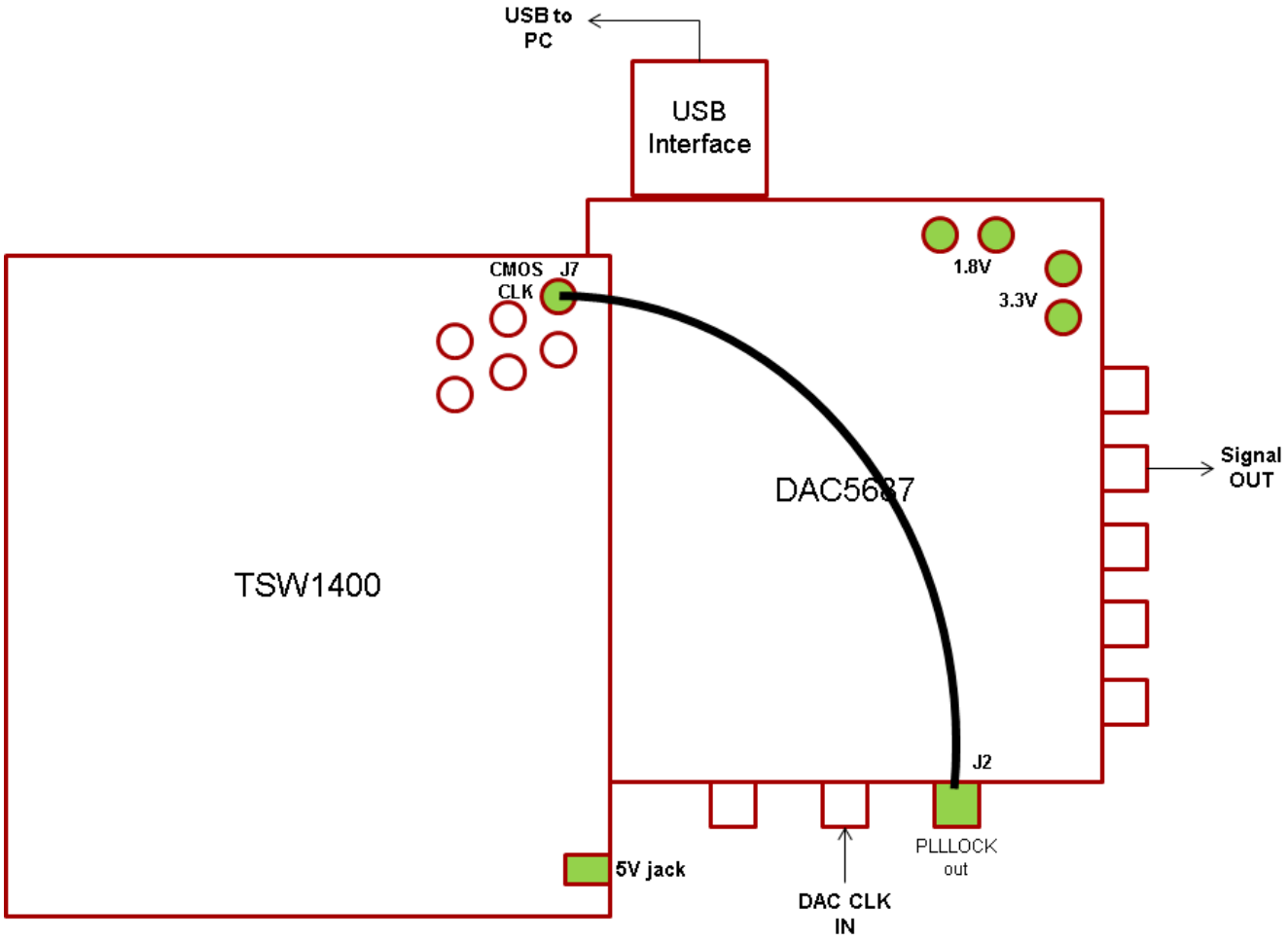


Figure 6. Clocks Synchronisation Between DAC5687 and TSW1400

2.3.3 DAC5687 Example Setup Procedure

Launch the DAC5687 GUI and check for valid connection for either parallel or USB connection. Press reset button on the DAC5687 EVM and press "Read All" button on the GUI to update the DAC5687 reset value to the GUI.

For this first test, disable NCO and leave the rest as default.

NOTE: One important detail is to make sure to enable Rev B bus since channel B is B(15:0) when A is A(0:15) on Rev. B of the EVM.

The Bus B is reversed to avoid data lines crossing on the layout, see Section 4.2 for details.

The setup should look like Figure 7.

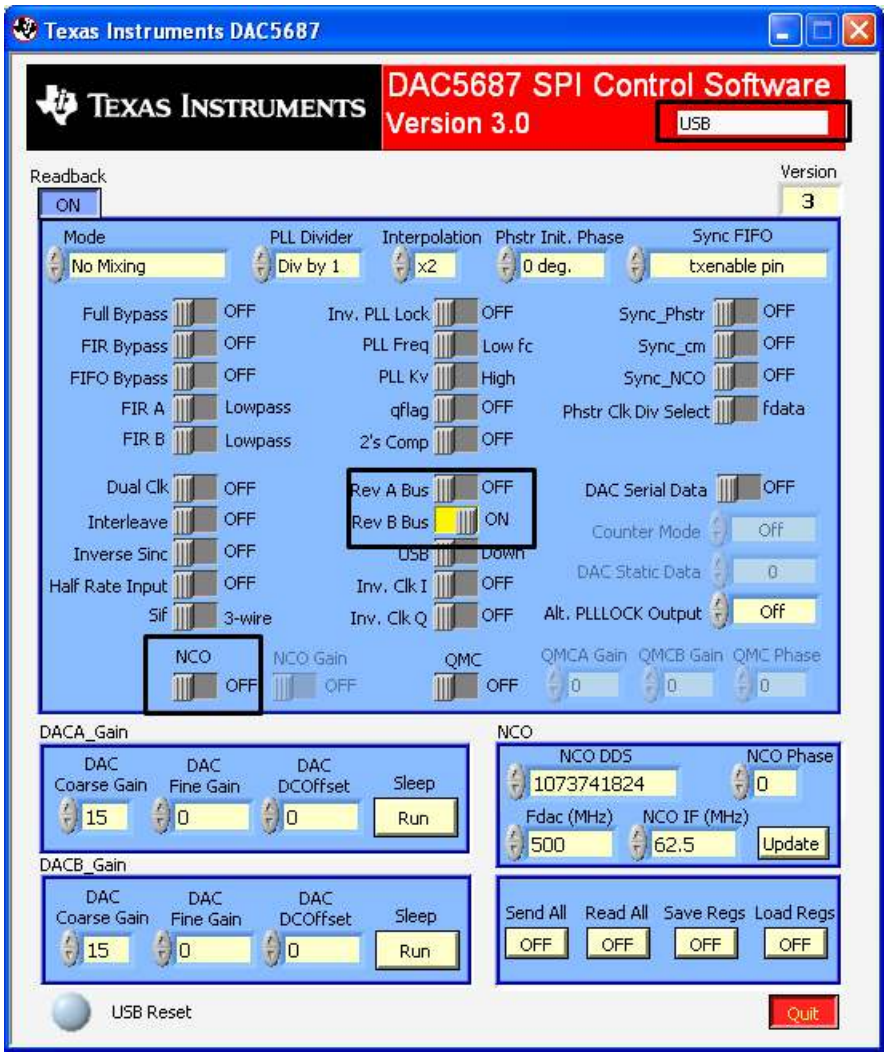


Figure 7. DAC5687 GUI Setup

2.3.4 TSW1400 Example Setup Procedure

A single tone with HSDC pro is generated in this section.

1. Start the High Speed Converter Pro GUI program. When the program starts, select the DAC tab and then select CMOS firmware in the “Select DAC” menu.

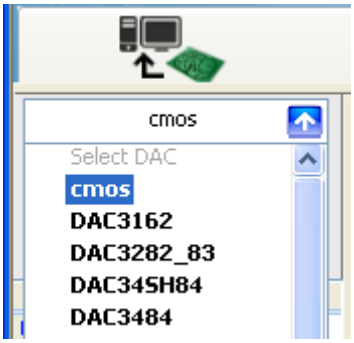


Figure 8. Select CMOS in HSDC PRO

2. When prompted ‘load DAC firmware?’, select YES.

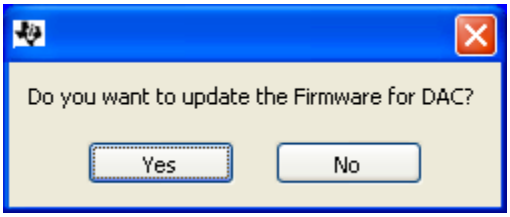


Figure 9. Load DAC Firmware Prompt

In this test, a 122.88MHz DAC clock is used with 2x interpolation, so Data rate is 61.44MHz.

3. Select 61.44Mhz Data rate, Offset bin
4. Generate a one tone test, here a 5MHz complex

Result should look like Figure 10.

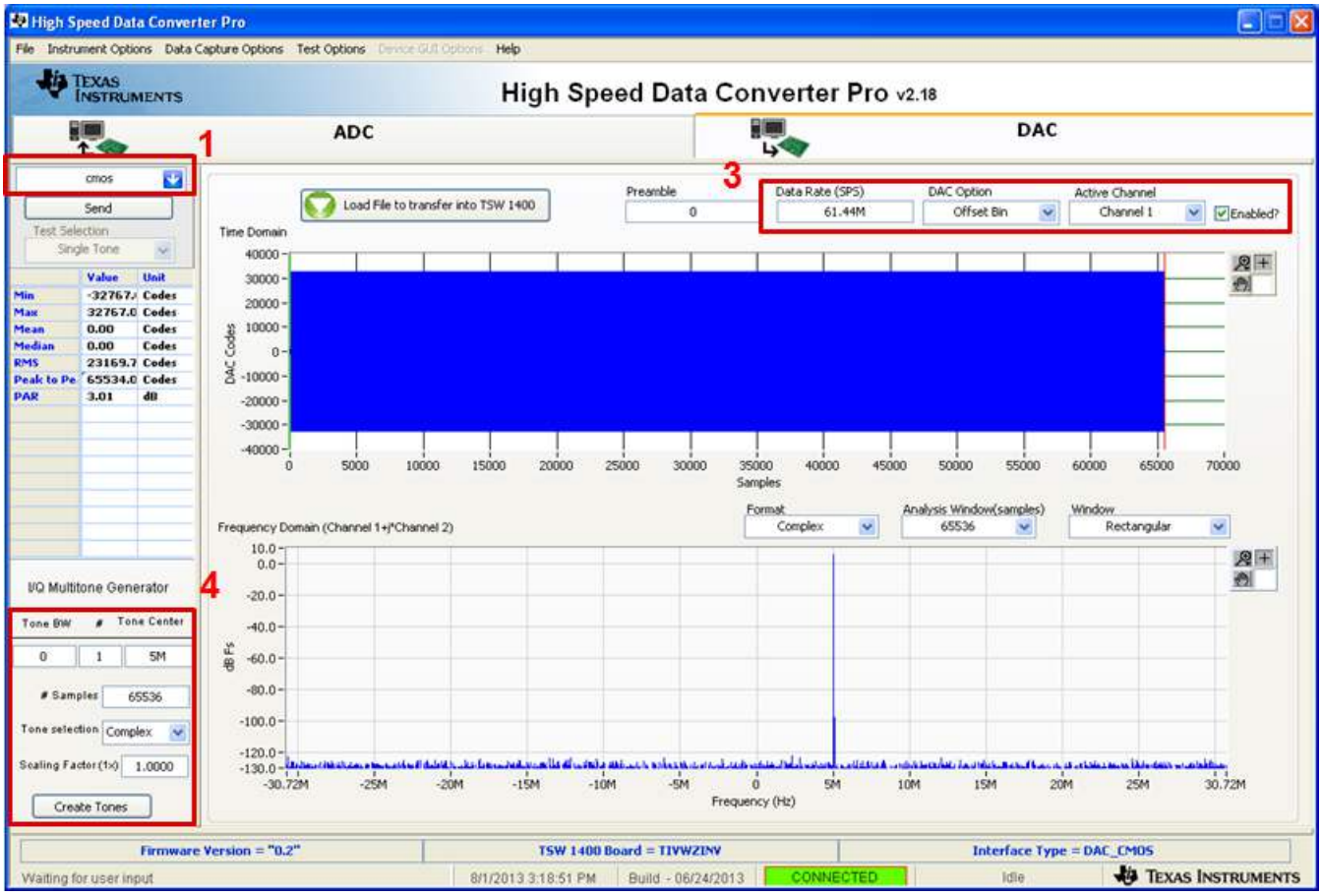


Figure 10. HSDC Pro Setup for One Tone Generation

Send the generated signal clicking on send. Remove and put the TXenable jumper to synchronize the FIFO.

Result on the signal analyzer should be similar to Figure 11.

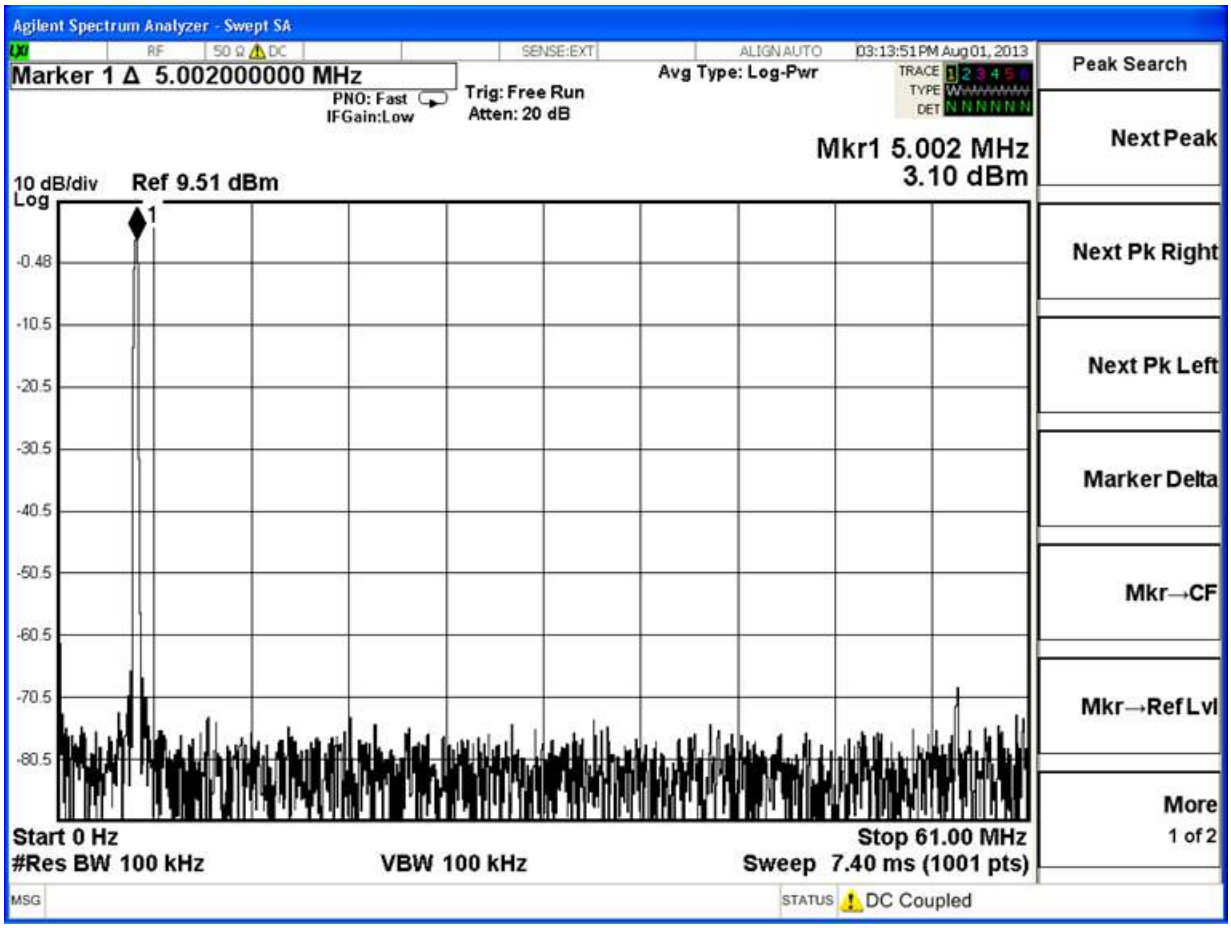


Figure 11. 1 Tone Test, no NCO

Next step can be to activate the NCO. To do so:

1. Switch on the NCO feature on the DAC5687 GUI.
2. Set F_{DAC} to 122.88Mhz and NCO IF to 20MHz for instance
3. Click on update, it will automatically calculate the NCO DDs value and send it

Result of the setup is shown in Figure 12.

Figure 12. NCO Configuration

Result on the signal analyzer is shown in Figure 13.

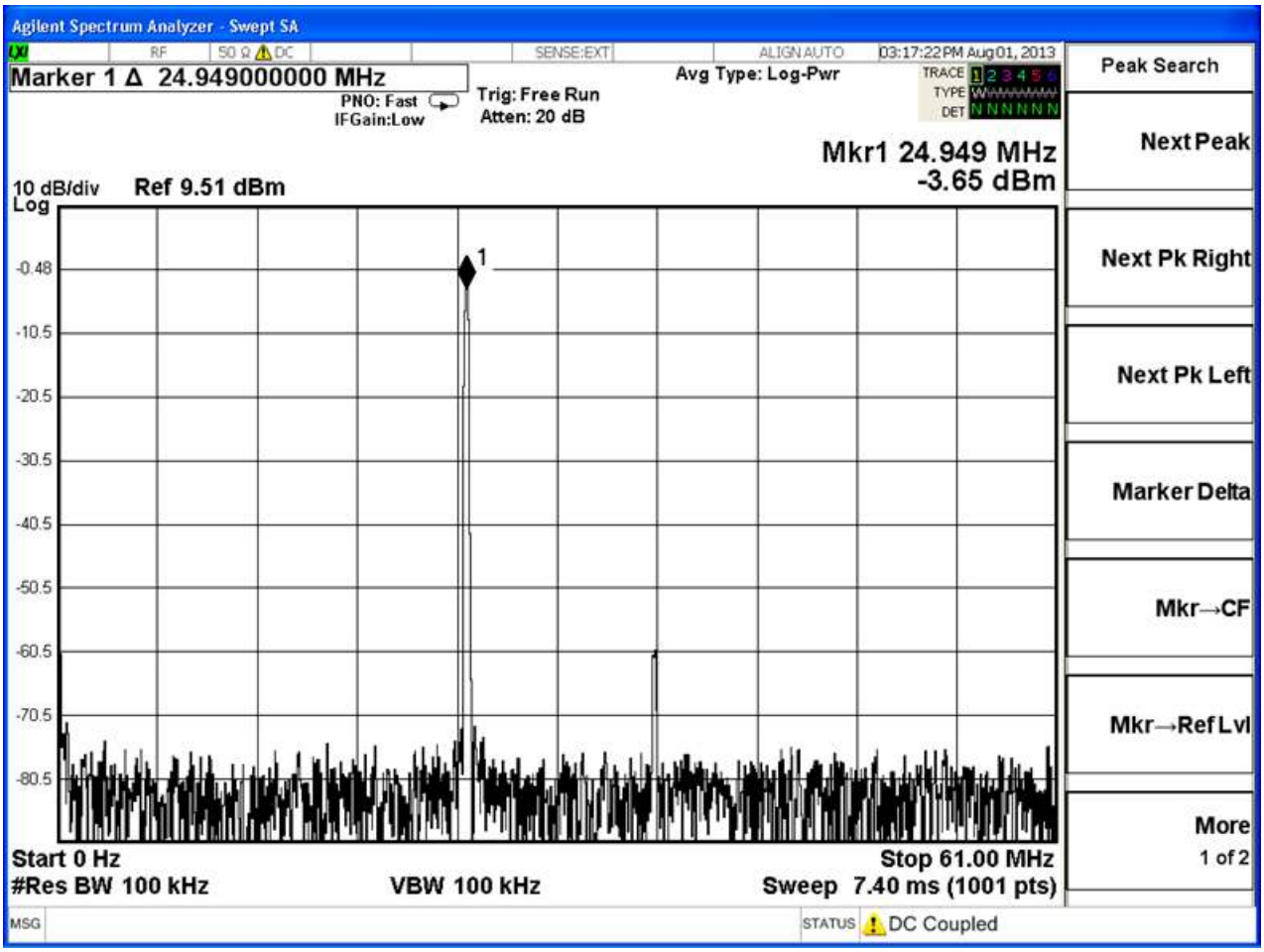


Figure 13. 1 Tone Test, NCO Activated, IF = 20Mhz

2.4 DAC5687 GUI Register Descriptions

2.4.1 Register Controls

- **Load Regs:** Loads register values from a saved file to the DAC5687 and updates the GUI.
- **Save Regs:** Saves current GUI registers settings to a text file for future use.
- **Read All:** Reads the current registers of the DAC5687. This is used to verify settings on the front panel.
- **Send All:** Sends the current front panel registers to the device. This is generally only used when the EVM power has recycled or the device has been reset and the user wants to load the displayed settings to the device.

2.4.2 Configuration Controls

- **Full Bypass:** When set, all filtering, QMC, and NCO functions are bypassed.
- **FIR Bypass:** When set, the interpolation filters are bypassed.
- **FIFO Bypass:** When set to bypass, the internal 4 sample FIFO is disabled. When cleared, the FIFO is enabled.
- **FIR A:** A side first FIR filter in highpass mode when set, lowpass mode when cleared.
- **FIR B:** B side first FIR filter in highpass mode when set, lowpass mode when cleared.
- **Dual Clk:** Only used when the PLL is disabled. When set, two differential clocks are used to input the data to the chip; CLK1/CLK1C is used to latch the input data into the chip, and CLK2/CLK2C is used as the DAC sample clock

- **Interleave:** When set, interleaved input data mode is enabled; both A and B data streams are input at the DA(15:0) input pins.
- **Inverse Sinc:** Enables inverse sinc filter.
- **Half Rate Input:** Enables half rate input mode. Input data for the DAC A data path is input to the chip at half speed using both the DA(15:0) and DB(15:0) input pins.
- **Sif:** Sets sif_4pin bit. 4 pin serial interface mode is enabled when on, 3 pin mode when off. The DAC5687 EVM is configured for a 3 pin serial interface. The 4 bit serial interface will not work with the DAC5687 EVM.
- **Inv. PLL Lock:** Only used when PLL is disabled and dual clock mode is disabled. When cleared, input data is latched into the chip on the rising edge of the PLLLOCK output pin. When set, input data is latched into the chip on the falling edge of the PLLLOCK output pin.
- **PLL Freq:** Sets PLL VCO center frequency to low or high center frequency.
- **PLL Kv:** Sets PLL VCO gain to either high or low gain.
- **Qflag:** Sets qflag bit. When set, the QFLAG input pin operates as a B sample indicator when interleaved data is enabled. When cleared, the TXENABLE rising determines the A/B timing relationship.
- **2's Comp:** When set, input data is interpreted as 2's complement. When cleared, input data is interpreted as offset binary.
- **Rev A Bus:** When cleared, Channel A input data MSB to LSB order is DA(15) = MSB and DA(0) = LSB. When set, Channel A input data MSB to LSB order is reversed, DA(15) = LSB and DA(0) = MSB.
- **Rev B Bus:** When cleared, Channel B input data MSB to LSB order is DB(15) = MSB and DB(0) = LSB. When set, Channel B input data MSB to LSB order is reversed, DB(15) = LSB and DB(0) = MSB.
- **USB:** When set, the data to DACB is inverted to generate upper side band output.
- **Inv. Clk I(Q):** Inverts the DAC core sample clock when set, normal when cleared.
- **Sync_Phstr:** When set, the internal clock divider logic is initialized with a PHSTR pin low to high transition.
- **Sync_cm:** When set, the coarse mixer is synchronized with a PHSTR low to high transition.
- **Sync_NCO:** When set, the NCO phase accumulator is cleared with a phstr low to high transition.
- **Phstr Clk Div Select:** Selects the clock used to latch the PHSTR input when restarting the internal clock dividers. When set, the full rate CLK2 signal latches PHSTR. When cleared, the divided down input clock signal latches PHSTR.
- **DAC Serial Data:** When set, both DAC A and DAC B input data is replaced with fixed data loaded into the 16 bit serial interface DAC Static Data.
  - **Counter Mode:** Controls the internal counter that can be used as the DAC data source. See the data sheet for more information.
  - **DAC Static Data:** When DAC Serial Data is set, both DAC A and DAC B input data is replaced with fixed data loaded with this value. Range = 0 to 65535.
- **NCO:** When set, enables NCO.
  - **NCO Gain:** Sets NCO gain resulting in a 2x increase in NCO output amplitude. Except for $F_S/2$ and $F_S/4$ mixing NCO frequencies, this selection can result in saturation for full scale inputs. Consider using QMC gain for lower gains.
- **QMC:** When set, enables the QMC.
  - **QMCA Gain:** Sets QMC gain A to a range = 0 to 2047. See the data sheet for more information.
  - **QMC B Gain:** Sets QMC gain B to a range = 0 to 2047. See the data sheet for more information.
  - **QMC Phase:** Sets QMC phase to a range = -512 to 511. See the data sheet for more information.
- **Mode:** Used to select the coarse mixer mode. See the DAC5687 data sheet for more information.
- **PLL Divider:** Sets VCO divider to div by 1, 2, 4, or 8.
- **Interpolation:** Sets FIR Interpolation factor: {X2, X4, X4L, X8}. X4 uses lower power than 4xL, but F_{DAC} = 320 MSPS max when NCO or QMC are used.
- **Phstr Init. Phase:** Adjusts the initial phase of the $F_S/2$ and $F_S/4$ cmix block at PHSTR.
- **Sync FIFO:** Sync source selection mode for the FIFO. When a low to high transition is detected on the selected sync source, the FIFO input and output pointers are initialized. See the DAC5687 data sheet for source description.
- **Alt. PLLLOCK Output:** Sets PLLLOCK output pin to F_{DAC} frequency when operating in the PLL mode. Settings must be used in conjunction with the interpolation setting to achieved desired rate (i.e. set to $F_{DAC}/2$ for 2x interpolation, set to $F_{DAC}/4$ for 4x interpolation). Note, there is no option for the 8x mode. The jumper at W1 (EXTLO) must be removed to utilize this functionality.

2.4.3 DAC A(B) Gain

- **DAC Coarse Gain:** Sets coarse gain of DAC A(B) full scale current. Range is 0 to 15. See the DAC5687 data sheet for full scale gain equation.
- **DAC Fine Gain:** Sets fine gain of DAC A(B) full scale current. Range is -128 to 127. See the DAC5687 data sheet for full scale gain equation.
- **DAC DC Offset:** Sets DAC A(B) DC offset register. Range is -4096 to 4095.
- **Sleep:** DAC A(B) sleeps when set, operational when cleared.

2.4.4 NCO

- **NCO DDS:** Sets NCO DDS registers. See the DAC5687 data sheet for formula.
- **NCO Phase:** Sets initial NCO phase registers. See the DAC5687 data sheet for more information.

FDac: Set the DAC frequency in Mhz for NCO DDS calculation

NCO IF: Set IF in Mhz for NCO DDS calculation

2.4.5 Additional Control/Monitor Registers

- **PII Port Config:** Selection of this button will bring up a separate window that shows the parallel port configuration of the software. The EVM Menu should be loaded with DAC EVM. This button also allows the user to change the LPT address used by the PC. This is set by entering a valid address inside the box labeled "LPT Address". The default setting is 378.
- **Quit:** Quits the operation of the DAC5687 software.
- **Version:** Displays the version of the silicon. If a version of 0 is read then the communication is not functioning and an error message will be displayed.
- **About:** Opens an additional window with help related topics for the software.

3 Physical Description

This chapter describes the physical characteristics and PCB layout of the EVM and lists the components used on the module.

3.1 PCB Layout

The EVM is constructed on a 4-layer, 4.9-inch x 6.5-inch, 0.055-inch thick PCB using FR-4 material. Figure 14 through Figure 17 show the PCB layout for the EVM.

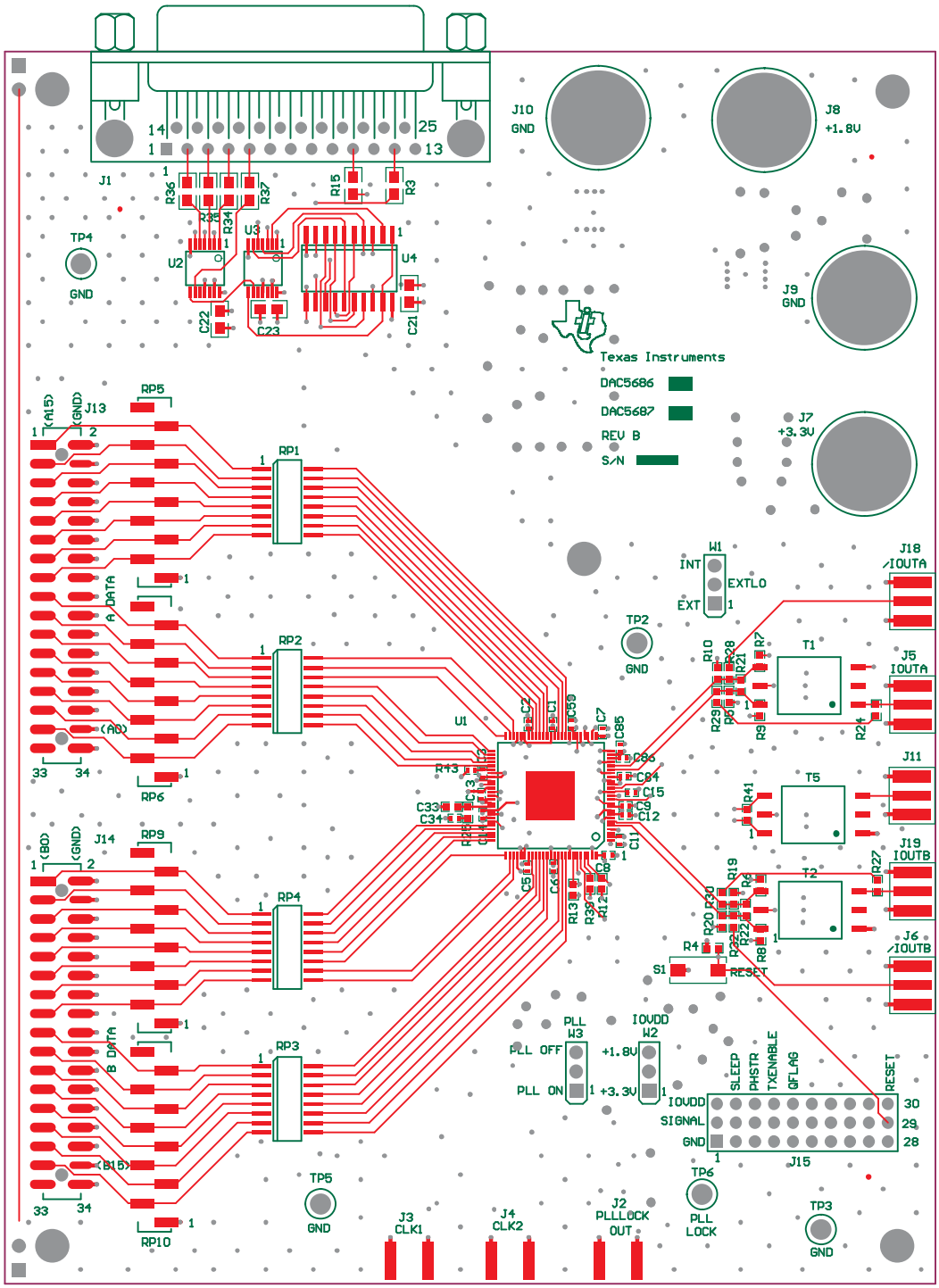


Figure 14. Top Layer 1

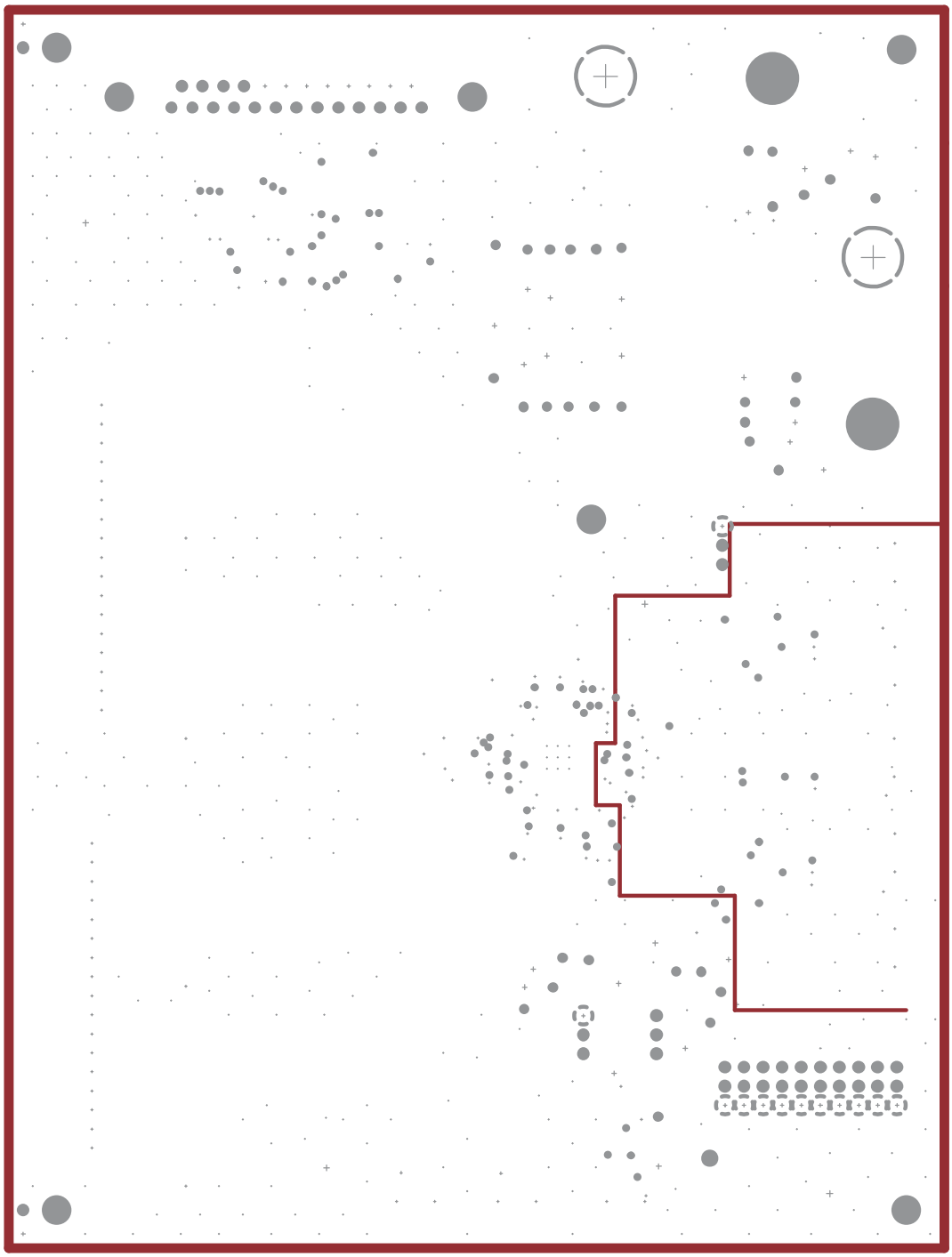


Figure 15. Layer 2, Ground Plane

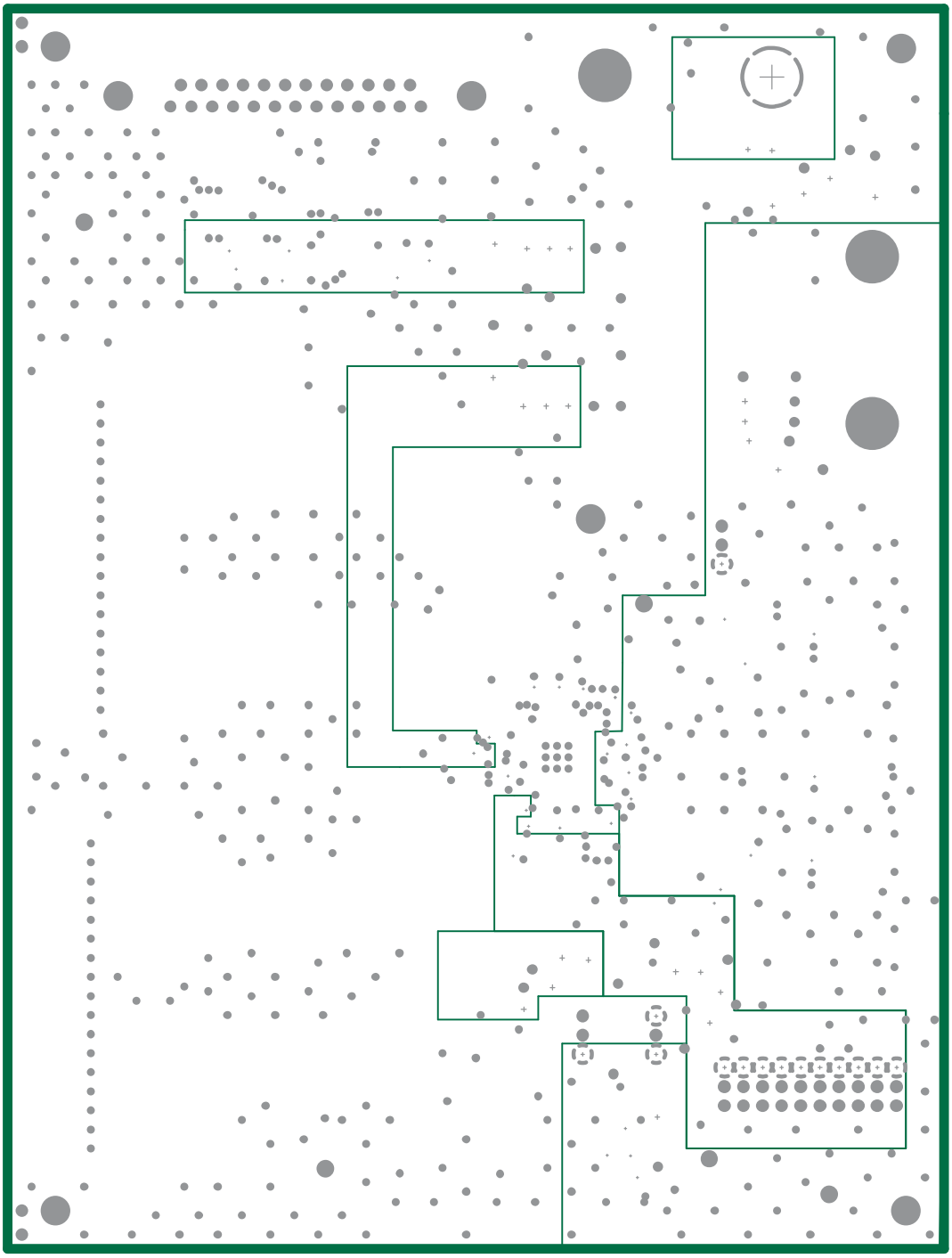


Figure 16. Layer 3, Power Plane

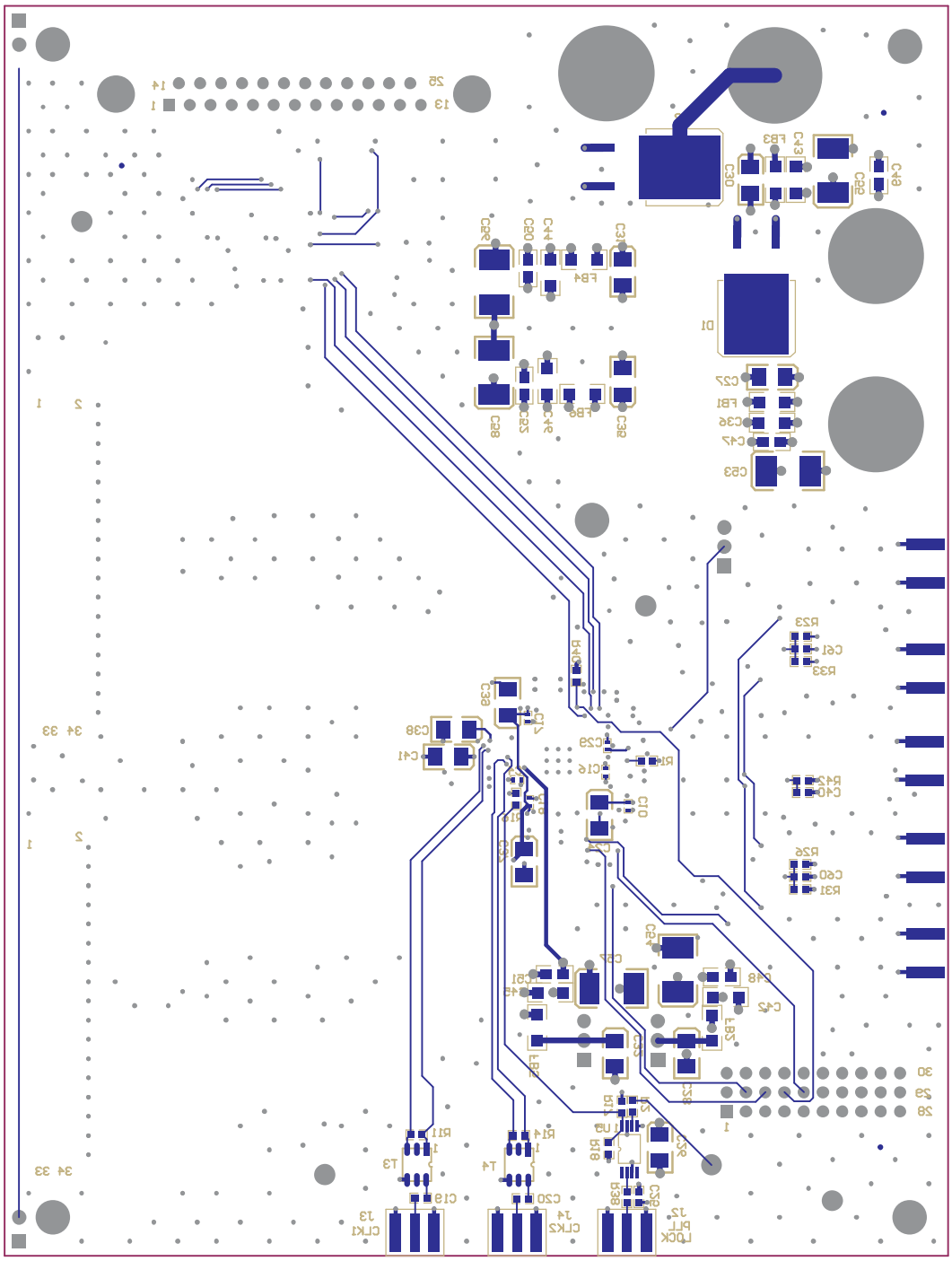


Figure 17. Bottom Layer

3.2 Parts List

Table 1 lists the parts used in constructing the EVM.

Table 1. DAC5687 EVM Parts List

Bill of Material For DAC5687					
Value	**Qty.**	**Part Number**	**Vendor**	**Ref Des**	**Not Installed**
CAPACITORS					
47 uF, tantalum, 10%, 10 V	6	10TPA47M	Sanyo	C53-C58	
10 uF, 10 V, 10% capacitor	12	GRM42X5R106K10	Murata	C24, C26-C28, C30-C32, C35, C37-C39, C41	
1 uF, 16 V, 10% capacitor	6	ECJ-3YB1C105K	Panasonic	C36, C42-C46	
0.1 uF, 16 V, 10% capacitor	3	ECJ-2VB1C104K	Panasonic	C21, C22, C23	
0.01 uF, 50 V, 5% capacitor	6	ECJ-2VB1H103K	Panasonic	C47-C52	
0.01 uF, 16 V, 10% capacitor	2	ECJ-1VB1C103K	Panasonic	C19, C20	
0.1 uF, 16 V, 10% capacitor	4	ECJ-1VB1C104K	Panasonic	C25, C40, C60, C61	
0.1 uF, 16 V, +80/-20% capacitor	21	ECJ-0EF1C104Z	Panasonic	C1 C2 C4-C13, C15-C18, C29, C59, C84-C86	
0.01 uF, 25 V, 10% capacitor	1	ECJ-0EF1E103Z	Panasonic	C14	
0.033 uF, 25 V, +80/-20% capacitor	1	ECU-E1C333ZFQ	Panasonic	C34	
10 pF, 50 V, 5% capacitor	1	ECU-E1H100DCQ	Panasonic	C3	
330 pF, 50 V, 5% capacitor	1	ECU-V1H331JCV	Panasonic	C33	
RESISTORS					
10-kΩ resistor 1/16 W, 1%	4	ERJ-6ENF1002V	Panasonic	R34-R37	
10-Ω resistor 1/16 W, 1%	1	ERJ-6ENF10R0V	Panasonic	R3	R15
10-Ω resistor 1/16 W, 1%	1	ERJ-2RFK10R0X	Panasonic	R43	
0-Ω resistor, 1/16 W, 1%	4	ERJ-3GEY0R00V	Panasonic	R23, R26, R38, R42	R6-R9, R24, R27-R33
49.9-Ω resistor, 1/16 W, 1%	3	ERJ-3EKF49R9V	Panasonic	R12, R13, R39	R40
110-Ω resistor, 1/10 W, 1%	0	ERA-3EKF110V	Panasonic		R18
200-Ω resistor, 1/16 W, 1%	2	ERJ-3EKF200V	Panasonic	R11, R14	
93.1-Ω resistor, 1/16 W, 1%	1	ERJ-3EKF93R1V	Panasonic	R25	
1-kΩ resistor, 1/16 W, 1%	2	ERJ-3EKF1001V	Panasonic	R1, R4	
221-Ω resistor, 1/10 W, 1%	0	ERA-3EKF221V	Panasonic		R17
22.1-Ω resistor, 1/10 W, 1%	2	ERJ-3EKF22R1V	Panasonic	R2, R16	
100-Ω resistor, 1/10 W, 1%	4	ERA-3EKF100V	Panasonic	R5, R10, R19, R20	R21, R22, R41
Surface mount socket strips	4	310-93-164-41-105000	Mill-Max	RP5, RP6, RP9, RP10	
51-Ω resistor pack	0	770-101-R51	CTS		RP5, RP6, RP9, RP10
22-Ω resistor pack	4	4816P-001-220	BOURNS	RP1-RP4	
FERRITE BEADS, CONNECTORS, JUMPERS, JACKS, ICs, etc.					
Ferrite bead	6	EXC-ML32A680U		FB1-FB6	
Diode	2	MBRB2515LT4	On-Semiconducter	D1, D2	
SMA connectors	8	713-4339 (901-144-8RFX)	Allied	J2-J6, J11, J18, J19	
Red test point	1	5010K	Keystone	TP6	
Black test point	4	5011K	Keystone	TP2-TP5	
3POS_header	3	TSW-150-07-L-S	Samtec	W1-W3	
30-pin header	1	TSW-120-07-L-T	Samtec	J15	
34-pin header	2	TSW-117-01-S-DV-LC	Samtec	J13, J14	
Red banana jacks	2	ST-351A	Allied	J7, J8	
Black banana jacks	2	ST-351B	Allied	J9, J10	
DAC5687	1	DAC5687IPZP	TI	U1	
CDCV304	1	CDCV304PW	TI	U5	
SN74HC241	1	SN74HC241DW	TI	U4	
SN74HCT14	2	SN74HCT14PWR	TI	U2, U3	
Transformer	2	T4-1-KK8	Mini-circuits	T1, T2	
Transformer	2	TCM4-1W	Mini-circuits	T3, T4	
Transformer	1	T1-6T-KK81	Mini-circuits	T5	
DB25F-RA	1	745536-2	AMP	J1	
Switch	1	EVQ-PJX04M	Panasonic	S1	

4 Circuit Description

This chapter describes the circuit functions of the DAC5687 EVM.

4.1 Input Clocks

The initial configuration of this EVM provides transformer-coupled differential clocks from single-ended input sources. With the EVM configured for PLL clock mode, a 1-V_{PP}, 0-V offset, 50% duty cycle external square wave is applied to SMA connector J3 to be used as the data input rate clock. The signal is converted to a differential clock by transformer T3 and provides the CLK1 and CLK1C inputs to the DAC5687 device. This input represents a 50-Ω load to the source. In order to preserve the specified performance of the DAC5687 converter, the clock source should feature very low jitter. Using a clock with a 50% duty cycle gives optimum dynamic performance.

With the EVM configured for external clock mode, a 1-V_{PP}, 0-V offset, 50% duty cycle external square wave is applied to SMA connector J4 to be used as the DAC sample clock. The signal is converted to a differential clock by transformer T4 and provides the CLK2 and CLK2C inputs to the DAC5687 device. This input represents a 50-Ω load to the source. In order to preserve the specified performance of the DAC5687 converter, the clock source should feature low jitter. Using a clock with a 50% duty cycle gives optimum dynamic performance.

4.2 Input Data

The DAC5687 EVM can accept 1.8-V or 3.3-V CMOS logic level data inputs through the 34-pin headers J13 and J14 per Table 2 and Table 3. The board provides options for 50-Ω termination to ground and series dampening resistors to minimize digital ringing and switching noise. Jumper W2 determines which voltage level is to be used for the logic inputs.

Table 2. Input Connector J13 (Data A Bus)

Pin	Description	Pin	Description
1	CMOS data bit 15 (MSB)	18	GND
2	GND	19	CMOS data bit 6
3	CMOS data bit 14	20	GND
4	GND	21	CMOS data bit 5
5	CMOS data bit 13	22	GND
6	GND	23	CMOS data bit 4
7	CMOS data bit 12	24	GND
8	GND	25	CMOS data bit 3
9	CMOS data bit 11	26	GND
10	GND	27	CMOS data bit 2
11	CMOS data bit 10	28	GND
12	GND	29	CMOS data bit 1
13	CMOS data bit 9	30	GND
14	GND	31	CMOS data bit 0 (LSB)
15	CMOS data bit 8	32	GND
16	GND	33	
17	CMOS data bit 7	34	GND

Table 3. Input Connector J14 (Data B Bus)

Pin	Description	Pin	Description
1	CMOS data bit 0 (LSB)	18	GND
2	GND	19	CMOS data bit 9
3	CMOS data bit 1	20	GND
4	GND	21	CMOS data bit 10
5	CMOS data bit 2	22	GND
6	GND	23	CMOS data bit 11
7	CMOS data bit 3	24	GND
8	GND	25	CMOS data bit 12
9	CMOS data bit 4	26	GND
10	GND	27	CMOS data bit 13
11	CMOS data bit 5	28	GND
12	GND	29	CMOS data bit 14
13	CMOS data bit 6	30	GND
14	GND	31	CMOS data bit 15 (MSB)
15	CMOS data bit 7	32	GND
16	GND	33	
17	CMOS data bit 8	34	GND

4.3 Output Data

The DAC5687 EVM can be configured to drive a doubly terminated 50-Ω cable or provide unbuffered differential outputs.

4.3.1 Transformer-Coupled Signal Output

The factory-set configuration of the demonstration board provides the user with single-ended output signals at SMA connectors J5 and J19. The DAC5687 outputs are configured to drive a doubly terminated 50-Ω cable using a 4:1 impedance ratio transformer with the center tap of the transformers connected to +3.3 VA as shown in Table 4. When using a 1:1 impedance ratio transformer, configure the EVM as shown in Table 4. The common mode input voltage of T1 and T2 can be adjusted by using the resistor divider networks. With the board configured to use transformer T5 per Table 4, the DAC outputs will be summed together and provide 40-mA full-scale output power at SMA connector J11.

Table 4. Transformer Output Configuration

Configuration	Components Installed (1)	Components Not Installed
1:1 Impedance ratio transformer	R5 (49.9), R10 (49.9), R19 (49.9), R20 (49.9), R21, R22, R23, R26, C60, C61, T1(1:1), T2 (1:1)	R6-R9, R24, R27-R33
4:1 Impedance ratio transformer	R5, R10, R19, R20, R23, R26, C60, C61, T1(4:1), T2 (4:1)	R6-R9, R21, R22, R24, R27-R33
Combined Output through 1:1 Impedance ratio Transformer	R6-R9, R42, C40, T5	R5, R10, R19-R22, R27-R33, R41, T1, T2

(1) All component values are per the schematic except where shown in parenthesis.

4.3.2 Unbuffered Differential Output

To provide unbuffered differential outputs, the EVM must be configured as follows: remove R6-R9, R21, R22, T1, and T2; install R5 (24.9), R10 (24.9), R19 (24.9), R20 (24.9), R24, R27-R30, and R32. With a 20 mA full-scale output current, this configuration will provide a 0.5 Vpp output.

4.3.3 PLL Lock

With the internal PLL enabled (W3 installed between pins 1 and 2), when the PLL is locked to the CLK1 input, PLLOCK OUT (J2) is driven high. With the internal PLL disabled, the PLLLOCK OUT is an output clock that can be used by external devices to clock the input data to the DAC5687. This signal is the CLK2 signal divided down by the interpolation rate and phase-aligned to allow the user to clock data into the DAC5687 with the required setup and hold times.

4.4 Control Inputs

The DAC5687 device has five discrete inputs to control the operation of the device.

4.4.1 Sleep Mode

The DAC5687 EVM provides a means of placing the DAC5687 device into a power-down mode. This mode is activated by placing a jumper between pins 5 and 6 on header J15.

4.4.2 Reset

The DAC5687 EVM provides a means of resetting the DAC5687 device. Pressing switch S1 or sending J15 pin 29 low provides an active low reset signal to the DAC5687 device.

4.4.3 Phase Synchronization

The DAC5687 EVM provides a means to phase synchronize the DAC5687 device. Placing an active high signal on J15 pin 8 (PHSTR) resets the internal NCO accumulator register.

4.4.4 TxENABLE

TxENABLE must be high to enable the DAC5687 to process data. When low, the DAC5687 device is forced to a constant dc output at IOUTA and IOUTB. When in the interleaved mode and MEM_QFLAG bit is set to 0, TxENABLE syncronizes the data of channels A and B. When TxENABLE goes high, data present at the next clock rising edge is treated as I data. The next valid data is then treated as Q data and so on. TxENABLE is controlled by J15 pin 11.

4.4.5 QFLAG

QFLAG is an input used to indicate Q sample data during the interleaved mode when the QFLAG interleave bit (3) is set in register #9, MEM_QFLAG. When QFLAG is high, input data is treated as Q data, and when low, data is treated as I data. QFLAG is controlled by J15 pin 14.

4.5 Internal Reference Operation

The full-scale output current is set by applying an external resistor (R1) between the BIASJ pin of the DAC5687 device and ground. The full-scale output current can be adjusted from 20 mA down to 2 mA by varying R1 or changing the externally applied reference voltage. The full-scale output current, IOUTFS, is defined as follows:

$$IOUT_{FS} = 16 \times \left(\frac{V_{EXTIO}}{R1} \right)$$

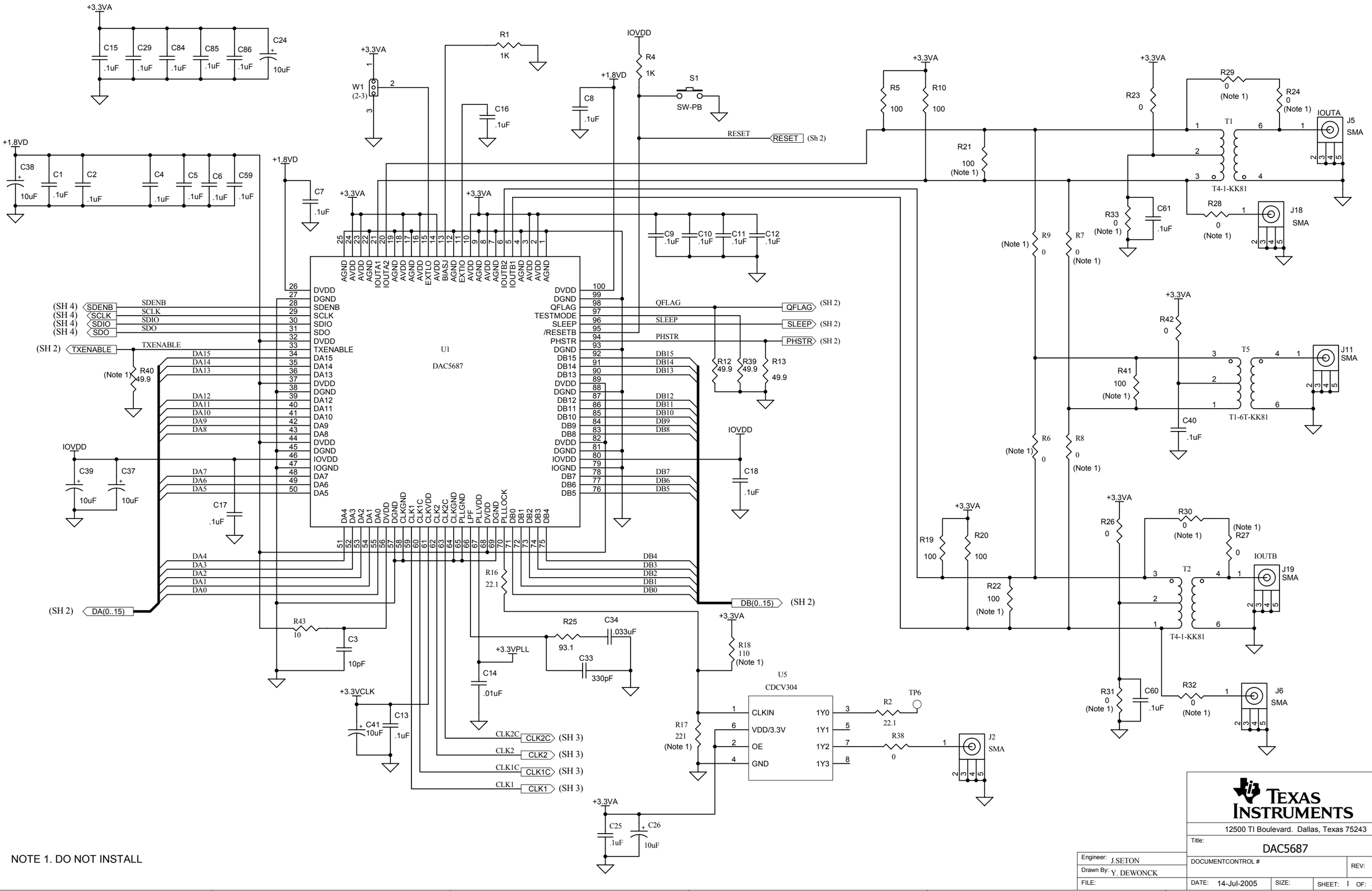
where VEXTIO is the voltage at pin EXTIO. This voltage is 1.2 V typical when using the internally provided bandgap reference voltage source.

4.6 External Reference Operation

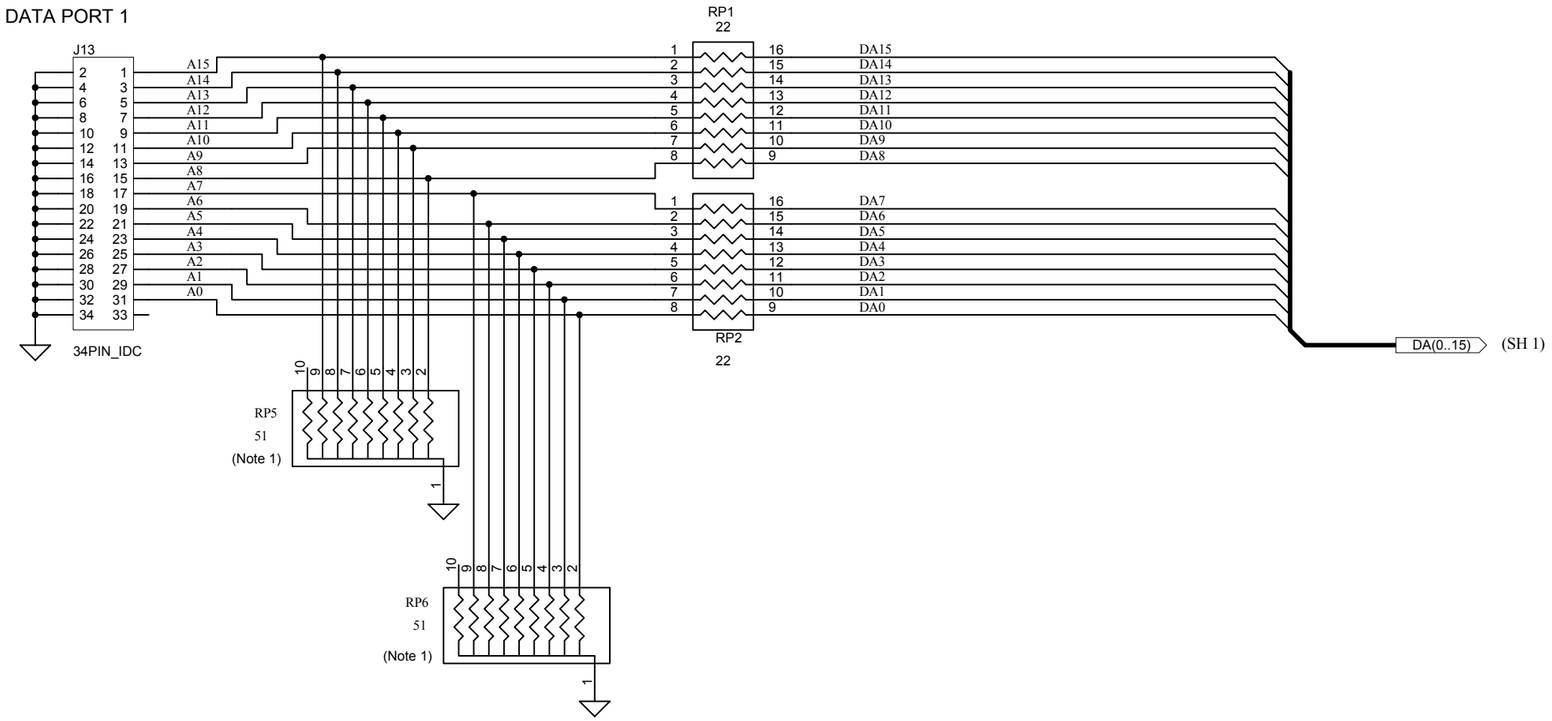
The internal reference can be disabled and overridden by an external reference by connecting a voltage source to EXTI/O and connecting EXTLO to +3.3VA (jumper W1 installed between pins 1 and 2). The specified range for external reference voltages must be observed (see the DAC5687 data sheet (SLWS164) for details).

5 Schematics

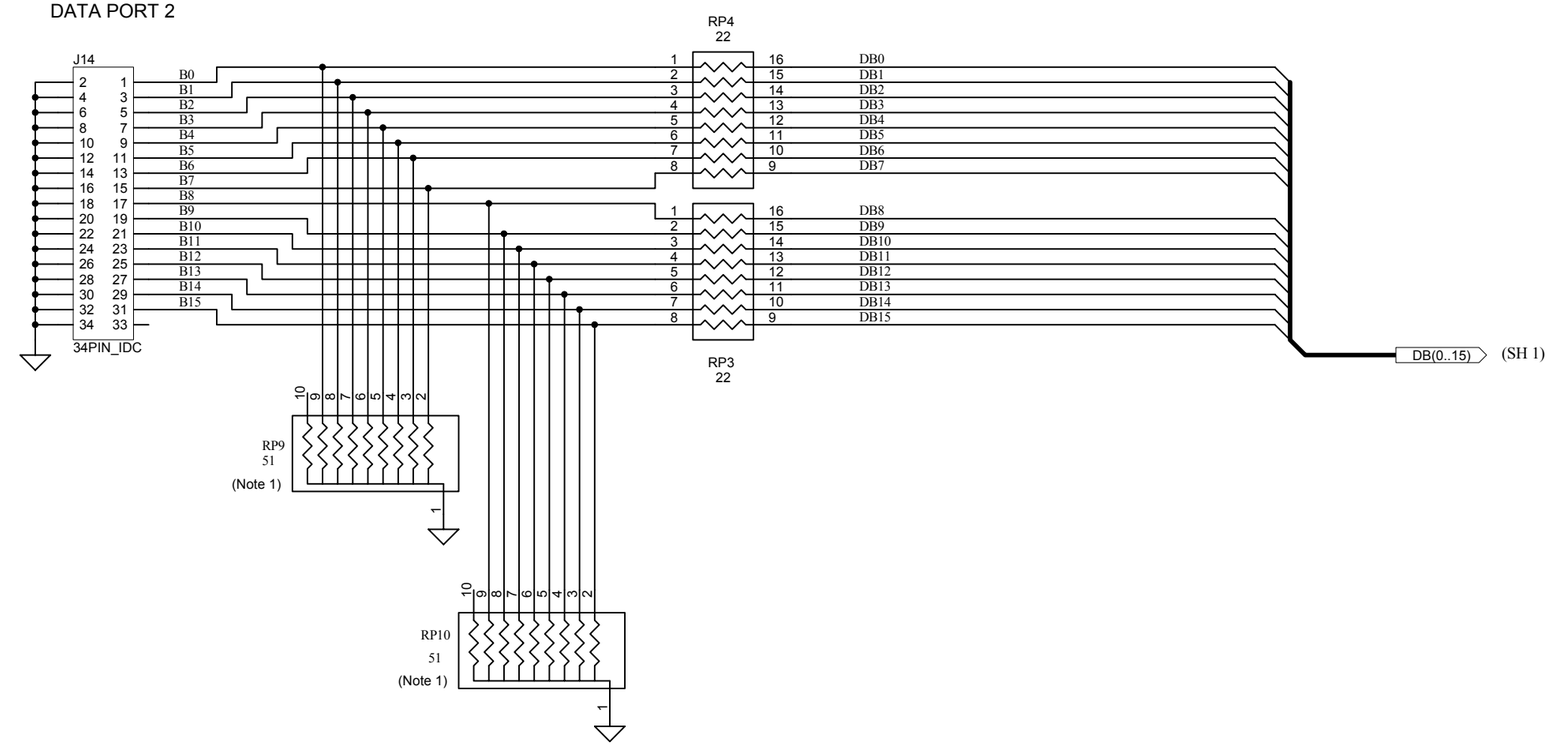
This chapter contains the DAC5687 EVM schematic diagrams.

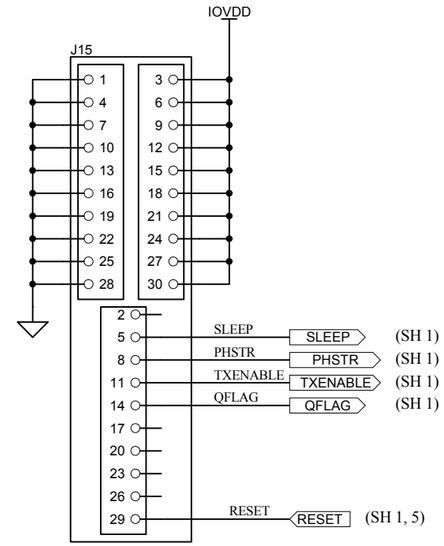

U1
DAC5687
U5
CDCV304
T1
T2
T5
T4-1-KK81
T1-6T-KK81
SW-PB
RESET
(SH 2)
(SH 3)
(SH 4)
DA(0..15)
DB(0..15)
SDENB
SCLK
SDIO
SDO
TXENABLE
QFLAG
SLEEP
PHSTR
CLK2C
CLK2
CLK1C
CLK1
IOUTA
IOUTB
(Note 1)
NOTE 1. DO NOT INSTALL
TEXAS INSTRUMENTS
12500 TI Boulevard. Dallas, Texas 75243
Title: DAC5687
Engineer: J.SETON
Drawn By: Y. DEWONCK
FILE:
DOCUMENTCONTROL #
REV: B
DATE: 14-Jul-2005
SIZE:
SHEET: 1 OF: 5

DATA PORT 1



DATA PORT 2





3 ROW 30 PIN CONNECTOR

NOTE 1. DO NOT INSTALL

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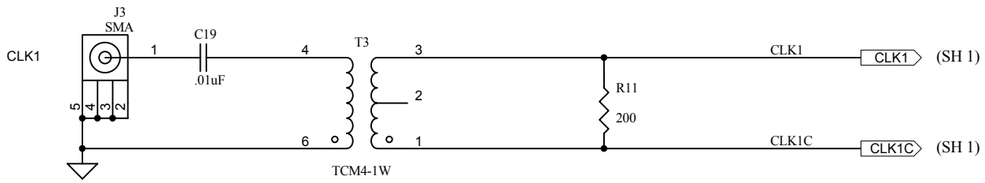

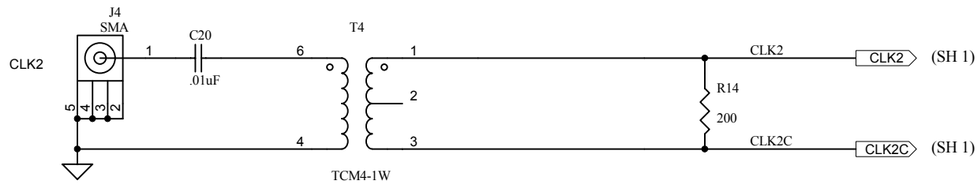

NOTES:
1. PART NOT INSTALLED

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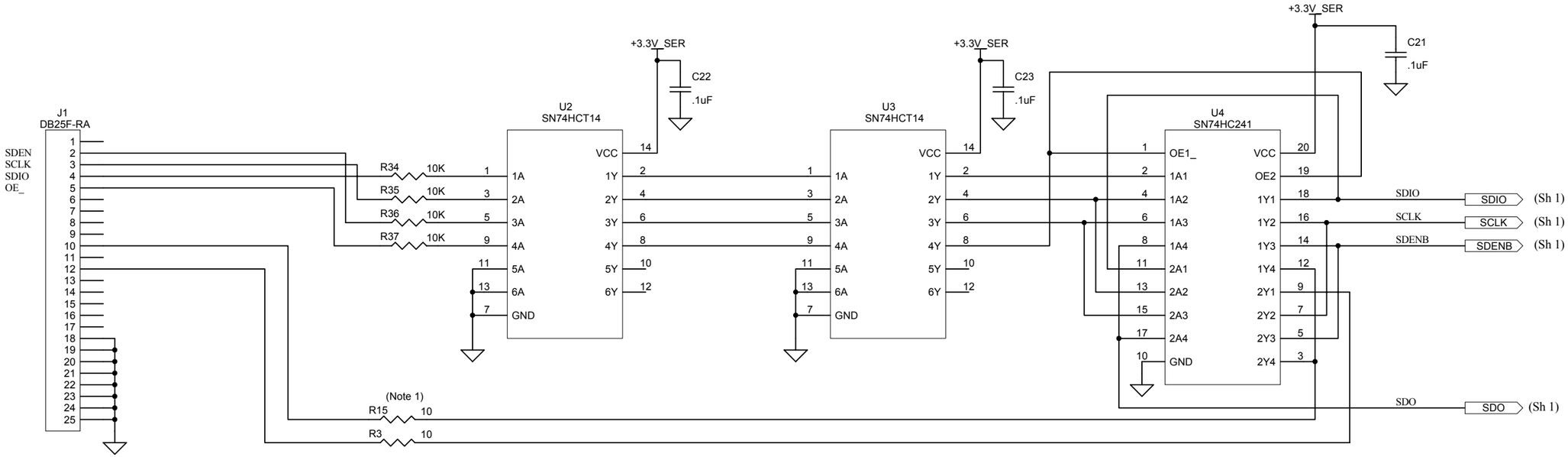
Drawn By: Y. DEWONCK	12500 TI Boulevard. Dallas, Texas 75243		
FILE:	Title: DAC5687		
	DOCUMENTCONTROL #		REV: B
	DATE: 14-Jul-2005	SIZE:	SHEET: 3 OF: 5



NOTE 1. DO NOT INSTALL

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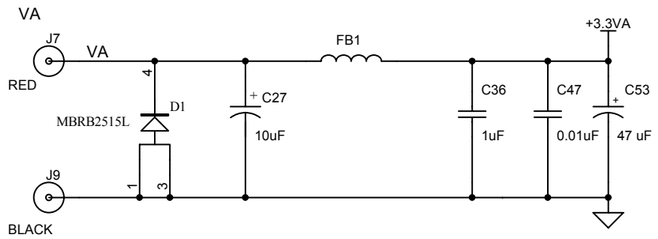
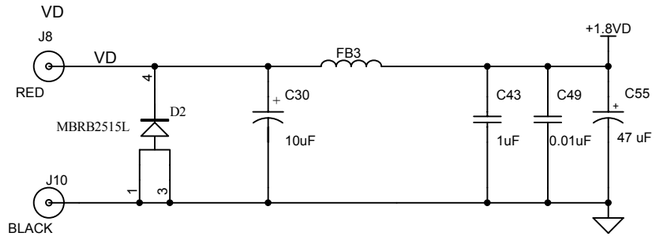
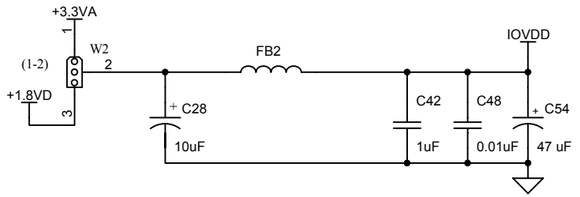
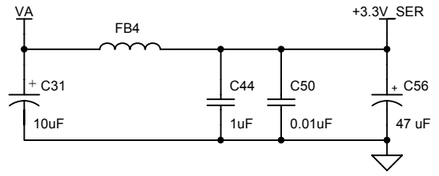
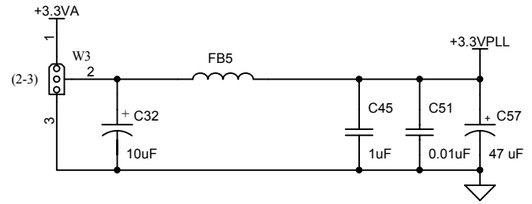
Drawn By: Y. DEWONCK	12500 TI Boulevard. Dallas, Texas 75243		
FILE:	Title: DAC5687		
	DOCUMENTCONTROL #		REV: B
	DATE: 14-Jul-2005	SIZE:	SHEET: 4 OF: 5

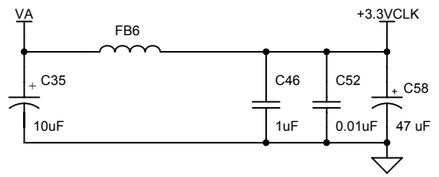


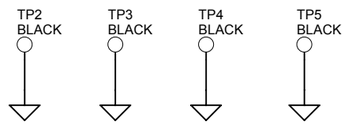












NOTES:
1. PART NOT INSTALLED

TEXAS INSTRUMENTS
12500 TI Boulevard. Dallas, Texas 75243

Title: DAC5687			
Engineer: J. SETON	DOCUMENTCONTROL #		REV: B
Drawn By: Y. DEWONCK			
FILE:	DATE: 14-Jul-2005	SIZE:	SHEET: 5 OF: 5

Revision A History

Changes from Original (April 2005) to A Revision **Page**

- Hardware Configuration Step 3: Changed input clock level from 300 mVpp to 1 Vpp. 5
- Changed Figure 1 - Updated to reflect new version of DAC5687 SPI software (V2.3). 9
- Changed Figure 2 - Updated to reflect new version of DAC5687 SPI software (V2.3). 10
- Changed Figure 3 - Updated to reflect new initial test setup. 11
- Changed Figure 4 - Updated to reflect new version of DAC5687 SPI software (V2.3). 12
- Changed the **PII Port Config:** description in Section 2.4.5 20

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision B History

Changes from A Revision (August 2005) to B Revision **Page**

- Changed Section 2 - DAC5687 EVM Operational Procedure. Added steps to prepare the DAC5687 EVM for operation. 6

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision C History

Changes from B Revision (March 2007) to C Revision **Page**

- Hardware Configuration Step 4: Added text "Another solution is to use the TSW1400 pattern generator .." 5
- Hardware Configuration Step 5: Added text "The user can also use the provided USB to SPI adapter .." 5
- Added text to Section 2.1 - "If you are using the USB interface card, change mode to USB in the upper right corner window." 9
- Changed Figure 1 9
- Changed Figure 2 10
- Changed Figure 3 11
- Changed Figure 4 12
- Added Section 2.3 - Basic Test Procedure with TSW1400 12
- Added F_{DAC}: to Section 2.4.4 20
- Added NCO IF: to Section 2.4.4 20

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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REGULATORY COMPLIANCE INFORMATION

As noted in the EVM User's Guide and/or EVM itself, this EVM and/or accompanying hardware may or may not be subject to the Federal Communications Commission (FCC) and Industry Canada (IC) rules.

For EVMs **not** subject to the above rules, this evaluation board/kit/module is intended for use for ENGINEERING DEVELOPMENT, DEMONSTRATION OR EVALUATION PURPOSES ONLY and is not considered by TI to be a finished end product fit for general consumer use. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC or ICES-003 rules, which are designed to provide reasonable protection against radio frequency interference. Operation of the equipment may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

General Statement for EVMs including a radio

User Power/Frequency Use Obligations: This radio is intended for development/professional use only in legally allocated frequency and power limits. Any use of radio frequencies and/or power availability of this EVM and its development application(s) must comply with local laws governing radio spectrum allocation and power limits for this evaluation module. It is the user's sole responsibility to only operate this radio in legally acceptable frequency space and within legally mandated power limitations. Any exceptions to this are strictly prohibited and unauthorized by Texas Instruments unless user has obtained appropriate experimental/development licenses from local regulatory authorities, which is responsibility of user including its acceptable authorization.

For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant

Caution

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

For EVMs annotated as IC – INDUSTRY CANADA Compliant

This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Concerning EVMs including radio transmitters

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concerning EVMs including detachable antennas

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada.

Les changements ou les modifications pas expressément approuvés par la partie responsable de la conformité ont pu vider l'autorité de l'utilisateur pour actionner l'équipement.

Concernant les EVMs avec appareils radio

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

【Important Notice for Users of EVMs for RF Products in Japan】

This development kit is NOT certified as Confirming to Technical Regulations of Radio Law of Japan

If you use this product in Japan, you are required by Radio Law of Japan to follow the instructions below with respect to this product:

1. Use this product in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use this product only after you obtained the license of Test Radio Station as provided in Radio Law of Japan with respect to this product, or
3. Use of this product only after you obtained the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to this product. Also, please do not transfer this product, unless you give the same notice above to the transferee. Please note that if you could not follow the instructions above, you will be subject to penalties of Radio Law of Japan.

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EVALUATION BOARD/KIT/MODULE (EVM)
WARNINGS, RESTRICTIONS AND DISCLAIMERS

For Feasibility Evaluation Only, in Laboratory/Development Environments. Unless otherwise indicated, this EVM is not a finished electrical equipment and not intended for consumer use. It is intended solely for use for preliminary feasibility evaluation in laboratory/development environments by technically qualified electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems and subsystems. It should not be used as all or part of a finished end product.

Your Sole Responsibility and Risk. You acknowledge, represent and agree that:

1. You have unique knowledge concerning Federal, State and local regulatory requirements (including but not limited to Food and Drug Administration regulations, if applicable) which relate to your products and which relate to your use (and/or that of your employees, affiliates, contractors or designees) of the EVM for evaluation, testing and other purposes.
2. You have full and exclusive responsibility to assure the safety and compliance of your products with all such laws and other applicable regulatory requirements, and also to assure the safety of any activities to be conducted by you and/or your employees, affiliates, contractors or designees, using the EVM. Further, you are responsible to assure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard.
3. Since the EVM is not a completed product, it may not meet all applicable regulatory and safety compliance standards (such as UL, CSA, VDE, CE, RoHS and WEEE) which may normally be associated with similar items. You assume full responsibility to determine and/or assure compliance with any such standards and related certifications as may be applicable. You will employ reasonable safeguards to ensure that your use of the EVM will not result in any property damage, injury or death, even if the EVM should fail to perform as described or expected.
4. You will take care of proper disposal and recycling of the EVM’s electronic components and packing materials.

Certain Instructions. It is important to operate this EVM within TI’s recommended specifications and environmental considerations per the user guidelines. Exceeding the specified EVM ratings (including but not limited to input and output voltage, current, power, and environmental ranges) may cause property damage, personal injury or death. If there are questions concerning these ratings please contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, some circuit components may have case temperatures greater than 60°C as long as the input and output are maintained at a normal ambient operating temperature. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors which can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during normal operation, please be aware that these devices may be very warm to the touch. As with all electronic evaluation tools, only qualified personnel knowledgeable in electronic measurement and diagnostics normally found in development environments should use these EVMs.

Agreement to Defend, Indemnify and Hold Harmless. You agree to defend, indemnify and hold TI, its licensors and their representatives harmless from and against any and all claims, damages, losses, expenses, costs and liabilities (collectively, "Claims") arising out of or in connection with any use of the EVM that is not in accordance with the terms of the agreement. This obligation shall apply whether Claims arise under law of tort or contract or any other legal theory, and even if the EVM fails to perform as described or expected.

Safety-Critical or Life-Critical Applications. If you intend to evaluate the components for possible use in safety critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, such as devices which are classified as FDA Class III or similar classification, then you must specifically notify TI of such intent and enter into a separate Assurance and Indemnity Agreement.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

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No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

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