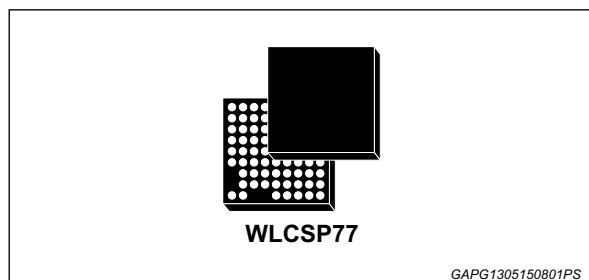


**GPS/Glonass/BeiDou2/QZSS ROM receiver****Datasheet - production data**

- IO ring voltage ( $V_{ddIO}$ ): 1.8 V  $\pm$  5 % or 3.3 V  $\pm$  10 %
- Package:
  - WLCSP77 (3.861 x 3.843 x 0.6 mm) 0.4 pitch
- Packing in Tape and Reel
- Ambient temperature range: -40/ +85 °C

**Features**

- STMicroelectronics® positioning receiver with 48 tracking channels and 2 fast acquisition channels supporting GPS, GLONASS, BeiDou and QZSS systems
- Single die standalone receiver embedding RF Front-End and low noise amplifier
- -163 dBm tracking sensitivity
- Fast TTFF < 1 s in Hot start and 30 s in Cold Start
- High performance ARM946 MCU (upto 196 MHz)
- 256 Kbyte embedded SRAM
- 8 free running timers/ counters (32 bit)
- Real Time Clock (RTC) circuit
- 32-bit Watch-dog timer
- 3 UARTs
- 1 I<sup>2</sup>C master interface
- 1 Synchronous Serial Port (SSP, Motorola-SPI supported)
- Power Management Unit (PMU) embedding switching regulator
- Operating condition:
  - Main voltage regulator ( $V_{INL}$ ): 1.6 V to 4.3 V
  - Backup voltage ( $V_{INB}$ ): 1.6 V to 4.3 V
  - Digital voltage ( $V_{DD}$ ): 1.0 V to 1.32 V
  - RF core voltage ( $V_{CC}$ ): 1.2 V  $\pm$  10 %

**Description**

STA8090WGR belongs to Teseo III family products.

STA8090WGR is a single die standalone positioning receiver which embeds the new ST GNSS positioning engine capable of receiving signals from multiple satellite navigation systems, including GPS, Glonass, BeiDou QZSS.

The minimum BOM and small WL-CSP package make STA8090WGR the ideal solution for low-cost and small footprint products such as hand-held computers, cameras, data loggers, and sports accessories.

The device is offered with a complete GNSS firmware which performs all GNSS operations including tracking, acquisition, navigation and data output.

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# 1 Overview

STA8090WGR is one of the part number of Teseo III STA8090x series.

STA8090WGR is a highly integrated System-On-Chip GNSS receiver designed for high-flexible and cost effective solution addressing hand-held, in-dash navigation and Telematics applications.

STA8090WGR embeds the new ST GNSS positioning engine capable of receiving signals from multiple satellite navigation systems, including the US GPS, Russia's GLONASS, Chinese BeiDou and Japan's QZSS.

The STA8090WGR ability of tracking simultaneously the signals from multiple satellites regardless of their constellation, makes this chip capable of delivering exceptional accuracy in urban canyons and in the environments where buildings and other obstructions make satellite visibility challenging.

STA8090WGR embeds innovative power management unit with switching regulator for power consumption optimization.

The extended voltage supply range from 1.6 V to 4.3 V, the 1.8 V and 3.3 V I/O compliance support make the STA8090WGR the suitable solution for different user applications.

The STA8090WGR combines a high performance ARM946 microprocessor with I/O capabilities and enhanced peripherals.

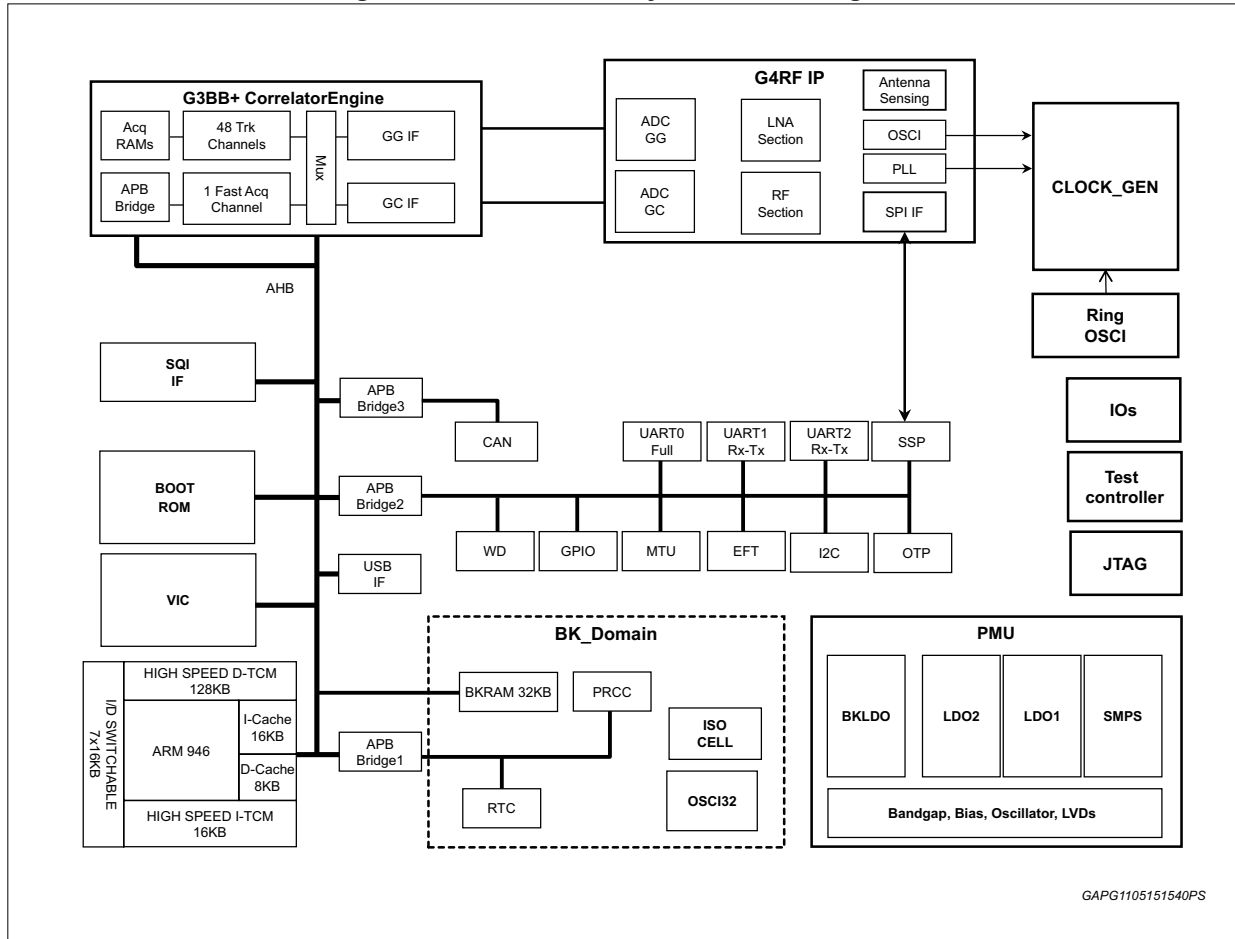
The chip embeds backup logic with real time clock.

The STA8090WGR, using STMicroelectronics CMOSRF Technology, is housed in a WLCSP77 (3.861 x 3.843 x 0.6 mm) 0.4 pitch with a Tape and Reel packing.

## 2 Pin description

### 2.1 Block diagram

Figure 1. STA8090WGR system block diagram



## 2.2 WLCSP 77 ball out

Figure 2. WLCSP 77 ball out diagram (bottom view)

	9	8	7	6	5	4	3	2	1	
A	I2C_SD	TDO	USB_DM	VOM	VDD_ANA	GND_ANA	VLX	GND_POWER	VINM	A
B	VDDIO_r2	I2C_SD	TDI	SPI_CLK	SPI_DI	SPI_DO	GND_ANA	VINM	SPI_CSN	B
C	I2C_CLK	TCK	GND_IO+GNDD	USB_DP	GND_IO+GNDD	UART0_TX	UART2_TX	UART0_RX	VDDIO_r1	C
D	Tsense	TRSTn	TMS	GND_IO+GNDD	GND_IO+GNDD	VDDD	UART2_RX	GPIO_0	GPIO_1	D
E	VCC_LNA	TP_IF_P	TP_IF_N	ANT_SENSE2	GND_IO+GNDD	GND_IO+GNDD	SQI_SIO0/SI	SQI_SIO3	SQI_CLK	E
F	GND_LNA	GND_LNA	VCC_RFA	ANT_SENSE1	GND_RF	WAKEUP	SQI_Cen	SQI_SIO2	SQI_SIO1/SO	F
G		LNA_IN	GND_LNA	VINL2	GND_RF	RSTn	GND_HM2	VINL1	HV	G
H		GND_RF	V0L2	GND_RF	XTAL_OUT	STDBY_Out	RTC_XTI	VINB	VOL1	H
J	GND_RF	VCC_CHAIN_PLL			XTAL_IN	STDBYn	VOB	RTC_XTO	VINB	J
	9	8	7	6	5	4	3	2	1	

GADG0606161348MAG

## 2.3 Power supply pins

Table 1. Power supply pins

Name	I/O voltage	I/O	Description	Pin #
VCC_CHAIN_PLL	1.2 V	PWR	Analog supply voltage for RF chain and PLL (1.2 V)	J8
VCC_RFA	1.2 V	PWR	Analog supply voltage for RF (1.2 V)	F7
VCC_LNA	1.2 V	PWR	Analog supply voltage for LNA (1.2 V)	E9



**Table 1. Power supply pins (continued)**

Name	I/O voltage	I/O	Description	Pin #
VDDD	1.2 V	PWR	Digital supply voltage	D4
VDDIO_r1	1.8 V or 3.3 V	PWR	Digital supply voltage for I/O ring 1 (1.8 V or 3.3 V)	C1
VDDIO_r2	3.3 V	PWR	Digital supply voltage for I/O ring 2 (3.3 V)	B9
VINB	1.6 V - 4.3 V	PWR	Backup LDO input supply voltage (1.6 V to 4.3 V)	H2, J1
VINL1	1.6 V - 4.3 V	PWR	LDO1 input supply voltage (1.6 V to 4.3 V)	G2
VINL2	1.6 V - 4.3 V	PWR	LDO2 input supply voltage (1.6 V to 4.3 V)	G6
VINM	1.6 V - 4.3 V	PWR	SMPS coil input supply (1.6 V to 4.3 V)	A1, B2
VDD_ANA	1.6 V - 4.3 V	PWR	SMPS input supply (1.6 V to 4.3 V)	A5
VLX	0 V - 4.3 V	PWR	SMPS coil output	A3
VOB	1.0 V	PWR	LDO backup output voltage (1.0 V)	J3
VOL1	1.2 V or 1.8 V	PWR	LDO1 output voltage (1.8 V)	H1
VOL2	1.2 V	PWR	LDO2 output voltage (1.2 V)	H7
VOM	1.2 V or 1.8 V	PWR	SMPS output voltage (1.2 V)	A6
GND_RF	GND	GND	Ground	F5, G5, H8, H6, J9
GND_LNA	GND	GND	Ground	F9, F8, G7
GND_IO+GNDD	GND	GND	Ground	C5, C7, D5, D6, E4, E5
GND_ANA	GND	GND	Ground	A4, B3
GND_POWER	GND	GND	Ground	A2
GND_HM2	GND	GND	Ground	G3

## 2.4 Main function pins

**Table 2. Main function pins**

Name	I/O voltage	I/O	Description	Pin #
RSTn	1.0 V	I	Reset Input with Schmitt-Trigger characteristics and noise filter.	G4
RTC_XTI	1.0 V (max)	I	Input of the 32 kHz oscillator amplifier circuit and input of the internal real time clock circuit.	H3
RTC_XTO	1.0 V (max)	O	Output of the oscillator amplifier circuit.	J2
STDBY_OUT	1.0 V	O	When low, indicates the chip is in Standby mode	H4
STDBYn	1.0 V	I	When low, the chip is forced in Standby Mode - All pins in high impedance except the ones powered by Backup supply	J4
WAKEUP	1.0 V	I	WAKEUP from STANDBY mode	F4

## 2.5 Test / emulated dedicated pins

**Table 3. Test/emulated dedicated pins**

Name	I/O voltage	I/O	Description	Pin #
TCK	VDDIO_R2	I	JTAG Test Clock	C8
TDI	VDDIO_R2	I	JTAG Test Data In	B7
TDO	VDDIO_R2	O	JTAG Test Data Out	A8
TMS	VDDIO_R2	I	JTAG Test Mode Select	D7
TRSTn	VDDIO_R2	I	JTAG Test Circuit Reset	D8
TP_IF_N	1.2 V	O	Diff.Test Point for IF — Neg.	E7
TP_IF_P	1.2 V	O	Diff.Test Point for IF — Pos.	E8

## 2.6 Reserved pins

**Table 4. Reserved pins**

Name	I/O voltage	I/O	Description	Pin #
SQI_Cen	VDD_SQI	O	Reserved	F3
SQI_CLK	VDD_SQI	O	Reserved	E1
SQI_SIO0/SI	VDD_SQI	I/O	Reserved	E3
SQI_SIO1/SO	VDD_SQI	I/O	Reserved	F1
SQI_SIO2	VDD_SQI	I/O	Reserved	F2
SQI_SIO3	VDD_SQI	I/O	Reserved	E2

## 2.7 Communication interface pins

Table 5. Communication interface pins

Name	I/O voltage	I/O	Alternative function	Function	Description	Pin #
I2C_CLK	VDDIO_R2	O	AF0	I2C_CLK	I2C clock	C9
		I/O	AF1 (default)	GPIO8	General purpose I/O #8	
		O	AF2	Reserved <sup>(1)</sup>	Reserved	
		O	AF3	SPI_CLK	SPI clock	
I2C_SD	VDDIO_R2	I/O	AF0	Reserved	Reserved	A9, B8
		I/O	AF1	i2s_out_sclk	MSP serial clock output	
		I	AF2	I2C_SD	I2C serial data	
		I/O	AF3 (default)	GPIO20	General purpose I/O #20	
SPI_CLK	VDDIO_R1	O	AF0 (default)	SPI_CLK	SPI clock	B6
		I/O	AF1	GPIO25	General purpose I/O #25	
		O	AF2	Reserved	Reserved	
		O	AF3	Reserved	Reserved	
SPI_CSN	VDDIO_R1	O	AF0 (default)	SPI_CSN	SPI chip select active low / IO_Power Sel Ring 1	B1
		I/O	AF1	GPIO24	General purpose I/O #24	
		I/O	AF2	Reserved	Reserved	
		I/O	AF3	Reserved	Reserved	
SPI_DI	VDDIO_R1	I	AF0 (default)	SPI_DI	SPI serial data input / BOOT2	B5
		I/O	AF1	Tsense	External temperature capture port	
		I/O	AF2	SQI_SIO1/SO	SQI Flash data IO 1 / ser. 0	
		I/O	AF3	MMC_D0	Multimedia card data 0	
SPI_DO	VDDIO_R1	O	AF0 (default)	SPI_DO	SPI serial data output	B4
		I/O	AF1	GPIO27	General purpose I/O #27	
		I/O	AF2	Reserved	Reserved	
		I/O	AF3	Reserved	Reserved	
Tsense	VDDIO_R2	I	AF0 (default)	Reserved	Reserved	D9
		I	AF1	Reserved	Reserved	
		I	AF2	Reserved	Reserved	
		I	AF3	Tsense	External temperature capture port	

Table 5. Communication interface pins (continued)

Name	I/O voltage	I/O	Alternative function	Function	Description	Pin #
UART0_RX	VDDIO_R1	I	AF0 (default)	UART0_RX	UART0 Rx data	C2
		O	AF1	SPI_DO	SPI serial data output	
		I/O	AF2	Reserved	Reserved	
		I	AF3	Timer_ICAPA	Extended Function Timer - Input Capture A	
UART0_TX	VDDIO_R1	O	AF0 (default)	UART0_TX	UART0 Tx data / BOOT1	C4
		I	AF1	SPI_DI	SPI serial data input	
		I/O	AF2	Reserved	Reserved	
		O	AF3	Timer_OCMPA	Extended Function Timer – Output Compare A	
UART2_RX	VDDIO_R1	I	AF0 (default)	UART2_RX	UART 2 Rx data	D3
		I/O	AF1	GPIO28	General purpose I/O #28	
		I/O	AF2	I2C_SD	I2C serial data	
		I/O	AF3	Reserved	Reserved	
UART2_TX	VDDIO_R1	O	AF0 (default)	UART2_TX	UART 2 Tx data / BOOT0	C3
		I/O	AF1	GPIO29	General purpose I/O #29	
		O	AF2	I2C_CLK	I2C clock	
		I/O	AF3	Reserved	Reserved	
USB_DM	VDDIO_R2	USB	AF0	Reserved	Reserved	A7
		I	AF1	UART1_RX	UART1 Rx data	
		I	AF2	Reserved <sup>(1)</sup>	Reserved	
		I/O	AF3 (default)	I2C_SD	I2C serial data	
USB_DP	VDDIO_R2	USB	AF0	Reserved	Reserved	C6
		O	AF1	UART1_TX	UART1 Tx data	
		O	AF2	Reserved <sup>(1)</sup>	Reserved	
		O	AF3 (default)	I2C_CLK	I2C clock	

1. Only for STA8090WGRBD.

## 2.8 General purpose pins

**Table 6. General purpose pins**

Name	I/O voltage	I/O	Alternative function	Function	Description	Pin #
GPIO0	VDDIO_R1	I/O	AF0 (default)	GPIO0	General purpose I/O #0	D2
		I	AF1	PPS_IN	Pulse per second input	
		O	AF2	Timer_OCMPB	Extended Function Timer – Output Compare B	
		O	AF3	Mag_0 GC	GLONASS and BeiDou 3-bit coding Output (MAG0)	
GPIO1	VDDIO_R1	I/O	AF0 (default)	GPIO1	General purpose I/O #1 / BOOT3	D1
		I	AF1	Reserved	Reserved	
		O	AF2	PPS_OUT	Pulse per second output	
		I/O	AF3	Tsense	External temperature capture port	

## 2.9 RF front-end pins

**Table 7. RF front-end pins**

Name	I/O voltage	I/O	Description	Pin #
LNA_IN	1.2 V	I	Low Noise Amplifier Input	G8
XTAL_IN	1.2 V	I	Input Side of Crystal Oscillator or TCXO Input	J5
XTAL_OUT	1.2 V	O	Output Side of Crystal Oscillator	H5

## 3 General description

### 3.1 RF front end

The RF front-end is able to down-convert the GPS signal from 1575.42 MHz to 4.092 MHz (4 F<sub>o</sub>, being F<sub>0</sub> = 1.023 MHz), the GLONASS signal from 1601.718 MHz to 8.57 MHz and the BeiDou signal from 1561.098 MHz to 10.23 MHz.

It embeds high performance LNA minimizing external component count and a LDO to supply the internal core facilitating requirements for external power supply. A three-bit ADC converts the IF signals to sign (SIGN) and magnitude (MAG0 and MAG1). They can be sampled or not by SPI. The magnitude bits are internally integrated in order to control the variable gain amplifiers. The VGA gain can be also set by the SPI interface.

The RF tuner accepts a wide range of reference clocks (10 to 52 MHz) and can generate 64 F<sub>o</sub> sampling clock for the baseband and 192 F<sub>o</sub> clock for MCU subsystem.

### 3.2 GPS/GLONASS/BeiDou Base Band (G3BB+) processor

STA8090WGR integrates G3BB+ proprietary IP, which is the ST last generation high-sensitivity Baseband processor fully compliant with GPS, GLONASS and BeiDou systems.

The baseband receives, from the embedded RF Front-End, two separate IF signals coded in sign-magnitude digital format on 3 bits and the related clocks. The GPS and GLONASS/BeiDou (GNSCOM) signals at the base band inputs are centered on 4.092 MHz, 8.57 MHz and 10.23 MHz.

The baseband processes the two IF signals performing data codification, sample rate conversion and final frequency conversion to zero IF before acquisition and tracking correlations.

The baseband processor has the capability of acquiring and tracking the GPS, GLONASS and BeiDou signals in a simultaneous or single way, or a combination of three, being GLONASS and BeiDou mutually exclusive. The number of tracking channels to be used is programmable; the not used tracking channels can be powered down.

A complete multi-OS software library is provided by ST to handle GPS processing, managing satellite acquisition, tracking, pseudo-range calculation and positioning, generating the output in the standard NMEA message format. The library includes support server-based ephemeris extension.

### 3.3 MCU Subsystem

The implemented sub-system includes an AHB Lite bus matrix.

An ARM946 core is embedded in the sub-system and masters the AHB bus. The totally available TCM SRAM is 256 KB. The amount of memory on ITCM and DTCM can be configured by the ARM946 (see [Table 8: TCM Configuration](#)). ITCM can be configured as N<sub>i</sub> x 16 KB; DTCM can be configured as 128 + N<sub>d</sub> x 16 KB, where N<sub>i</sub> + N<sub>d</sub> = 8, N<sub>i</sub> ≥ 1.

Table 8. TCM Configuration

TCMcfg [2]	TCMcfg [1]	TCMcfg [0]	ITCM	DTCM
0	0	0	16 KB	240 KB
0	0	1	32 KB	224 KB
0	1	0	48 KB	208 KB
0	1	1	64 KB	192 KB
1	0	0	80 KB	176 KB
1	0	1	96 KB	160 KB
1	1	0	112 KB	144 KB
1	1	1	128 KB	128 KB

### 3.3.1 AHB slaves

- G3 APB port that allows to interface with the G3BB acquisition memory and control registers
- 512 Kbytes ROM
- Vectored Interrupt Controller (VIC)
- SQI flash memory controller
- 3 x ARM946 APB peripheral bus (APB1, APB2, APB3)

#### Vectored Interrupt Controller (VIC)

This Vectored Interrupt Controller (VIC) allows the operative system interrupt handler to quickly dispatch interrupt service routines in response to peripheral interrupts. It provides a software interface to the interrupt system. There are up to 64 interrupt lines. The VIC uses a bit position for each different interrupt source.

The software can control each request line to generate software interrupts. Each interrupt line can be independently enabled and configured to trigger a non-vectored Normal Interrupt Request (IRQ) or Fast Interrupt Request (FIQ) to the ARM946 CPU. Sixteen interrupt lines can also be selected to trigger a vectored IRQ.

The VIC has two operation modes: the user mode and the privilege mode, in order to have the possibility to set (or not) one level of protection during execution.

## 3.4 APB peripherals

### 3.4.1 EFT

The Extended Function Timer (EFT) consists of a 16-bit counter driven by a programmable prescaler.

It may be used for a variety of purposes, including pulse length measurement of up to two input signals (input capture), generation of up to two output waveforms (output compare) and one PWM generation. Pulse lengths and waveform periods can be modulated from a very wide range using the timer prescaler.

### EFT features

- Programmable prescaler:  $f_{APB}$  divided from 1 to 256, prescaler register (0 to 255) value +1.
- Overflow status flag and maskable interrupts.
- Output compare functions with:
  - 2 dedicated 16-bit registers
  - 2 dedicated programmable signals
  - 2 dedicated status flags
  - 2 dedicated interrupt flags
- Input capture functions with:
  - 2 dedicated 16-bit registers
  - 2 dedicated active edge selection signals
  - 2 dedicated status flags
  - 2 dedicated interrupt flags
- Pulse Width Modulation mode (PWM).
- One Pulse Mode (OPM).
- PWM input mode.
- Timer global interrupt (5 internally ORed)
  - ICIA: timer input capture A interrupt
  - ICIB: timer input capture B interrupt
  - OCIA: timer output compare A interrupt
  - OCIB: timer output compare B interrupt
  - TOI: timer overflow interrupt

### 3.4.2 SSP

The SSP is a master interface for synchronous serial communication with peripheral devices that have Motorola SPI.

The SSP performs serial-to-parallel conversion on data received from a peripheral device on SPI\_DI pin, and parallel-to-serial conversion on data written by CPU for transmission on SPI\_DO pin. The transmit and receive paths are buffered with internal FIFO memories allowing up to 32 x 32-bit values to be stored independently in both transmit and receive modes. FIFOs may be burst-loaded or emptied by the system processor or DMA, from one to eight words per transfer. Each 32-bit word from the system fills one entry in FIFO.

The SSP includes a programmable bit rate clock divider and prescaler to generate the serial output clock SSPCLK from the on-chip clock. One combined interrupt is delivered, which is asserted from several internal maskable events.



### SSP features

The SSP has the following features:

- Parallel-to-serial conversion on data written to an internal 32-bit wide, 32-location deep transmit FIFO
- Serial-to-parallel conversion on received data, buffering it in a 32-bit wide, 32-location deep receive FIFO
- Programmable data frame size from 4 to 32-bit
- Programmable clock bit rate and prescaler
- Programmable clock phase and polarity in SPI mode

### 3.4.3 UART

The UARTx (x = 0|1|2) performs serial-to-parallel conversion on data asynchronously received from a peripheral device on UARTx\_RX pin, and parallel-to-serial conversion on data written by CPU for transmission on UARTx\_TX pin. The transmit and receive paths are buffered with internal FIFO memories allowing up to 64 data byte for transmission, and 64 data byte with 4-bit status (break, frame, parity, and overrun) for receive.

#### UART features

The UARTx (x = 0|1|2) are Universal Asynchronous Receiver/Transmitter that support much of the functionality of the industry-standard 16C650 UART. The main features are:

- Programmable baud rates up to  $\text{UARTCLK} / 16$  (1.5 Mbps with UARTCLK at 24 MHz), or up to  $\text{UARTCLK} / 8$  (3.0 Mbps with UARTCLK at 24 MHz), with fractional baud-rate generator
- 5, 6, 7 or 8-bit of data
- Even, odd, stick or no-parity bit generation and detection
- 1 or 2 stop bit generation
- Support of software flow control using programmable Xon/Xoff characters
- False start bit detection
- Line break generation and detection
- Separate 8-bit wide, 64-deep transmit FIFO and 12-bit wide, 64-deep receive FIFO
- Programmable FIFO disabling for 1-byte depth data path

These UARTs vary from industry-standard 16C650 on some minor points which are:

- Receive FIFO trigger levels
- The internal register map address space, and the bit function of each register differ
- The deltas of the modem status signals are not available
- 1.5 stop bits is not supported
- Independent receive clock feature is not supported

### 3.4.4 I2C

STA8090WGR includes an I2C interface configured slave.

### 3.4.5 MTU

The 2 Multi Timer Units provide access to eight interrupt generating programmable 32-bit Free-Running decrementing Counters (FRCs). The FRCs have their own clock input, allowing the counters to run from a much slower clock than the system clock.

The FRC is the part of the timer that performs the counting. There are four instantiations of the FRC block in each MTU, allowing eight counts to be performed in parallel. The 32-bit counter in the FRC is split up into two 16-bit counters.

### 3.4.6 WDT

Watchdog Timer (WDT) provides a way of recovering from software crashes. The watchdog clock is used to generate a regular interrupt (WDOGINT), depending on a programmed value.

The watchdog monitors the interrupt and asserts a reset signal (WDOGRES) if the interrupt remains unserved for the entire programmed period. You can enable or disable the watchdog unit as required.

*Note:* Watchdog is stalled when the ARM processor is in Debug mode.

### 3.4.7 GPIO

The GPIO block provides Twelve (12) programmable inputs or outputs. Each input or output can be controlled in two modes:

- software mode through an APB bus interface
- alternate mode, where GPIO becomes a peripheral input or output line

Any GPIO input can be independently enabled or disabled (masked) for interrupt generation. User can select for each GPIO which edge (rising, falling, both) will trigger an interrupt.

### 3.4.8 RTC

This is an always-on power domain dedicated to RTC logic (backup system) with 32 Kbyte SRAM and supplied with a dedicated voltage regulator.

The RTC provides a high resolution clock which can be used for GPS. It keeps the time when the system is inactive and can be used to wake the system up when a programmed alarm time is reached. It has a clock trimming feature to compensate for the accuracy of the 32.768 kHz crystal and a secured time update.

#### RTC features

- 47-bit counter clocked by 32.768 kHz clock
- 32-bit for the integer part (seconds) and 15-bit for the fractional part
- The integer part and the fractional part are readable independently
- The counter, once enabled, can be stopped
- Integer part load register (32-bit)
- Fractional part load register (15-bit)
- Load bit to transfer the content of the entire load register (integer+fractional part) to the 47-bit counter. Once set by the MCU this bits is cleared by the hardware to signal to the MCU that the RTC has been updated.

## 4 Electrical characteristics

### 4.1 Parameter conditions

Unless otherwise specified, all voltages are referred to GND.

### 4.2 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at  $T_A = 25\text{ °C}$ .

### 4.3 Typical values

Unless otherwise specified, typical data are based on  $T_A = 25\text{ °C}$ ,  $V_{\text{ddio}} = 1.8\text{ V}$ ,  $V_{\text{dd}} = 1.20\text{ V}$ . They are given only as design guidelines and are not tested.

### 4.4 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

### 4.5 Absolute maximum ratings

This product contains devices to protect the inputs against damage due to high static voltages, however it is advisable to take normal precautions to avoid application of any voltage higher than the specified maximum rated voltages.

*Table 9* lists the absolute maximum rating for STA8090WGR.

**Table 9. Voltage characteristics**

Symbol	Parameter	Min	Max	Unit
$V_{\text{CC\_CHAIN}}$	Analog supply voltage for RF chain (1.2 V)	-0.3	1.32	V
$V_{\text{CC\_PLL}}$	Analog supply voltage for PLL RF (1.2 V)	-0.3	1.32	V
$V_{\text{CC\_RF}}$	Analog supply voltage for RF (1.2 V)	-0.3	1.32	V
$V_{\text{DD\_SQI}}$	Digital supply voltage for SQI	-0.3	3.63	V
$V_{\text{DDD}}$	Power supply pins for the core logic.	-0.3	1.32	V
$V_{\text{DDIO\_R1}}$	Digital supply voltage for I/O ring 1 (1.8 V or 3.3 V)	-0.3	3.63	V
$V_{\text{DDIO\_R2}}$	Digital supply voltage for I/O ring 2 (3.3 V)	-0.3	3.63	V
$V_{\text{INB}}$	Backup LDO input supply voltage (1.6 V to 4.3 V)	-0.3	4.8	V
$V_{\text{INL1}}$	LDO1 input supply voltage (1.6 V to 4.3 V)	-0.3	4.8	V
$V_{\text{INL2}}$	LDO2 input supply voltage (1.6 V to 4.3 V)	-0.3	4.8	V

**Table 9. Voltage characteristics (continued)**

Symbol	Parameter	Min	Max	Unit
V <sub>INM</sub>	SMPS coil input supply (1.6 V to 4.3 V)	-0.3	4.8	V
V <sub>DD_ANA</sub>	SMPS input supply (1.6 V to 4.3 V)	-0.3	4.8	V
V <sub>ESD-HBM</sub> <sup>(1)</sup>	Electrostatic discharge, human body model.	-2	+2	KV
V <sub>ESD-CDM</sub>	Electrostatic discharge, charge device model.	-150	+150	V

1. Balls sustaining only ±500 V are A1, A2, A3,A4, A5, A6, B2, B3, G1, G2, G3, H1, H2, H4, H7, H8, J1, J2 and J3.

*Note:* Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Table 10. Thermal characteristics**

Symbol	Parameter	Min	Max	Unit
T <sub>oper</sub>	Operative ambient temperature	-40	85	°C
T <sub>j</sub>	Operative junction temperature	-40	125	°C
T <sub>stg</sub>	Storage temperature	-40	125	°C
R <sub>j-amb</sub>	Thermal resistance junction to ambient <sup>(1)</sup>	TBD	TBD	°C/W

1. According to JEDEC specification on a 2 layers board.

**Table 11. Frequency limits**

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
F <sub>CLK</sub>	Operating ARM9 CPU frequency	V <sub>DDD</sub> = 1.2 V; T <sub>C</sub> = 85 °C <sup>(1)</sup>	–	–	196	MHz
F <sub>AHB</sub>	AHB frequency		–	–	49	MHz

1. Not tested in production.

**Table 12. Power consumption**

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
P <sub>RF</sub>	RFIP power (total V <sub>INL2</sub> )	G2 = GPS; T <sub>amb</sub> = 25 °C; V <sub>INL2</sub> = 1.8 V	–	35	–	mW
		G2 + GLONASS; T <sub>amb</sub> = 25 °C; V <sub>INL2</sub> = 1.8 V	–	35	–	mW
		G2 + BeiDou; T <sub>amb</sub> = 25 °C; V <sub>INL2</sub> = 1.8 V	–	35	–	mW

**Table 12. Power consumption (continued)**

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
$P_{MVR}$	Switchable area power; (total $V_{INL1}$ )	$f_{ARM} = 196$ MHz; $f_{AHB} = 49$ MHz; $T_{amb} = 25$ °C; $V_{INL1} = 1.8$ V; UART active; other peripherals inactive	–	90	–	mW
$P_{LPVR}$	Always ON area power (total $V_{INB}$ )	$f_{ARM} = 196$ MHz; $f_{AHB} = 49$ MHz; $T_{amb} = 25$ °C; $V_{INB} = 3.3$ V	–	1	–	mW
$P_{IO}$	IO rings power (total $V_{DDIO\_R1} + V_{DDIO\_R2}$ )	$f_{ARM} = 196$ MHz; $f_{AHB} = 49$ MHz; $T_{amb} = 25$ °C; $V_{INL1} = 1.8$ V; UART active; other peripherals inactive	–	4	–	mW
$I_{DStandby}$	Standby mode supply current	RTC running = 32.768 kHz; $T_{amb} = 25$ °C; $V_{INB} = 1.8$ V	–	29	–	µA
$I_{DDeepStandby}$	Deep standby mode supply current <sup>(1)</sup>		–	7	–	µA

1. STDBY\_OUT pin not supported in deep standby.

## 4.6 Recommended DC operating conditions

Table 13 lists the functional recommended operating DC parameters for STA8090WGR.

**Table 13. Recommended DC operating conditions**

Symbol	Parameter	Min	Typ	Max	Unit
$V_{CC\_CHAIN}$	Analog supply voltage for RF chain (1.2 V)	1.08	1.20	1.32	V
$V_{CC\_PLL}$	Analog supply voltage for PLL RF (1.2 V)	1.08	1.20	1.32	V
$V_{CC\_RF}$	Analog supply voltage for RF (1.2 V)	1.08	1.20	1.32	V
$V_{DD\_SQI}$	Digital supply voltage for SQI I/O ring (1.8 V)	1.71	1.80	1.89	V
	Digital supply voltage for SQI I/O ring (3.3 V)	3.00	3.30	3.60	V
$V_{DDD}$	Power supply pins for the core logic.	1.00	1.10	1.32	V
$V_{DDIO\_R1}$	Digital supply voltage for I/O ring 1 (1.8 V)	1.71	1.80	1.89	V
	Digital supply voltage for I/O ring 1 (3.3 V)	3.00	3.30	3.60	V
$V_{DDIO\_R2}$	Digital supply voltage for I/O ring 2 (3.3 V)	3.00	3.30	3.60	V
$V_{INB}$	Backup LDO input supply voltage (1.6 V to 4.3 V)	1.60	–	4.30	V
$V_{INL1}$	LDO1 input supply voltage to generate 1.8 V	2.10	–	4.30	V
$V_{INL2}$	LDO2 input supply voltage to generate 1.2 V	1.60	–	4.30	V
$V_{INM}$	SMPS coil input supply voltage to generate 1.1 V	2.10	–	4.30	V

**Table 13. Recommended DC operating conditions (continued)**

Symbol	Parameter	Min	Typ	Max	Unit
V <sub>DD_ANA</sub>	SMPS input supply (1.6 V to 4.3 V)	1.60	–	4.30	V
T <sub>C</sub>	Operating case temperature	-40	–	85	°C

## 4.7 DC characteristics

Table 14 specifies the SMPS voltage regulator characteristics.

**Table 14. SMPS DC characteristics**

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
V <sub>OM</sub>	Output voltage (1.2 V)	1.6 V ≤ V <sub>INM</sub> ≤ 4.3 V; I <sub>OM</sub> ≤ 100 mA	1.08	1.20	1.32	V
	Output voltage (1.1 V)	1.6 V ≤ V <sub>INM</sub> ≤ 4.3 V; I <sub>OM</sub> ≤ 100 mA	1.0	1.10	1.2	V
I <sub>OM</sub>	Output current	–	0	–	100	mA

Table 15 specifies the LDO1 voltage regulator characteristics.

**Table 15. LDO1 DC characteristics**

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
V <sub>OL1</sub>	Output voltage (1.8V)	2.1 V ≤ V <sub>INL1</sub> ≤ 4.3 V; I <sub>OL1</sub> ≤ 70 mA	1.71	1.80	1.89	V
I <sub>OL1</sub>	Output current	–	0	–	70	mA

Table 16 specifies the LDO2 voltage regulator characteristics.

**Table 16. LDO2 DC characteristics**

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
V <sub>OL2</sub>	Output voltage	1.6 V ≤ V <sub>INL2</sub> ≤ 4.3 V; I <sub>OL2</sub> ≤ 30 mA	1.08	1.20	1.32	V
I <sub>OL2</sub>	Output current	–	0	–	30	mA

Table 17 specifies the low voltage detection thresholds

**Table 17. Low voltage detection thresholds**

Parameter		Min	Typ	Max	Unit
Input LVD always on and main VRs <sup>(1)</sup>	Upper voltage threshold	–	1.680	–	V
	Lower voltage threshold	–	1.650	–	V
Output LVD always on VR <sup>(1)</sup>	Upper voltage threshold	–	0.995	–	V
	Lower voltage threshold	–	0.935	–	V

**Table 17. Low voltage detection thresholds (continued)**

Parameter		Min	Typ	Max	Unit
Output LVD main VR (1.1 or 1.2 V) <sup>(1)</sup>	Upper voltage threshold @ V <sub>OM</sub> = 1.2 V	–	1.142	–	V
	Lower voltage threshold @ V <sub>OM</sub> = 1.2 V	–	1.076	–	V
	Upper voltage threshold @ V <sub>OM</sub> = 1.1 V	–	0.930	–	V
	Lower voltage threshold @ V <sub>OM</sub> = 1.1 V	–	0.900	–	V
Output LVD main VR (1.8 V) <sup>(1)</sup>	Upper voltage threshold @ V <sub>OL1</sub> = 1.8 V	–	1.645	–	V
	Lower voltage threshold @ V <sub>OL1</sub> = 1.8 V	–	1.626	–	V

1. By design.

Table 18 lists the DC characteristics for all the IO digital buffers expected for the following input buffers: STBYn (J4), STDBY\_OUT (H4), WAKEUP (F4) and RSTn (G4).

**Table 18. I/O buffers DC characteristics**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V <sub>IL</sub> <sup>(1)</sup>	Logical input low level voltage	V <sub>DDIO</sub> = 1.8 V	-0.3	–	0.3 * V <sub>DDIO</sub>	V
		V <sub>DDIO</sub> = 3.3 V	-0.3	–	0.8	V
V <sub>IH</sub> <sup>(1)</sup>	Logical input high level voltage	V <sub>DDIO</sub> = 1.8 V	0.7 * V <sub>DDIO</sub>	–	V <sub>DDIO</sub> + 0.3	V
		V <sub>DDIO</sub> = 3.3 V	2.0	–	V <sub>DDIO</sub> + 0.3	V
V <sub>HYST</sub> <sup>(2)</sup>	Schmitt-trigger hysteresis	–	50	–	–	mV
V <sub>OL</sub>	Low level output voltage	V <sub>DDIO</sub> = 1.8 V	–	–	0.4	V
		V <sub>DDIO</sub> = 3.3 V	–	–	0.4	V
V <sub>OH</sub>	High level output voltage	V <sub>DDIO</sub> = 1.8 V	V <sub>DDIO</sub> - 0.4	–	–	V
		V <sub>DDIO</sub> = 3.3 V	V <sub>DDIO</sub> - 0.4	–	–	V

1. Excludes oscillator inputs RTC\_XTI and XTAL\_IN. Refer to oscillator electrical specifications.

2. Apply to all digital inputs unless specified otherwise.

Table 19 lists the DC characteristics for the 1.0 V IO digital buffers input buffers: STBYn (J4), STDBY\_OUT (H4), WAKEUP (F4) and RSTn (G4).

**Table 19. 1.0 V I/O buffers DC characteristics**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V <sub>IL</sub>	Logical input low level voltage	V <sub>OB</sub> = 1.0 V	-0.3	–	0.35 * V <sub>OB</sub>	V
V <sub>IH</sub>	Logical input high level voltage	V <sub>OB</sub> = 1.0 V	0.65 * V <sub>OB</sub>	–	V <sub>OB</sub> + 0.3	V
V <sub>OL</sub>	Low level output voltage	V <sub>OB</sub> = 1.0 V	–	–	0.2	V
V <sub>OH</sub>	High level output voltage	V <sub>OB</sub> = 1.0 V	V <sub>OB</sub> - 0.2	–	–	V

## 4.8 AC characteristics

### 4.8.1 RF electrical specifications

**Table 20. RFCHAIN – GPS filter and VGA**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
S11	Input return loss	GPS band	–	-8	–	dB
f <sub>IF</sub>	IF frequency	PLL in default condition with 26Mhz as reference	–	4.045	–	MHz
NF	Noise figure	NF overall chain with AGC set at 0 dB	–	2 <sup>(1)</sup>	–	dB
C <sub>G</sub>	Conversion gain from RF input to ADC input	VGA at max gain	–	69	–	dB
		VGA at min gain	–	119	–	dB
IP <sub>1dB</sub>	RF-IF-VGA input compression point	VGA min	–	-80	–	dBm
IRR	Image rejection ratio	–	–	20	–	dB
BW <sub>GPS</sub>	-3dB IF bandwidth	GPS mode	–	2.4	–	MHz
ATT	Alias frequency rejection	F = 60 MHz (f <sub>s</sub> = 65.474 MHz)	–	30	–	dB
T <sub>gGPS</sub>	IF filter group delay variation	GPS mode	–	–	200 <sup>(1)</sup>	ns

1. Not tested in production.

**Table 21. RFCHAIN – GLONASS/BeiDou filter and VGA**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
S11	Input return loss	GLONASS band	–	-10	–	dB
		BeiDou band	–	-7	–	
f <sub>IFGNS/BDU</sub>	IF frequency for GLONASS	PLL in default condition with 26 Mhz as reference	–	8.519	–	MHz
	IF frequency for BeiDou		–	10.277	–	
NF	Noise figure	NF overall chain with AGC set at 0 dB	–	2 <sup>(1)</sup>	–	dB
C <sub>G</sub>	Conversion gain from RF input to ADC input	VGA at max gain	–	68	–	dB
		VGA at min gain	–	118	–	dB
IP <sub>1dB</sub>	RF-IF-VGA input compression point	VGA min	–	-80	–	dBm
IRR	Image rejection ratio	–	–	25	–	dB
BW <sub>GNS/BDU</sub>	-3dB IF bandwidth	–	–	10	–	MHz



Table 21. RFCHAIN – GLONASS/BeiDou filter and VGA (continued)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ATT	Alias frequency rejection	F = 53 MHz (fs = 65.474 MHz)	–	30	–	dB
T <sub>gGNS/BDU</sub>	IF filter group delay variation	–	–	–	20 <sup>(1)</sup>	ns

1. Not tested in production.

Table 22. Synthesizer

Symbol	Parameter	Min	Typ	Max	Unit
F <sub>TCXO_XTAL</sub>	Input frequency for xtal amplifier <sup>(1)</sup>	10	–	52	MHz
R <sub>DIV</sub>	Reference divider range	1	–	63	–
N <sub>DIV</sub>	Loop divider range	56	–	2047	–
F <sub>LO</sub>	LO operating frequency	–	3142.656	–	MHz

1. That amplifier can be used also as a TCXO input buffer.

## 4.8.2 Oscillator electrical specifications

This device contains two oscillators:

- A 32.768 kHz oscillator/buffer for RTC circuit.
- An OSCI oscillator/buffer in the RF Front-End

When used in oscillator mode, each oscillator requires a specific crystal, with parameters that must be as close as possible to the following recommended values. When used in input buffer mode, an external clock source must be applied.

### 32.768 kHz OSCI32 oscillator specifications

The 32.768 kHz OSCI32 oscillator is connected between RTC\_XTI (oscillator amplifier input) and RTC\_XTO (oscillator amplifier output). It also requires two external capacitors of 18 pF<sup>(a)</sup>, as shown on [Figure 3](#).

OSCI32 is disabled by default and must be enabled by setting bit28-OSCI\_EN of PRCC\_BACKUP\_REG0 to have 32.768 kHz oscillation when an XTAL pi-network is connected to RTC\_XTI/RTC\_XTO pins.

The recommended oscillator specifications are shown in [Table 23](#):

Table 23. Crystal recommended specifications

Symbol	Parameter	Min	Typ	Max	Unit
F <sub>SXTAL</sub>	Crystal frequency <sup>(1)</sup>	–	32.768	–	kHz
LM <sub>SXTAL</sub>	Motion inductance <sup>(1)</sup>	–	5	–	κH
CM <sub>SXTAL</sub>	Motional capacitance <sup>(1)</sup>	–	5.0	–	fF

a. Using crystal with recommended characteristics as per [Table 23](#).

**Table 23. Crystal recommended specifications (continued)**

Symbol	Parameter	Min	Typ	Max	Unit
CO <sub>SXTAL</sub>	Shunt capacitance <sup>(1)</sup>	–	1.3	–	pF
ESR	Resonance resistance <sup>(1)</sup>	–	–	80	kΩ
CL	External load capacitance <sup>(1)</sup>	–	18	–	pF

1. Not tested in production.

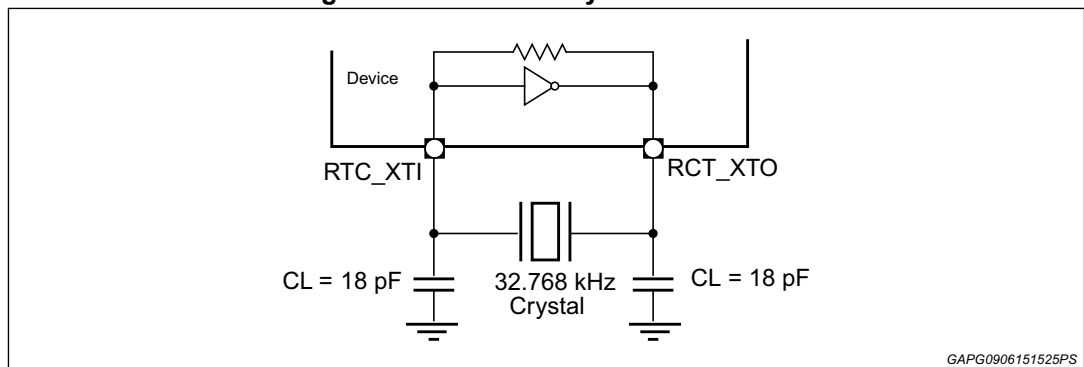
The oscillator amplifier specifications are shown in the following table:

**Table 24. Oscillator amplifier specifications**

Symbol	Parameter	Min	Typ	Max	Unit
T <sub>S</sub>	Startup time <sup>(1)</sup>	0.2	0.3	0.6	s
DL	Drive level <sup>(1)</sup>	–	–	<0.1	μW
RLC	Required load capacitance <sup>(1)</sup>	–	12.5	–	pF
GM	Startup transconductance	22.5	33.6	–	μA/V

1. Not tested in production.

**Figure 3. 32.768 kHz crystal connection**



To drive the 32.768 kHz crystal pins from an external clock source:

- Disable the oscillator (bit28-OSCI\_EN = 0b in PRCC\_BACKUP\_REG0 register). This disables the internal inverter, thus reducing the power consumption to minimum. This also allows to drive RTC\_XTI input even when a crystal is connected between RTC\_XTI and RTC\_XTO pins.
- Drive the RTC\_XTI pin with a square signal or a sine wave.

**Table 25. Characteristics of external slow clock input**

Symbol	Parameter	Min	Typ	Max	Unit
T <sub>JIT</sub> (cc)	Cycle-to-cycle jitter	-70	–	70	ps
T <sub>JIT</sub> (per)	Period jitter	-70	–	70	ps
–	Variation	-500	–	500	ppm
T <sub>DUTY</sub>	Duty cycle	45	–	55	%

### 4.8.3 OSCI oscillator specifications

Default supported value is 26 MHz.

## 5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com).

ECOPACK® is an ST trademark.

### 5.1 WLCSP77 (3.861 x 3.843 x 0.6 mm) 0.4 pitch package information

Figure 4. WLCSP77 package outline

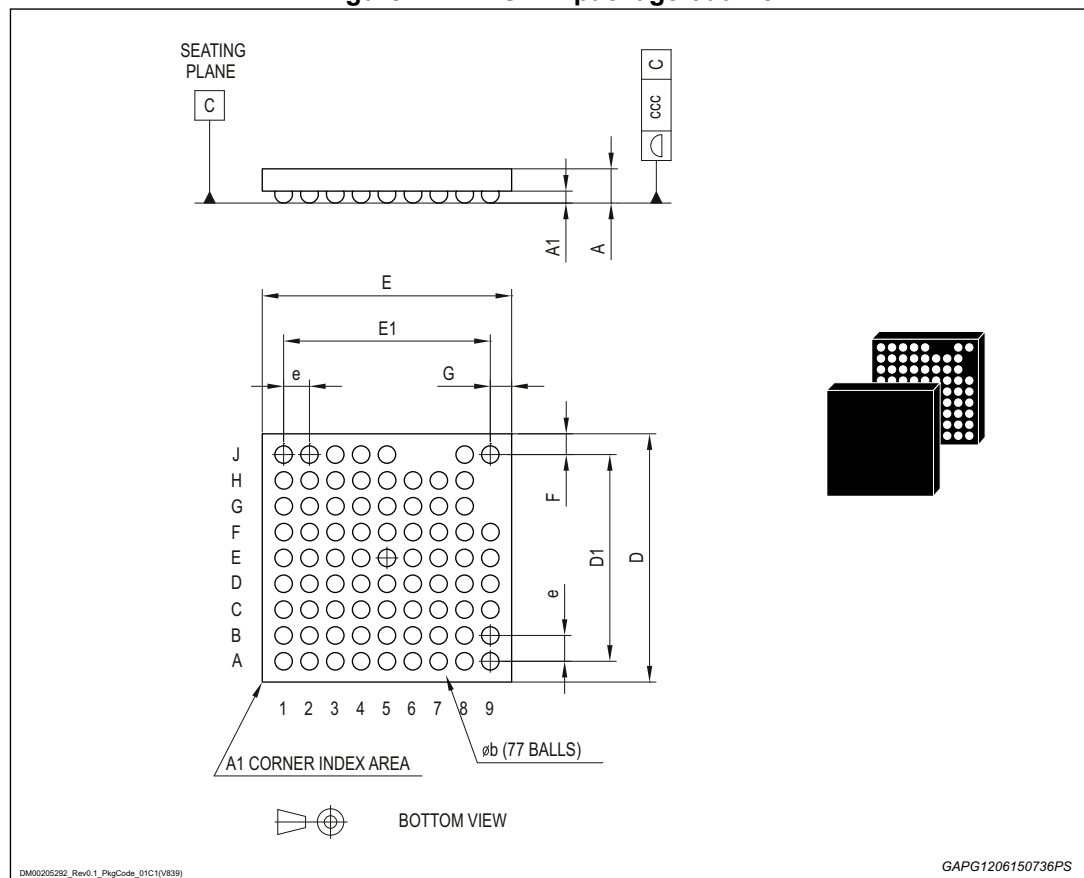


Table 26. WLCSP77 package mechanical data

Ref	Dimensions					
	Millimeters			Inches <sup>(1)</sup>		
	Min	Typ	Max	Min	Typ	Max
A	–	–	0.600	–	–	0.0236
A1	0.165	–	–	0.0065	–	–

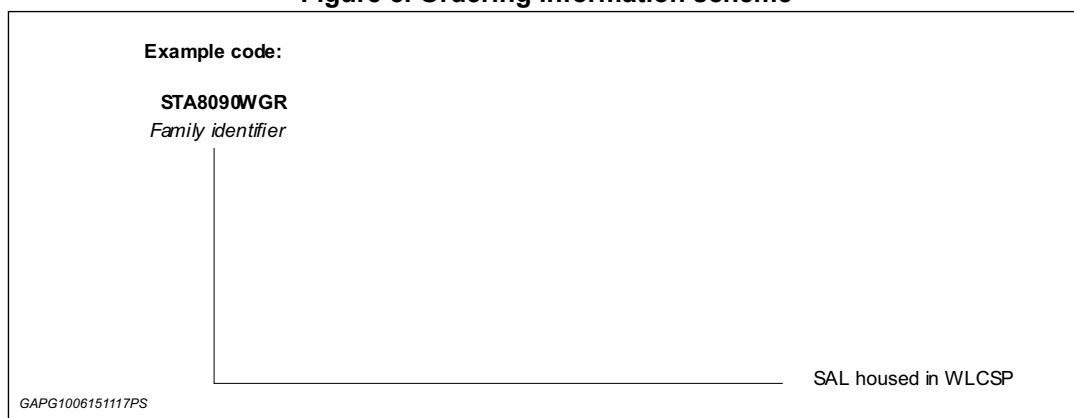
Table 26. WLCSP77 package mechanical data (continued)

Ref	Dimensions					
	Millimeters			Inches <sup>(1)</sup>		
	Min	Typ	Max	Min	Typ	Max
b	0.245	0.275	0.305	0.0096	0.0108	0.0120
D	3.813	3.843	3.873	0.1501	0.1513	0.1525
D1	–	3.200	–	–	0.1260	–
E	3.831	3.861	3.891	0.1508	0.1520	0.1532
E1	–	3.200	–	–	0.1260	–
e	–	0.400	–	–	0.0157	–
F	–	0.321	–	–	0.0126	–
G	–	0.330	–	–	0.0130	–
ccc	–	–	0.050	–	–	0.0020

1. Values in inches are converted from mm and rounded to four decimal digits.

## 6 Ordering information

Figure 5. Ordering information scheme



## 7 Revision history

Table 27. Document revision history

Date	Revision	Changes
16-Nov-2018	1	Initial release.

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