TC1762

32-Bit Single-Chip Microcontroller

TriCore

Microcontrollers

Never stop thinking

Edition 2008-04

Published by
Infineon Technologies AG
81726 München, Germany

Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics (“Beschaffenheitsgarantie”). With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office (**www.infineon.com**).

Warnings

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies Office.

Infineon Technologies Components may only be used in life-support devices or systems with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

TC1762

32-Bit Single-Chip Microcontroller

TriCore

Microcontrollers

Never stop thinking

Preliminary

TC1762 Data Sheet
Revision History: V1.0, 2008-04

Previous Version: V0.5 2007-03

Page	Subjects (major changes since last revision)
7	VSSOSC3 is deleted from the TC1762 Logic Symbol.
8, 10	TDATA0 of Pin 17, TCLK0 of Pin 20, TCLK0 of Pin 74 and TDATA0 of Pin 77 are updated in the Pinning Diagram and Pin Definition and Functions Table.
33	Transmit DMA request in Block Diagram of ASC Interfaces is updated.
35	Alternate output functions in block diagram of SSC interfaces are updated.
41	Programmable baud rate of the MLI is updated.
42	TDATA0 and TCLK0 of the block diagram of MLI interfaces are updated.
54	The description for WDT double reset detection is updated.
91	The power sequencing details is updated.
102	MLI timing, maximum operating frequency limit is extended, t31 is added.
106	Thermal resistance junction leads is updated.

Trademarks

TriCore® is a trademark of Infineon Technologies AG.

We Listen to Your Comments

Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to:

mcdocu.comments@infineon.com

Table of Contents

1 Summary of Features

The TC1762 has the following features:

- High-performance 32-bit super-scaler TriCore v1.3 CPU with 4-stage pipeline
  - Superior real-time performance
  - Strong bit handling
  - Fully integrated DSP capabilities
  - Single precision Floating Point Unit (FPU)
  - 66 or 80 MHz operation at full temperature range
- Multiple on-chip memories
  - 32 Kbyte Local Data Memory (SRAM)
  - 4 Kbyte Overlay Memory
  - 8 Kbyte Scratch-Pad RAM (SPRAM)
  - 8 Kbyte Instruction Cache (ICACHE)
  - 1024 Kbyte Flash Memory
  - 16 Kbyte Data Flash (2 Kbyte EEPROM emulation)
  - 16 Kbyte Boot ROM
- 8-channel DMA Controller
- Fast-response interrupt system with 255 hardware priority arbitration levels serviced by CPU
- High-performance on-chip bus structure
  - 64-bit Local Memory Bus (LMB) to Flash memory
  - System Peripheral Bus (SPB) for interconnections of functional units
- Versatile on-chip Peripheral Units
  - Two Asynchronous/Synchronous Serial Channels (ASCs) with baudrate generator, parity, framing and overrun error detection
  - One High Speed Synchronous Serial Channel (SSC) with programmable data length and shift direction
  - One Micro Second Bus (MSC) interface for serial port expansion to external power devices
  - One high-speed Micro Link Interface (MLI) for serial inter-processor communication
  - One MultiCAN Module with two CAN nodes and 64 free assignable message objects for high efficiency data handling via FIFO buffering and gateway data transfer
  - One General Purpose Timer Array Module (GPTA) with a powerful set of digital signal filtering and timer functionality to realize autonomous and complex Input/Output management
  - One 16-channel Analog-to-Digital Converter unit (ADC) with selectable 8-bit, 10-bit, or 12-bit, supporting 32 input channels
  - One 2-channel Fast Analog-to-Digital Converter unit (FADC) with concatenated comb filters for hardware data reduction: supporting 10-bit resolution, with minimum conversion time of 262.5ns (@ 80 MHz) or 318.2ns (@ 66 MHz)

- 32 analog input lines for ADC and FADC
- 81 digital general purpose I/O lines
- Digital I/O ports with 3.3 V capability
- On-chip debug support for OCDS Level 1 and 2 (CPU, DMA)
- Dedicated Emulation Device chip for multi-core debugging, tracing, and calibration via USB V1.1 interface available (TC1766ED)
- Power Management System
- Clock Generation Unit with PLL
- Core supply voltage of 1.5 V
- I/O voltage of 3.3 V
- Full automotive temperature range: -40° to +125°C
- PG-LQFP-176-2 package

Ordering Information

The ordering code for Infineon microcontrollers provides an exact reference to the required product. This ordering code identifies:

- The derivative itself, i.e. its function set, the temperature range, and the supply voltage
- The package and the type of delivery

For the available ordering codes for the TC1762, please refer to the “Product Catalog Microcontrollers” that summarizes all available microcontroller variants.

This document describes the derivatives of the device.The **Table 1-1** enumerates these derivatives and summarizes the differences.

Table 1-1 TC1762 Derivative Synopsis

Derivative	Ambient Temperature Range
SAK-TC1762-128F66HL	T_A = -40°C to +125°C; 66 MHz operation frequency
SAK-TC1762-128F80HL	T_A = -40°C to +125°C; 80 MHz operation frequency

2 General Device Information

Chapter 2 provides the general information for the TC1762.

2.1 Block Diagram

Figure 2-1 shows the TC1762 block diagram.

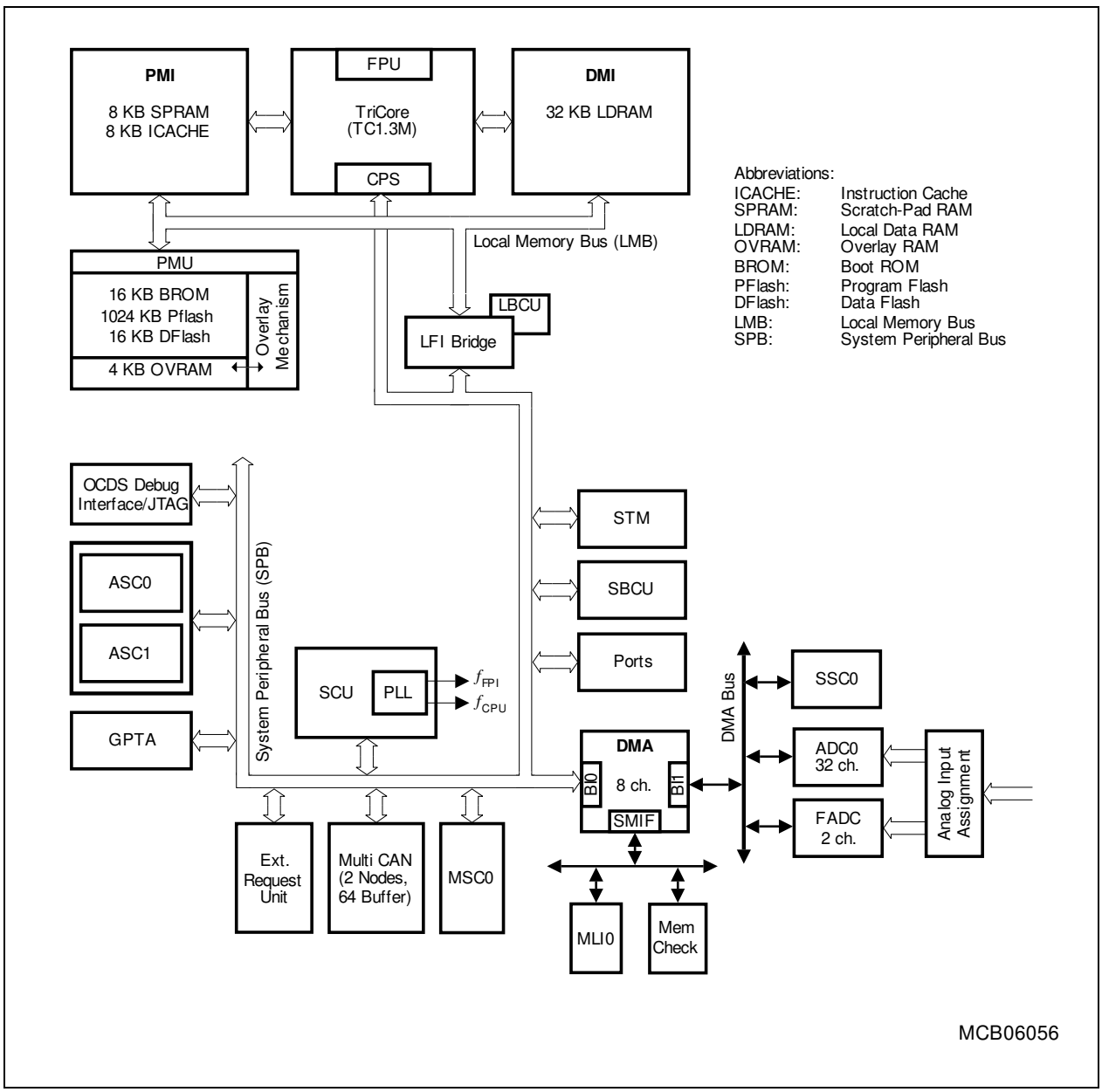


Figure 2-1 TC1762 Block Diagram

2.2 Logic Symbol

Figure 2-2 shows the TC1762 logic symbol.

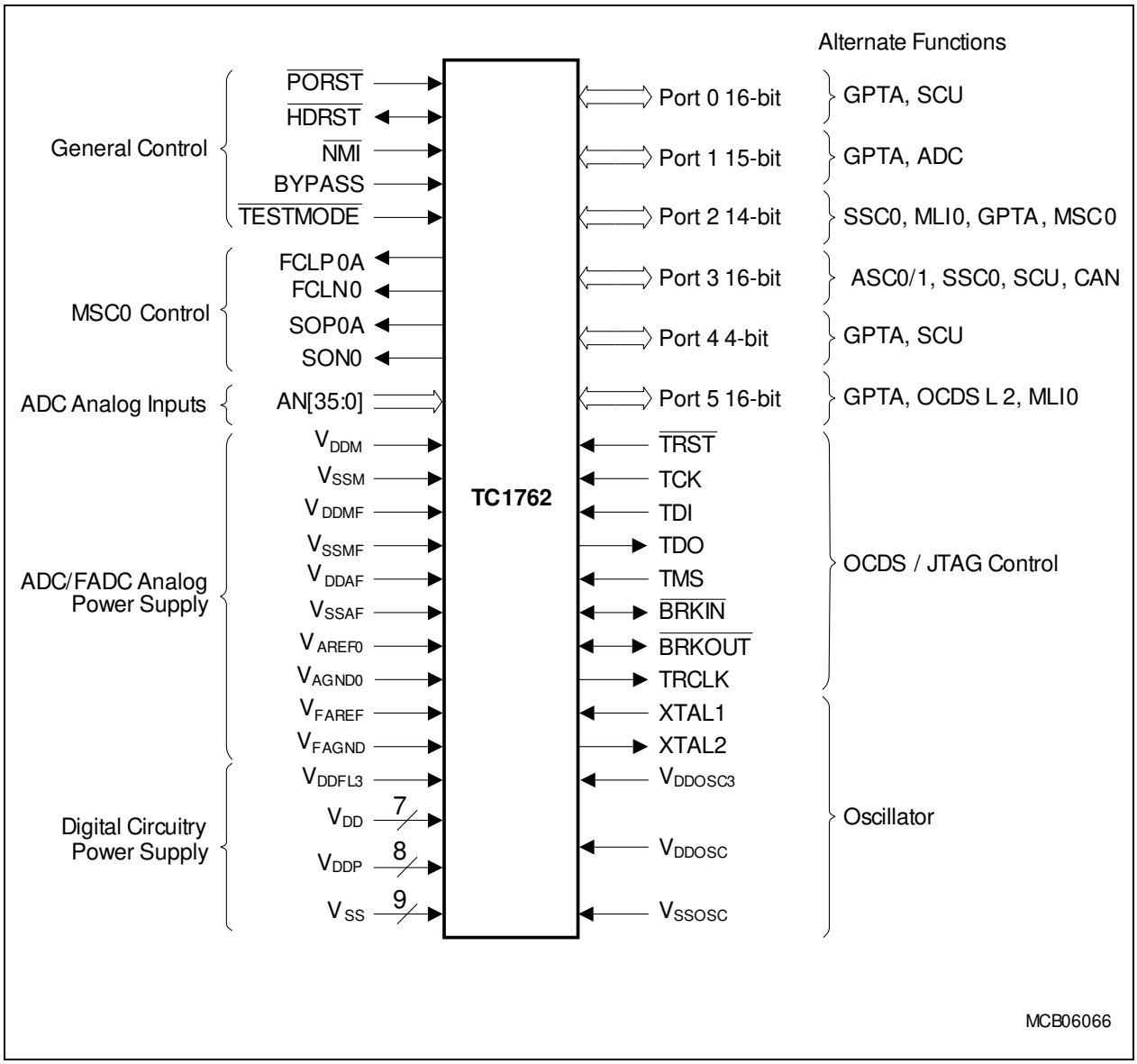


Figure 2-2 TC1762 Logic Symbol

2.3 Pin Configuration

Figure 2-3 shows the TC1762 pin configuration.

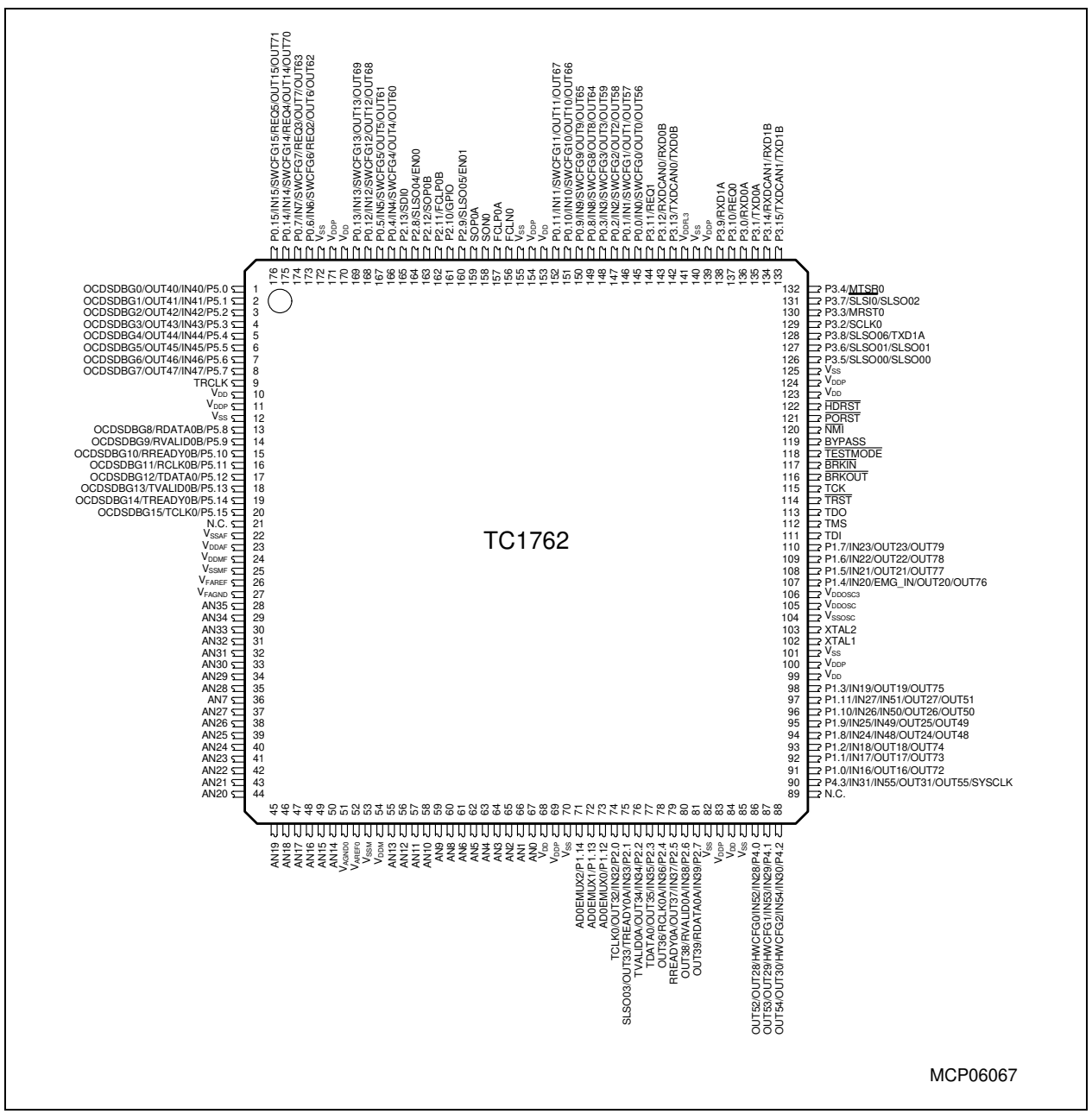


Figure 2-3 TC1762 Pinning for PG-LQFP-176-2 Package

2.4 Pad Driver and Input Classes Overview

The TC1762 provides different types and classes of input and output lines. For understanding of the abbreviations in **Table 2-1** starting at the next page, **Table 4-1** gives an overview on the pad type and class types.

2.5 Pin Definitions and Functions

Table 2-1 shows the TC1762 pin definitions and functions.

Table 2-1 Pin Definitions and Functions

Symbol	Pins	I/O	Pad Driver Class	Power Supply	Functions
Parallel Ports					
P0		I/O	A1	V_{DDP}	**Port 0** Port 0 is a 16-bit bi-directional general-purpose I/O port which can be alternatively used for GPTA I/O lines or external trigger inputs.
P0.0	145				IN0 / OUT0 / OUT56 line of GPTA
P0.1	146				IN1 / OUT1 / OUT57 line of GPTA
P0.2	147				IN2 / OUT2 / OUT58 line of GPTA
P0.3	148				IN3 / OUT3 / OUT59 line of GPTA
P0.4	166				IN4 / OUT4 / OUT60 line of GPTA
P0.5	167				IN5 / OUT5 / OUT61 line of GPTA
P0.6	173				IN6 / OUT6 / OUT62 line of GPTA REQ2 External trigger input 2
P0.7	174				IN7 / OUT7 / OUT63 line of GPTA REQ3 External trigger input 3
P0.8	149				IN8 / OUT8 / OUT64 line of GPTA
P0.9	150				IN9 / OUT9 / OUT65 line of GPTA
P0.10	151				IN10 / OUT10 / OUT66 line of GPTA
P0.11	152				IN11 / OUT11 / OUT67 line of GPTA
P0.12	168				IN12 / OUT12 / OUT68 line of GPTA
P0.13	169				IN13 / OUT13 / OUT69 line of GPTA
P0.14	175				IN14 / OUT14 / OUT70 line of GPTA REQ4 External trigger input 4
P0.15	176				IN15 / OUT15 / OUT71 line of GPTA REQ5 External trigger input 5 In addition, the state of the port pins are latched into the software configuration input register SCU_SCLIR at the rising edge of HDRST. Therefore, Port 0 pins can be used for operating mode selections by software.

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Driver Class	Power Supply	Functions
P1		I/O		V_{DDP}	**Port 1** Port 1 is a 15-bit bi-directional general purpose I/O port which can be alternatively used for GPTA I/O lines and ADC0 interface.
P1.0	91		A1		IN16 / OUT16 / OUT72 line of GPTA
P1.1	92		A1		IN17 / OUT17 / OUT73 line of GPTA
P1.2	93		A1		IN18 / OUT18 / OUT74 line of GPTA
P1.3	98		A1		IN19 / OUT19 / OUT75 line of GPTA
P1.4	107		A1		IN20 / OUT20 / OUT76 line of GPTA
P1.5	108		A1		IN21 / OUT21 / OUT77 line of GPTA
P1.6	109		A1		IN22 / OUT22 / OUT78 line of GPTA
P1.7	110		A1		IN23 / OUT23 / OUT79 line of GPTA
P1.8	94		A2		IN24 / OUT24 / IN48 / OUT48 line of GPTA
P1.9	95		A2		IN25 / OUT25 / IN49 / OUT49 line of GPTA
P1.10	96		A2		IN26 / OUT26 / IN50 / OUT50 line of GPTA
P1.11	97		A2		IN27 / OUT27 / IN51 / OUT51 line of GPTA
P1.12	73		A1		AD0EMUX0 ADC0 external multiplexer control output 0
P1.13	72		A1		AD0EMUX1 ADC0 external multiplexer control output 1
P1.14	71		A1		AD0EMUX2 ADC0 external multiplexer control output 2
					In addition, P1.4 also serves as **emergency shut-off input** for certain I/O lines (e.g. GPTA related outputs).

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Driver Class	Power Supply	Functions	
P2		I/O		V_{DDP}	**Port 2** Port 2 is a 14-bit bi-directional general-purpose I/O port which can be alternatively used for GPTA I/O, and interface for MLI0, MSC0 or SSC0.	
P2.0	74		A2		TCLK0	MLI0 transmit channel clock output A
					IN32 / OUT32	line of GPTA
P2.1	75		A2		TREADY0A	MLI0 transmit channel ready input A
					IN33 / OUT33	line of GPTA
					SLSO03	SSC0 slave select output 3
P2.2	76		A2		TVALID0A	MLI0 transmit channel valid output A
					IN34 / OUT34	line of GPTA
P2.3	77		A2		TDATA0	MLI0 transmit channel data output A
					IN35 / OUT35	line of GPTA
P2.4	78		A1		RCLK0A	MLI0 receive channel clock input A
					IN36 / OUT36	line of GPTA
P2.5	79		A2		RREADY0A	MLI0 receive channel ready output A
					IN37 / OUT37	line of GPTA
P2.6	80		A1		RVALID0A	MLI0 receive channel valid input A
					IN38 / OUT38	line of GPTA
P2.7	81		A1		RDATA0A	MLI0 receive channel data input A
					IN39 / OUT39	line of GPTA

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Driver Class	Power Supply	Functions	
P2.8	164		A2		SLSO04	SSC0 Slave Select output 4
					EN00	MSC0 enable output 0
P2.9	160		A2		SLSO05	SSC0 Slave Select output 5
					EN01	MSC0 enable output 1
P2.10	161		A2			
P2.11	162		A2		FCLP0B	MSC0 clock output B
P2.12	163		A2		SOP0B	MSC0 serial data output B
P2.13	165		A1		SDI0	MSC0 serial data input

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Driver Class	Power Supply	Functions	
P3		I/O		V_{DDP}	**Port 3** Port 3 is a 16-bit bi-directional general-purpose I/O port which can be alternatively used for ASC0/1, SSC0 and CAN lines.	
P3.0	136		A2		RXD0A	ASC0 receiver inp./outp. A
P3.1	135		A2		TXD0A	ASC0 transmitter output A
					This pin is sampled at the rising edge of $\overline{\text{PORST}}$. If this pin and the BYPASS input pin are both active, then oscillator bypass mode is entered.	
P3.2	129		A2		SCLK0	SSC0 clock input/output
P3.3	130		A2		MRST0	SSC0 master receive input/ slave transmit output
P3.4	132		A2		MTSR0	SSC0 master transmit output/slave receive input
P3.5	126		A2		SLSO00	SSC0 slave select output 0
P3.6	127		A2		$\overline{\text{SLSO01}}$	SSC0 slave select output 1
P3.7	131		A2		$\overline{\text{SLSI0}}$	SSC0 slave select input
					SLSO02	SSC0 slave select output 2
P3.8	128		A2		SLSO06	SSC0 slave select output 6
					TXD1A	ASC1 transmitter output A
P3.9	138		A2		RXD1A	ASC1 receiver inp./outp. A
P3.10	137		A1		REQ0	External trigger input 0
P3.11	144		A1		REQ1	External trigger input 1
P3.12	143		A2		RXDCAN0	CAN node 0 receiver input
					RXD0B	ASC0 receiver inp./outp. B
P3.13	142		A2		TXDCAN0	CAN node 0 transm. output
					TXD0B	ASC0 transmitter output B
P3.14	134		A2		RXDCAN1	CAN node 1 receiver input
					RXD1B	ASC1 receiver inp./outp. B
P3.15	133		A2		TXDCAN1	CAN node 1 transm. output
					TXD1B	ASC1 transmitter output B

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Driver Class	Power Supply	Functions
P4		I/O		V_{DDP}	**Port 4 / Hardware Configuration Inputs**
P4.[3:0]					HWCFG[3:0] Boot mode and boot location inputs; inputs are latched with the rising edge of HDRST. During normal operation, Port 4 pins may be used as alternate functions for GPTA or system clock output.
P4.0	86		A1		IN28 / OUT28 / IN52 / OUT52 line of GPTA
P4.1	87		A1		IN29 / OUT29 / IN53 / OUT53 line of GPTA
P4.2	88		A2		IN30 / OUT30 / IN54 / OUT54 line of GPTA
P4.3	90		A2		IN31 / OUT31 / IN55 / OUT55 line of GPTA SYSCLK System Clock Output

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Driver Class	Power Supply	Functions	
P5		I/O	A2	V_{DDP}	**Port 5** Port 5 is a 16-bit bi-directional general-purpose I/O port. In emulation, it is used as a trace port for OCDS Level 2 debug lines. In normal operation, it is used for GPTA I/O or the MLI0 interface.	
P5.0	1				OCDSDBG0	OCDS L2 Debug Line 0 (Pipeline Status Sig. PS0)
					IN40 / OUT40	line of GPTA
P5.1	2				OCDSDBG1	OCDS L2 Debug Line 1 (Pipeline Status Sig. PS1)
					IN41 / OUT41	line of GPTA
P5.2	3				OCDSDBG2	OCDS L2 Debug Line 2 (Pipeline Status Sig. PS2)
					IN42 / OUT42	line of GPTA
P5.3	4				OCDSDBG3	OCDS L2 Debug Line 3 (Pipeline Status Sig. PS3)
					IN43 / OUT43	line of GPTA
P5.4	5				OCDSDBG4	OCDS L2 Debug Line 4 (Pipeline Status Sig. PS4)
					IN44 / OUT44	line of GPTA
P5.5	6				OCDSDBG5	OCDS L2 Debug Line 5 (Break Qualification Line BRK0)
					IN45 / OUT45	line of GPTA
P5.6	7				OCDSDBG6	OCDS L2 Debug Line 6 (Break Qualification Line BRK1)
					IN46 / OUT46	line of GPTA
P5.7	8				OCDSDBG7	OCDS L2 Debug Line 7 (Break Qualification Line BRK2)
					IN47 / OUT47	line of GPTA

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Driver Class	Power Supply	Functions	
P5.8	13				OCDSDBG8	OCDS L2 Debug Line 8 (Indirect PC Addr. PC0)
					RDATA0B	MLI0 receive channel data input B
P5.9	14				OCDSDBG9	OCDS L2 Debug Line 9 (Indirect PC Addr. PC1)
					RVALID0B	MLI0 receive channel valid input B
P5.10	15				OCDSDBG10	OCDS L2 Debug Line 10 (Indirect PC Addr. PC2)
					RREADY0B	MLI0 receive channel ready output B
P5.11	16				OCDSDBG11	OCDS L2 Debug Line 11 (Indirect PC Addr. PC3)
					RCLK0B	MLI0 receive channel clock input B
P5.12	17				OCDSDBG12	OCDS L2 Debug Line 12 (Indirect PC Addr. PC04)
					TDATA0	MLI0 transmit channel data output B
P5.13	18				OCDSDBG13	OCDS L2 Debug Line 13 (Indirect PC Addr. PC05)
					TVALID0B	MLI0 transmit channel valid output B
P5.14	19				OCDSDBG14	OCDS L2 Debug Line 14 (Indirect PC Address PC6)
					TREADY0B	MLI0 transmit channel ready input B
P5.15	20				OCDSDBG15	OCDS L2 Debug Line 15 (Indirect PC Address PC7)
					TCLK0	MLI0 transmit channel clock output B

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Driver Class	Power Supply	Functions
MSC0 Outputs					
			C	V_{DDP}	**LVDS MSC Clock and Data Outputs**[2)]
FCLP0A	157	O			MSC0 Differential Driver Clock Output Positive A
FCLN0	156	O			MSC0 Differential Driver Clock Output Negative
SOP0A	159	O			MSC0 Differential Driver Serial Data Output Positive A
SON0	158	O			MSC0 Differential Driver Serial Data Output Negative

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Driver Class	Power Supply	Functions
Analog Inputs					
AN[35:0]		I	D	–	**Analog Input Port** The Analog Input Port provides altogether 36 analog input lines to ADC0 and FADC. AN[31:0]: ADC0 analog inputs [31:0] AN[35:32]: FADC analog differential inputs
AN0	67				Analog input 0
AN1	66				Analog input 1
AN2	65				Analog input 2
AN3	64				Analog input 3
AN4	63				Analog input 4
AN5	62				Analog input 5
AN6	61				Analog input 6
AN7	36				Analog input 7
AN8	60				Analog input 8
AN9	59				Analog input 9
AN10	58				Analog input 10
AN11	57				Analog input 11
AN12	56				Analog input 12
AN13	55				Analog input 13
AN14	50				Analog input 14
AN15	49				Analog input 15
AN16	48				Analog input 16
AN17	47				Analog input 17
AN18	46				Analog input 18
AN19	45				Analog input 19
AN20	44				Analog input 20
AN21	43				Analog input 21
AN22	42				Analog input 22
AN23	41				Analog input 23
AN24	40				Analog input 24
AN25	39				Analog input 25
AN26	38				Analog input 26
AN27	37				Analog input 27
AN28	35				Analog input 28
AN29	34				Analog input 29
AN30	33				Analog input 30

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Driver Class	Power Supply	Functions
AN31 AN32 AN33 AN34 AN35	32 31 30 29 28	I	D	–	Analog input 31 Analog input 32 Analog input 33 Analog input 34 Analog input 35
System I/O					
TRST	114	I	A2[1]	V_{DDP}	**JTAG Module Reset/Enable Input**
TCK	115	I	A2[1]	V_{DDP}	**JTAG Module Clock Input**
TDI	111	I	A1[1]	V_{DDP}	**JTAG Module Serial Data Input**
TDO	113	O	A2	V_{DDP}	**JTAG Module Serial Data Output**
TMS	112	I	A2[1]	V_{DDP}	**JTAG Module State Machine Control Input**
BRKIN	117	I/O	A3	V_{DDP}	**OCDS Break Input (Alternate Output)[2][3]**
BRK OUT	116	I/O	A3	V_{DDP}	**OCDS Break Output (Alternate Input)[2][3]**
TRCLK	9	O	A4	V_{DDP}	**Trace Clock for OCDS_L2 Lines[2]**
NMI	120	I	A2[4][5]	V_{DDP}	**Non-Maskable Interrupt Input**
HDRST	122	I/O	A2[6]	V_{DDP}	**Hardware Reset Input / Reset Indication Output**
PORST[7]	121	I	A2[4]	V_{DDP}	**Power-on Reset Input**
BYPASS	119	I	A1[1]	V_{DDP}	**PLL Clock Bypass Select Input** This input has to be held stable during power-on resets. With BYPASS = 1, the spike filters in the HDRST, PORST and NMI inputs are switched off.
TEST MODE	118	I	A2[4][8]	V_{DDP}	**Test Mode Select Input** For normal operation of the TC1762, this pin should be connected to high level.
XTAL1 **XTAL2**	102 103	I O	n.a.	V_{DDOSC}	**Oscillator/PLL/Clock Generator Input/Output Pins**
N.C.	21, 89	–	–	–	**Not Connected** These pins are reserved for future extension and must not be connected externally.

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Driver Class	Power Supply	Functions
Power Supplies					
V_{DDM}	54	–	–	–	**ADC Analog Part Power Supply (3.3 V)**
V_{SSM}	53	–	–	–	**ADC Analog Part Ground for V_{DDM}**
V_{DDMF}	24	–	–	–	**FADC Analog Part Power Supply (3.3 V)**
V_{SSMF}	25	–	–	–	**FADC Analog Part Ground for V_{DDMF}**
V_{DDAF}	23	–	–	–	**FADC Analog Part Logic Power Supply (1.5 V)**
V_{SSAF}	22	–	–	–	**FADC Analog Part Logic Ground for V_{DDAF}**
V_{AREF0}	52	–	–	–	**ADC Reference Voltage**
V_{AGND0}	51	–	–	–	**ADC Reference Ground**
V_{FAREF}	26	–	–	–	**FADC Reference Voltage**
V_{FAGND}	27	–	–	–	**FADC Reference Ground**
V_{DDOSC}	105	–	–	–	**Main Oscillator and PLL Power Supply (1.5 V)**
V_{DDOSC3}	106	–	–	–	**Main Oscillator Power Supply (3.3 V)**
V_{SSOSC}	104	–	–	–	**Main Oscillator and PLL Ground**
V_{DDFL3}	141	–	–	–	**Power Supply for Flash (3.3 V)**
V_{DD}	10, 68, 84, 99, 123, 153, 170	–	–	–	**Core Power Supply (1.5 V)**

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Driver Class	Power Supply	Functions
V_{DDP}	11, 69, 83, 100, 124, 154, 171, 139	–	–	–	**Port Power Supply (3.3 V)**
V_{SS}	12, 70, 85, 101, 125, 155, 172, 140, 82	–	–	–	**Ground**

1) These pads are I/O pads with input only function. Its input characteristics are identical with the input characteristics as defined for class A pads.
2) In case of a power-fail condition (one or more power supply voltages drop below the specified voltage range), an undefined output driving level may occur at these pins.
3) Programmed by software as either break input or break output.
4) These pads are input only pads with input characteristics.
5) Input only pads with input spike filter.
6) Open drain pad with input spike filter.
7) The dual input reset system of TC1762/TC1766ED, assumes that the $\overline{\text{PORST}}$ reset pin is used for power-on reset only. It has to be taken into account that if a system uses the $\overline{\text{PORST}}$ reset input for other system resets, the emulation part of the TC1766ED Emulation Device is reset as well. Thus, it will always force a complete re-initialization of the emulator and will prevent the user debugging across these types of resets.
8) Input only pads without input spike filter.

Table 2-2 List of Pull-up/Pull-down Reset Behavior of the Pins

Pins	$\overline{\text{PORST}}$ = 0	$\overline{\text{PORST}}$ = 1
All GPIOs, TDI, TMS, TDO	Pull-up	
$\overline{\text{HDRST}}$	Drive-low	Pull-up
BYPASS	Pull-up	High-impedance
$\overline{\text{TRST}}$, TCK	High-impedance	Pull-down
TRCLK	High-impedance	
$\overline{\text{BRKIN}}$, $\overline{\text{BRKOUT}}$, TESTMODE	Pull-up	
$\overline{\text{NMI}}$, $\overline{\text{PORST}}$	Pull-down	

3 Functional Description

Chapter 3 provides an overview of the TC1762 functional description.

3.1 System Architecture and On-Chip Bus Systems

The TC1762 has two independent on-chip buses (see also TC1762 block diagram on **Page 2-6**):

- Local Memory Bus (LMB)
- System Peripheral Bus (SPB)

The LMB Bus connects the CPU local resources for data and instruction fetch. The Local Memory Bus interconnects the memory units and functional units, such as CPU and PMU. The main target of the LMB bus is to support devices with fast response times, optimized for speed. This allows the DMI and PMI fast access to local memory and reduces load on the FPI bus. The Tricore system itself is located on LMB bus.

The Local Memory Bus is a synchronous, pipelined, split bus with variable block size transfer support. It supports 8-, 16-, 32- and 64-bit single transactions and variable length 64-bit block transfers.

The SPB Bus is accessible to the CPU via the LMB Bus bridge. The System Peripheral Bus (SPB Bus) in TC1762 is an on-chip FPI Bus. The FPI Bus interconnects the functional units of the TC1762, such as the DMA and on-chip peripheral components. The FPI Bus is designed to be quick to be acquired by on-chip functional units, and quick to transfer data. The low setup overhead of the FPI Bus access protocol guarantees fast FPI Bus acquisition, which is required for time-critical applications.The FPI Bus is designed to sustain high transfer rates. For example, a peak transfer rate of up to 320 Mbyte/s can be achieved with a 80 MHz bus clock and 32-bit data bus. With a 66 MHz bus clock, the peak transfer rate is up to 264 Mbytes/s. Multiple data transfers per bus arbitration cycle allow the FPI Bus to operate at close to its peak bandwidth.

Both the LMB Bus and the SPB Bus runs at full CPU speed. The maximum CPU speed is 66 or 80 MHz depending on the derivative.

Additionally, two simplified bus interfaces are connected to and controlled by the DMA Controller:

- DMA Bus
- SMIF Interface

3.2 On-Chip Memories

As shown in the TC1762 block diagram on **Page 2-6**, some of the TC1762 units provide on-chip memories that are used as program or data memory.

- Program memory in PMU
  - 16 Kbyte Boot ROM (BROM)
  - 1024 Kbyte Program Flash (PFlash)
- Program memory in PMI
  - 8 Kbyte Scratch-Pad RAM (SPRAM)
  - 8 Kbyte Instruction Cache (ICACHE)
- Data memory in PMU
  - 16 Kbyte Data Flash (DFlash)
  - 4 Kbyte Overlay RAM (OVRAM)
- Data memory in DMI
  - 32 Kbyte Local Data RAM (LDRAM)
- On-chip SRAM with parity error protection

Features of Program Flash

- 1024 Kbyte on-chip program Flash memory
- Usable for instruction code or constant data storage
- 256-byte program interface
  - 256 bytes are programmed into PFLASH page in one step/command
- 256-bit read interface
  - Transfer from PFLASH to CPU/PMI by four 64-bit single cycle burst transfers
- Dynamic correction of single-bit errors during read access
- Detection of double-bit errors
- Fixed sector architecture
  - Eight 16 Kbyte, one 128 Kbyte, one 256 Kbyte and one 512 Kbyte sectors
  - Each sector separately erasable
  - Each sector separately write-protectable
- Configurable read protection for complete PFLASH with sophisticated read access supervision, combined with write protection for complete PFLASH (protection against “Trojan horse” software)
- Configurable write protection for each sector
  - Each sector separately write-protectable
  - With capability to be re-programmed
  - With capability to be locked forever (OTP)
- Password mechanism for temporary disabling of write and read protection
- On-chip generation of programming voltage
- JEDEC-standard based command sequences for PFLASH control
  - Write state machine controls programming and erase operations
  - Status and error reporting by status flags and interrupt
- Margin check for detection of problematic PFLASH bits

Features of Data Flash

- 16 Kbyte on-chip data Flash memory, organized in two 8 Kbyte banks
- Usable for data storage with EEPROM functionality
- 128 Byte of program interface
  – 128 bytes are programmed into one DFLASH page by one step/command
- 64-bit read interface (no burst transfers)
- Dynamic correction of single-bit errors during read access
- Detection of double-bit errors
- Fixed sector architecture
  – Two 8 Kbyte banks/sectors
  – Each sector separately erasable
- Configurable read protection (combined with write protection) for complete DFLASH together with PFLASH read protection
- Password mechanism for temporary disabling of write and read protection
- Erasing/programming of one bank possible while reading data from the other bank
- Programming of one bank while erasing the other bank possible
- On-chip generation of programming voltage
- JEDEC-standard based command sequences for DFLASH control
  – Write state machine controls programming and erase operations
  – Status and error reporting by status flags and interrupt
- Margin check for detection of problematic DFLASH bits

3.3 Architectural Address Map

Table 3-1 shows the overall architectural address map as defined for the TriCore and as implemented in TC1762.

Table 3-1 TC1762 Architectural Address Map

Segment	Contents	Size	Description
0-7	Global	8 x 256 Mbyte	Reserved (MMU space); cached
8	Global Memory	256 Mbyte	Reserved (246 Mbyte); PMU, Boot ROM; cached
9	Global Memory	256 Mbyte	FPI space; cached
10	Global Memory	256 Mbyte	Reserved (246 Mbyte), PMU, Boot ROM; non-cached
11	Global Memory	256 Mbyte	FPI space; non-cached
12	Local LMB Memory	256 Mbyte	Reserved; bottom 4 Mbyte visible from FPI bus in segment 14; cached
13	DMI	64 Mbyte	Local Data Memory RAM; non-cached
	PMI	64 Mbyte	Local Code Memory RAM; non-cached
	EXT_PER	96 Mbyte	Reserved; non-cached
	EXT_EMU	16 Mbyte	Reserved; non-cached
	BOOTROM	16 Mbyte	Boot ROM space, Boot ROM mirror; non-cached
14	EXTPER	128 Mbyte	Reserved; non-speculative; non-cached; no execution
	CPU[0 ..15] image region	16 x 8 Mbyte	Non-speculative; non-cached; no execution
15	LMB_PER CSFRs INT_PER	256 Mbyte	CSFRs of CPUs[0 ..15]; LMB & FPI Peripheral Space; non-speculative; non-cached; no execution

3.4 Memory Protection System

The TC1762 memory protection system specifies the addressable range and read/write permissions of memory segments available to the current executing task. The memory protection system controls the position and range of addressable segments in memory. It also controls the types of read and write operations allowed within addressable memory segments. Any illegal memory access is detected by the memory protection hardware, which then invokes the appropriate Trap Service Routine (TSR) to handle the error. Thus, the memory protection system protects critical system functions against both software and hardware errors. The memory protection hardware can also generate signals to the Debug Unit to facilitate tracing illegal memory accesses.

There are two Memory Protection Register Sets in the TC1762, numbered 0 and 1, which specify memory protection ranges and permissions for code and data. The PSW.PRS bit field determines which of these is the set currently in use by the CPU. As the TC1762 uses a Harvard-style memory architecture, each Memory Protection Register Set is broken down into a Data Protection Register Set and a Code Protection Register Set. Each Data Protection Register Set can specify up to four address ranges to receive a particular protection modes. Each Code Protection Register Set can specify up to two address ranges to receive a particular protection modes.

Each Data Protection Register Sets and Code Protection Register Sets determines the range and protection modes for a separate memory area. Each set contains a pair of registers which determine the address range (the Data Segment Protection Registers and Code Segment Protection Registers) and one register (Data Protection Mode Register) which determines the memory access modes that applies to the specified range.

3.5 DMA Controller and Memory Checker

The DMA Controller of the TC1762 transfers data from data source locations to data destination locations without intervention of the CPU or other on-chip devices. One data move operation is controlled by one DMA channel. Eight DMA channels are provided in one DMA Sub-Block. The Bus Switch provides the connection of the DMA Sub-Block to the two FPI Bus interfaces and an MLI bus interface. In the TC1762, the FPI Bus interfaces are connected to the System Peripheral Bus and the DMA Bus. The third specific bus interface provides a connection to the Micro Link Interface module (MLI0 in the TC1762) and other DMA-related devices (Memory Checker module in the TC1762). Clock control, address decoding, DMA request wiring, and DMA interrupt service request control are implementation-specific and managed outside the DMA controller kernel. **Figure 3-1** shows the implementation details and interconnections of the DMA module.

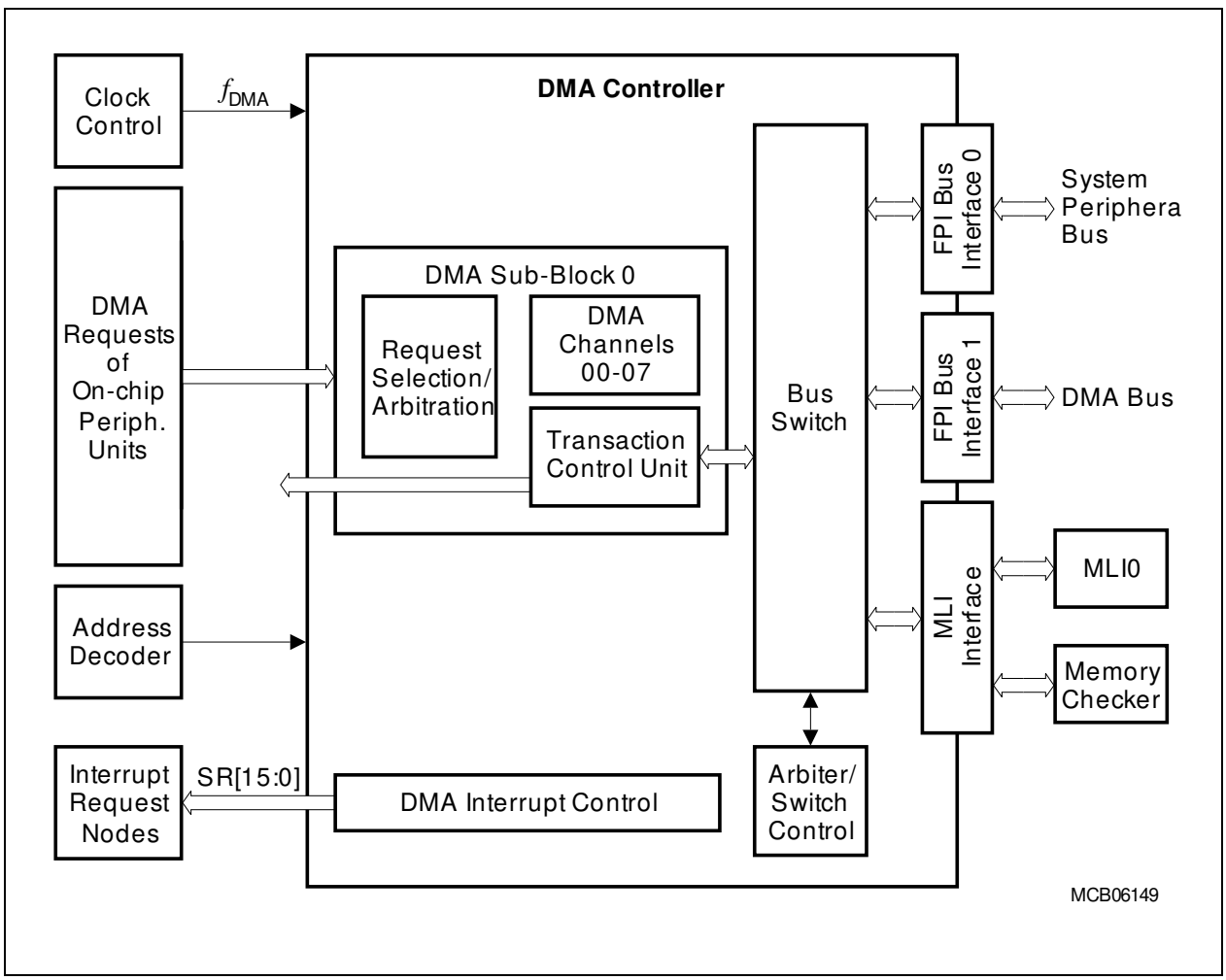


Figure 3-1 DMA Controller Block Diagram

Features

- 8 independent DMA channels

  - 8 DMA channels in the DMA Sub-Block
  - Up to 8 selectable request inputs per DMA channel
  - 2-level programmable priority of DMA channels within the DMA Sub-Block
  - Software and hardware DMA request
  - Hardware requests by selected on-chip peripherals and external inputs
- Programmable priority of the DMA Sub-Blocks on the bus interfaces
- Buffer capability for move actions on the buses (at least 1 move per bus is buffered).
- Individually programmable operation modes for each DMA channel
  - Single Mode: stops and disables DMA channel after a predefined number of DMA transfers
  - Continuous Mode: DMA channel remains enabled after a predefined number of DMA transfers; DMA transaction can be repeated.
  - Programmable address modification
- Full 32-bit addressing capability of each DMA channel
  - 4 Gbyte address range
  - Support of circular buffer addressing mode
- Programmable data width of DMA transfer/transaction: 8-bit, 16-bit, or 32-bit
- Micro Link bus interface support
- Register set for each DMA channel
  - Source and destination address register
  - Channel control and status register
  - Transfer count register
- Flexible interrupt generation (the service request node logic for the MLI channels is also implemented in the DMA module)
- All buses connected to the DMA module must work at the same frequency.
- Read/write requests of the System Bus side to the peripherals on DMA Bus are bridged to the DMA Bus (only the DMA is the master on the DMA bus), allowing easy access to these peripherals by CPU

Memory Checker

The Memory Checker Module (MCHK) makes it possible to check the data consistency of memories. Any SPB bus master may access the memory checker. It is preferable the DMA does it as described hereafter. It uses DMA 8-bit, 16-bit, or 32-bit moves to read from the selected address area and to write the value read in a memory checker input register. With each write operation to the memory checker input register, a polynomial checksum calculation is triggered and the result of the calculation is stored in the memory checker result register.

The memory checker uses the standard Ethernet polynomial, which is given by:

$G^{32} = x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^{8} + x^{7} + x^{5} + x^{4} + x^{2} + x + 1$

Note: Although the polynomial above is used for generation, the generation algorithm differs from the one that is used by the Ethernet protocol.

3.6 Interrupt System

The TC1762 interrupt system provides a flexible and time-efficient means of processing interrupts. An interrupt request is serviced by the CPU, which is called the “Service Provider”. Interrupt requests are called “Service Requests” rather than “Interrupt Requests” in this document.

Each peripheral in the TC1762 can generate service requests. Additionally, the Bus Control Units, the Debug Unit, and even the CPU itself can generate service requests to the Service Provider.

As shown in **Figure 3-2**, each TC1762 unit that can generate service requests is connected to one or multiple Service Request Nodes (SRN). Each SRN contains a Service Request Control Register mod_SRCx, where “mod” is the identifier of the service requesting unit and “x” an optional index. The CPU Interrupt Arbitration Bus connects the SRNs with the Interrupt Control Unit (ICU), which arbitrates service requests for the CPU and administers the CPU Interrupt Arbitration Bus.

The Debug Unit can generate service requests to the CPU. The CPU makes service requests directly to itself (via the ICU). The CPU Service Request Nodes are activated through software.

Depending on the selected system clock frequency f_{SYS}, the number of f_{SYS} clock cycles per arbitration cycle must be selected as follows:

- $f_{SYS} < 60$ MHz: ICR.CONECYC = 1
- $f_{SYS} > 60$ MHz: ICR.CONECYC = 0

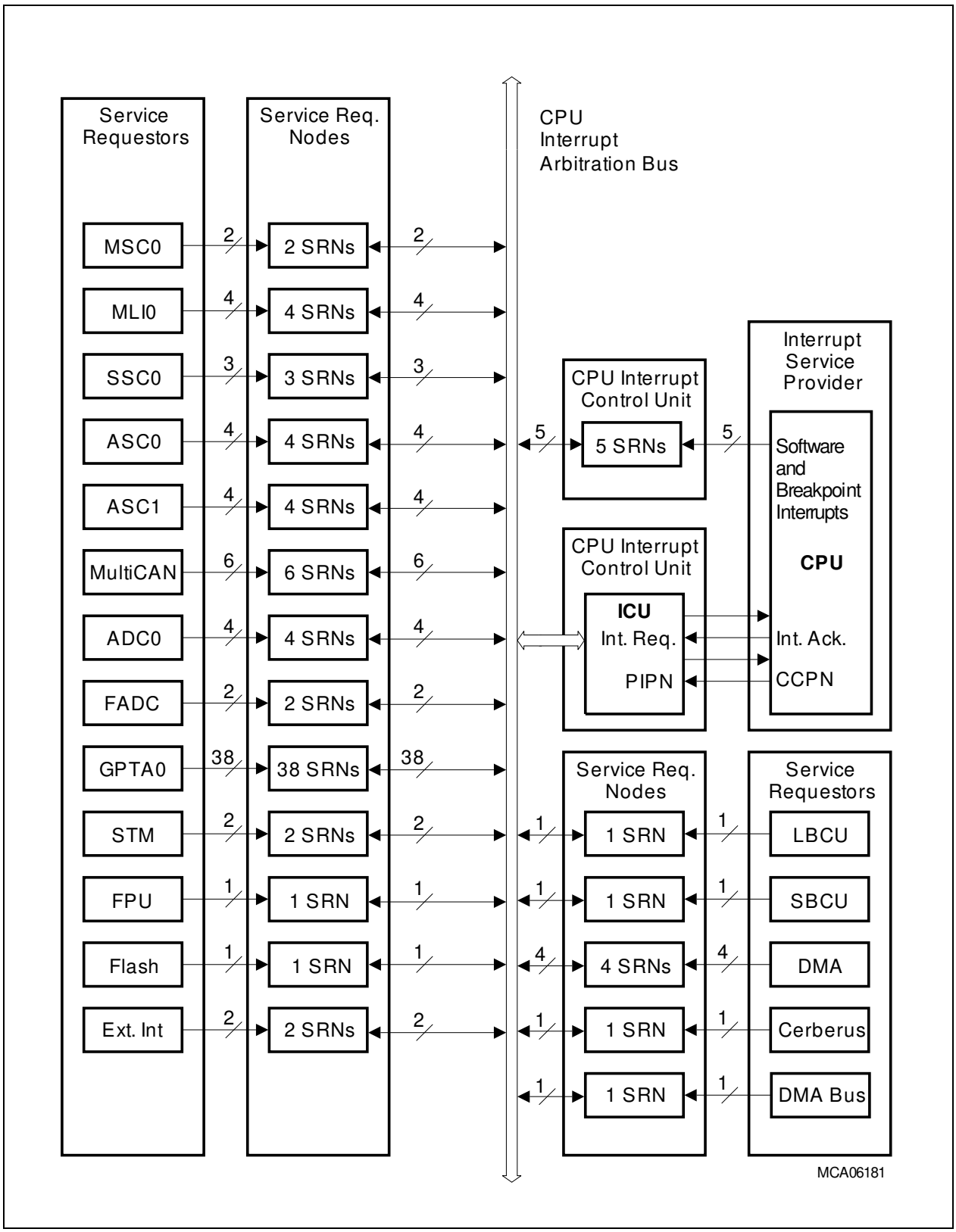


Figure 3-2 Block Diagram of the TC1762 Interrupt System

3.7 Asynchronous/Synchronous Serial Interfaces (ASC0, ASC1)

Figure 3-3 shows a global view of the functional blocks and interfaces of the two Asynchronous/Synchronous Serial Interfaces, ASC0 and ASC1.

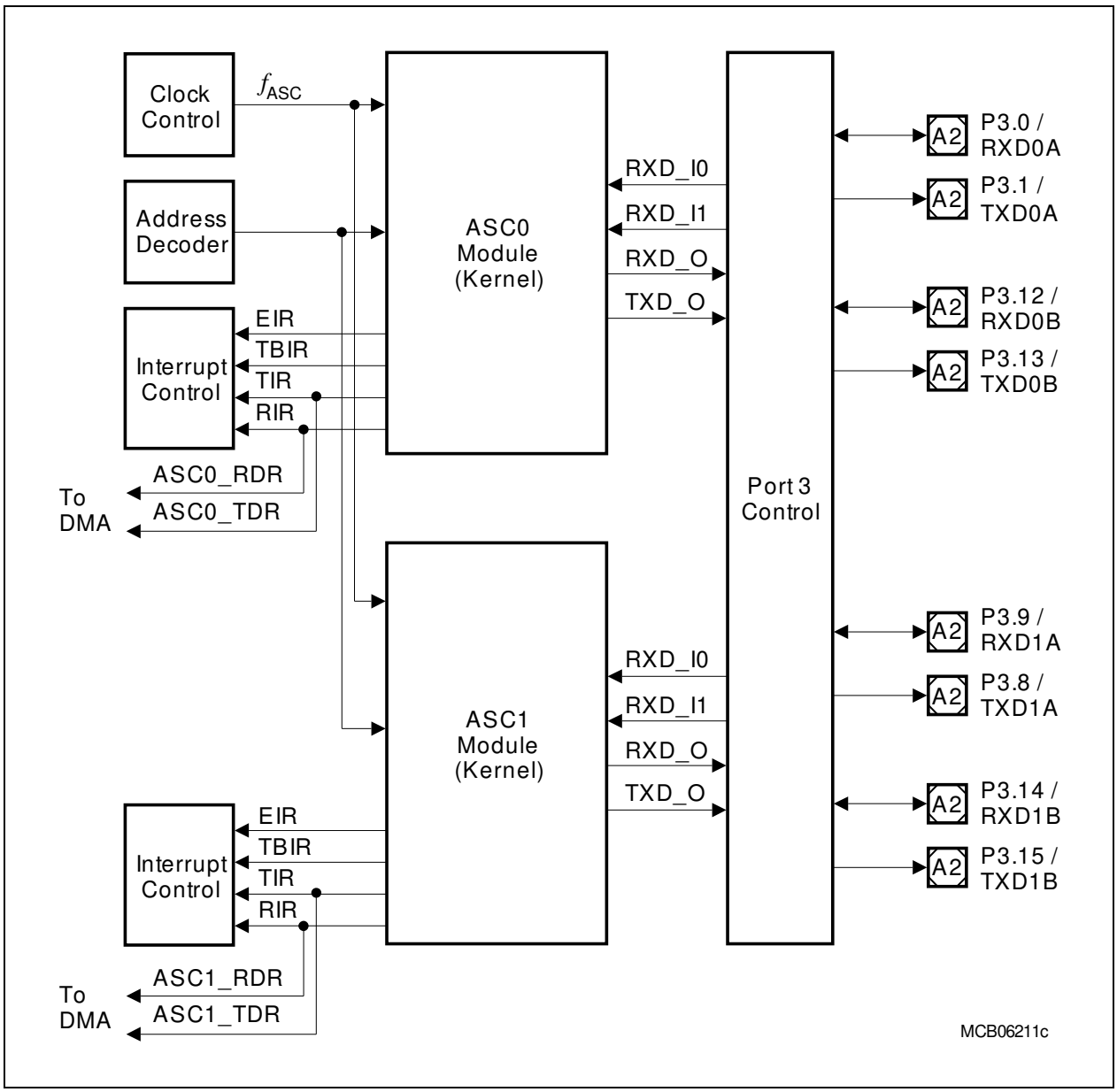


Figure 3-3 Block Diagram of the ASC Interfaces

The ASC provides serial communication between the TC1762 and other microcontrollers, microprocessors, or external peripherals.

The ASC supports full-duplex asynchronous communication and half-duplex synchronous communication. In Synchronous Mode, data is transmitted or received synchronous to a shift clock that is generated by the ASC internally. In Asynchronous Mode, 8-bit or 9-bit data transfer, parity generation, and the number of stop bits can be

selected. Parity, framing, and overrun error detection are provided to increase the reliability of data transfers. Transmission and reception of data is double-buffered. For multiprocessor communication, a mechanism is included to distinguish address bytes from data bytes. Testing is supported by a loop-back option. A 13-bit baud rate generator provides the ASC with a separate serial clock signal, which can be accurately adjusted by a prescaler implemented as fractional divider.

Features

- Full-duplex asynchronous operating modes
  - 8-bit or 9-bit data frames, LSB first
  - Parity-bit generation/checking
  - One or two stop bits
  - Baud rate from 5.0 Mbit/s to 1.19 bit/s (@ 80 MHz module clock) and 4.1Mbit/s to 0.98 bit/s (@ 66 MHz module clock)
  - Multiprocessor mode for automatic address/data byte detection
  - Loop-back capability
- Half-duplex 8-bit synchronous operating mode
  - Baud rate from 10.0 Mbit/s to 813.8 bit/s (@ 80 MHz module clock) and 8.25 Mbit/s to 671.4 bit/s (@ 66 MHz module clock)
- Double-buffered transmitter/receiver
- Interrupt generation
  - On a transmit buffer empty condition
  - On a transmit last bit of a frame condition
  - On a receive buffer full condition
  - On an error condition (frame, parity, overrun error)

3.8 High-Speed Synchronous Serial Interface (SSC0)

Figure 3-4 shows a global view of the functional blocks and interfaces of the high-speed Synchronous Serial Interface, SSC0.

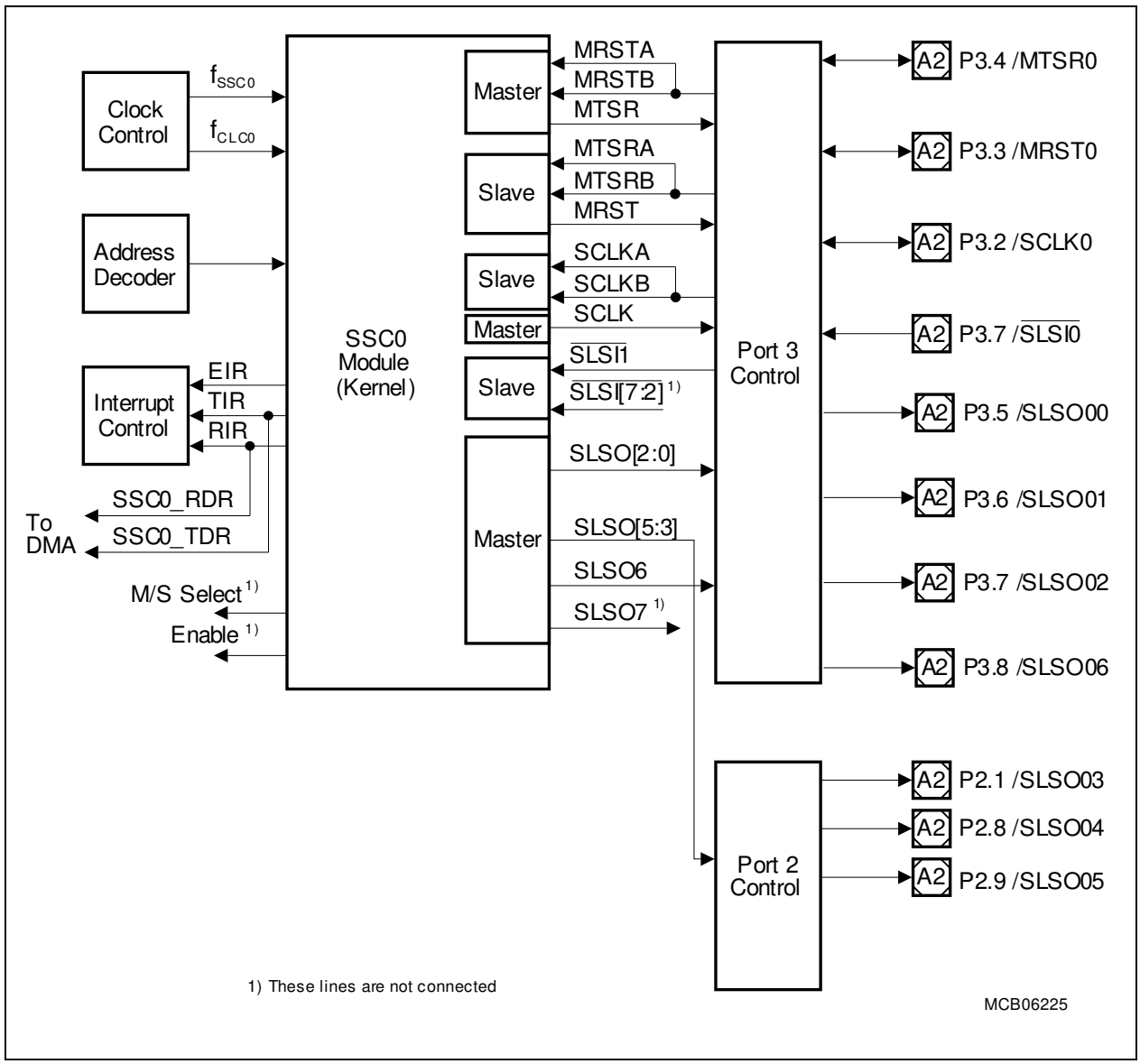


Figure 3-4 Block Diagram of the SSC Interfaces

The SSC supports full-duplex and half-duplex serial synchronous communication up to 40.0 MBaud at 80 MHz module clock and up to 33 MBaud at 66 MHz module clock. The serial clock signal can be generated by the SSC itself (Master Mode) or can be received from an external master (Slave Mode). Data width, shift direction, clock polarity and phase are programmable. This allows communication with SPI-compatible devices. Transmission and reception of data is double-buffered. A shift clock generator provides the SSC with a separate serial clock signal. Seven slave select inputs are available for

Slave Mode operation. Eight programmable slave select outputs (chip selects) are supported in Master Mode.

Features

- Master and Slave Mode operation
  - Full-duplex or half-duplex operation
  - Automatic pad control possible
- Flexible data format
  - Programmable number of data bits: 2 to 16 bits
  - Programmable shift direction: LSB or MSB shift first
  - Programmable clock polarity: Idle low or idle high state for the shift clock
  - Programmable clock/data phase: Data shift with leading or trailing edge of the shift clock
- Baud rate generation from 40.0 Mbit/s to 610.36 bit/s (@ 80 MHz module clock) and 503.5 bit/s to 33 Mbit/s (@ 66 MHz module clock)
- Interrupt generation
  - On a transmitter empty condition
  - On a receiver full condition
  - On an error condition (receive, phase, baud rate, transmit error)
- Flexible SSC pin configuration
- Seven slave select inputs $\overline{\text{SLSI}}$[7:1] in Slave Mode
- Eight programmable slave select outputs SLSO[7:0] in Master Mode
  - Automatic SLSO generation with programmable timing
  - Programmable active level and enable control

3.9 Micro Second Bus Interface (MSC0)

The MSC interface provides a serial communication link typically used to connect power switches or other peripheral devices. The serial communication link includes a fast synchronous downstream channel and a slow asynchronous upstream channel. **Figure 3-5** shows a global view of the MSC interface signals.

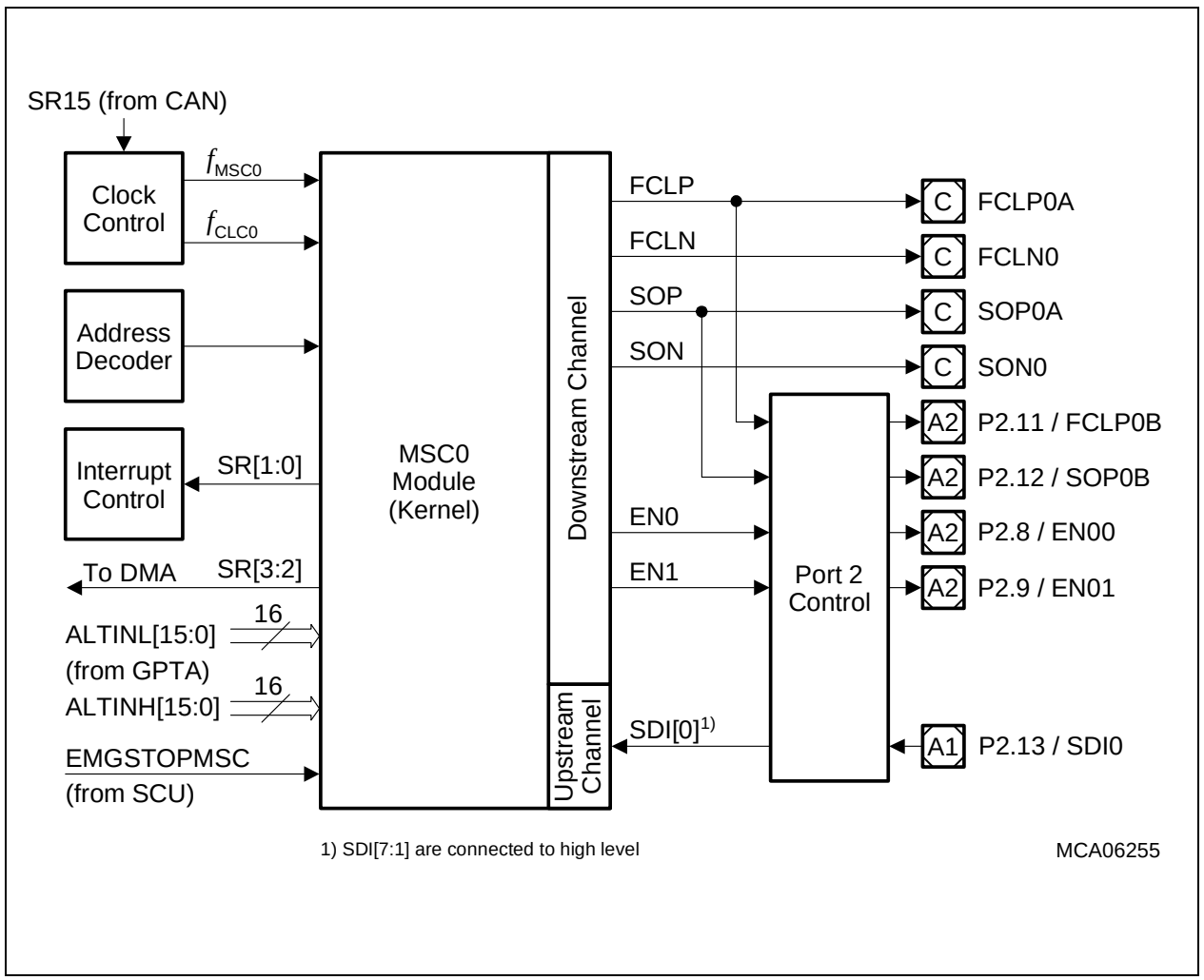


Figure 3-5 Block Diagram of the MSC Interfaces

The downstream and upstream channels of the MSC module communicate with the external world via nine I/O lines. Eight output lines are required for the serial communication of the downstream channel (clock, data, and enable signals). One out of eight input lines SDI[7:0] is used as serial data input signal for the upstream channel. The source of the serial data to be transmitted by the downstream channel can be MSC register contents or data that is provided at the ALTINL/ALTINH input lines. These input lines are typically connected to other on-chip peripheral units (for example with a timer unit like the GPTA). An emergency stop input signal makes it possible to set bits of the serial data stream to dedicated values in emergency cases.

Clock control, address decoding, and interrupt service request control are managed outside the MSC module kernel. Service request outputs are able to trigger an interrupt or a DMA request.

Features

- Fast synchronous serial interface to connect power switches in particular, or other peripheral devices via serial buses
- High-speed synchronous serial transmission on downstream channel
  - Serial output clock frequency: $f_{FCL} = f_{MSC}/2$
  - Fractional clock divider for precise frequency control of serial clock f_{MSC}
  - Command, data, and passive frame types
  - Start of serial frame: Software-controlled, timer-controlled, or free-running
  - Programmable upstream data frame length (16 or 12 bits)
  - Transmission with or without SEL bit
  - Flexible chip select generation indicates status during serial frame transmission
  - Emergency stop without CPU intervention
- Low-speed asynchronous serial reception on upstream channel
  - Baud rate: f_{MSC} divided by 4, 8, 16, 32, 64, 128, or 256
  - Standard asynchronous serial frames
  - Parity error checker
  - 8-to-1 input multiplexer for SDI lines
  - Built-in spike filter on SDI lines

3.10 MultiCAN Controller (CAN)

Figure 3-6 shows a global view of the MultiCAN module with its functional blocks and interfaces.

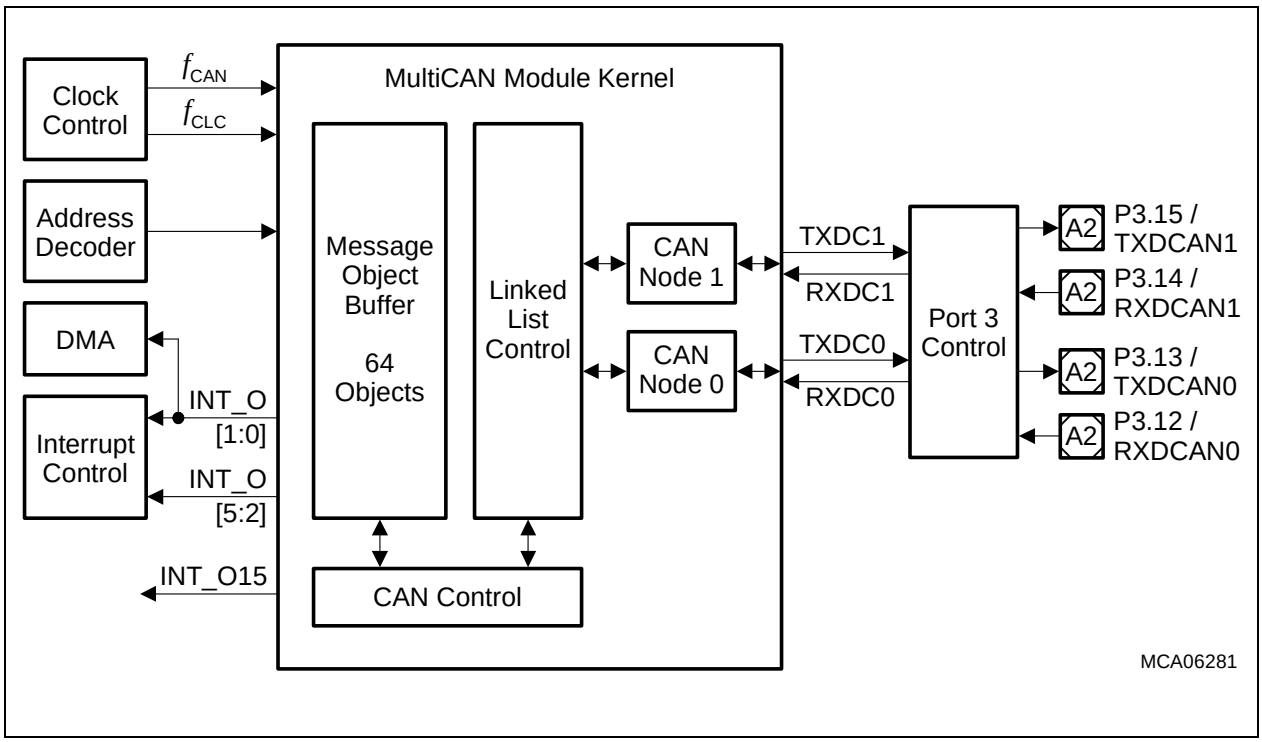


Figure 3-6 Block Diagram of MultiCAN Module

The MultiCAN module contains two independently-operating CAN nodes with Full-CAN functionality that are able to exchange Data and Remote Frames via a gateway function. Transmission and reception of CAN frames is handled in accordance with CAN specification V2.0 B (active). Each CAN node can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers.

Both CAN nodes share a common set of message objects. Each message object can be individually allocated to one of the CAN nodes. Besides serving as a storage container for incoming and outgoing frames, message objects can be combined to build gateways between the CAN nodes or to setup a FIFO buffer.

The message objects are organized in double-chained linked lists, where each CAN node has its own list of message objects. A CAN node stores frames only into message objects that are allocated to the message object list of the CAN node, and it transmits only messages belonging to this message object list. A powerful, command-driven list controller performs all message object list operations.

The bit timings for the CAN nodes are derived from the module timer clock (f_{CAN}), and are programmable up to a data rate of 1 Mbit/s. External bus transceivers are connected to a CAN node via a pair of receive and transmit pins.

MultiCAN Features

- CAN functionality conforms to CAN specification V2.0 B active for each CAN node (compliant to ISO 11898)
- Two independent CAN nodes
- 64 independent message objects (shared by the CAN nodes)
- Dedicated control registers for each CAN node
- Data transfer rate up to 1Mbit/s, individually programmable for each node
- Flexible and powerful message transfer control and error handling capabilities
- Full-CAN functionality: message objects can be individually
  - assigned to one of the two CAN nodes
  - configured as transmit or receive object
  - configured as message buffer with FIFO algorithm
  - configured to handle frames with 11-bit or 29-bit identifiers
  - provided with programmable acceptance mask register for filtering
  - monitored via a frame counter
  - configured for Remote Monitoring Mode
- Automatic Gateway Mode support
- 6 individually programmable interrupt nodes
- CAN analyzer mode for bus monitoring

3.11 Micro Link Serial Bus Interface (MLI0)

The Micro Link Interface is a fast synchronous serial interface that allows data exchange between microcontrollers of the 32-bit AUDO microcontroller family without intervention of a CPU or other bus masters. **Figure 3-7** shows how two microcontrollers are typically connected together via their MLI interface. The MLI operates in both microcontrollers as a bus master on the system bus.

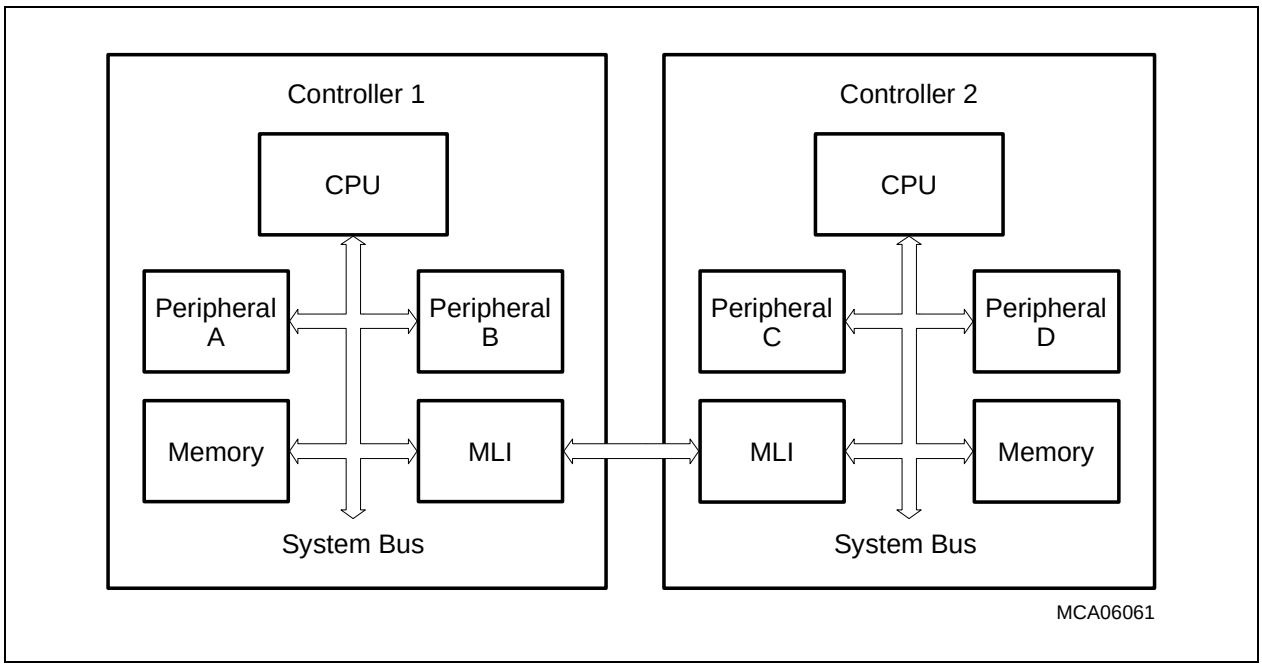


Figure 3-7 Typical Micro Link Interface Connection

Features

- Synchronous serial communication between MLI transmitters and MLI receivers located on the same or on different microcontroller devices
- Automatic data transfer/request transactions between local/remote controller
- Fully transparent read/write access supported (= remote programming)
- Complete address range of remote controller available
- Specific frame protocol to transfer commands, addresses and data
- Error control by parity bit
- 32-bit, 16-bit, and 8-bit data transfers
- Programmable baud rates
  - MLI transmitter baud rate: max. $f_{MLI}/2$ (= 40 Mbit/s @ 80 MHz module clock)
  - MLI receiver baud rate: max. f_{MLI}
- Multiple remote (slave) controllers are supported

MLI transmitter and MLI receiver communicate with other off-chip MLI receivers and MLI transmitters via a 4-line serial I/O bus each. Several I/O lines of these I/O buses are available outside the MLI module kernel as four-line output or input buses.

Figure 3-8 shows a global view of the functional blocks of the MLI module with its interfaces.

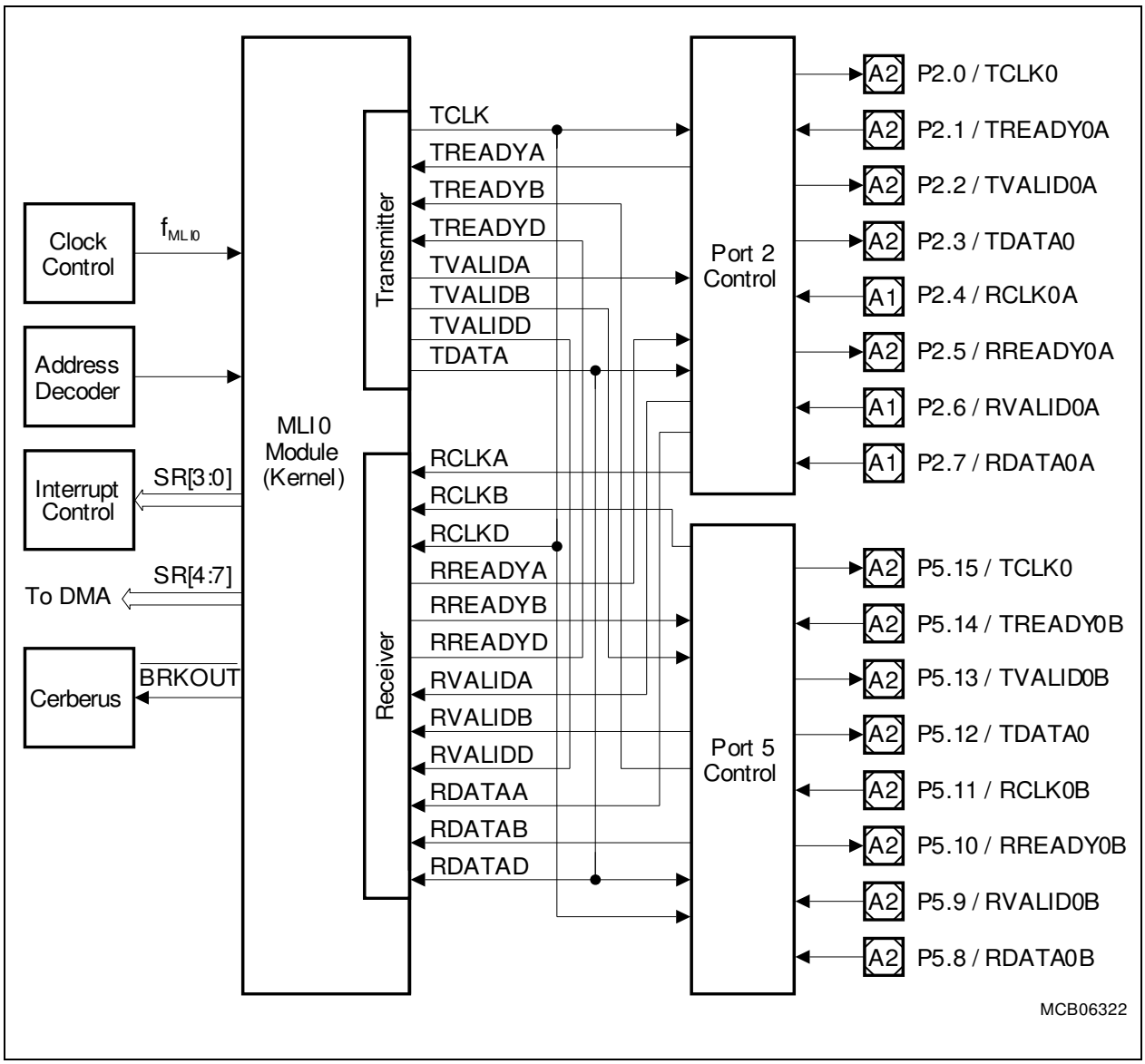


Figure 3-8 Block Diagram of the MLI Module

3.12 General Purpose Timer Array

The GPTA provides a set of timer, compare, and capture functionalities that can be flexibly combined to form signal measurement and signal generation units. They are optimized for tasks typical of engine, gearbox, electrical motor control applications, but can also be used to generate simple and complex signal waveforms needed in other industrial applications.

The TC1762 contains one General Purpose Timer Array (GPTA0). **Figure 3-9** shows a global view of the GPTA module.

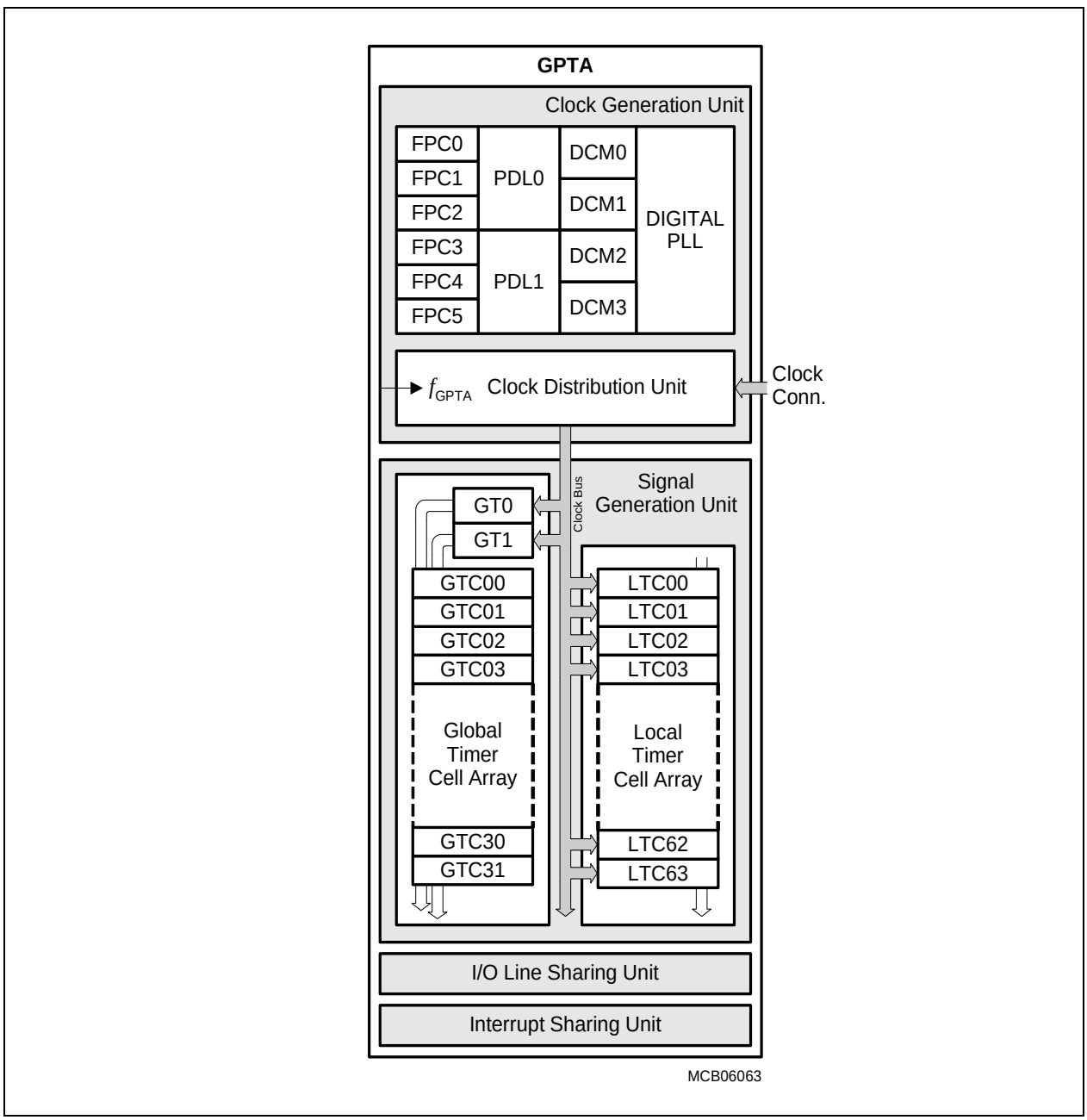


Figure 3-9 Block Diagram of the GPTA Module

3.12.1 Functionality of GPTA0

The General Purpose Timer Array GPTA0 provides a set of hardware modules required for high-speed digital signal processing:

- Filter and Prescaler Cells (FPC) support input noise filtering and prescaler operation.
- Phase Discrimination Logic units (PDL) decode the direction information output by a rotation tracking system.
- Duty Cycle Measurement Cells (DCM) provide pulse-width measurement capabilities.
- A Digital Phase Locked Loop unit (PLL) generates a programmable number of GPTA module clock ticks during an input signal's period.
- Global Timer units (GT) driven by various clock sources are implemented to operate as a time base for the associated Global Timer Cells.
- Global Timer Cells (GTC) can be programmed to capture the contents of a Global Timer on an external or internal event. A GTC may also be used to control an external port pin depending on the result of an internal compare operation. GTCs can be logically concatenated to provide a common external port pin with a complex signal waveform.
- Local Timer Cells (LTC) operating in Timer, Capture, or Compare Mode may also be logically tied together to drive a common external port pin with a complex signal waveform. LTCs — enabled in Timer Mode or Capture Mode — can be clocked or triggered by various external or internal events.

Input lines can be shared by an LTC and a GTC to trigger their programmed operation simultaneously.

The following list summarizes the specific features of the GPTA unit.

Clock Generation Unit

- Filter and Prescaler Cell (FPC)
  - Six independent units
  - Three basic operating modes:
    Prescaler, Delayed Debounce Filter, Immediate Debounce Filter
  - Selectable input sources:
    Port lines, GPTA module clock, FPC output of preceding FPC cell
  - Selectable input clocks:
    GPTA module clock, prescaled GPTA module clock, DCM clock, compensated or uncompensated PLL clock
  - $f_{GPTA}/2$ maximum input signal frequency in Filter Modes
- Phase Discriminator Logic (PDL)
  - Two independent units
  - Two operating modes (2- and 3-sensor signals)
  - $f_{GPTA}/4$ maximum input signal frequency in 2-sensor Mode, $f_{GPTA}/6$ maximum input signal frequency in 3-sensor Mode

- Duty Cycle Measurement (DCM)
  - Four independent units
  - 0 - 100% margin and time-out handling
  - f_{GPTA} maximum resolution
  - f_{GPTA}/2 maximum input signal frequency
- Digital Phase Locked Loop (PLL)
  - One unit
  - Arbitrary multiplication factor between 1 and 65535
  - f_{GPTA} maximum resolution
  - f_{GPTA}/2 maximum input signal frequency
- Clock Distribution Unit (CDU)
  - One unit
  - Provides nine clock output signals:
    f_{GPTA}, divided f_{GPTA} clocks, FPC1/FPC4 outputs, DCM clock, LTC prescaler clock

Signal Generation Unit

- Global Timers (GT)
  - Two independent units
  - Two operating modes (Free-Running Timer and Reload Timer)
  - 24-bit data width
  - f_{GPTA} maximum resolution
  - f_{GPTA}/2 maximum input signal frequency
- Global Timer Cell (GTC)
  - 32 units related to the Global Timers
  - Two operating modes (Capture, Compare and Capture after Compare)
  - 24-bit data width
  - f_{GPTA} maximum resolution
  - f_{GPTA}/2 maximum input signal frequency
- Local Timer Cell (LTC)
  - 64 independent units
  - Three basic operating modes (Timer, Capture and Compare) for 63 units
  - Special compare modes for one unit
  - 16-bit data width
  - f_{GPTA} maximum resolution
  - f_{GPTA}/2 maximum input signal frequency

Interrupt Control Unit

- 111 interrupt sources, generating up to 38 service requests

I/O Sharing Unit

- Interconnecting inputs and outputs from internal clocks, FPC, GTC, LTC, ports, and MSC interface

3.13 Analog-to-Digital Converter (ADC0)

Section 3.13 shows the global view of the ADC module with its functional blocks and interfaces and the features which are provided by the module.

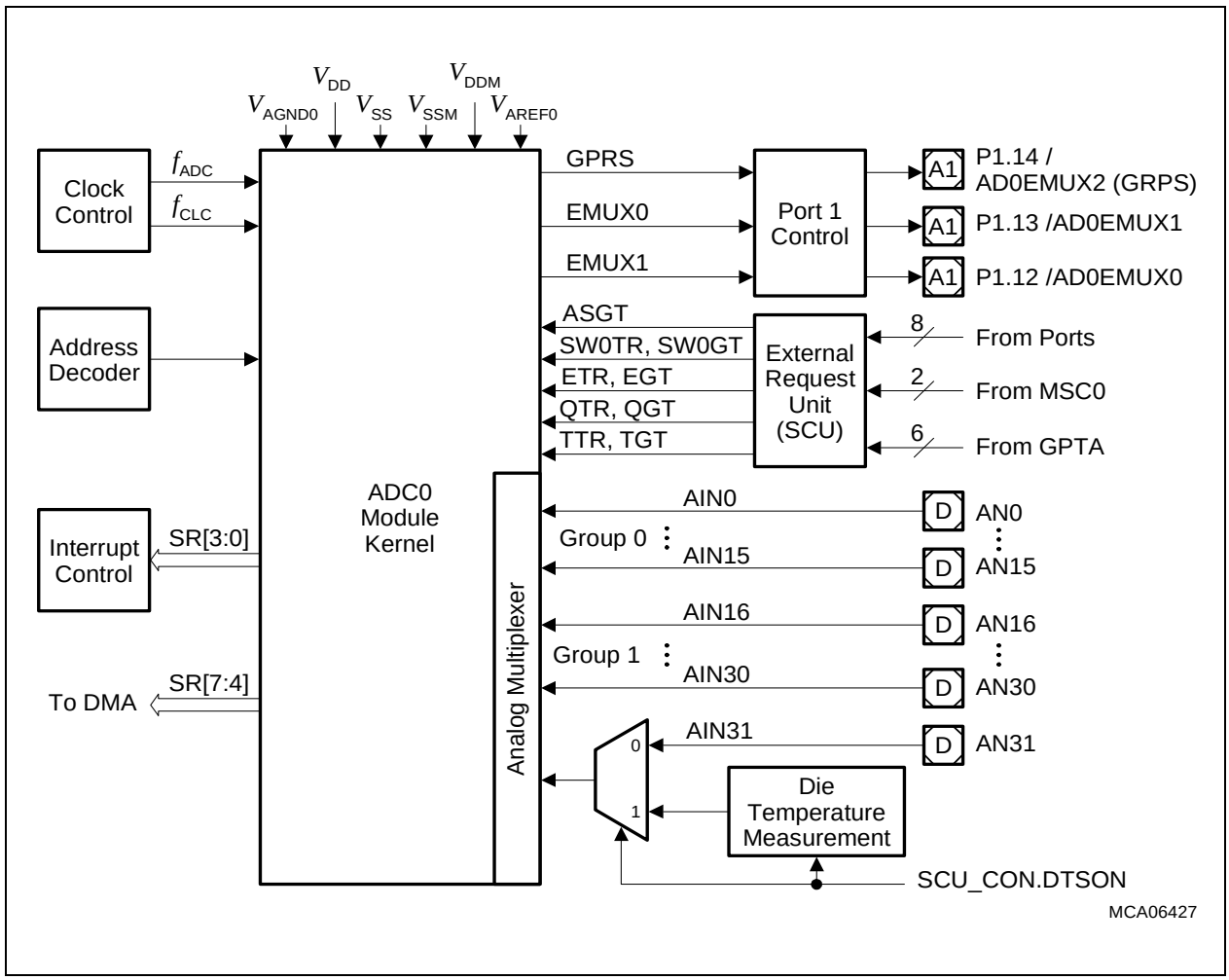


Figure 3-10 Block Diagram of the ADC Module

The ADC module has 16 analog input channels. An analog multiplexer selects the input line for the analog input channels from among 32 analog inputs. Additionally, an external analog multiplexer can be used for analog input extension. External Clock control, address decoding, and service request (interrupt) control are managed outside the ADC module kernel. External trigger conditions are controlled by an External Request Unit. This unit generates the control signals for auto-scan control (ASGT), software trigger control (SW0TR, SW0GT), the event trigger control (ETR, EGT), queue control (QTR, QGT), and timer trigger control (TTR, TGT).

An automatic self-calibration adjusts the ADC module to changing temperatures or process variations. Figure 3-10 shows the global view of the ADC module with its functional blocks and interfaces.

Features

- 8-bit, 10-bit, 12-bit A/D conversion
- Conversion time below 2.5µs @ 10-bit resolution
- Extended channel status information on request source
- Successive approximation conversion method
- Total Unadjusted Error (TUE) of ±2 LSB @ 10-bit resolution
- Integrated sample & hold functionality
- Direct control of up to 16 analog input channels
- Dedicated control and status registers for each analog channel
- Powerful conversion request sources
- Selectable reference voltages for each channel
- Programmable sample and conversion timing schemes
- Limit checking
- Flexible ADC module service request control unit
- Automatic control of external analog multiplexers
- Equidistant samples initiated by timer
- External trigger and gating inputs for conversion requests
- Power reduction and clock control feature
- On-chip die temperature sensor output voltage measurement

3.14 Fast Analog-to-Digital Converter Unit (FADC)

The on-chip FADC module of the TC1762 basically is a 2-channel A/D converter with 10-bit resolution that operates by the method of the successive approximation.

As shown in **Figure 3-11**, the main FADC functional blocks are:

- The Input Stage — contains the differential inputs and the programmable amplifier
- The A/D Converter — is responsible for the analog-to-digital conversion
- The Data Reduction Unit — contains programmable antialiasing and data reduction filters
- The Channel Trigger Control block — determines the trigger and gating conditions for the two FADC channels
- The Channel Timers — can independently trigger the conversion of each FADC channel
- The A/D Control block is responsible for the overall FADC functionality

The FADC module is supplied by the following power supply and reference voltage lines:

- V_{DDMF}/V_{DDMF}:FADC Analog Part Power Supply (3.3 V)
- V_{DDAF}/V_{DDAF}:FADC Analog Part Logic Power Supply (1.5 V)
- V_{FAREF}/V_{FAGND}:FADC Reference Voltage (3.3 V)/FADC Reference Ground

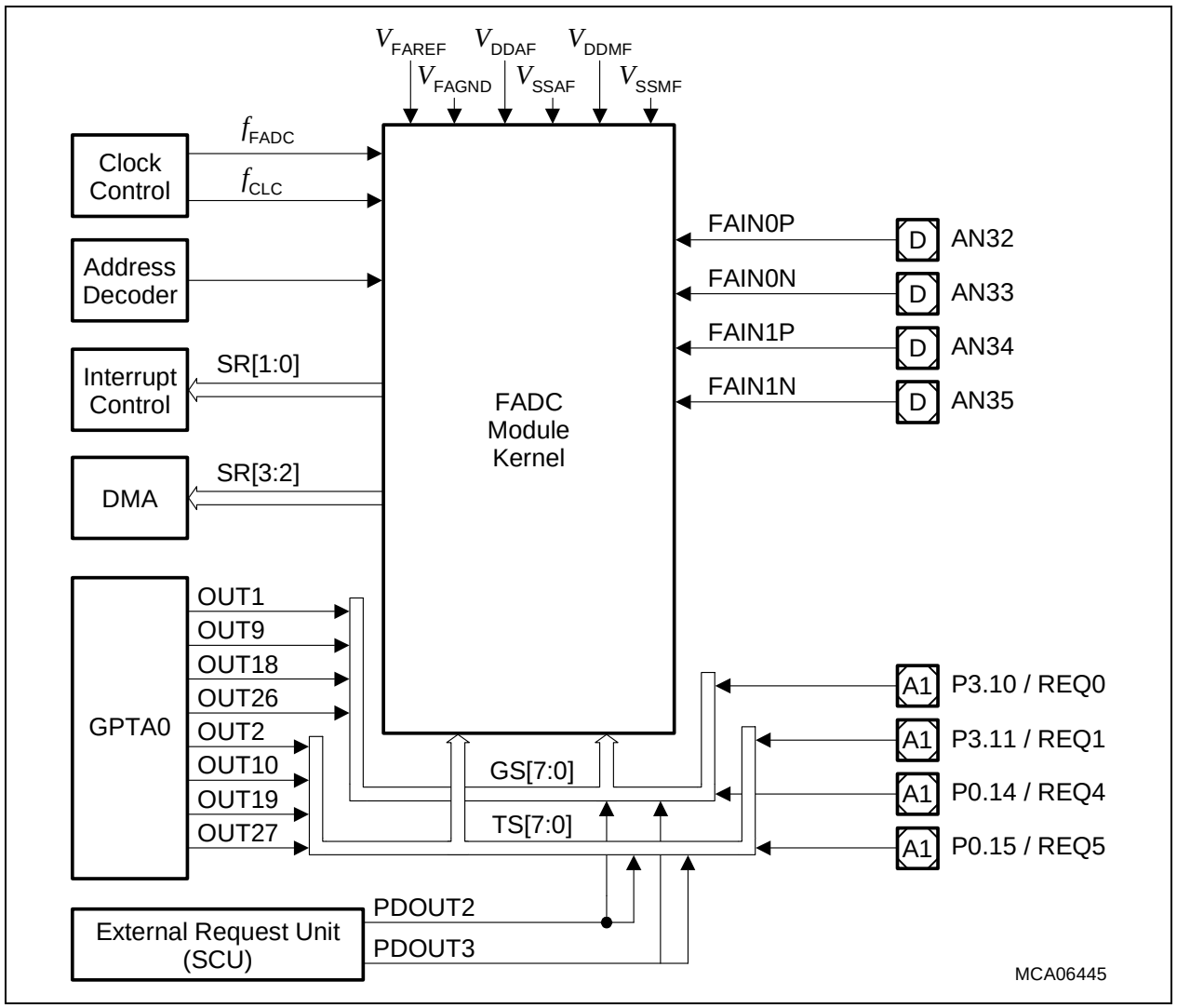


Figure 3-11 Block Diagram of the FADC Module

Features

- Extreme fast conversion, 21 cycles of f_{FADC} clock (262.5 ns @ f_{FADC} = 80 MHz and 318.2 ns @ f_{FADC} = 66 MHz)
- 10-bit A/D conversion
  - Higher resolution by averaging of consecutive conversions is supported
- Successive approximation conversion method
- Two differential input channels
- Offset and gain calibration support for each channel
- Differential input amplifier with programmable gain of 1, 2, 4 and 8 for each channel
- Free-running (Channel Timers) or triggered conversion modes
- Trigger and gating control for external signals
- Built-in Channel Timers for internal triggering
- Channel timer request periods independently selectable for each channel

- Selectable, programmable anti-aliasing and data reduction filter block

3.15 System Timer

The TC1762's STM is designed for global system timing applications requiring both high precision and long period.

Features

- Free-running 56-bit counter
- All 56 bits can be read synchronously
- Different 32-bit portions of the 56-bit counter can be read synchronously
- Flexible interrupt generation based on compare match with partial STM content
- Driven by maximum 66 or 80 MHz (= f_{SYS}, default after reset = $f_{SYS}/2$) depending on derivative
- Counting starts automatically after a reset operation
- STM is reset by:
  - Watchdog reset
  - Software reset (RST_REQ.RRSTM must be set)
  - Power-on reset
- STM (and clock divider STM_CLC.RMC) is not reset at a hardware reset ($\overline{\text{HDRST}}$ = 0)
- STM can be halted in debug/suspend mode (via STM_CLC register)

The STM is an upward counter, running either at the system clock frequency f_{SYS} or at a fraction of it. The STM clock frequency is $f_{STM} = f_{SYS}$/RMC with RMC = 0-7 (default after reset is $f_{STM} = f_{SYS}/2$, selected by RMC = $010_{B)}$. RMC is a bit field in register STM_CLC. In case of a power-on reset, a watchdog reset, or a software reset, the STM is reset. After one of these reset conditions, the STM is enabled and immediately starts counting up. It is not possible to affect the content of the timer during normal operation of the TC1762. The timer registers can only be read but not written to.

The STM can be optionally disabled for power-saving purposes, or suspended for debugging purposes via its clock control register. In suspend mode of the TC1762 (initiated by writing an appropriate value to STM_CLC register), the STM clock is stopped but all registers are still readable.

Due to the 56-bit width of the STM, it is not possible to read its entire content with one instruction. It needs to be read with two load instructions. Since the timer would continue to count between the two load operations, there is a chance that the two values read are not consistent (due to possible overflow from the low part of the timer to the high part between the two read operations). To enable a synchronous and consistent reading operation of the STM content, a capture register (STM_CAP) is implemented. It latches the content of the high part of the STM each time when one of the registers STM_TIM0 to STM_TIM5 is read. Thus, STM_CAP holds the upper value of the timer at exactly the

same time when the lower part is read. The second read operation would then read the content of the STM_CAP to get the complete timer value.

The STM can also be read in sections from seven registers, STM_TIM0 through STM_TIM6, that select increasingly higher-order 32-bit ranges of the STM. These can be viewed as individual 32-bit timers, each with a different resolution and timing range.

The content of the 56-bit System Timer can be compared with the content of two compare values stored in the STM_CMP0 and STM_CMP1 registers. Interrupts can be generated on a compare match of the STM with the STM_CMP0 or STM_CMP1 registers.

The maximum clock period is $2^{56} \times f_{STM}$. At f_{STM} = 80 MHz, for example, the STM counts 28.56 years before overflowing. Thus, it is capable of timing the entire expected product life-time of a system without overflowing continuously.

Figure 3-12 shows an overview on the System Timer with the options for reading parts of the STM contents.

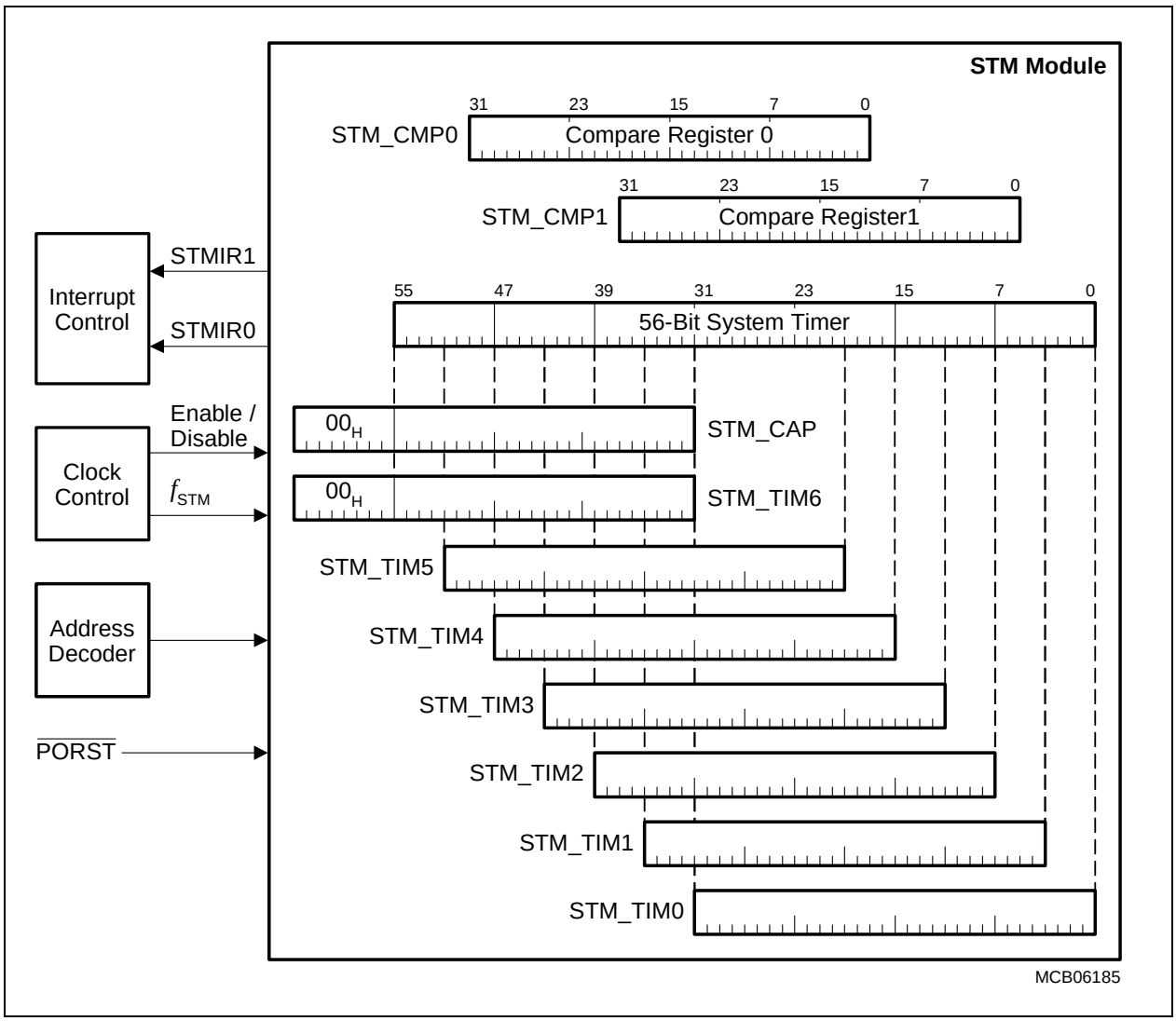


Figure 3-12 General Block Diagram of the STM Module Registers

3.16 Watchdog Timer

The WDT provides a highly reliable and secure way to detect and recover from software or hardware failure. The WDT helps to abort an accidental malfunction of the TC1762 in a user-specified time period. When enabled, the WDT will cause the TC1762 system to be reset if the WDT is not serviced within a user-programmable time period. The CPU must service the WDT within this time interval to prevent the WDT from causing a TC1762 system reset. Hence, routine service of the WDT confirms that the system is functioning as expected.

In addition to this standard “Watchdog” function, the WDT incorporates the End-of-Initialization (Endinit) feature and monitors its modifications. A system-wide line is connected to the WDT_CON0.ENDINIT bit, serving as an additional write-protection for critical registers (besides Supervisor Mode protection). Registers protected via this line can only be modified when Supervisor Mode is active and bit ENDINIT = 0.

A further enhancement in the TC1762’s WDT is its reset prewarning operation. Instead of resetting the device upon the detection of an error immediately (the way that standard Watchdogs do), the WDT first issues a Non-Maskable Interrupt (NMI) to the CPU before resetting the device at a specified time period later. This step gives the CPU a chance to save the system state to the memory for later investigation of the cause of the malfunction; an important aid in debugging.

Features

- 16-bit Watchdog counter
- Selectable input frequency: $f_{SYS}/256$ or $f_{SYS}/16384$
- 16-bit user-definable reload value for normal Watchdog operation, fixed reload value for Time-Out and Prewarning Modes
- Incorporation of the ENDINIT bit and monitoring of its modifications
- Sophisticated Password Access mechanism with fixed and user-definable password fields
- Proper access always requires two write accesses. The time between the two accesses is monitored by the WDT and is limited.
- Access Error Detection: Invalid password (during first access) or invalid guard bits (during second access) trigger the Watchdog reset generation
- Overflow Error Detection: An overflow of the counter triggers the Watchdog reset generation.
- Watchdog function can be disabled; access protection and ENDINIT monitor function remain enabled.
- Double Reset Detection: If a Watchdog induced reset occurs twice, a severe system malfunction is assumed and the TC1762 is held in reset until a power-on or hardware reset occurs. This prevents the device from being periodically reset if, for instance, connection to the external memory has been lost such that system initialization could not even be performed.

- Important debugging support is provided through the reset prewarning operation by first issuing an NMI to the CPU before finally resetting the device after a certain period of time.

3.17 System Control Unit

The System Control Unit (SCU) of the TC1762 handles several system control tasks. The system control tasks of the SCU are:

- Clock system selection and control
- Reset and boot operation control
- Power management control
- Configuration input sampling
- External Request Unit
- System clock output control
- On-chip SRAM parity control
- Pad driver temperature compensation control
- Emergency stop input control for GPTA outputs
- GPTA input IN1 control
- Pad test mode control for dedicated pins
- ODCS level 2 trace control
- NMI control
- Miscellaneous SCU control

3.18 Boot Options

The TC1762 booting schemes provide a number of different boot options for the start of code execution. **Table 3-2** shows the boot options available in the TC1762.

Table 3-2 TC1762 Boot Selections

BRKIN	HWCFG [3:0]	TESTMODE	Type of Boot	BootROM Exit Jump Address
Normal Boot Options				
1	0000_B	1	Enter bootstrap loader mode 1: Serial ASC0 boot via ASC0 pins	D400 0000_H
	0001_B		Enter bootstrap loader mode 2: Serial CAN boot via P3.12 and P3.13 pins	
	0010_B		Start from internal PFLASH	A000 0000_H
	0011_B		Alternate boot mode (ABM): Start from internal PFLASH after CRC check is correctly executed; enter a serial bootstrap loader mode[1] if CRC check fails	Defined in ABM header or D400 0000_H
	1111_B		Enter bootstrap loader mode 3: Serial ASC0 boot via P3.12 and P3.13 pins	D400 0000_H
	others		Reserved; execute stop loop	–
Debug Boot Options				
0	0000_B	1	Tri-state chip	–
	others	irrel.	Reserved; execute stop loop	–

1) The type of the alternate bootstrap loader mode is selected by the value of the SCU_SCLIR.SWOPT[2:0] bit field, which contains the levels of the P0.[2:0] latched in with the rising edge of the HDRST.

3.19 Power Management System

The TC1762 power management system allows software to configure the various processing units so that they automatically adjust to draw the minimum necessary power for the application. There are three power management modes:

- Run Mode
- Idle Mode
- Sleep Mode

The operation of each system component in each of these states can be configured by software. The power-management modes provide flexible reduction of power consumption through a combination of techniques, including stopping the CPU clock, stopping the clocks of other system components individually, and individually clock-speed reduction of some peripheral components.

Besides these explicit software-controlled power-saving modes, special attention has been paid to automatic power-saving in those operating units which are not required at a certain point of time, or idle in the TC1762. In that case, they are shut off automatically until their operation is required again.

Table 3-3 describes the features of the power management modes.

Table 3-3 Power Management Mode Summary

Mode	Description
Run	The system is fully operational. All clocks and peripherals are enabled, as determined by software.
Idle	The CPU clock is disabled, waiting for a condition to return it to Run Mode. Idle Mode can be entered by software when the processor has no active tasks to perform. All peripherals remain powered and clocked. Processor memory is accessible to peripherals. A reset, Watchdog Timer event, a falling edge on the NMI pin, or any enabled interrupt event will return the system to Run Mode.
Sleep	The system clock signal is distributed only to those peripherals programmed to operate in Sleep Mode. The other peripheral module will be shut down by the suspend signal. Interrupts from operating peripherals, the Watchdog Timer, a falling edge on the NMI pin, or a reset event will return the system to Run Mode. Entering this state requires an orderly shut-down controlled by the Power Management State Machine.

In typical operation, Idle Mode and Sleep Mode may be entered and exited frequently during the run time of an application. For example, system software will typically cause the CPU to enter Idle Mode each time it has to wait for an interrupt before continuing its tasks. In Sleep Mode and Idle Mode, wake-up is performed automatically when any

enabled interrupt signal is detected, or when the count value (WDT_SR.WDTTIM) changes from $7FFF_H$ to 8000_H.

3.20 On-Chip Debug Support

Figure 3-13 shows a block diagram of the TC1762 OCDS system.

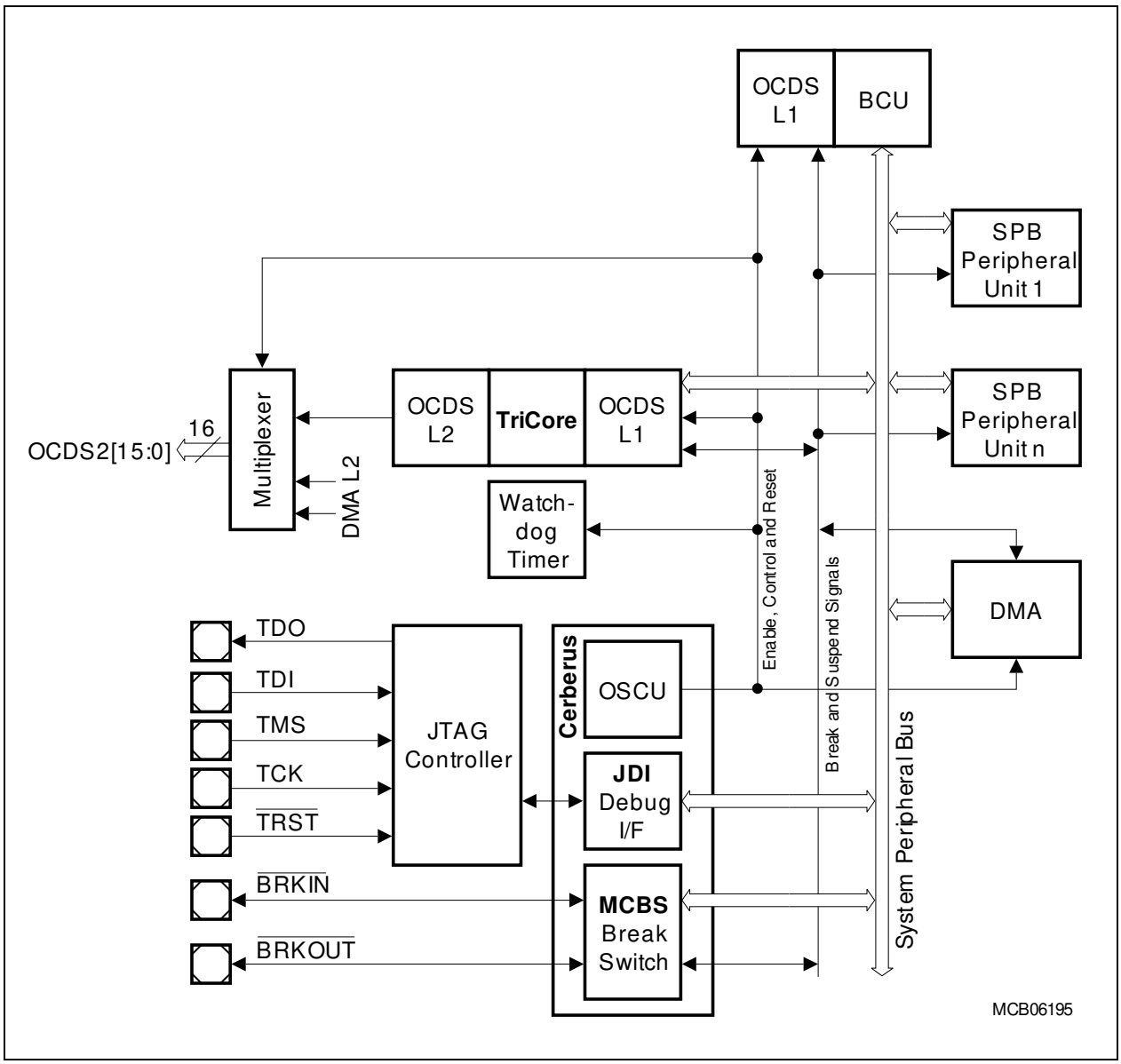


Figure 3-13 OCDS System Block Diagram

The TC1762 basically supports three levels of debug operation:

- OCDS Level 1 debug support
- OCDS Level 2 debug support
- OCDS Level 3 debug support

OCDS Level 1 Debug Support

The OCDS Level 1 debug support is mainly assigned for real-time software debugging purposes which have a demand for low-cost standard debugger hardware.

The OCDS Level 1 is based on a JTAG interface that is used by the external debug hardware to communicate with the system. The on-chip Cerberus module controls the interactions between the JTAG interface and the on-chip modules. The external debug hardware may become master of the internal buses, and read or write the on-chip register/memory resources. The Cerberus also makes it possible to define breakpoint and trigger conditions as well as to control user program execution (run/stop, break, single-step).

OCDS Level 2 Debug Support

The OCDS Level 2 debug support makes it possible to implement program tracing capabilities for enhanced debuggers by extending the OCDS Level 1 debug functionality with an additional 16-bit wide trace output port with trace clock. With the trace extension, the following four trace capabilities are provided (only one of the three trace capabilities can be selected at a time):

- Trace of the CPU program flow
- Trace of the DMA Controller transaction requests
- Trace of the DMA Controller Move Engine status information

OCDS Level 3 Debug Support

The OCDS Level 3 debug support is based on a special TC1766 emulation device, the TC1766ED, which provides additional features required for high-end emulation purposes. The TC1766ED is a device which includes the TC1766 product chip and additional emulation extension hardware in a package with the same footprint as the TC1766.

3.21 Clock Generation and PLL

The TC1762 clock system performs the following functions:

- Acquires and buffers incoming clock signals to create a master clock frequency
- Distributes in-phase synchronized clock signals throughout the TC1762's entire clock tree
- Divides a system master clock frequency into lower frequencies required by the different modules for operation.
- Dynamically reduces power consumption during operation of functional units
- Statically reduces power consumption through programmable power-saving modes
- Reduces electromagnetic interference (EMI) by switching off unused modules

The clock system must be operational before the TC1762 can function, so it contains special logic to handle power-up and reset operations. Its services are fundamental to the operation of the entire system, so it contains special fail-safe logic.

Features

- PLL operation for multiplying clock source by different factors
- Direct drive capability for direct clocking
- Comfortable state machine for secure switching between basic PLL, direct or prescaler operation
- Sleep and Power-Down Mode support

The TC1762 Clock Generation Unit (CGU) as shown in **Figure 3-14** allows a very flexible clock generation. It basically consists of an main oscillator circuit and a Phase-Locked Loop (PLL). The PLL can converts a low-frequency external clock signal from the oscillator circuit to a high-speed internal clock for maximum performance.

The system clock f_{SYS} is generated from an oscillator clock f_{OSC} in either one of the four hardware/software selectable ways:

- **Direct Drive Mode (PLL Bypass)**:
  In Direct Drive Mode, the TC1762 clock system is directly driven by an external clock signal. input, i.e. $f_{CPU} = f_{OSC}$ and $f_{SYS} = f_{OSC}$. This allows operation of the TC1762 with a reasonably small fundamental mode crystal.
- **VCO Bypass Mode (Prescaler Mode)**:
  In VCO Bypass Mode, f_{CPU} and f_{SYS} are derived from f_{OSC} by the two divider stages, P-Divider and K-Divider. The system clock f_{SYS} is equal to f_{CPU}.
- **PLL Mode:**
  In PLL Mode, the PLL is running. The VCO clock f_{VCO} is derived from f_{OSC}, divided by the P factor, multiplied by the PLL (N-Divider). The clock signals f_{CPU} and f_{SYS} are derived from f_{VCO} by the K-Divider. The system clock f_{SYS} is equal to f_{CPU}.
- **PLL Base Mode**:
  In PLL Base Mode, the PLL is running at its VCO base frequency and f_{CPU} and f_{SYS}

are derived from f_{VCO} only by the K-Divider. In this mode, the system clock f_{SYS} is equal to f_{CPU}.

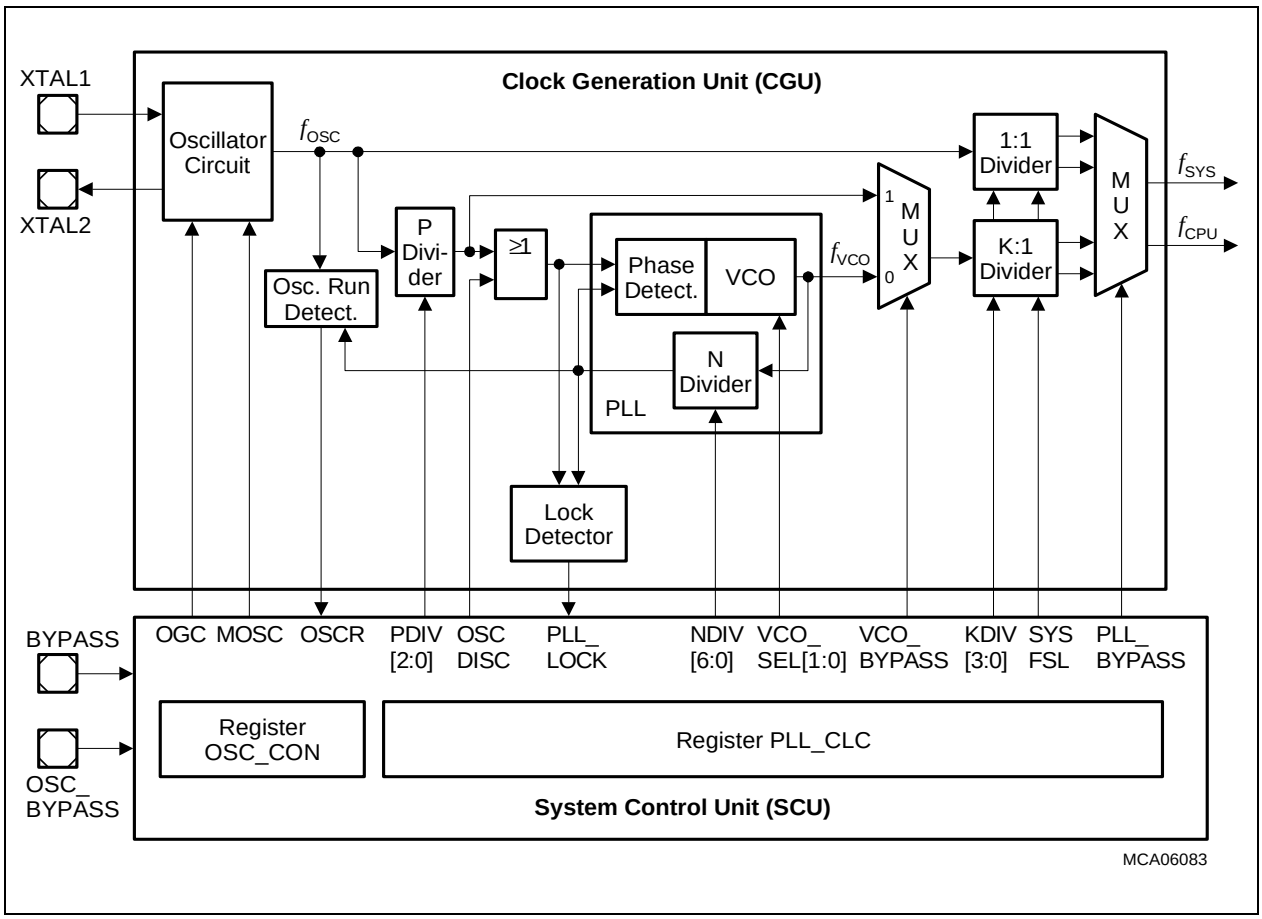


Figure 3-14 Clock Generation Unit

Recommended Oscillator Circuits

The oscillator circuit, a Pierce oscillator, is designed to work with both, an external crystal oscillator or an external stable clock source. It basically consists of an inverting amplifier and a feedback element with XTAL1 as input, and XTAL2 as output.

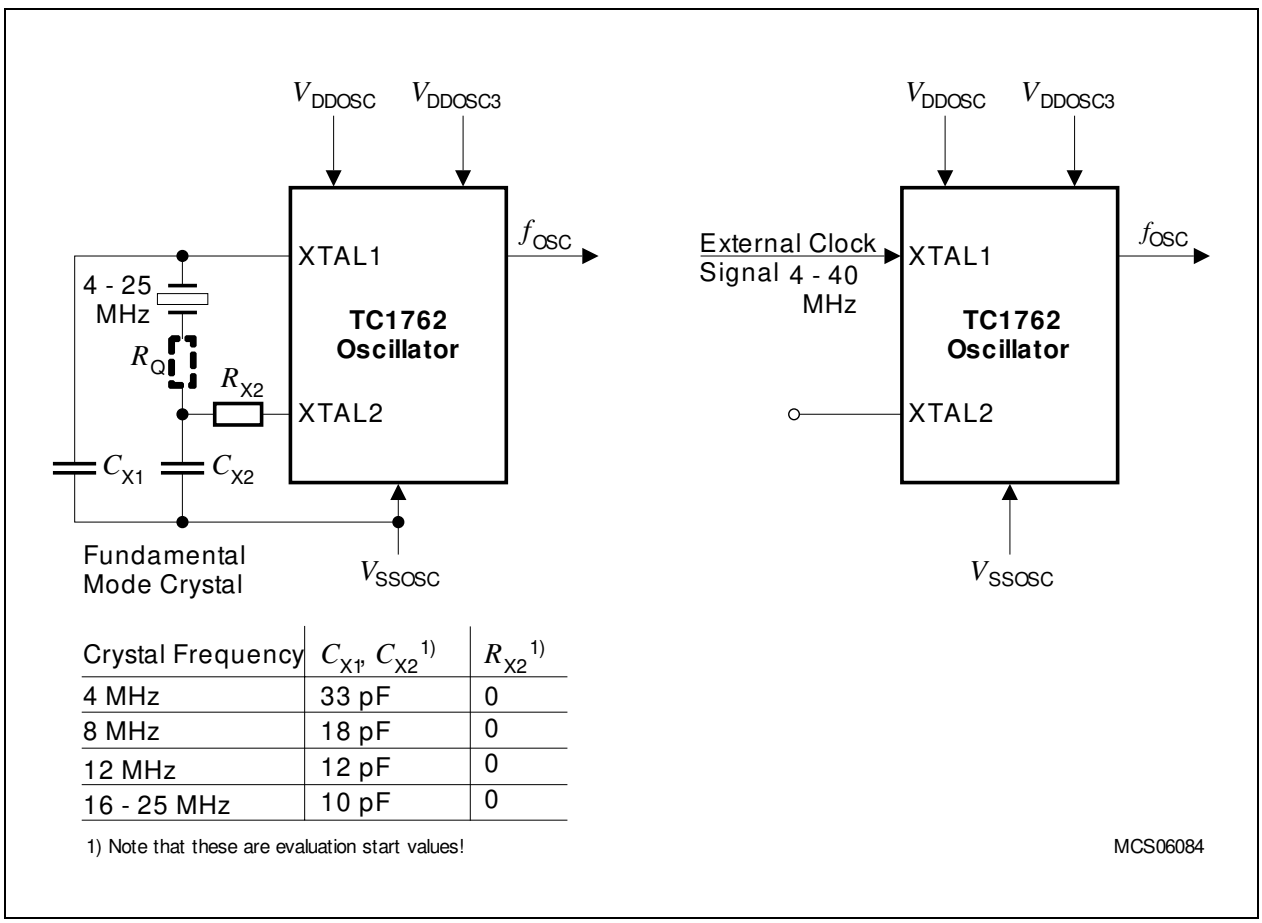
When using a crystal, a proper external oscillator circuitry must be connected to both pins, XTAL1 and XTAL2. The crystal frequency can be within the range of 4 MHz to 25 MHz. Additionally, it is necessary to have two load capacitances C_{X1} and C_{X2}, and depending on the crystal type, a series resistor R_{X2}, to limit the current. A test resistor R_Q may be temporarily inserted to measure the oscillation allowance (negative resistance) of the oscillator circuitry. R_Q values are typically specified by the crystal vendor. The C_{X1} and C_{X2} values shown in **Figure 3-15** can be used as starting points for the negative resistance evaluation and for non-productive systems. The exact values and related operating range are dependent on the crystal frequency and have to be determined and optimized together with the crystal vendor using the negative resistance method.

Oscillation measurement with the final target system is strongly recommended to verify the input amplitude at XTAL1 and to determine the actual oscillation allowance (margin negative resistance) for the oscillator-crystal system.

When using an external clock signal, the signal must be connected to XTAL1. XTAL2 is left open (unconnected). The external clock frequency can be in the range of 0 - 40 MHz if the PLL is bypassed, and 4 - 40 MHz if the PLL is used.

The oscillator can also be used in combination with a ceramic resonator. The final circuitry must also be verified by the resonator vendor.

Figure 3-15 shows the recommended external oscillator circuitries for both operating modes, external crystal mode and external input clock mode. A block capacitor is recommended to be placed between V_{DDOSC}/V_{DDOSC3} and V_{SSOSC}.



Crystal Frequency	C_{X1}, C_{X2} 1)	R_{X2} 1)
4 MHz	33 pF	0
8 MHz	18 pF	0
12 MHz	12 pF	0
16 - 25 MHz	10 pF	0

1) Note that these are evaluation start values!

Figure 3-15 Oscillator Circuitries

Note: For crystal operation, it is strongly recommended to measure the negative resistance in the final target system (layout) to determine the optimum parameters for the oscillator operation. Please refer to the minimum and maximum values of the negative resistance specified by the crystal supplier.

3.22 Power Supply

The TC1762 has several power supply lines for different voltage classes:

- 1.5 V: Core logic, oscillator and A/D converter supply
- 3.3 V: I/O ports, Flash memories, oscillator, and A/D converter supply with reference voltages

Figure 3-16 shows the power supply concept of the TC1762 with the power supply pins and its connections to the functional units.

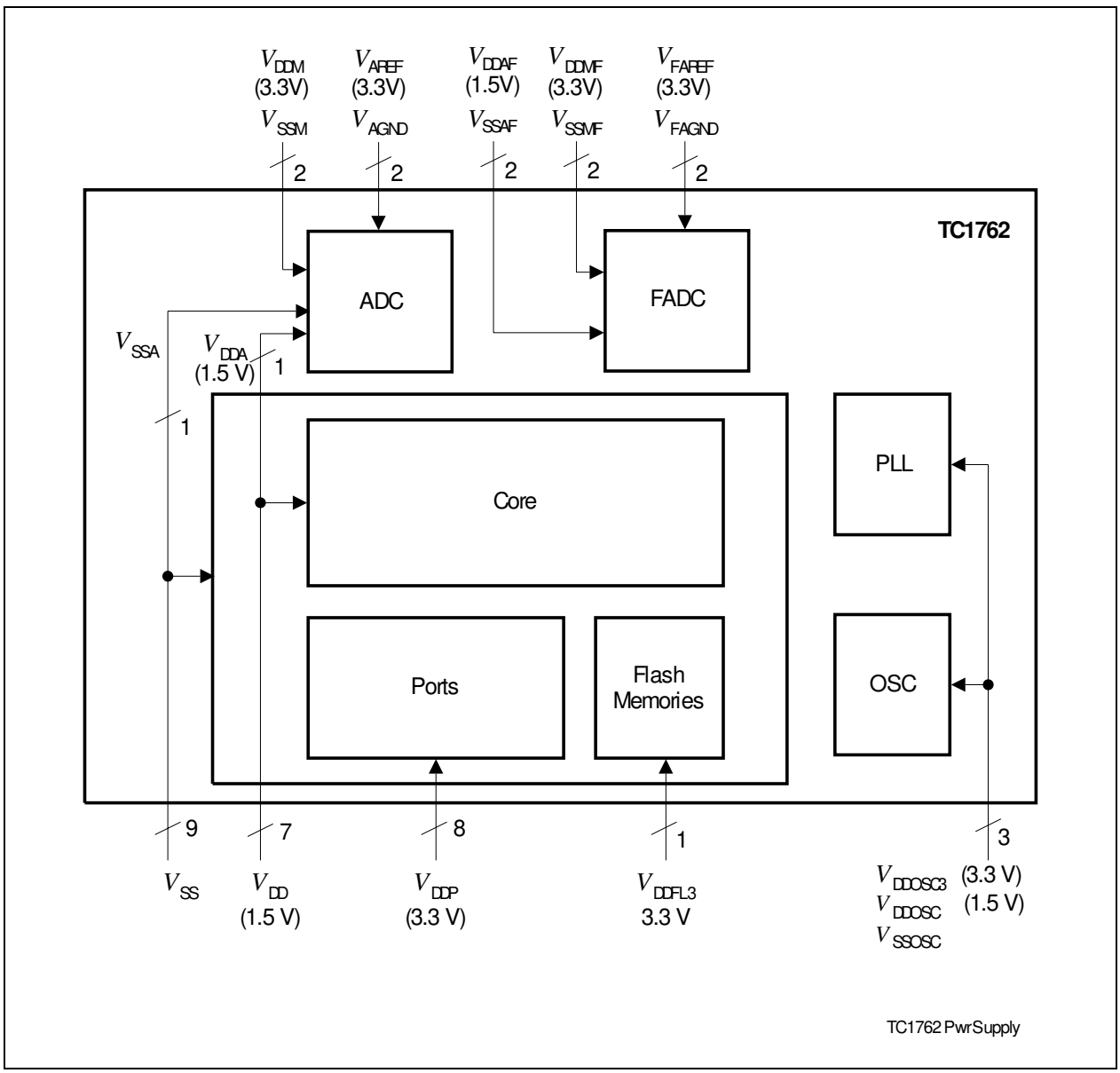


Figure 3-16 Power Supply Concept of TC1762

3.23 Identification Register Values

Table 3-4 shows the address map and reset values of the TC1762 Identification Registers.

Table 3-4 TC1762 Identification Registers

Short Name	Address	Reset Value	Stepping
SCU_ ID	F000 0008$_H$	002C C002$_H$	-
MANID	F000 0070$_H$	0000 1820$_H$	-
CHIPID	F000 0074$_H$	0000 8B02$_H$	-
RTID	F000 0078$_H$	0000 0001$_H$	AA-Step
		0000 0011$_H$	AB-Step
		0000 0007$_H$	AC-Step
SBCU_ID	F000 0108$_H$	0000 6A0A$_H$	-
STM_ID	F000 0208$_H$	0000 C006$_H$	-
CBS_ JDPID	F000 0408$_H$	0000 6307$_H$	-
MSC0_ ID	F000 0808$_H$	0028 C001$_H$	-
ASC0_ ID	F000 0A08$_H$	0000 4402$_H$	-
ASC1_ ID	F000 0B08$_H$	0000 4402$_H$	-
GPTA0_ ID	F000 1808$_H$	0029 C004$_H$	-
DMA_ID	F000 3C08$_H$	001A C012$_H$	-
CAN_ID	F000 4008$_H$	002B C012$_H$	-
SSC0_ ID	F010 0108$_H$	0000 4510$_H$	-
FADC_ ID	F010 0308$_H$	0027 C012$_H$	-
ADC0_ID	F010 0408$_H$	0030 C001$_H$	-
MLI0_ ID	F010 C008$_H$	0025 C006$_H$	-
MCHK_ ID	F010 C208$_H$	001B C001$_H$	-
CPS_ID	F7E0 FF08$_H$	0015 C006$_H$	-
CPU_ID	F7E1 FE18$_H$	000A C005$_H$	-
PMU_ID	F800 0508$_H$	002E C012$_H$	-
FLASH_ID	F800 2008$_H$	0041 C002$_H$	-
DMI_ID	F87F FC08$_H$	0008 C004$_H$	-
PMI_ID	F87F FD08$_H$	000B C004$_H$	-

Table 3-4 TC1762 Identification Registers

Short Name	Address	Reset Value	Stepping
LBCU_ID	F87F FE08$_H$	000F C005$_H$	-
LFI_ID	F87F FF08$_H$	000C C005$_H$	-

4 Electrical Parameters

Chapter 4 provides the characteristics of the electrical parameters which are implementation-specific for the TC1762.

4.1 General Parameters

The general parameters are described here to aid the users in interpreting the parameters mainly in Section 4.2 and Section 4.3. The absolute maximum ratings and its operating conditions are provided for the appropriate setting in the TC1762.

4.1.1 Parameter Interpretation

The parameters listed in this section partly represent the characteristics of the TC1762 and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are marked with an two-letter abbreviation in column “Symbol”:

- **CC**
  Such parameters indicate **C**ontroller **C**haracteristics which are a distinctive feature of the TC1762 and must be regarded for a system design.
- **SR**
  Such parameters indicate **S**ystem **R**equirements which must provided by the microcontroller system in which the TC1762 designed in.

4.1.2 Pad Driver and Pad Classes Summary

This section gives an overview on the different pad driver classes and its basic characteristics. More details (mainly DC parameters) are defined in **Section 4.2.1**.

Table 4-1 Pad Driver and Pad Classes Overview

Class	Power Supply	Type	Sub Class	Speed Grade	Load	Leakage[1)]	Termination
A	3.3V	LVTTL I/O, LVTTL outputs	**A1** (e.g. GPIO)	6 MHz	100 pF	500 nA	No
			A2 (e.g. serial I/Os)	40 MHz	50 pF	6 µA	Series termination recommended
			A3 (e.g. BRKIN, BRKOUT)	66 or 80 MHz[2)]	50 pF	6 µA	Series termination recommended (for f > 25 MHz)
			A4 (e.g. Trace Clock)	66 or 80 MHz[2)]	25 pF	6 µA	Series termination recommended
C	3.3V	LVDS	–	50 MHz		–	Parallel termination[3)], 100Ω ± 10%
D	–	Analog inputs, reference voltage inputs					

1) Values are for T_{Jmax} = 150 °C.

2) This value corresponds to the operating frequency of the device, which depending on the derivative, can be 66 or 80 MHz.

3) In applications where the LVDS pins are not used (disabled), these pins must be either left unconnected, or properly terminated with the differential parallel termination of 100Ω ± 10%.

4.1.3 Absolute Maximum Ratings

Table 4-2 shows the absolute maximum ratings of the TC1762 parameters.

Table 4-2 Absolute Maximum Rating Parameters

Parameter	Symbol		Limit Values		Unit	Notes
			Min.	Max.		
Ambient temperature	T_A	SR	-40	125	°C	Under bias
Storage temperature	T_{ST}	SR	-65	150	°C	–
Junction temperature	T_J	SR	-40	150	°C	Under bias
Voltage at 1.5 V power supply pins with respect to V_{SS} 1)	V_{DD}	SR	–	2.25	V	–
Voltage at 3.3 V power supply pins with respect to V_{SS} 2)	V_{DDP}	SR	–	3.75	V	–
Voltage on any Class A input pin and dedicated input pins with respect to V_{SS}	V_{IN}	SR	-0.5	V_{DDP} + 0.5 or max. 3.7	V	Whatever is lower
Voltage on any Class D analog input pin with respect to V_{AGND}	V_{AIN}, V_{AREFx}	SR	-0.5	V_{DDM} + 0.5 or max. 3.7	V	Whatever is lower
Voltage on any Class D analog input pin with respect to V_{SSAF}	V_{AINF}, V_{FAREF}	SR	-0.5	V_{DDMF} + 0.5 or max. 3.7	V	Whatever is lower
CPU & LMB Bus Frequency 3)4)	f_{CPU}	SR	–	66 or 80	MHz	–
FPI Bus Frequency 3)4)	f_{SYS}	SR	–	66 or 80	MHz	5)

1) Applicable for V_{DD}, V_{DDOSC}, V_{DDPLL}, and V_{DDAF}.

2) Applicable for V_{DDP}, V_{DDFL3}, V_{DDM}, and V_{DDMF}.

3) The PLL jitter characteristics add to this value according to the application settings. See the PLL jitter parameters.

4) This value depend on the derivative and the operating frequency it is designated for. For a device operating at 66 MHz, the absolute maximum frequency is also 66 MHz. Similarly, for a device operating at 80 MHz, the absolute maximum frequency is 80 MHz.

5) The ratio between f_{CPU} and f_{SYS} is fixed at 1:1.

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute

maximum rating conditions for extended periods may affect device reliability. During absolute maximum rating overload conditions (V_{IN} > related V_{DD} or V_{IN} < V_{SS}) the voltage on the related V_{DD} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

4.1.4 Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation of the TC1762. All parameters specified in the following table refer to these operating conditions, unless otherwise noted.

Table 4-3 Operating Condition Parameters

Parameter	Symbol		Limit Values		Unit	Notes Conditions
			Min.	Max.		
Digital supply voltage[1]	V_{DD} V_{DDOSC}	SR	1.42	1.58[2]	V	–
	V_{DDP} V_{DDOSC3}	SR	3.13	3.47[3]	V	For Class A pins (3.3V ± 5%)
	V_{DDFL3}	SR	3.13	3.47[3]	V	–
Digital ground voltage	V_{SS}	SR	0		V	–
Ambient temperature under bias	T_A	SR	-40	+125	°C	–
Analog supply voltages	–		–	–	–	See separate specification Page 4-75, Page 4-82
CPU clock	f_{CPU}	SR	–[4]	80[5]	MHz	–
Short circuit current	I_{SC}	SR	-5	+5	mA	[6]
Absolute sum of short circuit currents of a pin group (see Table 4-4)	$\Sigma\|I_{SC}\|$	SR	–	20	mA	See note[7]
Absolute sum of short circuit currents of the device	$\Sigma\|I_{SC}\|$	SR	–	100	mA	See note [7]

Table 4-3 Operating Condition Parameters

Parameter	Symbol		Limit Values		Unit	Notes Conditions
			Min.	Max.		
Inactive device pin current (V_{DD} = V_{DDP} = 0)	I_{ID}	SR	-1	1	mA	Voltage on all power supply pins V_{DDx} = 0
External load capacitance	C_L	SR	–	See DC characteristics	pF	Depending on pin class

1) Digital supply voltages applied to the TC1762 must be static regulated voltages which allow a typical voltage swing of ±5%.

2) Voltage overshoot up to 1.7 V is permissible at Power-Up and $\overline{\text{PORST}}$ low, provided the pulse duration is less than 100 µs and the cumulated summary of the pulses does not exceed 1 h.

3) Voltage overshoot to 4 V is permissible at Power-Up and $\overline{\text{PORST}}$ low, provided the pulse duration is less than 100 µs and the cumulated summary of the pulses does not exceed 1 h.

4) The TC1762 uses a static design, so the minimum operation frequency is 0 MHz. Due to test time restriction no lower frequency boundary is tested, however.

5) The PLL jitter characteristics add to this value according to the application settings. See the PLL jitter parameters.

6) Applicable for digital outputs.

7) See additional document “TC1796 Pin Reliability in Overload“ for overload current definitions.

Table 4-4 Pin Groups for Overload/Short-Circuit Current Sum Parameter

Group	Pins
1	TRCLK, P5.[7:0], P0.[7:6], P0.[15:14]
2	P0.[13:12], P0.[5:4], P2.[13:8], SOP0A, SON0, FCLP0A, FCLN0
3	P0.[11:8], P0.[3:0], P3.[13:11]
4	P3[10:0], P3.[15:14]
5	$\overline{\text{HDRST}}$, $\overline{\text{PORST}}$, $\overline{\text{NMI}}$, $\overline{\text{TESTMODE}}$, $\overline{\text{BRKIN}}$, $\overline{\text{BRKOUT}}$, BYPASS, TCK, $\overline{\text{TRST}}$, TDO, TMS, TDI, P1.[7:4]
6	P1.[3:0], P1.[11:8], P4.[3:0]
7	P2.[7:0], P1.[14:12]
8	P5.[15:8]

4.2 DC Parameters

The electrical characteristics of the DC Parameters are detailed in this section.

4.2.1 Input/Output Pins

Table 4-5 provides the characteristics of the input/output pins of the TC1762.

Table 4-5 Input/Output DC-Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
General Parameters						
Pull-up current[1)]	$\|I_{PUH}\|$	CC	10	100	µA	$V_{IN} < V_{IHAmin}$; class A1/A2/Input pads.
			20	200	µA	$V_{IN} < V_{IHAmin}$; class A3/A4 pads.
Pull-down current[1)]	$\|I_{PDL}\|$	CC	10	150	µA	$V_{IN} > V_{ILAmax}$; class A1/A2/Input pads.
			20	200	µA	$V_{IN} > V_{ILAmax}$; class A3/A4 pads.
Pin capacitance[1)] (Digital I/O)	C_{IO}	CC	–	10	pF	f = 1 MHz T_A = 25 °C
Input only Pads (V_{DDP} = 3.13 to 3.47 V = 3.3V ±5%)						
Input low voltage class A1/A2 pins	V_{ILA}	SR	-0.3	0.34 × V_{DDP}	V	–
Input high voltage class A1/A2 pins	V_{IHA}	SR	0.64 × V_{DDP}	V_{DDP}+ 0.3 or max. 3.6	V	Whatever is lower
Ratio V_{IL}/V_{IH}		CC	0.53	–	–	–
Input low voltage class A3 pins	V_{ILA3}	SR	–	0.8	V	–
Input high voltage class A3 pins	V_{IHA3}	SR	2.0	–	V	–
Input hysteresis	HYSA	CC	0.1 × V_{DDP}	–	V	[2)5)]
Input leakage current	I_{OZI}	CC	–	±3000 ±6000	nA	$((V_{DDP}/2)-1) < V_{IN} < ((V_{DDP}/2)+1)$ otherwise[3)]

Table 4-5 Input/Output DC-Characteristics (cont'd)(Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
Class A Pads (V_{DDP} = 3.13 to 3.47 V = 3.3V ±5%)						
Output low voltage[4]	V_{OLA}	CC	–	0.4	V	I_{OL} = 2 mA for strong driver mode, (Not applicable to Class A1 pins) I_{OL} = 1.8 mA for medium driver mode, A2 pads I_{OL} = 1.4 mA for medium driver mode, A1 pads I_{OL} = 370 µA for weak driver mode
Output high voltage[3]	V_{OHA}	CC	2.4	–	V	I_{OH} = -2 mA for strong driver mode, (Not applicable to Class A1 pins) I_{OH} = -1.8 mA for medium driver mode, A1/A2 pads I_{OH} = -370 µA for weak driver mode
			V_{DDP} - 0.4	–	V	I_{OH} = -1.4 mA for strong driver mode, (Not applicable to Class A1 pins) I_{OH} = -1 mA for medium driver mode, A1/A2 pads I_{OH} = -280 µA for weak driver mode
Input low voltage class A1/2 pins	V_{ILA}	SR	-0.3	0.34 × V_{DDP}	V	–
Input high voltage class A1/2 pins	V_{IHA}	SR	0.64 × V_{DDP}	V_{DDP} + 0.3 or 3.6	V	Whatever is lower
Ratio V_{IL}/V_{IH}		CC	0.53	–	–	–
Input hysteresis	HYSA	CC	0.1 × V_{DDP}	–	V	2)5)

Table 4-5 Input/Output DC-Characteristics (cont'd)(Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
Input leakage current Class A2/3/4 pins	I_{OZA24}	CC	–	±3000 ±6000	nA	$((V_{DDP}/2)-1) < V_{IN} < ((V_{DDP}/2)+1)$ otherwise[3]
Input leakage current Class A1 pins	I_{OZA1}	CC	–	±500	nA	$0\ V < V_{IN} < V_{DDP}$
Class C Pads (V_{DDP} = 3.13 to 3.47 V = 3.3V ±5%)						
Output low voltage	V_{OL}	CC	815		mV	Parallel termination 100 Ω ± 1%
Output high voltage	V_{OH}	CC		1545	mV	
Output differential voltage	V_{OD}	CC	150	600	mV	
Output offset voltage	V_{OS}	CC	1075	1325	mV	
Output impedance	R_0	CC	40	140		–
Class D Pads						
see ADC Characteristics			–	–	–	–

1) Not subject to production test, verified by design / characterization.

2) The pads that have spike filter function in the input path: $\overline{\text{PORST}}$, $\overline{\text{HDRST}}$, $\overline{\text{NMI}}$ do not have hysteresis.

3) Only one of these parameters is tested, the other is verified by design characterization

4) Max. resistance between pin and next power supply pin 25 Ω for strong driver mode (verified by design characterization).

5) Function verified by design, value is not subject to production test - verified by design/characterization. Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It cannot be guaranteed that it suppresses switching due to external system noise.

4.2.2 Analog to Digital Converter (ADC0)

Table 4-6 provides the characteristics of the ADC module in the TC1762.

Table 4-6 ADC Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Test Conditions / Remarks
			Min.	Typ.	Max.		
Analog supply voltage	V_{DDM}	SR	3.13	3.3	3.47[1)]	V	–
	V_{DD}	SR	1.42	1.5	1.58[2)]	V	Power supply for ADC digital part, internal supply
Analog ground voltage	V_{SSM}	SR	-0.1	–	0.1	V	–
Analog reference voltage [17)]	V_{AREFx}	SR	V_{AGNDx}+ 1V	V_{DDM}	V_{DDM}+ 0.05[1)] [3)4)]	V	–
Analog reference ground [17)]	V_{AGNDx}	SR	V_{SSMx} - 0.05V	0	V_{AREF} - 1 V	V	–
Analog reference voltage range[5)17)]	V_{AREFx}- V_{AGNDx}	SR	V_{DDM}/2		V_{DDM} + 0.05		
Analog input voltage range	V_{AIN}	SR	V_{AGNDx}	–	V_{AREFx}	V	–
V_{DDM} supply current	I_{DDM}	SR		2.5	4	mA rms	[6)]
Power-up calibration time	t_{PUC}	CC	–	–	3840	f_{ADC} CLK	–
Internal ADC clocks	f_{BC}	CC	2	–	40	MHz	$f_{BC} = f_{ANA} \times 4$
	f_{ANA}	CC	0.5	–	10	MHz	$f_{ANA} = f_{BC} / 4$
Sample time	t_S	CC	4 × (CHCONn.STC + 2) × t_{BC}			µs	–
			8 × t_{BC}	–	–	µs	

Table 4-6 ADC Characteristics (cont'd) (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Test Conditions / Remarks
			Min.	Typ.	Max.		
Conversion time	t_C	CC	$t_S + 40 \times t_{BC} + 2 \times t_{DIV}$			µs	For 8-bit conversion
			$t_S + 48 \times t_{BC} + 2 \times t_{DIV}$			µs	For 10-bit conversion
			$t_S + 56 \times t_{BC} + 2 \times t_{DIV}$			µs	For 12-bit conversion
Total unadjusted error [4]	TUE[7]	CC	–	–	±1	LSB	For 8-bit conv.
			–	–	±2	LSB	For 10-bit conv.
			–	–	±4	LSB	For 12-bit conv.[8][9]
			–	–	±8	LSB	For 12-bit conv.[10][9]
DNL error[11][5]	TUE_{DNL}	CC	–	±1.5	±3.0	LSB	For 12-bit conv.[12][9]
INL error[11][5]	TUE_{INL}	CC	–	±1.5	±3.0	LSB	For 12-bit conv.[12][9]
Gain error[11][5]	TUE_{GAIN}	CC	–	±0.5	±3.5	LSB	For 12-bit conv.[12][9]
Offset error[11][5]	TUE_{OFF}	CC	–	±1.0	±4.0	LSB	For 12-bit conv.[12][9]
Input leakage current at analog inputs AN0, AN1 and AN31. see **Figure 4-3**[13]	I_{OZ1}[14]	CC	–1000	–	300	nA	(0% V_{DDM}) < V_{IN} < (2% V_{DDM})
			–200		400	nA	(2% V_{DDM}) < V_{IN} < (95% V_{DDM})
			–200		1000	nA	(95% V_{DDM}) < V_{IN} < (98% V_{DDM})
			–200		3000	nA	(98% V_{DDM}) < V_{IN} < (100% V_{DDM})

Table 4-6 ADC Characteristics (cont'd) (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Test Conditions / Remarks
			Min.	Typ.	Max.		
Input leakage current at analog inputs AN2 to AN30, see **Figure 4-3**	I_{OZ1}[14]	CC	–1000	–	200	nA	(0% V_{DDM}) < V_{IN} < (2% V_{DDM})
			–200		300	nA	(2% V_{DDM}) < V_{IN} < (95% V_{DDM})
			–200		1000	nA	(95% V_{DDM}) < V_{IN} < (98% V_{DDM})
			–200		3000	nA	(98% V_{DDM}) < V_{IN} < (100% V_{DDM})
Input leakage current at V_{AREF}	I_{OZ2}	CC	–	–	±1	µA	0 V < V_{AREF} < V_{DDM}, no conversion running
Input current at V_{AREF}[17]	I_{AREF}	CC	–	35	75	µA rms	0 V < V_{AREF} < V_{DDM}[15]
Total capacitance of the voltage reference inputs[16][17]	$C_{AREFTOT}$	CC	–	–	25	pF	[9]
Switched capacitance at the positive reference voltage input [17]	C_{AREFSW}	CC	–	15	20	pF	[9][18]
Resistance of the reference voltage input path[16]	R_{AREF}	CC	–	1	1.5	kΩ	500 Ohm increased for AN[1:0] used as reference input [9]
Total capacitance of the analog inputs[16]	C_{AINTOT}	CC	–	–	25	pF	[6][9]
Switched capacitance at the analog voltage inputs	C_{AINSW}	CC	–	–	7	pF	[9][19]

Table 4-6 ADC Characteristics (cont'd) (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Test Conditions / Remarks
			Min.	Typ.	Max.		
ON resistance of the transmission gates in the analog voltage path	R_{AIN}	CC	–	1	1.5	kΩ	9)
ON resistance for the ADC test (pull-down for AIN7)	R_{AIN7T}	CC	200	300	1000	Ω	Test feature available only for AIN7 9)
Current through resistance for the ADC test (pull-down for AIN7)	I_{AIN7T}	CC	–	15 rms	30 peak	mA	Test feature available only for AIN7 9)

1) Voltage overshoot to 4 V are permissible, provided the pulse duration is less than 100 µs and the cumulated summary of the pulses does not exceed 1 h.

2) Voltage overshoot to 1.7 V are permissible, provided the pulse duration is less than 100 µs and the cumulated summary of the pulses does not exceed 1 h.

3) A running conversion may become inexact in case of violating the normal operating conditions (voltage overshoot).

4) If the reference voltage V_{AREF} increases or the V_{DDM} decreases, so that V_{AREF} = (V_{DDM} + 0.05 V to V_{DDM} + 0.07 V), then the accuracy of the ADC decreases by 4LSB12.

5) If a reduced reference voltage in a range of V_{DDM}/2 to V_{DDM} is used, then the ADC converter errors increase. If the reference voltage is reduced with the factor k (k<1), then TUE, DNL, INL Gain and Offset errors increase with the factor 1/k.
If a reduced reference voltage in a range of 1 V to V_{DDM}/2 is used, then there are additional decrease in the ADC speed and accuracy.

6) Current peaks of up to 6 mA with a duration of max. 2 ns may occur

7) TUE is tested at V_{AREF} = 3.3 V, V_{AGND} = 0 V and V_{DDM} = 3.3 V

8) ADC module capability.

9) Not subject to production test, verified by design / characterization.

10) Value under typical application conditions due to integration (switching noise, etc.).

11) The sum of DNL/INL/Gain/Offset errors does not exceed the related TUE total unadjusted error.

12) For 10-bit conversions the DNL/INL/Gain/Offset error values must be multiplied with factor 0.25.
For 8-bit conversions the DNL/INL/Gain/Offset error values must be multiplied with 0.0625.

13) The leakage current definition is a continuous function, as shown in **Figure 4-3**. The numerical values defined determine the characteristic points of the given continuous linear approximation - they do not define step function.

14) Only one of these parameters is tested, the other is verified by design characterization.

15) I_{AREF_MAX} is valid for the minimum specified conversion time. The current flowing during an ADC conversion with a duration of up to t_C = 25µs can be calculated with the formula $I_{AREF\_MAX} = Q_{CONV}/t_C$. Every conversion needs a total charge of Q_{CONV} = 150pC from V_{AREF}.
All ADC conversions with a duration longer than t_C = 25µs consume an I_{AREF_MAX} = 6µA.

16) For the definition of the parameters see also **Figure 4-2**.

17) Applies to AIN0 and AIN1, when used as auxiliary reference inputs.

18) This represents an equivalent switched capacitance. This capacitance is not switched to the reference voltage at once. Instead of this smaller capacitances are successively switched to the reference voltage.

19) The sampling capacity of the conversion C-Network is pre-charged to V_{AREF}/2 before the sampling moment. Because of the parasitic elements the voltage measured at AINx is lower then V_{AREF}/2.

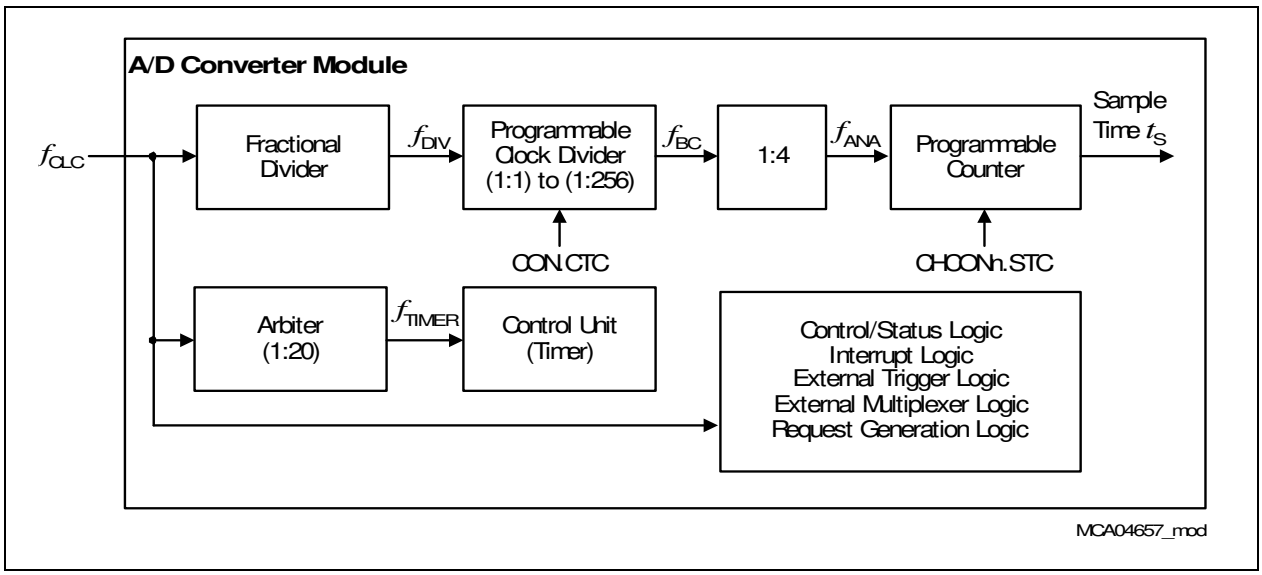


Figure 4-1 ADC0 Clock Circuit

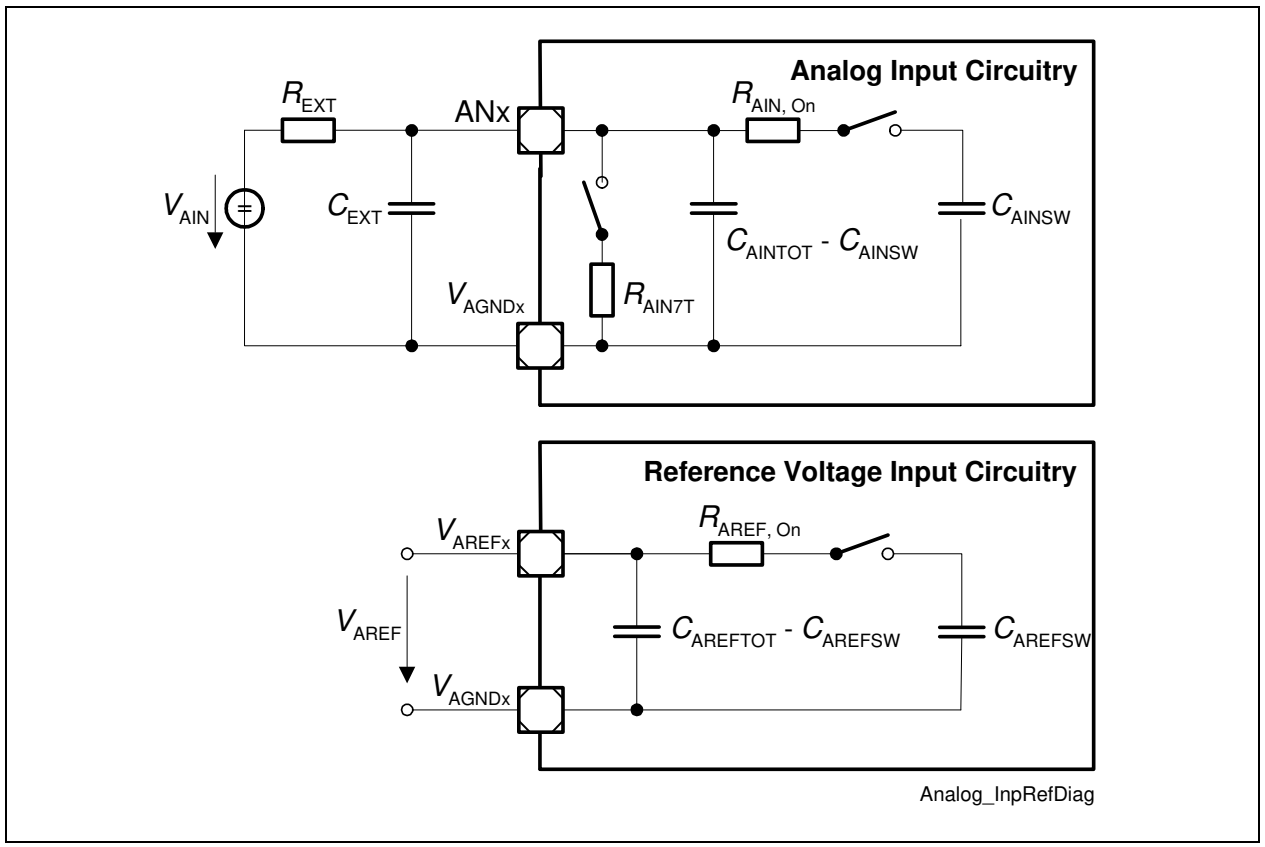


Figure 4-2 ADC0 Input Circuits

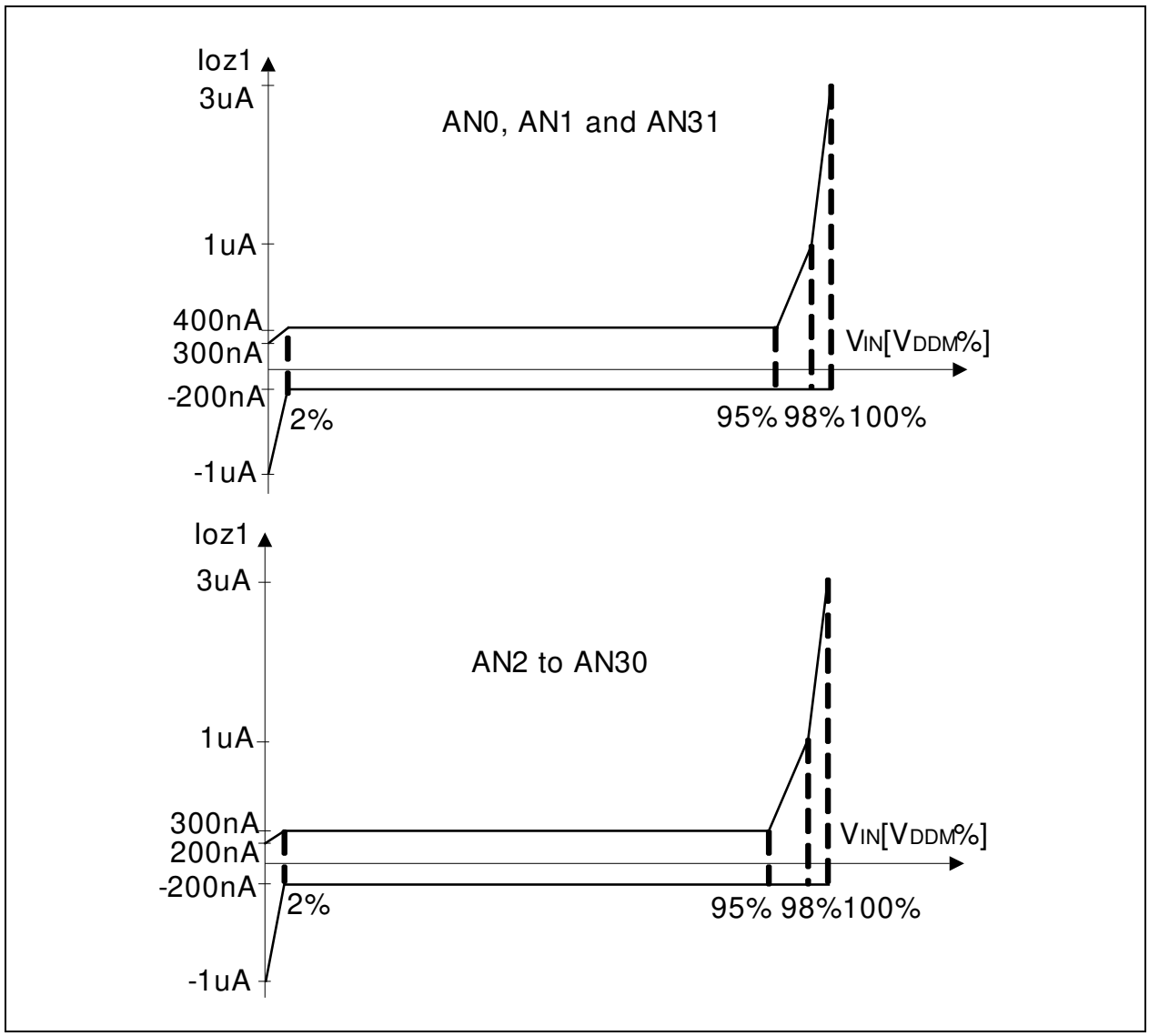


Figure 4-3 ADC0 Analog Inputs Leakage

4.2.3 Fast Analog to Digital Converter (FADC)

Table 4-7 provides the characteristics of the FADC module in the TC1762.

Table 4-7 FADC Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit	Remarks Conditions
			Min.	Max.		
DNL error	E_{DNL}	CC	–	±1	LSB	12)
INL error	E_{INL}	CC	–	±4	LSB	12)
Gradient error1)12)	E_{GRAD}	CC	–	±3	%	2)With calibration, gain 1, 2
			–	±5	%	Without calibration gain 1, 2, 4
			–	±6	%	Without calibration gain 8
Offset error12)	E_{OFF}3)	CC	–	±204)	mV	2)With calibration
			–	±604)	mV	Without calibration
Reference error of internal $V_{FAREF}/2$	E_{REF}	CC	–	±60	mV	–
Input leakage current at analog inputs AN32 to AN35. 5) see Figure 4-5	I_{OZ1}6)	CC	–1000	300	nA	(0% V_{DDM}) < V_{IN} < (2% V_{DDM})
			–200	400	nA	(2% V_{DDM}) < V_{IN} < (95% V_{DDM})
			–200	1000	nA	(95% V_{DDM}) < V_{IN} < (98% V_{DDM})
			–200	3000	nA	(98% V_{DDM}) < V_{IN} < (100% V_{DDM})
Analog supply voltages	V_{DDMF}	SR	3.13	3.477)	V	–
	V_{DDAF}	SR	1.42	1.588)	V	–
Analog ground voltage	V_{SSAF}	SR	-0.1	0.1	V	–
Analog reference voltage	V_{FAREF}	SR	3.13	3.477)9)	V	Nominal 3.3 V
Analog reference ground	V_{FAGND}	SR	V_{SSAF} - 0.05V	V_{SSAF} +0.05V	V	–
Analog input voltage range	V_{AINF}	SR	V_{FAGND}	V_{DDMF}	V	–

Table 4-7 FADC Characteristics (cont'd)(Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit	Remarks Conditions
			Min.	Max.		
Analog supply currents	I_{DDMF}	SR	–	9	mA	–
	I_{DDAF}	SR	–	17	mA	10)
Input current at each V_{FAREF}	I_{FAREF}	CC	–	150	µA rms	Independent of conversion
Input leakage current at V_{FAREF} 11)	I_{FOZ2}	CC	–	±500	nA	0 V < V_{IN} < V_{DDMF}
Input leakage current at V_{FAGND}	I_{FOZ3}	CC		±8	µA	
Conversion time	t_C	CC	–	21	CLK of f_{ADC}	For 10-bit conv.
Converter Clock	f_{ADC}	CC	–	80	MHz	–
Input resistance of the analog voltage path (Rn, Rp)	R_{FAIN}	CC	100	200	kΩ	12)
Channel Amplifier Cutoff Frequency	f_{COFF}	CC	2		MHz	–
Settling Time of a Channel Amplifier after changing ENN or ENP	t_{SET}	CC		5	µsec	–

1) Calibration of the gain is possible for the gain of 1 and 2, and not possible for the gain of 4 and 8.

2) Calibration should be performed at each power-up. In case of continuous operation, calibration should be performed minimum once per week.

3) The offset error voltage drifts over the whole temperature range typically ±2 LSB.

4) Applies when the gain of the channel equals one. For the other gain settings, the offset error increases; it must be multiplied with the applied gain.

5) The leakage current definition is a continuous function, as shown in **Figure 4-5**. The numerical values defined determine the characteristic points of the given continuous linear approximation - they do not define step function.

6) Only one of these parameters is tested, the other is verified by design characterization.

7) Voltage overshoot to 4 V are permissible, provided the pulse duration is less than 100 µs and the cumulated summary of the pulses does not exceed 1 h.

8) Voltage overshoot to 1.7 V are permissible, provided the pulse duration is less than 100 µs and the cumulated sum of the pulses does not exceed 1 h.

9) A running conversion may become inexact in case of violating the normal operating conditions (voltage overshoots).

10) Current peaks of up to 40 mA with a duration of max. 2 ns may occur

11) This value applies in power-down mode.

12) Not subject to production test, verified by design / characterization.

The calibration procedure should run after each power-up, when all power supply voltages and the reference voltage have stabilized. The offset calibration must run first, followed by the gain calibration.

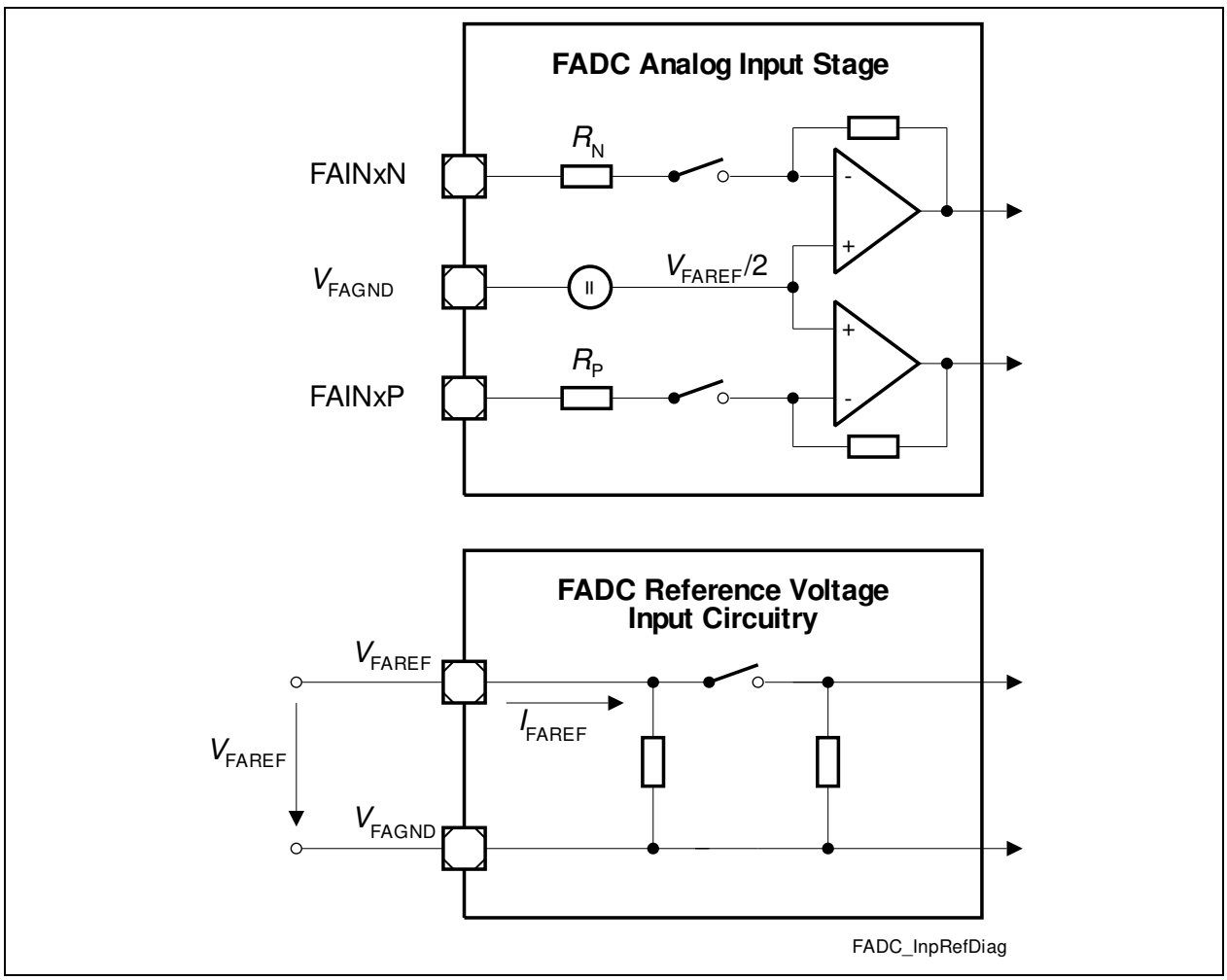


Figure 4-4 FADC Input Circuits

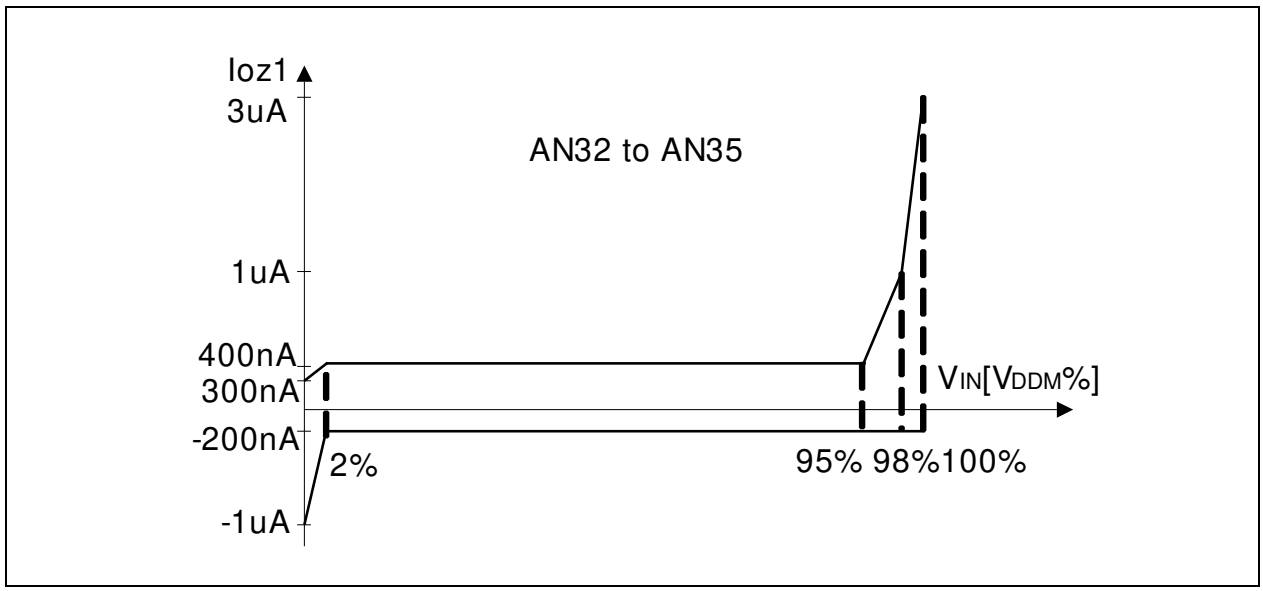


Figure 4-5 Analog Inputs AN32-AN35 Leakage

4.2.4 Oscillator Pins

Table 4-8 provides the characteristics of the oscillator pins in the TC1762.

Table 4-8 Oscillator Pins Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit values		Unit	Test Conditions
			Min.	Max.		
Frequency Range	f_{OSC}	CC	4	25	MHz	–
Input low voltage at XTAL1[1)]	V_{ILX}	SR	-0.2	0.3 × V_{DDOSC3}	V	–
Input high voltage at XTAL1[1)]	V_{IHX}	SR	0.7 × V_{DDOSC3}	V_{DDOSC3} + 0.2	V	–
Input current at XTAL1	I_{IX1}	CC	–	±25	µA	0 V < V_{IN} < V_{DDOSC3}

1) If the XTAL1 pin is driven by a crystal, reaching a minimum amplitude (peak-to-peak) of 0.3 × V_{DDOSC3} is necessary.

Note: It is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimal parameters for the oscillator operation. Please refer to the limits specified by the crystal supplier.

4.2.5 Temperature Sensor

Table 4-9 provides the characteristics of the temperature sensor in the TC1762.

Table 4-9 Temperature Sensor Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit	Remarks
			Min.	Max.		
Temperature Sensor Range	T_{SR}	SR	-40	150	°C	–
Start-up time after resets inactive	t_{TSST}	SR		10	µs	
Temperature of the die at the sensor location	T_{TS}	CC	T_{TS} = (ADC_Code - 487) × 0.396 - 40		°C	10-bit ADC result
			T_{TS} = (ADC_Code - 1948) × 0.099 - 40		°C	12Bit ADC result
Sensor Inaccuracy	T_{TSA}	CC		±10	°C	
A/D Converter clock for DTS signal	f_{ANA}	SR	–	10	MHz	Conversion with ADC0

4.2.6 Power Supply Current

Table 4-10 provides the characteristics of the power supply current in the TC1762.

Table 4-10 Power Supply Current (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Test Conditions / Remarks
			Min.	Typ.	Max.		
$\overline{\text{PORST}}$ low current at V_{DD}	I_{DD_PORST}	CC	–	–	96[1] 138[2]	mA	The PLL running at the base frequency
$\overline{\text{PORST}}$ low current at V_{DDP}	I_{DDP_PORST}	CC	–	–	12[1] 13[2]	mA	The PLL running at the base frequency
Active mode core supply current[3][4]	I_{DD}	CC	–	–	290[1] 330[2]	mA	f_{CPU} = 80MHz f_{CPU}/f_{SYS} = 1:1
Active mode core supply current[3][4]	I_{DD}	CC	–	–	250[1] 300[2]	mA	f_{CPU} = 66MHz f_{CPU}/f_{SYS} = 1:1
Active mode analog supply current	I_{DDAx}; I_{DDMx}	CC	–	–	–	mA	See ADC0/FADC
Oscillator and PLL core power supply	I_{DDOSC}	CC	–	–	5	mA	–
Oscillator and PLL pads power supply	I_{DDOSC3}	CC	–	–	3.6[5]	mA	–
FLASH power supply current	I_{DDFL3}	CC	–	–	45	mA	–
LVDS port supply (via V_{DDP})[6]	I_{LVDS}	CC	–	–	25	mA	LVDS pads active
Maximum Allowed Power Dissipation[7]	P_{Dmax}	SR	$P_D \times R_{TJA} < 25°C$			–	At worst case, T_A = 125 °C

1) Maximum value measured at T_A = 125 °C.

2) Maximum value measured at T_J = 150 °C.

3) Infineon Power Loop: CPU and PCP running, all peripherals active. The power consumption of each custom application will most probably be lower than this value, but must be evaluated separately.

4) The I_{DD} decreases typically to 240mA if the f_{CPU} is decreased to 40 MHz, at constant T_J = 150 °C, for the Infineon Max. Power Loop.

5) Estimated value; double-bonded at package level with V_{DDP}.

6) In case the LVDS pads are disabled, the power consumption per pair is negligible (less than 1µA).

7) For the calculation of the junction to ambient thermal resistance R_{TJA}, see Chapter 5.1.

4.3 AC Parameters

All AC parameters are defined with the temperature compensation disabled, which means that pads are constantly kept at the maximum strength.

4.3.1 Testing Waveforms

The testing waveforms for rise/fall time, output delay and output high impedance are shown in **Figure 4-6**, **Figure 4-7** and **Figure 4-8**.

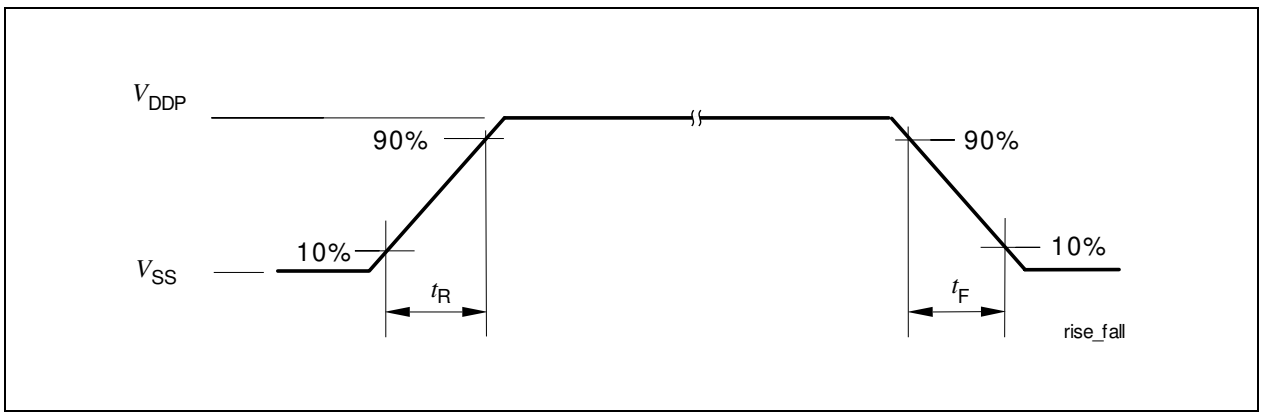


Figure 4-6 Rise/Fall Time Parameters

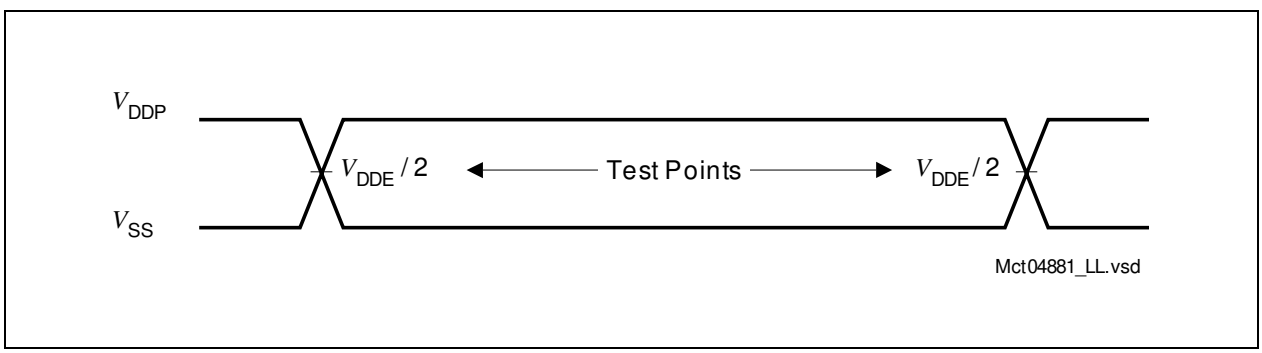


Figure 4-7 Testing Waveform, Output Delay

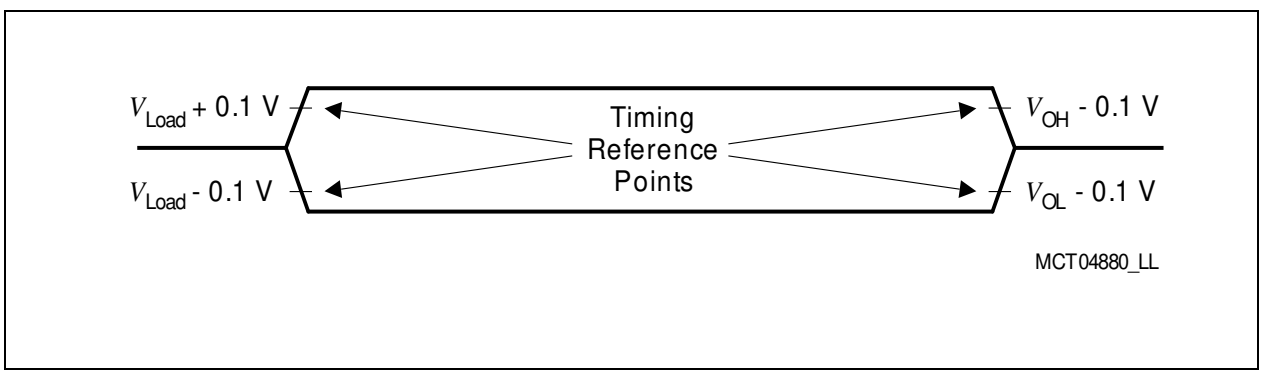


Figure 4-8 Testing Waveform, Output High Impedance

4.3.2 Output Rise/Fall Times

Table 4-11 provides the characteristics of the output rise/fall times in the TC1762.

Table 4-11 Output Rise/Fall Times (Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Conditions
		Min.	Max.		
Class A1 Pads					
Rise/fall times[1)] Class A1 pads	t_{RA1}, t_{FA1}		50 140 18000 150 550 65000	ns	Regular (medium) driver, 50 pF Regular (medium) driver, 150 pF Regular (medium) driver, 20 nF Weak driver, 20 pF Weak driver, 150 pF Weak driver, 20 000 pF
Class A2 Pads					
Rise/fall times [1)] Class A2 pads	t_{FA2}, t_{FA2}		3.3 6 5.5 16 50 140 18000 150 550 65000	ns	Strong driver, sharp edge, 50 pF Strong driver, sharp edge, 100pF Strong driver, med. edge, 50 pF Strong driver, soft edge, 50 pF Medium driver, 50 pF Medium driver, 150 pF Medium driver, 20 000 pF Weak driver, 20 pF Weak driver, 150 pF Weak driver, 20 000 pF
Class A3 Pads					
Rise/fall times [1)] Class A3 pads	t_{FA3}, t_{FA3}		2.5	ns	50 pF
Class A4 Pads					
Rise/fall times [1)] Class A4 pads	t_{FA4}, t_{FA4}		2.0	ns	25 pF
Class C Pads					
Rise/fall times Class C pads	t_{rC}, t_{fC}		2	ns	

1) Not all parameters are subject to production test, but verified by design/characterization and test correlation.

4.3.3 Power Sequencing

There is a restriction for the power sequencing of the 3.3 V domain as shown in **Figure 4-9**. It must always be higher than 1.5 V domain - 0.5 V. The gray area shows the valid range for $V_{3.3V}$ relative to an exemplary $V_{1.5V}$ ramp. V_{DDP}, V_{DDOSC3}, V_{DDM}, V_{DDMF}, V_{DDFL3} belong to the 3.3 V domain. The V_{DDM} and V_{DDMF} subdomains are connected with antiparallel ESD protection diodes. There are no other such connections between the subdomains. V_{DD} , V_{DDOSC} and V_{DDAF} belong to the 1.5 V domain.

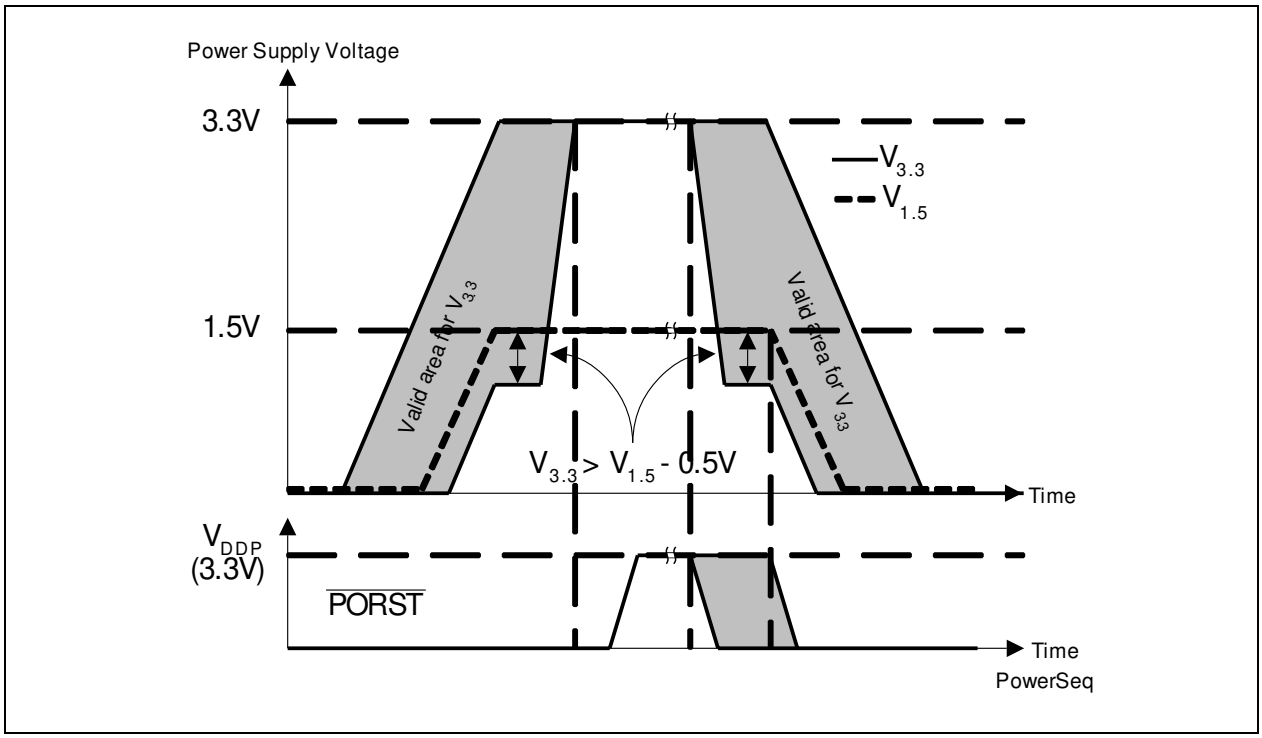


Figure 4-9 V_{DDP} / V_{DD} Power Up Sequence

All ground pins V_{SS} must be externally connected to one single star point in the system. The difference voltage between the ground pins must not exceed 200 mV.

The $\overline{\text{PORST}}$ signal must be activated at latest before any power supply voltage falls below the levels shown on the figure below. In this case, only the memory row of a Flash memory that was the target of the write at the moment of the power loss will contain unreliable content. Additionally, the $\overline{\text{PORST}}$ signal should be activated as soon as possible. The sooner the $\overline{\text{PORST}}$ signal is activated, the less time the system operates outside of the normal operating power supply range.

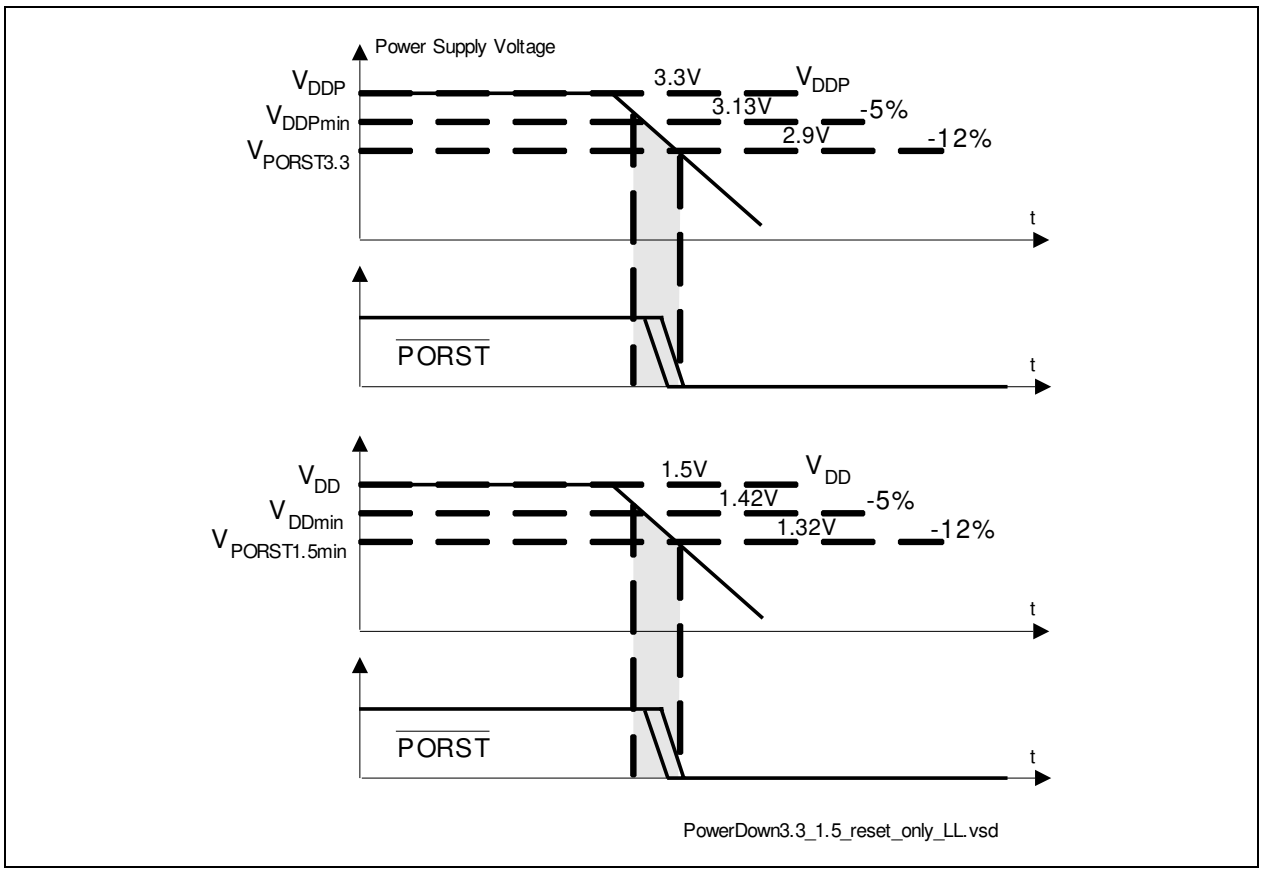


Figure 4-10 Power Down / Power Loss Sequence

4.3.4 Power, Pad and Reset Timing

Table 4-12 provides the characteristics of the power, pad and reset timing in the TC1762.

Table 4-12 Power, Pad and Reset Timing Parameters

Parameter	Symbol		Limit Values		Unit
			Min.	Max.	
Min. V_{DDP} voltage to ensure defined pad states[1]	V_{DDPPA}	CC	0.6	–	V
Oscillator start-up time[2]	t_{OSCS}	CC	–	10	ms
Minimum $\overline{\text{PORST}}$ active time after power supplies are stable at operating levels	t_{POA}	SR	10	–	ms
$\overline{\text{HDRST}}$ pulse width	t_{HD}	CC	1024 clock cycles[3]	–	f_{SYS}
$\overline{\text{PORST}}$ rise time	t_{POR}	SR	–	50	ms
Setup time to $\overline{\text{PORST}}$ rising edge[4]	t_{POS}	SR	0	–	ns
Hold time from $\overline{\text{PORST}}$ rising edge[4]	t_{POH}	SR	100	–	ns
Setup time to $\overline{\text{HDRST}}$ rising edge[5]	t_{HDS}	SR	0	–	ns
Hold time from $\overline{\text{HDRST}}$ rising edge[5]	t_{HDH}	SR	100 + $(2 \times 1/f_{SYS})$	–	ns
Ports inactive after $\overline{\text{PORST}}$ reset active[6][7]	t_{PIP}	CC	–	150	ns
Ports inactive after $\overline{\text{HDRST}}$ reset active[8]	t_{PI}	CC	–	150 + $5 \times 1/f_{SYS}$	ns
Minimum V_{DDP} $\overline{\text{PORST}}$ activation threshold.[9]	$V_{PORST3.3}$	SR	–	2.9	V
Minimum V_{DD} $\overline{\text{PORST}}$ activation threshold. [9]	$V_{PORST1.5}$	SR	–	1.32	V
Power-on Reset Boot Time[10]	t_{BP}	CC	2.15	3.50	ms
Hardware/Software Reset Boot Time at f_{CPU}=80MHz[11]	t_B	CC	500	800	µs
Hardware/Software Reset Boot Time at f_{CPU}=66MHz[11]	t_B	CC	560	860	µs

1) This parameter is valid under assumption that $\overline{\text{PORST}}$ signal is constantly at low-level during the power-up/power-down of the V_{DDP}.

2) This parameter is verified by device characterization. The external oscillator circuitry must be optimized by the customer and checked for negative resistance as recommended and specified by crystal suppliers.
3) Any $\overline{\text{HDRST}}$ activation is internally prolonged to 1024 FPI bus clock (f_{SYS}) cycles.
4) Applicable for input pins $\overline{\text{TESTMODE}}$, $\overline{\text{TRST}}$, $\overline{\text{BRKIN}}$, and TXD1A with noise suppression filter of $\overline{\text{PORST}}$ switched-on (BYPASS = 0).
5) The setup/hold values are applicable for Port 0 and Port 4 input pins with noise suppression filter of $\overline{\text{HDRST}}$ switched-on (BYPASS = 0), independently whether $\overline{\text{HDRST}}$ is used as input or output.
6) Not subject to production test, verified by design / characterization.
7) This parameter includes the delay of the analog spike filter in the $\overline{\text{PORST}}$ pad.
8) Not subject to production test, verified by design / characterization.
9) In case of power loss during internal flash write, prevents Flash write to random address.
10) Booting from Flash, the duration of the boot-time is defined between the rising edge of the $\overline{\text{PORST}}$ and the moment when the first user instruction has entered the CPU and its processing starts.
11) Booting from Flash, the duration of the boot time is defined between the following events:
1. Hardware reset: the falling edge of a short $\overline{\text{HDRST}}$ pulse and the moment when the first user instruction has entered the CPU and its processing starts, if the $\overline{\text{HDRST}}$ pulse is shorter than 1024 × T_{SYS}.
If the $\overline{\text{HDRST}}$ pulse is longer than 1024 × T_{SYS}, only the time beyond the 1024 × T_{SYS} should be added to the boot time ($\overline{\text{HDRST}}$ falling edge to first user instruction).
2. Software reset: the moment of starting the software reset and the moment when the first user instruction has entered the CPU and its processing starts

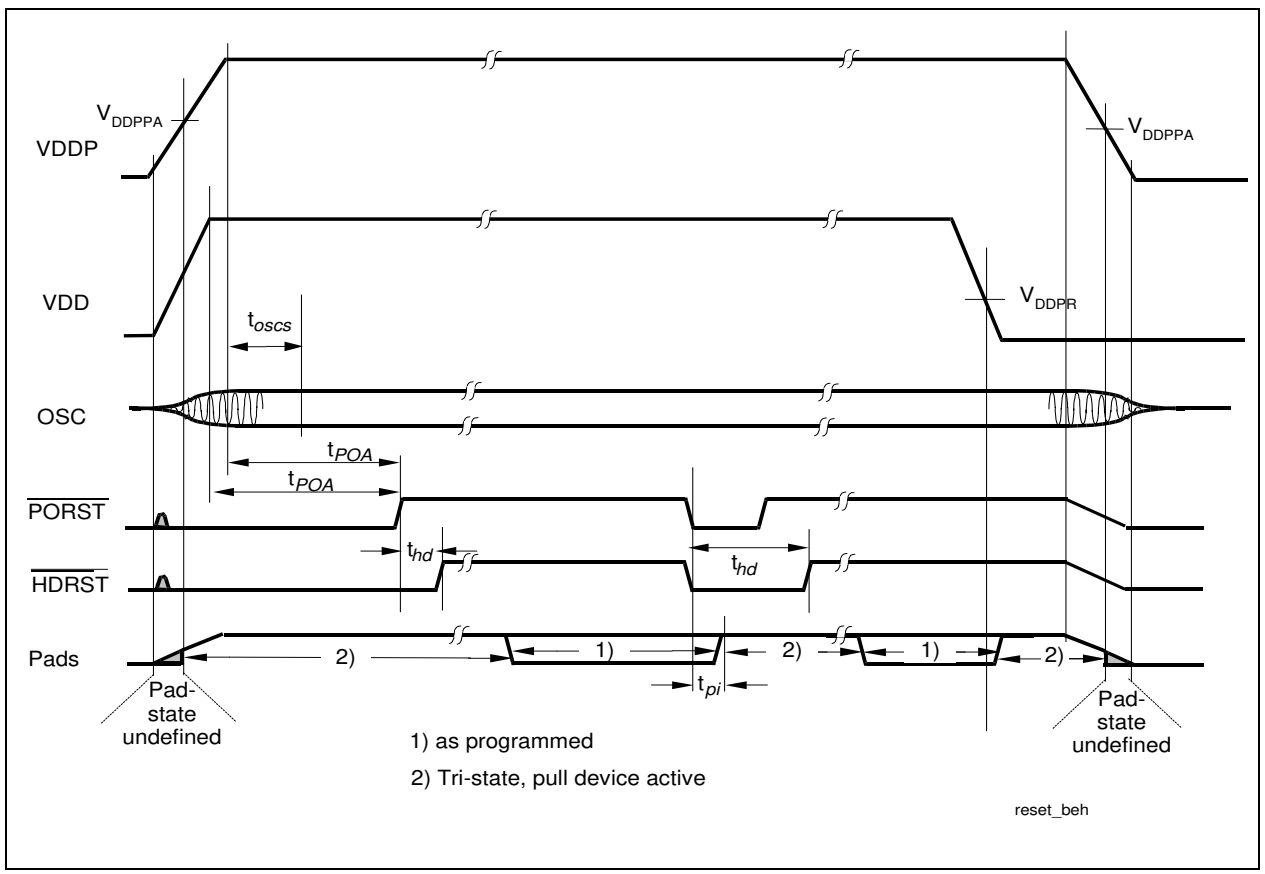


Figure 4-11 Power, Pad and Reset Timing

4.3.5 Phase Locked Loop (PLL)

Section 4.3.5 provides the characteristics of the PLL parameters and its operation in the TC1762.

Note: All PLL characteristics defined on this and the next page are verified by design characterization.

Table 4-13 PLL Parameters (Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit
		Min.	Max.	
Accumulated jitter	D_P	See Figure 4-12		–
VCO frequency range	f_{VCO}	400	500	MHz
		500	600	MHz
		600	700	MHz
PLL base frequency[1)]	$f_{PLLBASE}$	140	320	MHz
		150	400	MHz
		200	480	MHz
PLL lock-in time	t_L	–	200	µs

1) The CPU base frequency which is selected after reset is calculated by dividing the limit values by 16 (this is the K factor after reset).

Phase Locked Loop Operation

When PLL operation is enabled and configured, the PLL clock f_{VCO} (and with it the CPU clock f_{CPU}) is constantly adjusted to the selected frequency. The relation between f_{VCO} and f_{SYS} is defined by: $f_{VCO} = K \times f_{CPU}$. The PLL causes a jitter of f_{CPU} and affects the clock outputs TRCLK and SYSCLK (P4.3) which are derived from the PLL clock f_{VCO}.

There are two formulas that define the (absolute) approximate maximum value of jitter D_P in ns dependent on the K-factor, the CPU clock frequency f_{CPU} in MHz, and the number P of consecutive f_{CPU} clock periods.

$$P \times K < 900 \qquad Dp[ns] = \pm\left(\frac{5 \times P}{fcpu[MHz]} + 0,9\right) \tag{4.1}$$

$$P \times K \geq 900 \qquad Dp[ns] = \pm\left(\frac{4500}{fcpu[MHz] \times K} + 0,9\right) \tag{4.2}$$

K : K-Divider Value

P : Number of f_{CPU} periods

D_P : Jitter in ns

f_{CPU} : CPU frequency in MHz

Note: The frequency of system clock f_{SYS} can be selected to be either f_{CPU} or $f_{CPU}/2$.

With rising number P of clock cycles the maximum jitter increases linearly up to a value of P that is defined by the K-factor of the PLL. Beyond this value of P the maximum accumulated jitter remains at a constant value. Further, a lower CPU clock frequency f_{CPU} results in a higher absolute maximum jitter value.

Figure 4-12 illustrates the jitter curve for for several K/ f_{CPU} combinations.

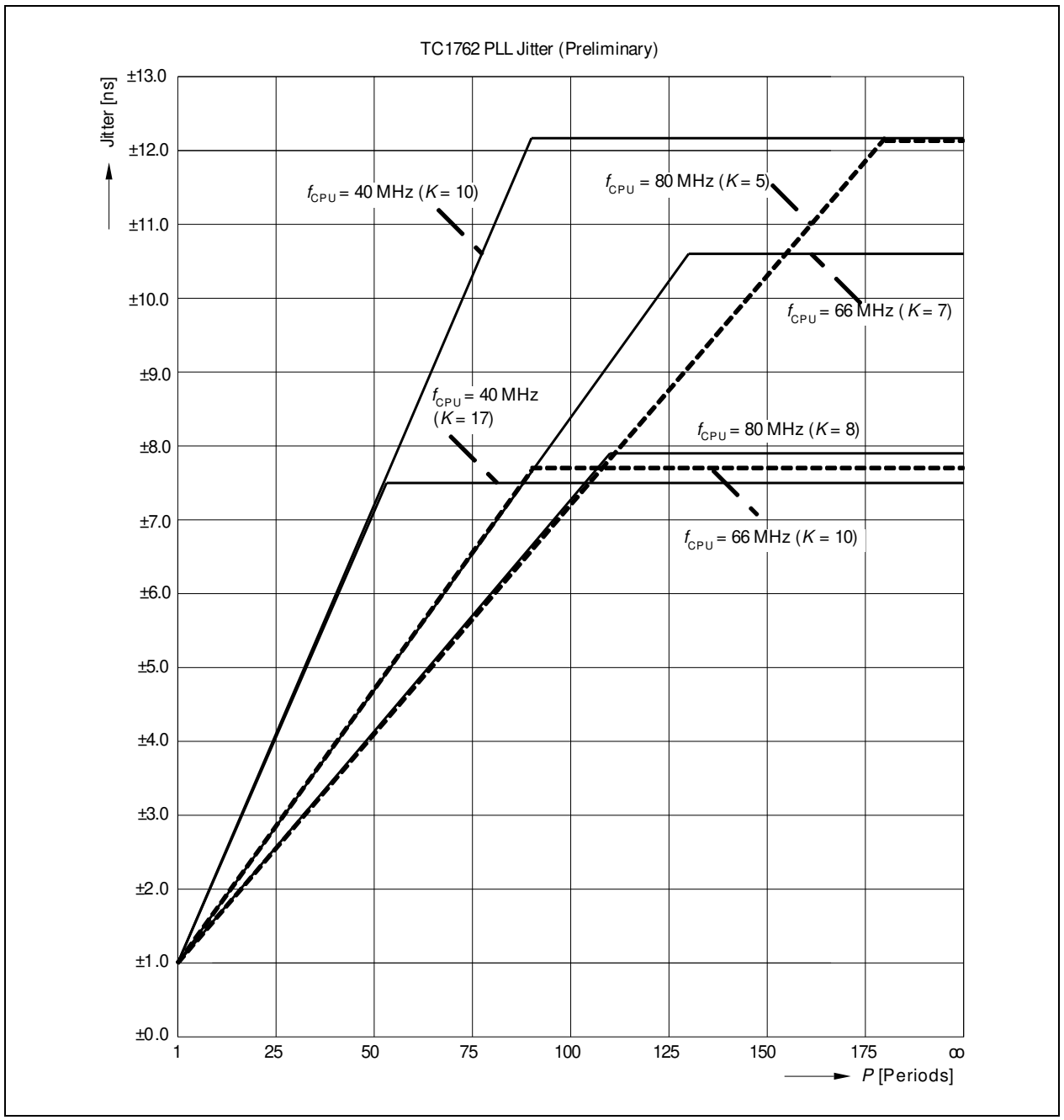


Figure 4-12 Approximated Maximum Accumulated PLL Jitter for Typical CPU Clock Frequencies f_{CPU} (overview)

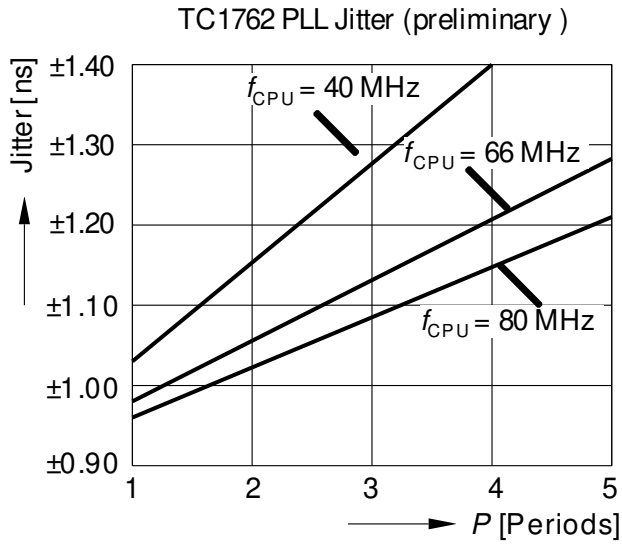


Figure 4-13 Approximated Maximum Accumulated PLL Jitter for Typical CPU Clock Frequencies f_{CPU} (detail)

Note: The maximum peak-to-peak noise on the main oscillator and PLL power supply (measured between V_{DDOSC} and V_{SSOSC}) is limited to a peak-to-peak voltage of V_{PP} = 10 mV. This condition can be achieved by appropriate blocking to the supply pins and using PCB supply and ground planes.

4.3.6 Debug Trace Timing

V_{SS} = 0 V; V_{DDP} = 3.13 to 3.47 V (Class A); T_A = -40 °C to +125 °C;
C_L (TRCLK) = 25 pF; C_L (TR[15:0]) = 50 pF

Table 4-14 Debug Trace Timing Parameter[1)]

Parameter	Symbol		Limit Values		Unit
			Min.	Max.	
TR[15:0] new state from TRCLK ↓	t_9	CC	-1	4	ns

1) Not subject to production test, verified by design/characterization.

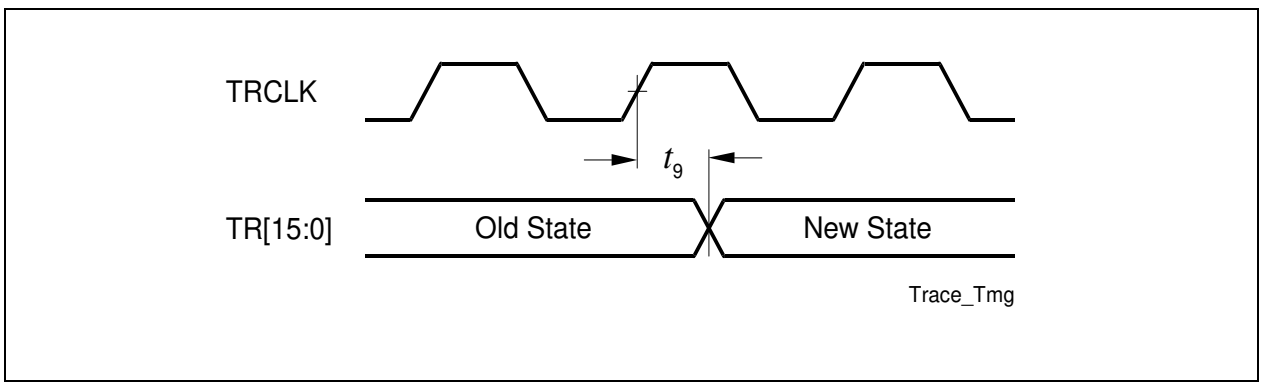


Figure 4-14 Debug Trace Timing

4.3.7 Timing for JTAG Signals

(Operating Conditions apply, C_L = 50 pF)

Table 4-15 TCK Clock Timing Parameter

Parameter	Symbol		Limit Values		Unit
			Min.	Max.	
TCK clock period[1)]	t_{TCK}	SR	25	–	ns
TCK high time	t_1	SR	10	–	ns
TCK low time	t_2	SR	10	–	ns
TCK clock rise time	t_3	SR	–	4	ns
TCK clock fall time	t_4	SR	–	4	ns

1) f_{TCK} should be lower or equal to f_{SYS}

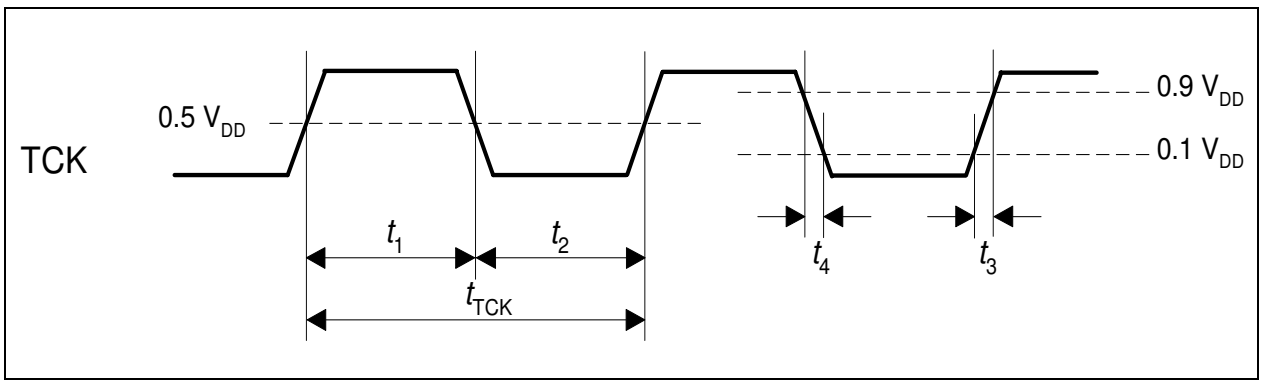


Figure 4-15 TCK Clock Timing

Table 4-16 JTAG Timing Parameter[1)]

Parameter	Symbol		Limit Values		Unit	Test Conditions / Remarks
			Min.	Max.		
TMS setup to TCK	t_1	SR	6.0	–	ns	–
TMS hold to TCK	t_2	SR	6.0	–	ns	–
TDI setup to TCK	t_1	SR	6.0	–	ns	–
TDI hold to TCK	t_2	SR	6.0	–	ns	–
TDO valid output from TCK[2)]	t_3	CC	–	14.5	ns	C_L = 50 pF[3)4)]
			3.0	–		C_L = 20 pF
TDO high impedance to valid output from TCK[2)]	t_4	CC	–	15.5	ns	C_L = 50 pF[3)4)]
TDO valid output to high impedance from TCK[2)]	t_5	CC	–	14.5	ns	C_L = 50 pF[4)]

1) Not subject to production test, verified by design / characterization.

2) The falling edge on TCK is used to capture the TDO timing.

3) By reducing the load from 50 pF to 20 pF, a reduction of approximately 1.0 ns in timing is expected.

4) By reducing the power supply range from +/-5 % to +5/-2 %, a reduction of approximately 0.5 ns in timing is expected.

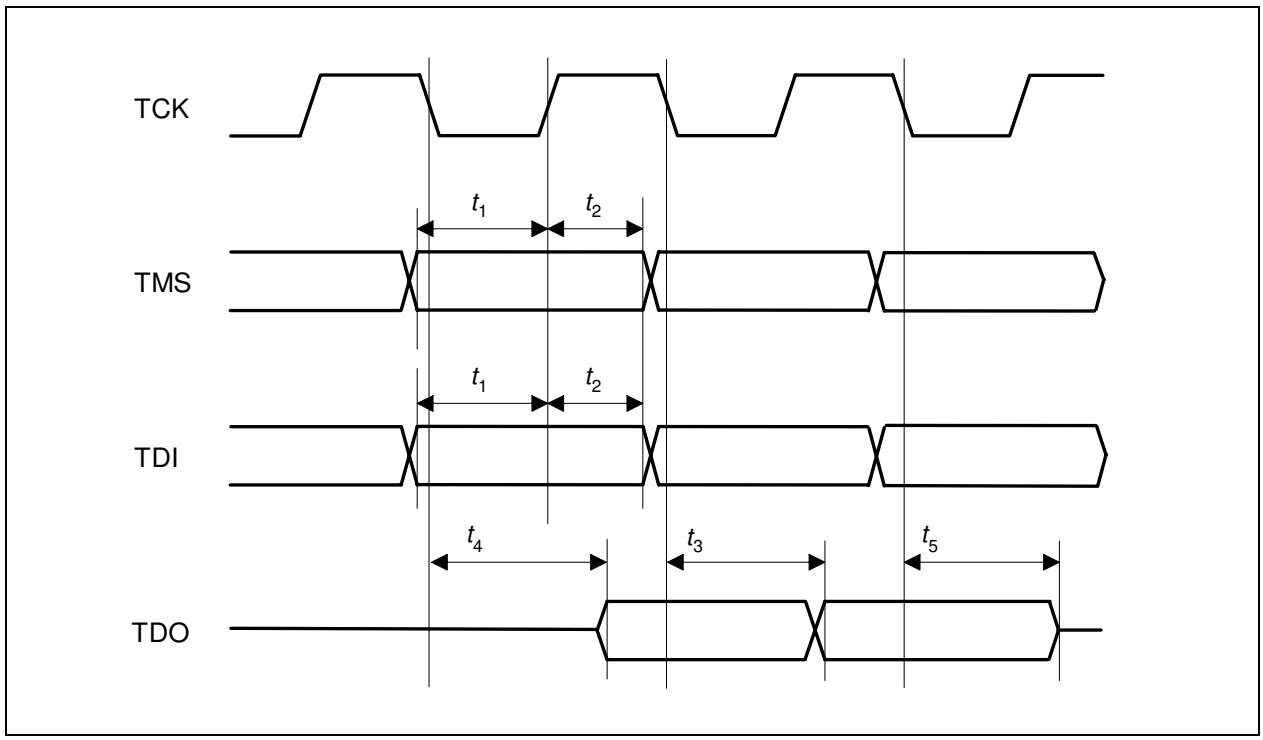


Figure 4-16 JTAG Timing

*Note: The JTAG module is fully compliant with IEEE1149.1-2000 with JTAG clock at 20 MHz. The JTAG clock at 40 MHz is possible with the modified timing diagram shown in **Figure 4-16**.*

4.3.8 Peripheral Timings

Section 4.3.8 provides the characteristics of the peripheral timings in the TC1762.

Note: Peripheral timing parameters are not subject to production test. They are verified by design/characterization.

4.3.8.1 Micro Link Interface (MLI) Timing

Table 4-17 provides the characteristics of the MLI timing in the TC1762.

Table 4-17 MLI Timing (Operating Conditions apply, C_L = 50 pF)

Parameter	Symbol		Limit Values		Unit
			Min.	Max.	
TCLK clock period[1)2)]	t_{30}	CC	2[3)]	–	$1/f_{SYS}$
RCLK clock period	t_{31}	SR	1	–	$1/f_{SYS}$
MLI outputs delay from TCLK ↓	t_{35}	CC	0	8	ns
MLI inputs setup to RCLK ↓	t_{36}	SR	4	–	ns
MLI inputs hold to RCLK ↓	t_{37}	SR	4	–	ns
RREADY output delay from RCLK ↓	t_{38}	CC	0	8	ns

1) TCLK signal rise/fall times are the same as the A2 Pads rise/fall times.

2) TCLK high and low times can be minimum 1 × T_{MLI}

3) $T_{MLImin} = T_{SYS} = 1/f_{SYS}$. When f_{SYS} = 80MHz, t_{30} = 25ns

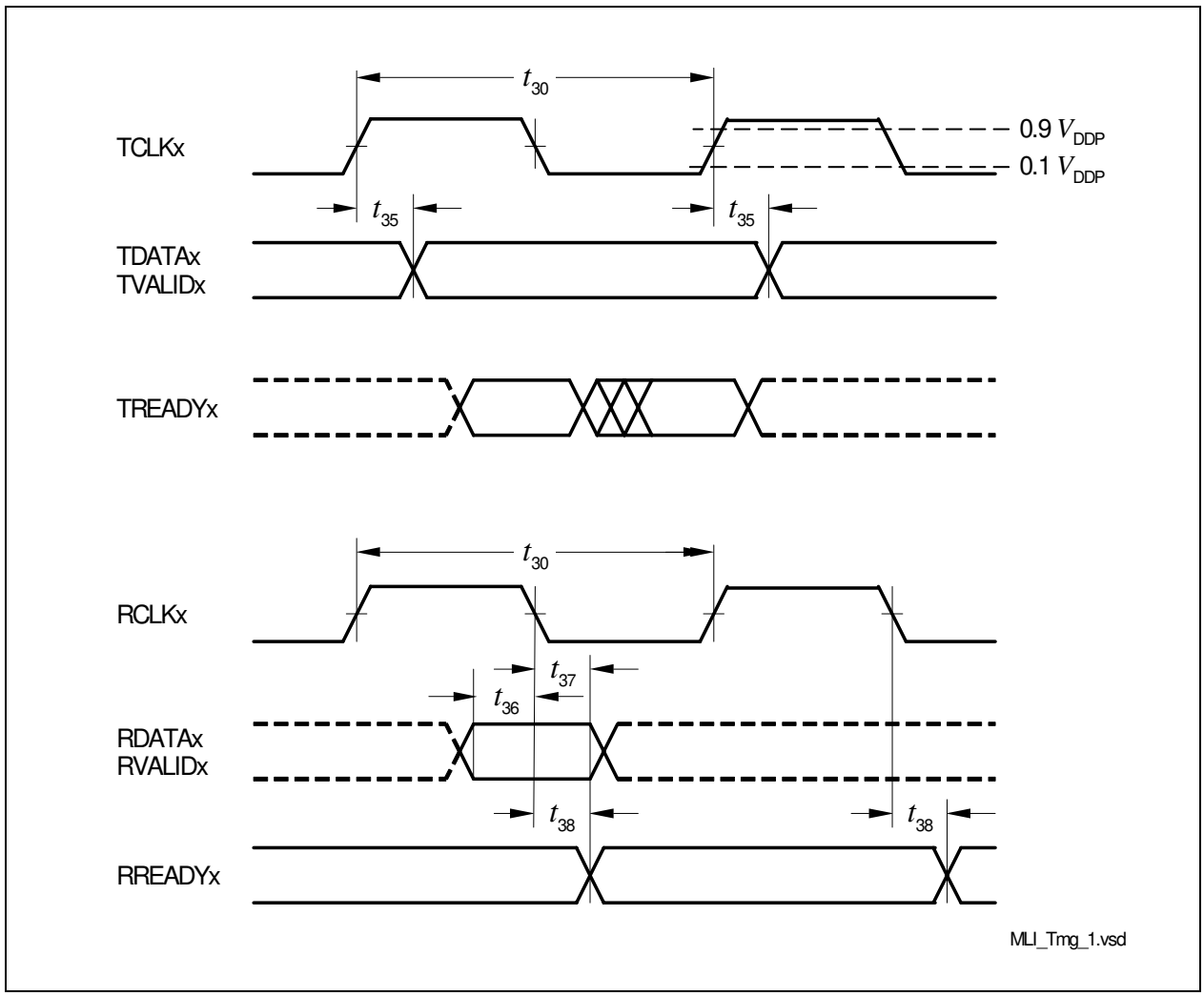


Figure 4-17 MLI Interface Timing

Note: The generation of RREADYx is in the input clock domain of the receiver. The reception of TREADYx is asynchronous to TCLKx.

4.3.8.2 Micro Second Channel (MSC) Interface Timing

Table 4-18 provides the characteristics of the MSC timing in the TC1762.

Table 4-18 MSC Interface Timing (Operating Conditions apply, CL = 50 pF)

Parameter	Symbol		Limit Values		Unit
			Min.	Max.	
FCLP clock period[1)2)]	t_{40}	CC	$2 \times T_{MSC}$[3)]	–	ns
SOP/ENx outputs delay from FCLP ↓	t_{45}	CC	-10	10	ns
SDI bit time	t_{46}	SR	$8 \times T_{MSC}$	–	ns
SDI rise time	t_{48}	SR		100	ns
SDI fall time	t_{49}	SR		100	ns

1) FCLP signal rise/fall times are the same as the A2 Pads rise/fall times.

2) FCLP signal high and low can be minimum $1 \times T_{MSC}$.

3) $T_{MSCmin} = T_{SYS} = 1/f_{SYS}$. When f_{SYS} = 80MHz, t_{40} = 25ns

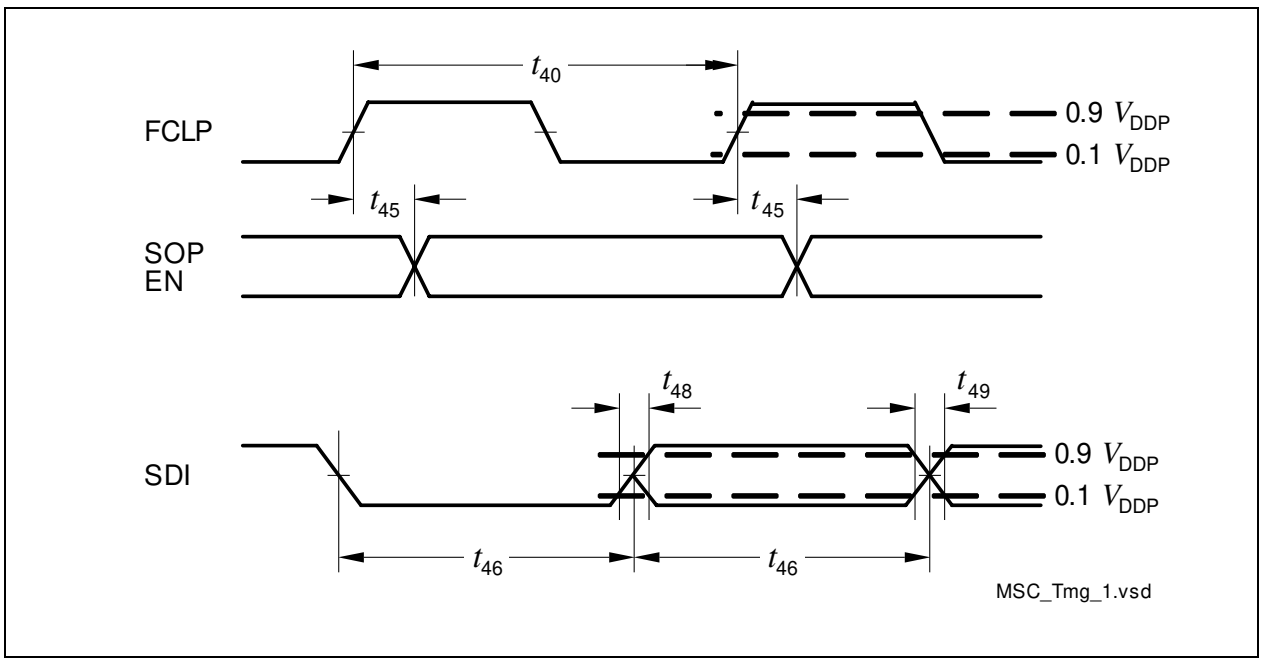


Figure 4-18 MSC Interface Timing

Note: The data at SOP should be sampled with the falling edge of FCLP in the target device.

4.3.8.3 Synchronous Serial Channel (SSC) Master Mode Timing

Table 4-19 provides the characteristics of the SSC timing in the TC1762.

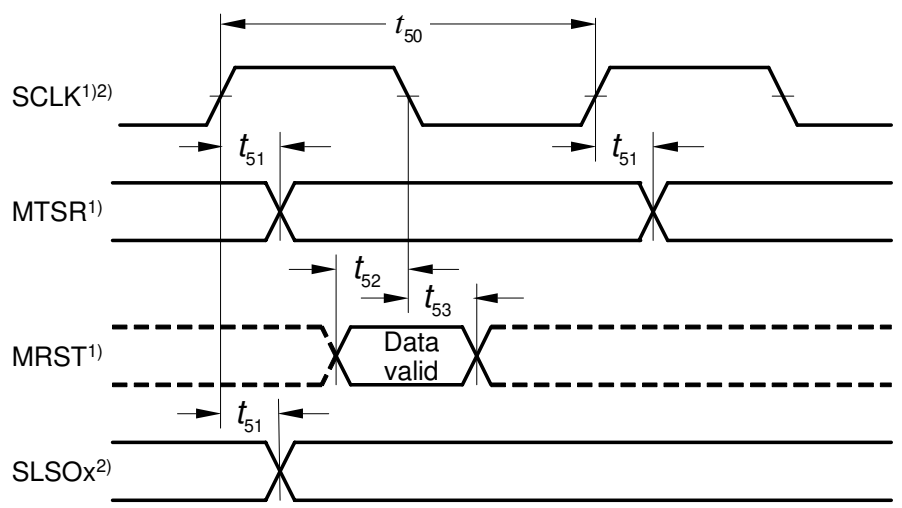
Table 4-19 SSC Master Mode Timing (Operating Conditions apply, CL = 50 pF)

Parameter	Symbol		Limit Values		Unit
			Min.	Max.	
SCLK clock period[1)2)]	t_{50}	CC	$2 \times T_{SSC}$[3)]	–	ns
MTSR/SLSOx delay from SCLK	t_{51}	CC	0	8	ns
MRST setup to SCLK	t_{52}	SR	10	–	ns
MRST hold from SCLK	t_{53}	SR	5	–	ns

1) SCLK signal rise/fall times are the same as the A2 Pads rise/fall times.

2) SCLK signal high and low times can be minimum $1 \times T_{SSC}$.

3) $T_{SSCmin} = T_{SYS} = 1/f_{SYS}$. When f_{SYS} = 80 MHz, t_{50} = 25ns



1) This timing is based on the following setup: CON.PH = CON.PO = 0.

2) The transition at SLSOx is based on the following setup: SSOTC.TRAIL = 0 and the first SCLK high pulse is in the first one of a transmission.

SSC_Tmg_1.vsd

Figure 4-19 SSC Master Mode Timing

5 Packaging

Chapter 5 provides the information of the TC1762 package and reliability section.

5.1 Package Parameters

Table 5-1 provides the characteristics of the package parameters.

Table 5-1 Package Parameters (PG-LQFP-176-2)

Parameter	Symbol		Limit Values		Unit	Notes
			Min.	Max.		
Thermal resistance junction case top[1)]	R_{TJCT}	CC	–	5.4	K/W	–
Thermal resistance junction leads[1)]	R_{TJL}	CC	–	21.5	K/W	–

1) The thermal resistances between the case top and the ambient (R_{TCAT}), the leads and the ambient (R_{TLA}) are to be combined with the thermal resistances between the junction and the case top (R_{TJCT}), the junction and the leads (R_{TJL}) given above, in order to calculate the total thermal resistance between the junction and the ambient (R_{TJA}). The thermal resistances between the case top and the ambient (R_{TCAT}), the leads and the ambient (R_{TLA}) depend on the external system (PCB, case) characteristics, and are under user responsibility. The junction temperature can be calculated using the following equation: $T_J=T_A+R_{TJA} \times P_D$, where the R_{TJA} is the total thermal resistance between the junction and the ambient. This total junction ambient resistance R_{TJA} can be obtained from the upper four partial thermal resistances.

5.2 Package Outline

Figure 5-1 shows the package outlines of the TC1762.

PG-LQFP-176-2
Plastic Low Profile Quad Flat Package

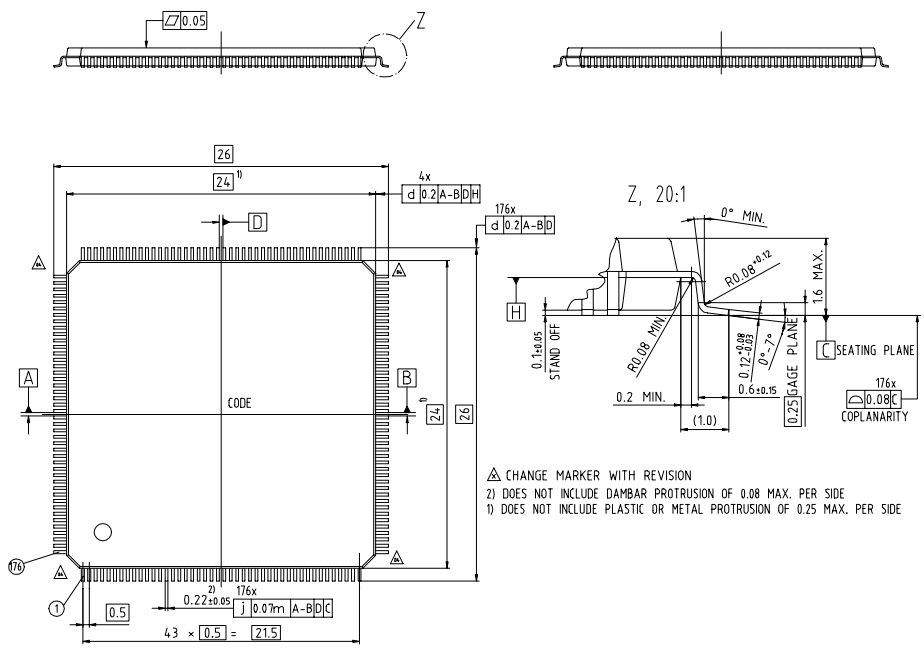


Figure 5-1 Package Outlines PG-LQFP-176-2

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: http://www.infineon.com/products.

SMD = Surface Mounted Device

Dimensions in mm

5.3 Flash Memory Parameters

The data retention time of the TC1762's Flash memory (i.e. the time after which stored data can still be retrieved) depends on the number of times the Flash memory has been erased and programmed.

Table 5-2 Flash Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Program Flash Retention Time, Physical Sector[1) 2)]	t_{RET}	20	–	years	Max. 1000 erase/program cycles
Program Flash Retention Time, Logical Sector[1)2)]	t_{RETL}	20	–	years	Max. 50 erase/program cycles
Data Flash Endurance (32 Kbyte)	N_E	15 000	–	–	Max. data retention time 5 years
Data Flash Endurance, EEPROM Emulation (8 × 4 Kbyte)	N_{E8}	120 000	–	–	Max. data retention time 5 years
Programming Time per Page[3)]	t_{PR}	–	5	ms	–
Program Flash Erase Time per 256-Kbyte sector	t_{ERP}	–	5	s	f_{CPU} = 80 MHz
Data Flash Erase Time per 16-Kbyte sector	t_{ERD}	–	0.625	s	f_{CPU} = 80 MHz
Wake-up time	t_{WU}	$4300 \times 1/f_{CPU}$ + 40µs			

1) Storage and inactive time included.

2) At average weighted junction temperature T_J = 100 °C, or
the retention time at average weighted temperature of T_J = 110 °C is minimum 10 years, or
the retention time at average weighted temperature of T_J = 150 °C is minimum 0.7 years.

3) In case the Program Verify feature detects weak bits, these bits will be programmed once more. The reprogramming takes additional 5ms.

5.4 Quality Declaration

Table 5-3 shows the characteristics of the quality parameters in the TC1762.

Table 5-3 Quality Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Operation Lifetime[1)2)]	t_{OP}	–	24000	hours	At average weighted junction temperature T_J = 127°C
		–	66000	hours	At average weighted junction temperature T_J = 100°C
		–	20	years	At average weighted junction temperature T_J = 85°C
ESD susceptibility according to Human Body Model (HBM)	V_{HBM}	–	2000	V	Conforming to EIA/JESD22-A114-B
ESD susceptibility of the LVDS pins	V_{HBM1}	–	500	V	–
ESD susceptibility according to Charged Device Model (CDM) pins	V_{CDM}	–	500	V	Conforming to JESD22-C101-C
Moisture Sensitivity Level (MSL)	-	–	3	V	Conforming to J-STD-020C for 240°C

1) This lifetime refers only to the time when the device is powered-on.

2) An example of a detailed temperature profile is as below:
2000 hours at T_J = 150°C
16000 hours at T_J = 125°C
6000 hours at T_J = 110°C
This example is equivalent to the operation lifetime and average temperatures given in Table 5-3.

Note: Information about soldering can be found on the "package" information page under: ***http://www.infineon.com/products****.*

w w w . i n f i n e o n . c o m

Published by Infineon Technologies AG