TPS65270 4.5-V to 18-V Input Voltage, 2-A or 3-A Output Current, Dual Synchronous Step-Down Regulator With Integrated MOSFET

1 Features

- Wide Input Supply Voltage Range: 4.5 V to 18 V
- 0.8 V, ±1% Accuracy Reference
- Up to 2-A (Buck 1) and 3-A (Buck 2) Maximum Continuous Output Loading Current
- Low-Power Pulse Skipping Mode to Achieve High Light Load Efficiency
- Adjustable Switching Frequency 300 kHz to 1.4 MHz Set by External Resistor
- Startup With a Prebiased Output Voltage
- Dedicated Enable and Soft Start for Each Buck
- Peak Current-Mode Control With Simple Compensation Circuit
- Cycle-by-Cycle Overcurrent Protection
- 180° Out-of-Phase Operation to Reduce Input Capacitance and Power Supply Induced Noise
- Available in 24-Lead Thermally Enhanced HTSSOP (PWP) and VQFN 4-mm × 4-mm (RGE) Packages

2 Applications

- DTV
- DSL Modems
- Cable Modems
- Set-Top Boxes
- Car DVD Players
- Home Gateway and Access Point Networks
- Wireless Routers

3 Description

The TPS65270 is a monolithic, dual synchronous buck regulator with a wide operating input voltage that can operate in 5-V, 9-V, 12-V, or 15-V bus voltages and battery chemistries. The converters are designed to simplify its application while giving the designer the option to optimize their usage according to the target application.

The TPS65270 features a precision 0.8-V reference and can produce output voltages up to 15 V. Each converter features an enable pin that allows dedicated control of each channel that provides flexibility for power sequencing. Soft-start time in each channel can be adjusted by choosing different external capacitors. TPS65270 is also able to start up with a prebiased output. The converter begins switching when output voltage reaches the prebiased voltage.

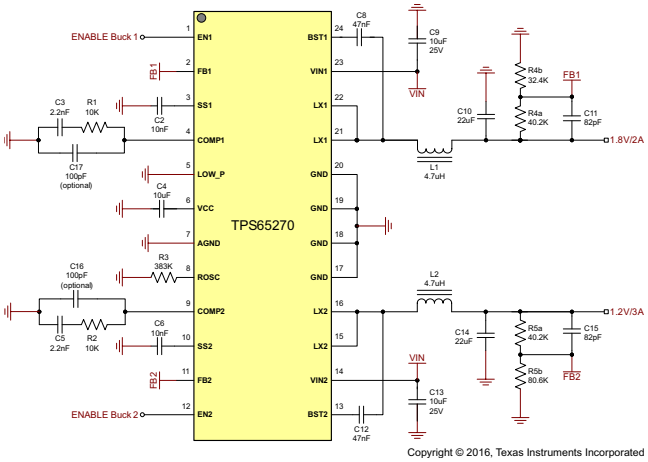
Constant frequency peak current-mode control simplifies the compensation and provides fast transient response. Cycle-by-cycle overcurrent protection and hiccup mode operation limits MOSFET power dissipation in short-circuit or overloading fault conditions. Low-side reverse current protection also prevents excessive sinking current from damaging the converter.

Device Information[1]

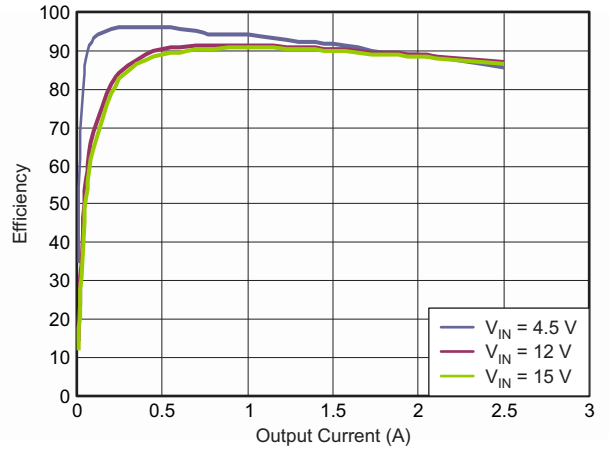
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS65270	HTSSOP (24)	7.80 mm × 4.40 mm
	VQFN (24)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application



Efficiency vs Output Load



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (April 2013) to Revision E **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Deleted *Ordering Information* table; see POA at the end of the data sheet ... 1
- Changed maximum value of Voltage on VIN1, VIN2, LX1, LX2 from 18 to 20 ... 4
- Changed maximum value of Voltage at LX1, LX2 (maximum withstand voltage transient < 10 ns) from 18 to 23 ... 4
- Changed maximum value of Operating virtual junction temperature, T_J from 125 to 150 ... 4
- Changed Ambient temperature (T_A) to Junction temperature (T_J) in *Recommended Operating Conditions* table and maximum value from 85 to 125 ... 4
- Updated values in the *Thermal Information* table to align with JEDEC standards ... 5
- Changed EN1 and EN2 pin threshold (falling) typical value to maximum value in *Electrical Characteristics* table ... 5
- Changed PSM low power mode threshold (falling) typical value to maximum value in *Electrical Characteristics* table ... 5

5 Description (continued)

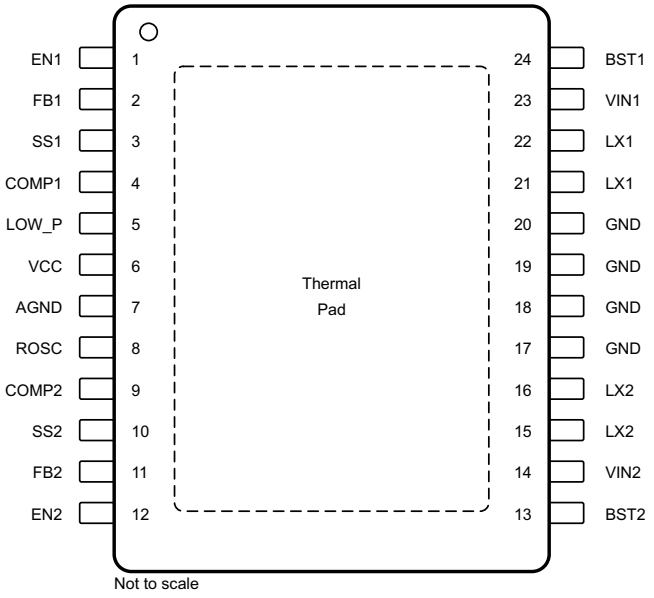
The switching frequency of the converters can be set from 300 KHz to 1.4 MHz with an external resistor. Two converters have 180° out-of-phase clock signals to minimize the input filter requirements and alleviate EMI and input capacitor requirements.

TPS65270 also features a light-load pulse skipping mode (PSM). The PSM mode allows a power loss reduction on the input power supplied to the system at light loading in order to achieve light-load high efficiency.

The TPS65270 is available in a 24-pin, thermally enhanced HTSSOP (PWP) package and 24-pin VQFN (RGE) package.

6 Pin Configuration and Functions

PWP Package
24-Pin HTSSOP
Top View



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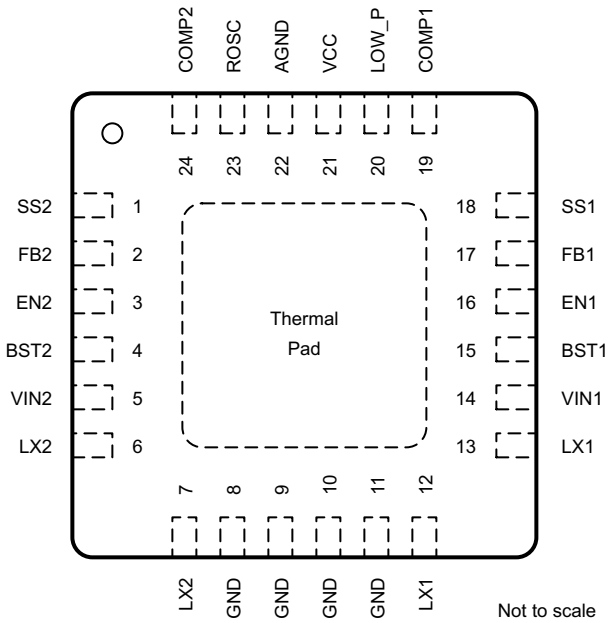
RGE Package
24-Pin VQFN
Top View



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Pin Functions

PIN			I/O	DESCRIPTION
NAME	HTSSOP	VQFN		
AGND	7	22	Power	Analog ground. Connect all GND pins and power pad together.
BST1	24	15	O	Bootstrapped power supply to high side floating gate driver in Buck 1. Connect a 47-nF ceramic capacitor from this pin to the switching node pin LX1.
BST2	13	4	O	Bootstrapped power supply to high side floating gate driver in Buck 2. Connect a 47-nF ceramic capacitor from this pin to the switching node pin LX2.
COMP1	4	19	O	Loop compensation pin for Buck 1. Connect a series RC circuit to this pin to compensate the control loop of this converter.
COMP2	9	24	O	Loop compensation pin for Buck 2. Connect a series RC circuit to this pin to compensate the control loop of this converter.
EN1	1	16	I	Enable for Buck 1. Logic high enables the Buck 1; Logic low disables Buck 1. If pin is left open a weak internal pullup to internal V5V allows for automatic enable; For a delayed start-up add a small ceramic capacitor from this pin to ground.
EN2	12	3	I	Enable for Buck 2. Logic high enables the Buck 2. Logic low disables Buck 2. If pin is left open a weak internal pullup to internal V5V allows for automatic enable; For a delayed start-up add a small ceramic capacitor from this pin to ground.
FB1	2	17	I	Feedback voltage for Buck 1. Connect a resistor divider to set 0.8 V from the output of the converter to ground.

Pin Functions (continued)

PIN			I/O	DESCRIPTION
NAME	HTSSOP	VQFN		
FB2	11	2	I	Feedback voltage for Buck 2. Connect a resistor divider to set 0.8 V from the output of the converter to ground.
GND	17, 18, 19, 20	8, 9, 10, 11	Power	Power ground for Buck 1 and Buck 2.
LOW_P	5	20	I	Low power operation mode. With active high, Buck 1 and Buck 2 operate at pulse skipping mode at light load; active low forces both Buck 1 and Buck 2 to PWM mode; this pin cannot be left open.
LX1	21, 22	12, 13	O	Switching node connecting to inductor for Buck 1.
LX2	15, 16	6, 7	O	Switching node connecting to inductor for Buck 2.
ROSC	8	23	O	Oscillator frequency setup. Connect a resistor to ground to set the frequency of internal oscillator clock.
SS1	3	18	O	Soft start input for Buck 1. An internal 5-µA charging current is sourcing to this pin. Connect a small ceramic capacitor to this pin to set the Buck 1 soft-start time.
SS2	10	1	O	Soft start input for Buck 2. An internal 5-µA charging current is sourcing to this pin. Connect a small ceramic capacitor to this pin to set the Buck 1 soft-start time.
VCC	6	21	O	Internal 6.5-V power supply bias. Connect a 10-µF ceramic capacitor from this pin to ground.
VIN1	23	14	Power	Input supply for Buck 1. Conne ct a 10-µF ceramic capacitor close to this pin.
VIN2	14	5	Power	Input supply for Buck 2. Connect a 10-µF ceramic capacitor close to this pin.
Thermal Pad	—	—	—	Must be soldered to PCB for optimal thermal performance. Have thermal vias on the PCB to enhance power dissipation.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Voltage at VIN1, VIN2, LX1, LX2	–0.3	20	V
Voltage at LX1, LX2 (maximum withstand voltage transient < 10 ns)	–1	23	V
Voltage at BST1, BST2, referenced to LX1, LX2 pin	–0.3	7	V
Voltage at VCC, EN1, EN2, COMP1, COMP2, LOW_P	–0.3	7	V
Voltage at SS1, SS2, FB1, FB2, ROSC	–0.3	3.6	V
Voltage at AGND, GND	–0.3	0.3	V
Operating virtual junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Input operating voltage	4.5	18	V
T_J	Junction temperature	–40	125	°C

7.4 Thermal Information

THERMAL METRIC(1)(2)		TPS65270		UNIT
		PWP (HTSSOP)	RGE (VQFN)	
		24 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	41.3	33.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	23.9	36.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.6	12.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.8	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	22.4	12.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4	2.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) See *PowerPAD™ Thermally Enhanced Package*.

7.5 Electrical Characteristics

T_A = –40°C to 125°C, V_{IN} = 12 V, f_{SW} = 625 kHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY						
V_{IN}	Input Voltage	VIN1 and VIN2	4.5		18	V
IDD_{SDN}	Shutdown	EN1 = EN2 = 0 V		10		µA
IDD_{Q_nsw}	Nonswitching quiescent power supply current	V_{FB1} = V_{FB2} = 900 mV, LOW_P = high		1		mA
UVLO	V_{IN} undervoltage lockout	Rising V_{IN}	4	4.2	4.45	V
		Falling V_{IN}	3.65	3.85	4.1	
		Hysteresis		0.35		
V_{CC}	Internal biasing supply	V_{CC} load current = 0 A, V_{IN} = 12 V		6.25		V
V_{CC_drop}	V_{CC}LDO Dropout Voltage	V_{IN} = 5 V, V_{CC} load current = 20 mA		180		mV
I_{VCC}	V_{CC} current limit	4.5 V < V_{IN} < 18 V		200		mA
FEEDBACK AND ERROR AMPLIFIER						
V_{FB}	Regulated feedback voltage	V_{IN} = 12 V , V_{COM}P = 1.2 V, T_J = 25°C	–1%	0.8	1%	V
		V_{IN} = 12 V, V_{COMP} = 1.2 V, T_J = –40°C to 125°C	–2%	0.8	2%	
$V_{LINEREG}$	Line regulation: DC	V_{IN} = 4.5 V to 18 V, I_{OUT} = 1 A		0.5		%/V
$V_{LOADREG}$	Load regulation: DC	I_{OUT} = 10% to 90%, $I_{OUT,MAX}$		0.4		%/A
G_{m_EA}	Error amplifier transconductance	–2 µA < I_{COMP} < 2 µA		130		µs
G_{m_SRC}	COMP voltage to inductor current Gm	ILX = 0.5 A		10		A/V
ENABLE, PFM MODE AND SOFT START						
V_{EN}	EN1 and EN2 pin threshold	Rising	1.55			V
		Falling			0.4	
V_{PSM}	PSM low power mode threshold	Rising	1.55			V
		Falling			0.4	
I_{SS}	SS1 and SS2 soft-start charging current			5		µA
OSCILLATOR						
F_{SW_BK}	Switching frequency	Set by external resistor ROSC	0.3		1.4	MHz
F_{SW}	Programmable frequency	ROSC = 250 kΩ	0.85	1	1.15	MHz
		ROSC = 500 kΩ	425	500	575	kHz
PROTECTION						
I_{LIMIT1}	Buck 1 peak inductor current limit	4.5 V < V_{IN} < 18 V		3.2		A
I_{LIMIT1_LS1}	Buck 1 low side MOSFET current limit	4.5 V < V_{IN} < 18 V		2		A
I_{LIMIT2}	Buck 2 peak inductor current limit	4.5 V < V_{IN} < 18 V		4.1		A
I_{LIMIT1_LS2}	Buck 2 low side MOSFET current limit	4.5 V < V_{IN} < 18 V		2		A

Electrical Characteristics (continued)

T_A = –40°C to 125°C, V_{IN} = 12 V, f_{SW} = 625 kHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
MOSFET ON-RESISTANCES						
R_{dson_HS1}	On resistance of high side FET on CH1	BST1 to LX1 = 6.25 V		120		mΩ
R_{dson_LS1}	On resistance of low side FET on CH1	V_{IN} = 12 V		80		mΩ
R_{dson_HS2}	On resistance of high side FET on CH2	BST2 to LX2 = 6.25 V		95		mΩ
R_{dson_LS2}	On resistance of low side FET on CH2	V_{IN} = 12 V		50		mΩ
T_{on_min}	Minimum in time			80	120	ns
THERMAL SHUTDOWN						
T_{TRIP}	Thermal protection trip point	Rising temperature		160		°C
T_{HYST}	Thermal protection hysteresis			20		°C

7.6 Typical Characteristics

T_A = 25°C, V_{IN} = 12 V, f_{SW} = 625 kHz (unless otherwise noted)

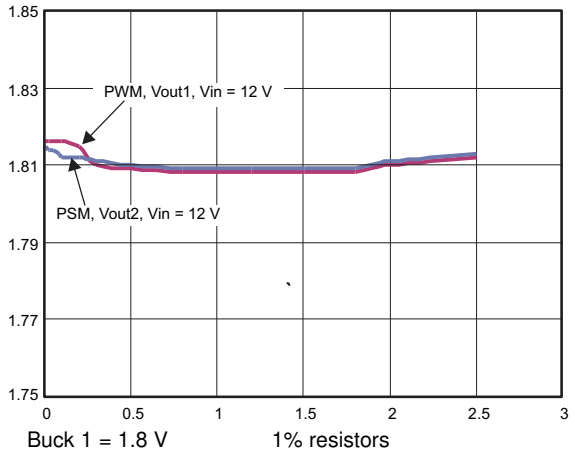


Figure 1. Load Regulation

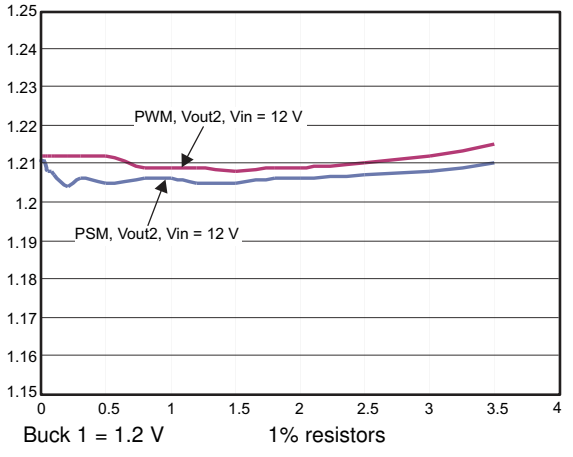


Figure 2. Load Regulation

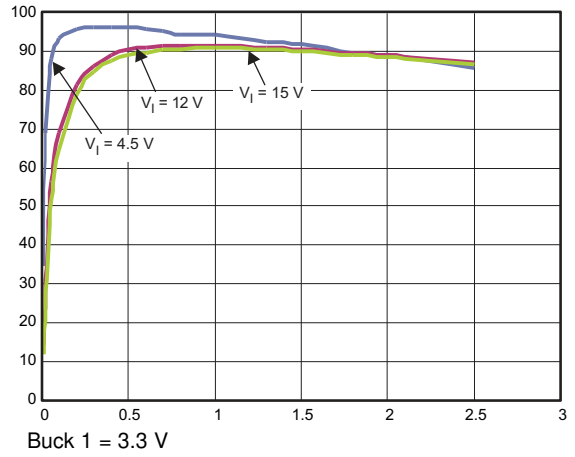


Figure 3. Efficiency

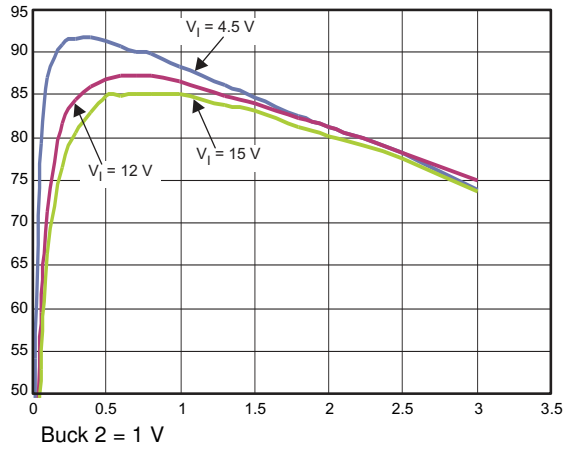


Figure 4. Efficiency

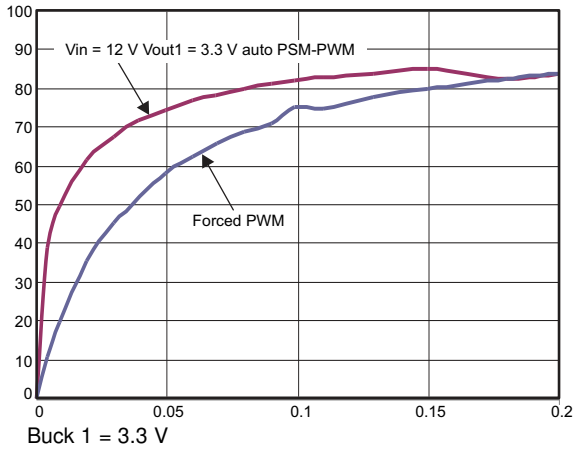


Figure 5. Efficiency

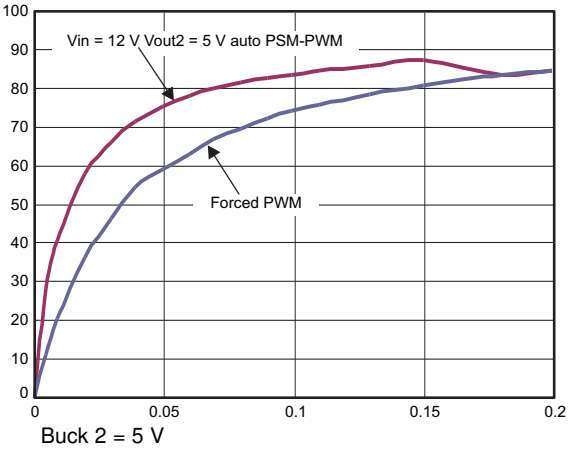


Figure 6. Efficiency

8 Detailed Description

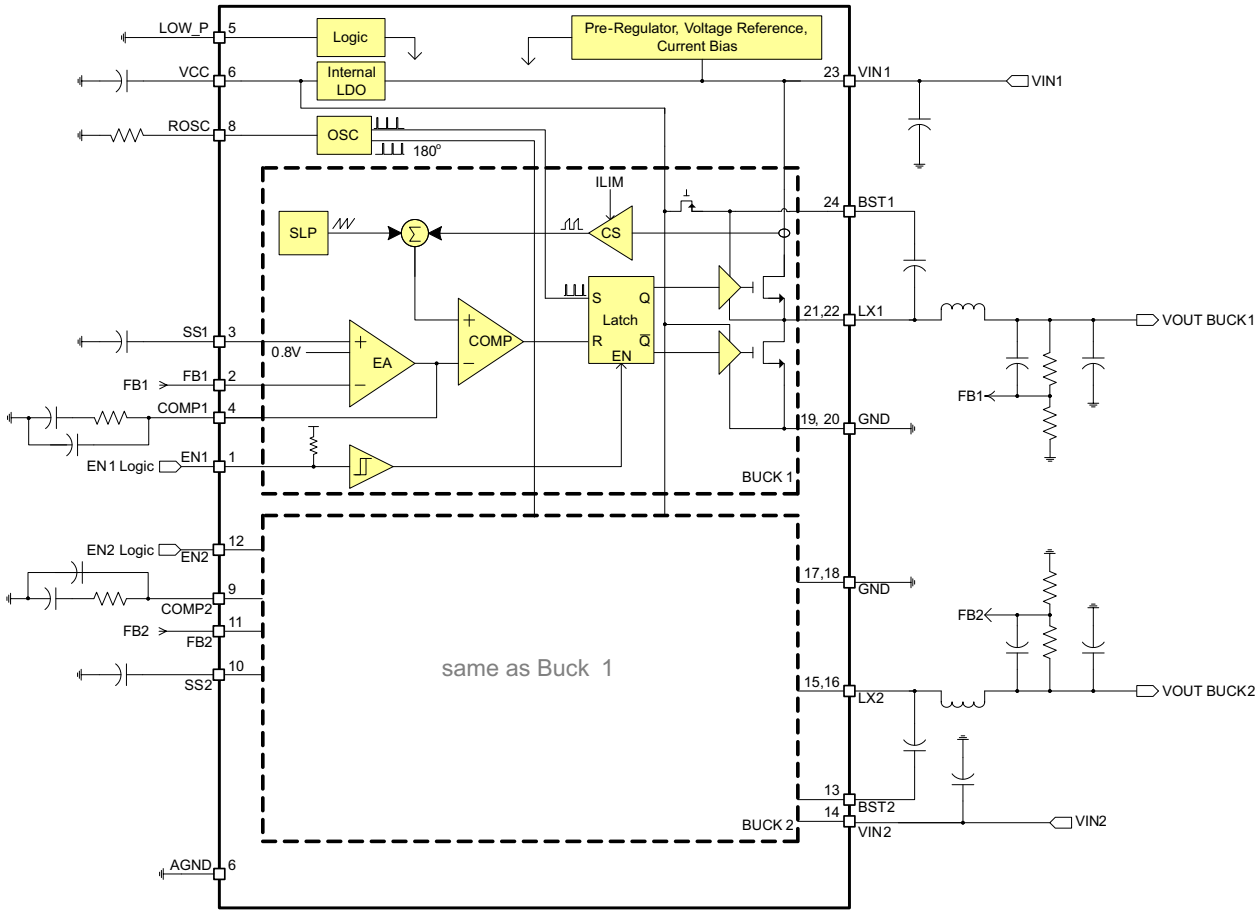
8.1 Overview

TPS65270 is a power management IC with two step-down buck converters. Both high-side and low-side MOSFETs are integrated to provide fully synchronous conversion with higher efficiency. TPS65270 can support 4.5-V to 18-V input supply, 2-A continuous current for Buck 1 and 3 A for Buck 2. The buck converters have an automatic PSM mode, which can improve power dissipation during light loads. Alternatively, the device implements a constant frequency mode by connecting the LOW_P pin to ground. The wide switching frequency of 300 kHz to 1.4 MHz allows for efficiency and size optimization. The switching frequency is adjustable by selecting a resistor to ground on the ROSC pin. Input ripple is reduced by 180° out-of-phase operation between Buck 1 and Buck 2.

Both buck converters have peak current mode control which simplifies the loop compensation. A traditional type II compensation network can stabilize the system and achieve fast transient response. Moreover, an optional capacitor in parallel with the upper resistor of the feedback divider provides one more zero and makes the crossover frequency over 100 kHz. Each buck converter has an individual cycle-by-cycle current limit and low side reverse current limit.

The device has a built-in LDO regulator. During a standby mode, the 6.5-V LDO can be used to drive MCU and other active loads. with this LDO, system is able to turn off the two buck converters so as to reduce the power consumption and improve the standby efficiency. Each converter has its own programmable soft start that can reduce the input inrush current. The individual Enable pins for each independent control of each output voltage and power sequence.

8.2 Functional Block Diagram



Note: Pin numbers in block diagram are for HTSSOP (PWP) 24-pin package.

8.3 Feature Description

8.3.1 Adjustable Switching Frequency

To select the internal switching frequency connect a resistor from ROSC to ground. Figure 7 shows the required resistance for a given switching frequency.

Feature Description (continued)

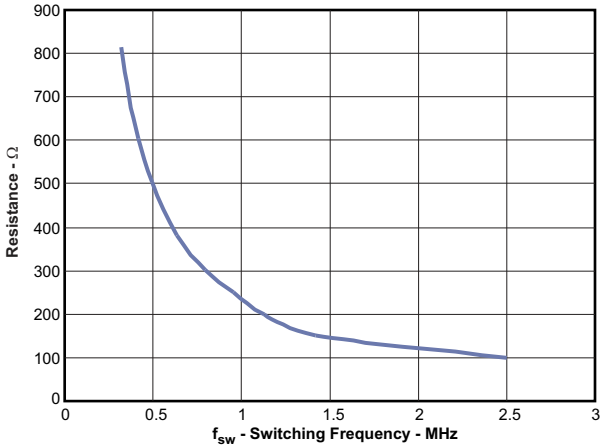


Figure 7. ROSC vs Switching Frequency

$$R_{OSC}(k\Omega) = 239.13 \times f_{SW}^{-1.149} \quad (1)$$

For operation at 800 kHz, a 300-kΩ resistor is required.

8.3.2 Out-of-Phase Operation

To reduce input ripple current, Buck 1 and Buck 2 operate 180° out-of-phase. This enables the system having less input ripple, then to lower component cost, save board space and reduce EMI.

8.3.3 Delayed Start-Up

If a delayed start-up is required on any of the buck converters fit a ceramic capacitor to the ENx pins. The delay added is approximately 0.75 ms per nF connected to the pin. The EN pins have a weak 1-MΩ pullup to the 5-V rail.

8.3.4 Soft-Start Time

The device has an internal pullup current source of 5 µA that charges an external slow start capacitor to implement a slow start time. Equation 2 shows how to select a slow start capacitor based on an expected slow start time. The voltage reference (V_{REF}) is 0.8 V and the slow start charge current (I_{ss}) is 5 µA. The soft-start circuit requires 1 nF per 160 µs to be connected at the SS pin. An 800-µs soft-start time is implemented for all converters fitting 4.7 nF to the relevant pins.

$$t_{SS}\ (ms) = V_{REF}\ (V) \times \left(\frac{C_{SS}\ (nF)}{I_{SS}\ (\mu A)} \right) \quad (2)$$

8.3.5 Adjusting the Output Voltage

The output voltage is set with a resistor divider from the output node to the FB pin. TI recommends using divider resistors of 1% tolerance or better. To improve efficiency at light load, start with 40.2 kΩ for the R1 resistor and use the Equation 3 to calculate R2.

$$R2 = R1 \times \left(\frac{0.8\ V}{V_O - 0.8\ V} \right) \quad (3)$$

Feature Description (continued)

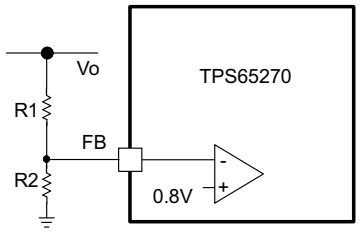


Figure 8. Voltage Divider Circuit

8.3.6 Error Amplifier

The device has a transconductance error amplifier. The transconductance of the error amplifier is 130 µA/V during normal operation. The frequency compensation network is connected between the COMP pin and ground.

8.3.7 Slope Compensation

The device has a built-in slope compensation ramp. The slope compensation can prevent subharmonic oscillations in peak current mode control when duty cycle becomes too large.

8.3.8 Overcurrent Protection

The current through the internal high-side MOSFET is sampled and scaled through an internal pilot device during the hig time. The sampled current is compared to overcurrent limit. If the peak inductor current exceeds the overcurrent limit reference level, an internal overcurrent fault counter is set to 1 and an internal flag is set. The internal power MOSFET is immediately turned off and is not turned on again until the next switching cycle. The protection circuitry continues to monitor the current and turns off the internal MOSFET as described. If the overcurrent condition persists for four sequential clock cycles, the overcurrent fault counter overflows indicating an overcurrent fault condition exists. The regulator is shut down and power good goes low. If the overcurrent condition clears before the counter reaches four consecutive cycles, the internal flag and counter are reset. The protection circuitry attempts to recover from the overcurrent condition after waiting four soft-start cycles. The internal overcurrent flag and counter are reset. A normal soft-start cycle is attempted and normal operation continues if the fault condition has cleared. If the overcurrent fault counter overflows during soft start, the converter shuts down and this hiccup mode operation repeats.

8.3.9 Thermal Shutdown

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 160°C. The thermal shutdown forces the device to stop switching when the junction temperature exceeds thermal trip threshold. Once the die temperature decreases below 140°C, the device reinitiates the power up sequence. The thermal shutdown hysteresis is 20°C.

8.3.10 Low Power Mode Operation

By pulling the Low_P pin high all converters operate in pulse-skipping mode, greatly reducing the overall power consumption at light and no load conditions. When LOW_P is tied to low, all converters run in forced PWM mode.

8.4 Device Functional Modes

8.4.1 Operation With Minimum V_{IN} (V_{IN} < 4.45 V)

The device will operate with input voltages above the 4.45-V UVLO maximum voltage. The typical UVLO voltage is 4.2 V and the device may operate at input voltage above this point. The device may also operate with lower input voltages; the minimum UVLO voltage is 4 V (rising) and 3.65 V (falling). The device will not operate with input voltages below the UVLO minimum voltage.

Device Functional Modes (continued)

8.4.2 Operation With EN Control

The enable rising edge threshold voltage is 1.55 V (minimum) and falling edge threshold voltage is 0.4 V (maximum). With EN held below 0.4 V the device is disabled and switching is inhibited. The IC quiescent current is reduced in this state. The device becomes active when input voltage is above the UVLO threshold and the EN voltage is increased above 1.55 V. Switching is enabled and the internal soft-start sequence is initiated as shown in Figure 13.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The device is a dual-synchronous, step-down DC-DC converter. It is typically used to convert a higher DC voltage to lower DC voltages with continuous available output current of 2 A or 3 A.

9.2 Typical Application

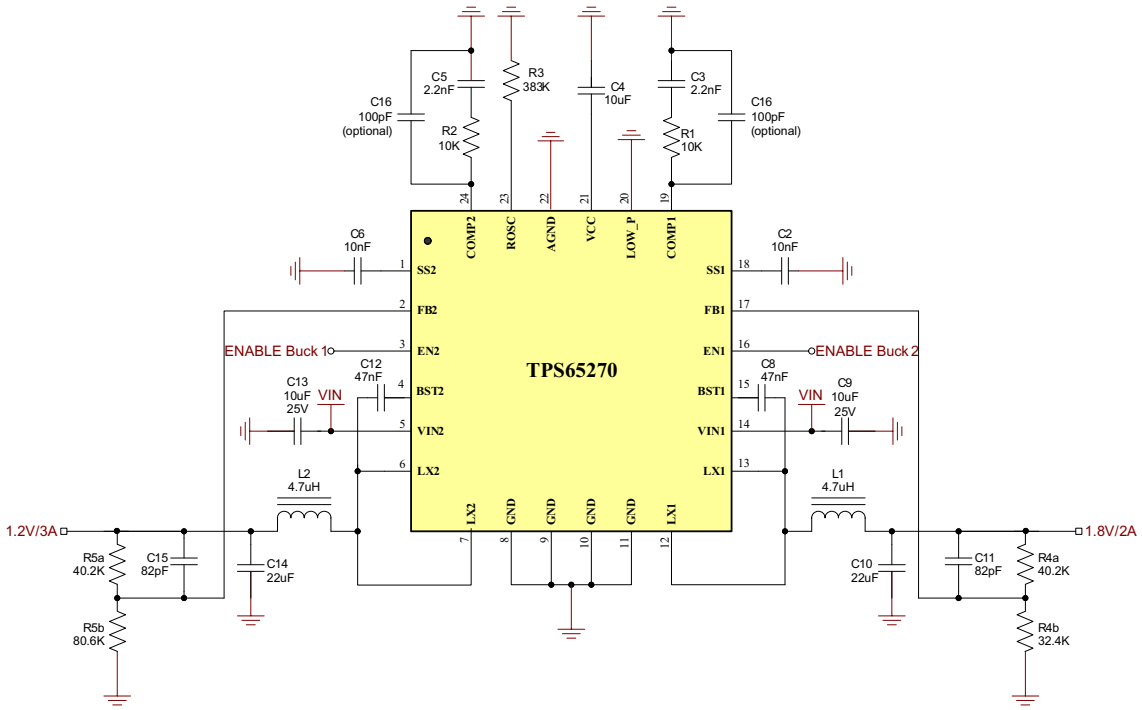


Figure 9. Typical Application Schematic

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 1 as the input parameters.

Table 1. Design Parameters

PARAMETER	EXAMPLE VALUE
$V_{OUT}1$	1.8 V
$I_{OUT}1$	2 A
$V_{OUT}2$	1.2 V
$I_{OUT}2$	3 A
Transient response (1-A load step)	±5%
Input voltage	12 V (typical), 4.5 V to 18 V
Output voltage ripple	±1%
Switching frequency	625 kHz

9.2.2 Detailed Design Procedure

9.2.2.1 Output Inductor Selection

To calculate the value of the output inductor, use Equation 4. LIR is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. The inductor ripple current is filtered by the output capacitor. Therefore, choosing high inductor ripple currents impact the selection of the output capacitor since the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. In general, the inductor ripple value is at the discretion of the designer; however, LIR is normally from 0.1 to 0.3 for the majority of applications.

$$L = \frac{V_{IN\ max} - V_{OUT}}{I_O \times LIR} \times \frac{V_{OUT}}{V_{IN\ max} \times f_{SW}} \quad (4)$$

For the output filter inductor, it is important that the RMS current and saturation current ratings not be exceeded. The RMS and peak inductor current can be found from Equation 6 and Equation 7.

$$I_{ripple} = \frac{V_{IN\ max} - V_{OUT}}{L} \times \frac{V_{OUT}}{V_{IN\ max} \times f_{SW}} \quad (5)$$

$$I_{Lrms} = \sqrt{I_O^2 + \frac{\left(\frac{V_{OUT} \times (V_{IN\ max} - V_{OUT})}{V_{IN\ max} \times L \times f_{SW}}\right)^2}{12}} \quad (6)$$

$$I_{Lpeak} = I_{OUT} + \frac{I_{ripple}}{2} \quad (7)$$

The current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults or transient load conditions, the inductor current can increase above the calculated peak inductor current level calculated above. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switch current limit rather than the peak inductor current.

9.2.2.2 Output Capacitor Selection

There are three primary considerations for selecting the value of the output capacitor. The output capacitor determines the modulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance needs to be selected based on the most stringent of these three criteria.

The desired response to a large change in the load current is the first criteria. The output capacitor needs to supply the load with current when the regulator cannot. This situation would occur if there are desired hold-up times for the regulator where the output capacitor must hold the output voltage above a certain level for a specified amount of time after the input power is removed. The regulator is also temporarily not able to supply sufficient output current if there is a large, fast increase in the current needs of the load such as a transition from no load to full load. The regulator usually needs two or more clock cycles for the control loop to see the change in load current and output voltage and adjust the duty cycle to react to the change. The output capacitor must be sized to supply the extra current to the load until the control loop responds to the load change. The output capacitance must be large enough to supply the difference in current for 2 clock cycles while only allowing a tolerable amount of droop in the output voltage. Equation 8 shows the minimum output capacitance necessary to accomplish this.

$$C_O = \frac{2 \times \Delta I_{OUT}}{f_{SW} \times \Delta V_{OUT}} \quad (8)$$

where

- ΔI_{out} is the change in output current
- f_{sw} is the regulators switching frequency
- ΔV_{out} is the allowable change in the output voltage.

Equation 9 calculates the minimum output capacitance needed to meet the output voltage ripple specification.

$$C_O > \frac{1}{8 \times f_{SW}} \times \frac{1}{\frac{V_{Oripple}}{I_{Oripple}}}$$

where

- f_{sw} is the switching frequency.
- V_{ripple} is the maximum allowable output voltage ripple.
- I_{ripple} is the inductor ripple current. (9)

Equation 10 calculates the maximum ESR an output capacitor can have to meet the output voltage ripple specification.

$$R_{esr} < \frac{V_{Oripple}}{I_{Oripple}} \quad (10)$$

Additional capacitance deratings for aging, temperature and DC bias should be factored in which increases this minimum value. Capacitors generally have limits to the amount of ripple current they can handle without failing or producing excess heat. An output capacitor that can support the inductor ripple current must be specified. Some capacitor data sheets specify the root mean square (RMS) value of the maximum ripple current. Equation 11 can be used to calculate the RMS ripple current the output capacitor needs to support.

$$I_{Lrms} = \frac{V_{OUT} \times (V_{IN\ max} - V_{OUT})}{\sqrt{12} \times V_{IN\ max} \times L \times f_{SW}} \quad (11)$$

9.2.2.3 Input Capacitor Selection

The TPS65265 requires a high quality ceramic, type X5R or X7R, input decoupling capacitor of at least 10 µF of effective capacitance on the PVIN input voltage pins. These capacitors must be connected as close as physically possible to the input pins of the converters. In some applications additional bulk capacitance may also be required for the PVIN input. The effective capacitance includes any DC bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of The TPS65265. The input ripple current can be calculated using Equation 12.

$$I_{INrms} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN\ min}} \times \frac{(V_{IN\ min} \times V_{OUT})}{V_{IN\ min}}} \quad (12)$$

The value of a ceramic capacitor varies significantly over temperature and the amount of DC bias applied to the capacitor. The capacitance variations due to temperature can be minimized by selecting a dielectric material that is stable over temperature. X5R and X7R ceramic dielectrics are usually selected for power regulator capacitors because they have a high capacitance to volume ratio and are fairly stable over temperature. The output capacitor must also be selected with the DC bias taken into account. The capacitance value of a capacitor decreases as the DC bias across a capacitor increases. The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 13.

$$\Delta V_{IN} = \frac{I_{OUT\,max} \times 0.25}{C_{IN} \times f_{SW}} \quad (13)$$

9.2.2.4 Bootstrap Capacitor Selection

The device has two integrated boot regulators and requires a small ceramic capacitor between BST and LX pins to provide the gate drive voltage for the high side MOSFET. TI recommends a ceramic capacitor of 0.047 µF. A ceramic capacitor with an X7R or X5R grade dielectric is desired because of the stable characteristics over temperature and voltage.

9.2.2.5 Loop Compensation

TPS65270 is a current mode control DC-DC converter. The error amplifier has 130-µA/V transconductance.

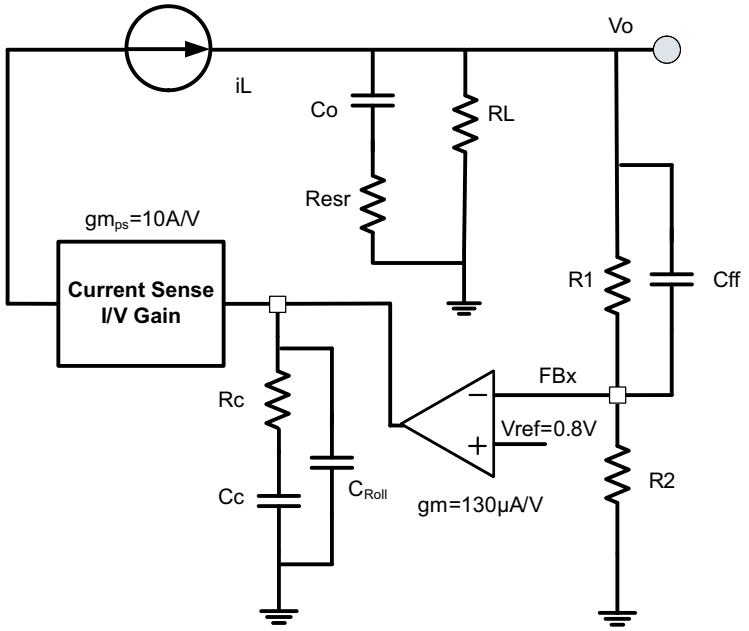


Figure 10. Loop Compensation

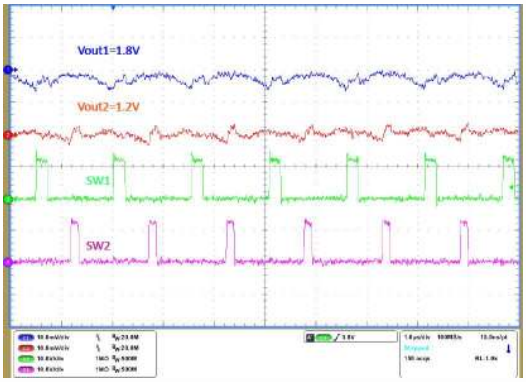
A typical compensation circuit could be type II (R_C and C_C) to have a phase margin from 60 to 90 degrees, or type III (R_C, C_C and C_{ff}) to improve the converter transient response. C_{Roll} adds a high frequency pole to attenuate high-frequency noise when required. It may also prevent noise coupling from other rails if there is possibility of cross coupling between rails when layout is very compact.

To calculate the external compensation components follow the following steps:

	TYPE II CIRCUIT	TYPE III CIRCUIT
Select switching frequency that is appropriate for application depending on L, C sizes, output ripple, EMI concerns and etc. Switching frequencies from 500 kHz to 1 MHz give best trade off between performance and cost. When using smaller L and Cs, switching frequency can be increased. To optimize efficiency, switching frequency can be lowered.	—	Use type III circuit for switching frequencies higher than 500 kHz.
Select cross over frequency (f_C) to be less than 1/5 to 1/10 of switching frequency.	Suggested $f_C = f_S / 10$	Suggested $f_C = f_S / 10$
Set and calculate R_C.	$R_C = \frac{2\pi \times f_c \times V_O \times C_O}{g_M \times Vref \times gm_{ps}}$	$R_C = \frac{2\pi \times f_c \times C_O}{g_M \times gm_{ps}}$
Calculate C_C by placing a compensation zero at or before the converter dominant pole $fp = \frac{1}{C_O \times R_L \times 2\pi}$	$C_c = \frac{R_L \times Co}{R_c}$	$C_c = \frac{R_L \times Co}{R_c}$
Add C_{Roll} if required to remove large signal coupling to high impedance COMP node. Make sure that $fp_{Roll} = \frac{1}{2 \times \pi \times R_C \times C_{Roll}}$ is at least twice the cross over frequency.	$C_{Roll} = \frac{Re_{sr} \times C_O}{R_C}$	$C_{Roll} = \frac{Re_{sr} \times C_O}{R_C}$
Calculate C_{ff} compensation zero at low frequency to boost the phase margin at the crossover frequency. Make sure that the zero frequency (fz_{ff} is smaller than soft start equivalent frequency (1 / T_{ss}).	—	$C_{ff} = \frac{1}{2 \times \pi \times fz_{ff} \times R_1}$

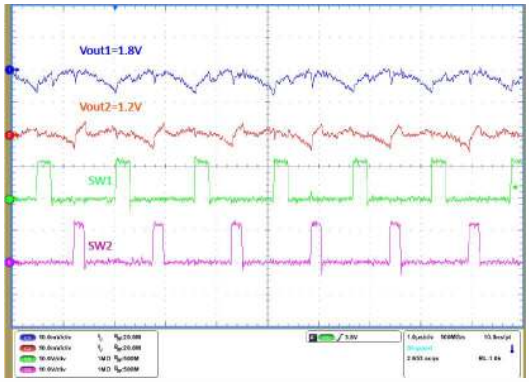
9.2.3 Application Curves

T_A = 25°C, V_{IN} = 12 V, f_{SW} = 625 kHz (unless otherwise noted).



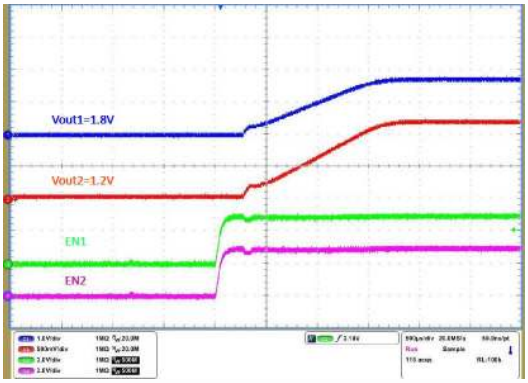
I_{O1} = 0 A I_{O2} = 0 A

Figure 11. Buck 1 and Buck 2 in Steady State



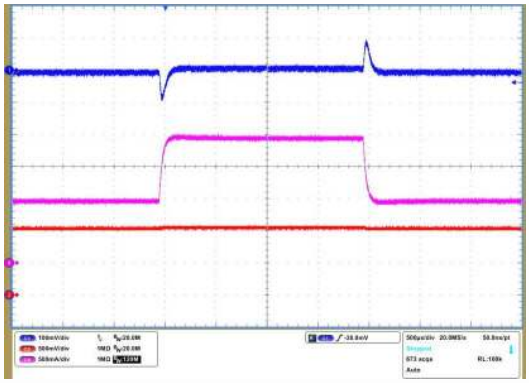
I_{O1} = 2 A I_{O2} = 3 A

Figure 12. Buck 1 and Buck 2 in Steady State



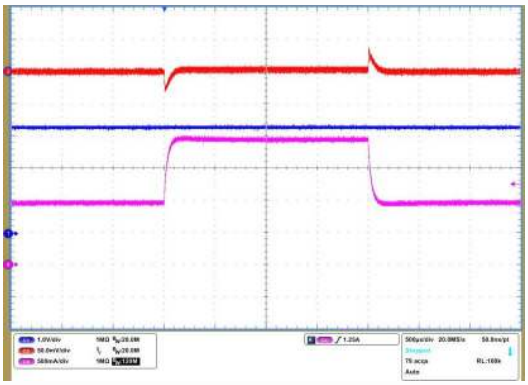
V_{O1} = 1.8 V V_{O2} = 1.2 V

Figure 13. Start-Up With EN



V_{O1} = 3.3 V I_{O1} = 1 A to 2 A

Figure 14. Buck 1 Load Transient



V_{O2} = 1 V I_{O1} = 1 A to 2 A

Figure 15. Buck 2 Load Transient

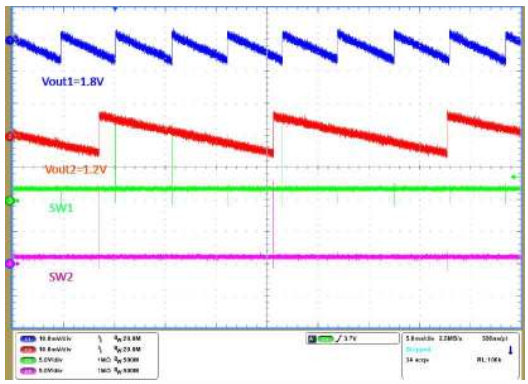


Figure 16. Buck 1 and Buck 2 in PSM Mode

T_A = 25°C, V_{IN} = 12 V, f_{SW} = 625 kHz (unless otherwise noted).

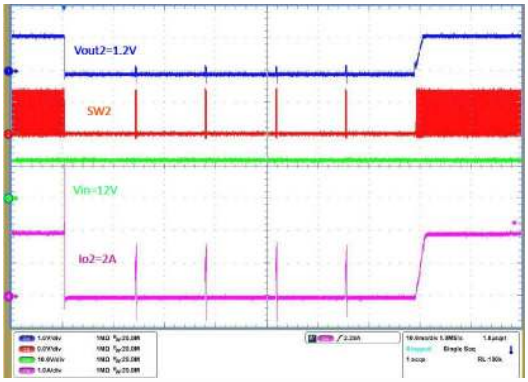


Figure 17. Buck 2 Hard Short and Recover

10 Power Supply Recommendations

The device is designed to operate with an input voltage supply from 4.5 V to 18 V. This input power supply must be well regulated. If the input supply is placed more than a few inches from the TPS65270 converter, bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 47 µF is a typical choice.

11 Layout

11.1 Layout Guidelines

Layout is a critical portion of PMIC designs.

- Place VOUT, and LX on the top layer and an inner power plane for VIN.
- Fit also on the top layer connections for the remaining pins of the PMIC and a large top side area filled with ground.
- The top layer ground area sould be connected to the bottom ground layer(s) using vias at the input bypass capacitor, the output filter cpacitor and directly under the TPS65270 device to provide a thermal path from the Powerpad land to ground.
- The AGND pin must be tied directly to the power pad under the IC and the power pad.
- For operation at full rated load, the top side ground area together with the bottom ground plane, must provide adequate heat dissipating area.
- There are several signals paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance. To help eliminate these problems, the VIN pin must be bypassed to ground with a low ESR ceramic bypass capacitor with X5R or X7R dielectric. Minimize the loop area formed by the bypass capacitor connections, the VIN pins, and the ground connections. Because the LX connection is the switching node, the output inductor must be placed close to the LX pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling.
- The output filter capacitor ground must use the same power ground trace as the VIN input bypass capacitor. Try to minimize this conductor length while maintaining adequate width.
- The compensation must be as close as possible to the COMP pins. The COMP and OSC pins are sensitive to noise so the components associated to these pins must be placed as close as possible to the IC and routed with minimal lengths of trace.

11.2 Layout Example

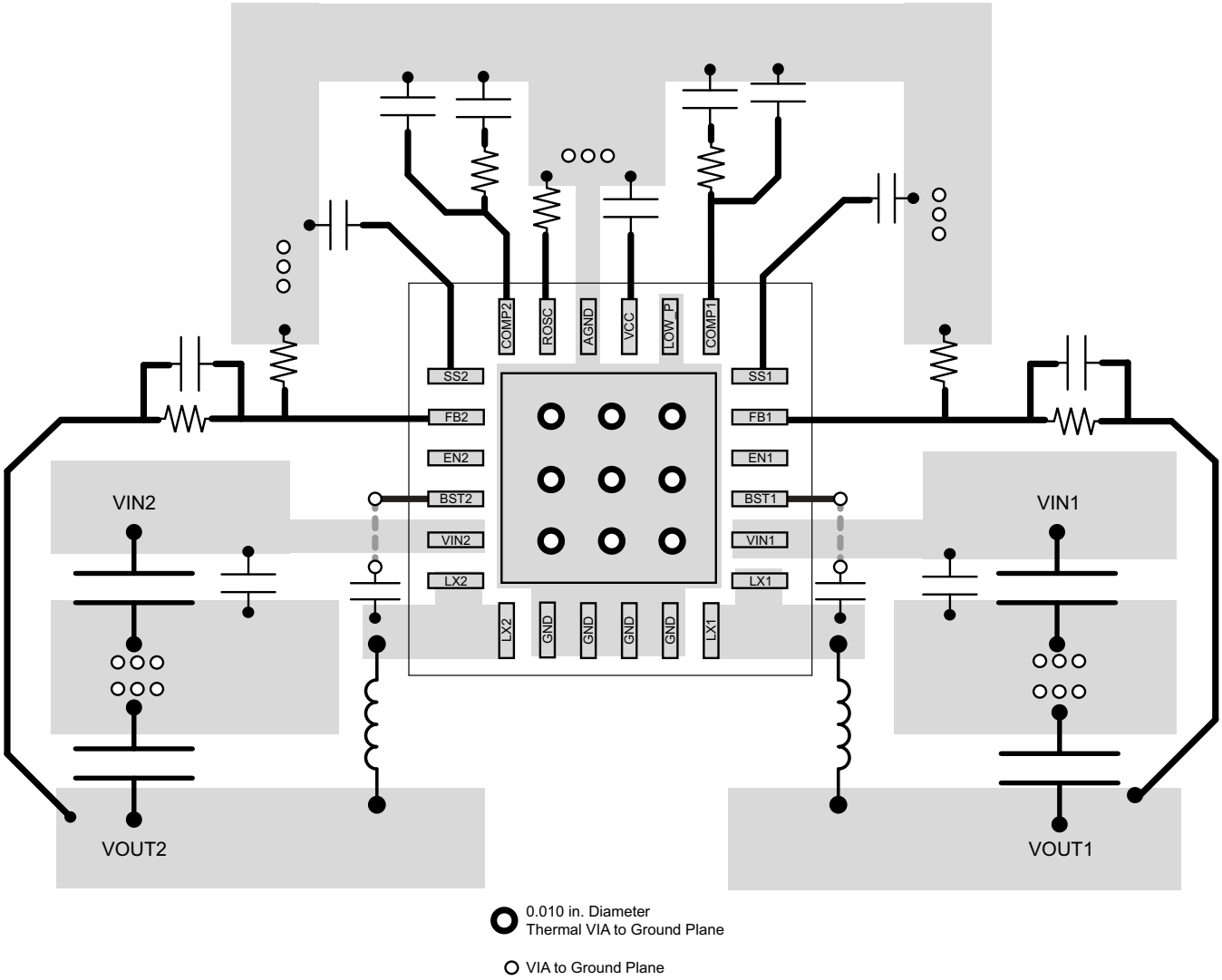


Figure 18. Example Layout for the TPS65270

11.3 Power Dissipation

The total power dissipation inside TPS65270 must not exceed the maximum allowable junction temperature of 125°C to maintain reliable operation. The maximum allowable power dissipation is a function of the thermal resistance of the package ($R_{\theta JA}$) and ambient temperature.

To calculate the temperature inside the device under continuous loading use the following procedure.

1. Define the set voltage for each converter.
2. Define the continuous loading on each converter. Make sure do not exceed the converter maximum loading.
3. Determine from the graphs below the expected losses in watts per converter inside the device. The losses depend on the input supply, the selected switching frequency, the output voltage and the converter chosen.

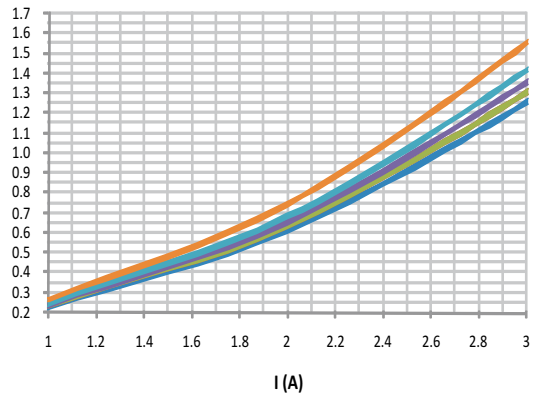
Power Dissipation (continued)

4. To calculate the maximum temperature inside the IC use the following formula:

$$T_{HOT\_SPOT} = T_A + P_{DIS} \times R_{\theta JA} \quad (14)$$

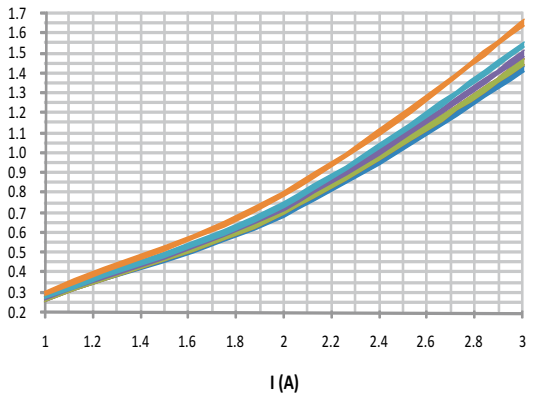
where

- P_{DIS} is the sum of losses in all converters
- $R_{\theta JA}$ is the junction to ambient thermal impedance of the device and it is heavily dependant on board layout



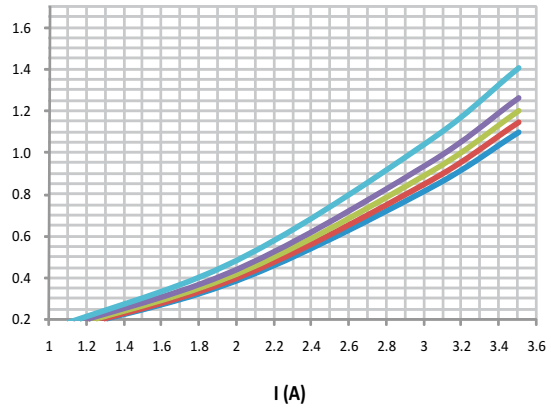
V_{IN} = 12 V f_{SW} = 500 kHz
V_{OUT} (from top to bottom) = 5 V, 3.3 V, 2.5 V, 1.8 V, 1.2 V

Figure 19. Buck 1



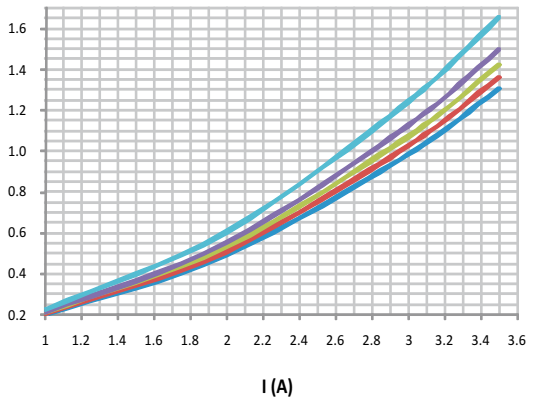
V_{IN} = 12 V f_{SW} = 1.1 MHz
V_{OUT} (from top to bottom) = 5 V, 3.3 V, 2.5 V, 1.8 V, 1.2 V

Figure 20. Buck 1



V_{IN} = 12 V f_{SW} = 500 kHz
V_{OUT} (from top to bottom) = 5 V, 3.3 V, 2.5 V, 1.8 V, 1.2 V

Figure 21. Buck 2



V_{IN} = 12 V f_{SW} = 1.1 MHz
V_{OUT} (from top to bottom) = 5 V, 3.3 V, 2.5 V, 1.8 V, 1.2 V

Figure 22. Buck 2

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

PowerPAD™ Thermally Enhanced Package (SLMA002)

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65270PWPR	ACTIVE	HTSSOP	PWP	24	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS65270	Samples
TPS65270RGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS 65270	Samples
TPS65270RGET	ACTIVE	VQFN	RGE	24	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS 65270	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

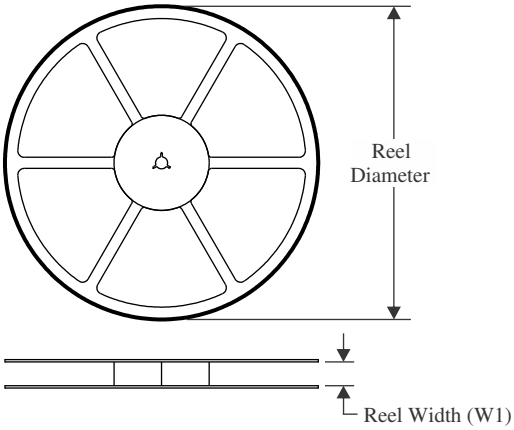
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

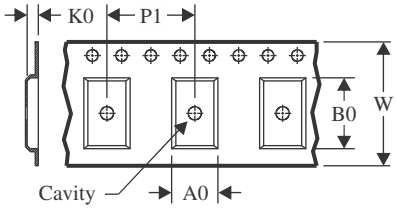
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

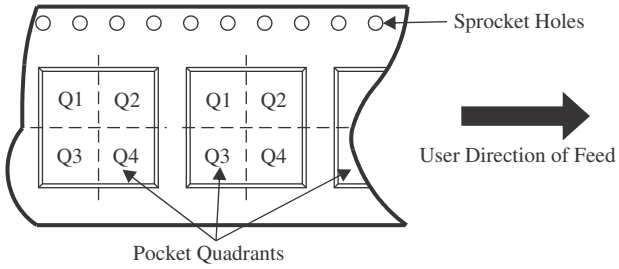


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

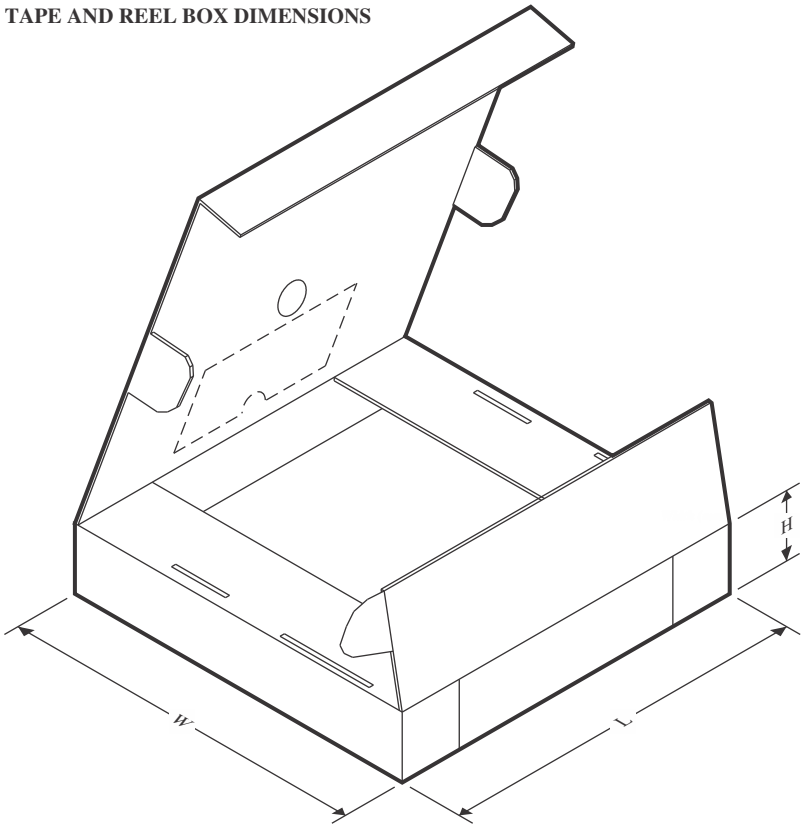
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65270PWPR	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
TPS65270RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS65270RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65270PWPR	HTSSOP	PWP	24	2000	356.0	356.0	35.0
TPS65270RGER	VQFN	RGE	24	3000	346.0	346.0	33.0
TPS65270RGET	VQFN	RGE	24	250	182.0	182.0	20.0

GENERIC PACKAGE VIEW

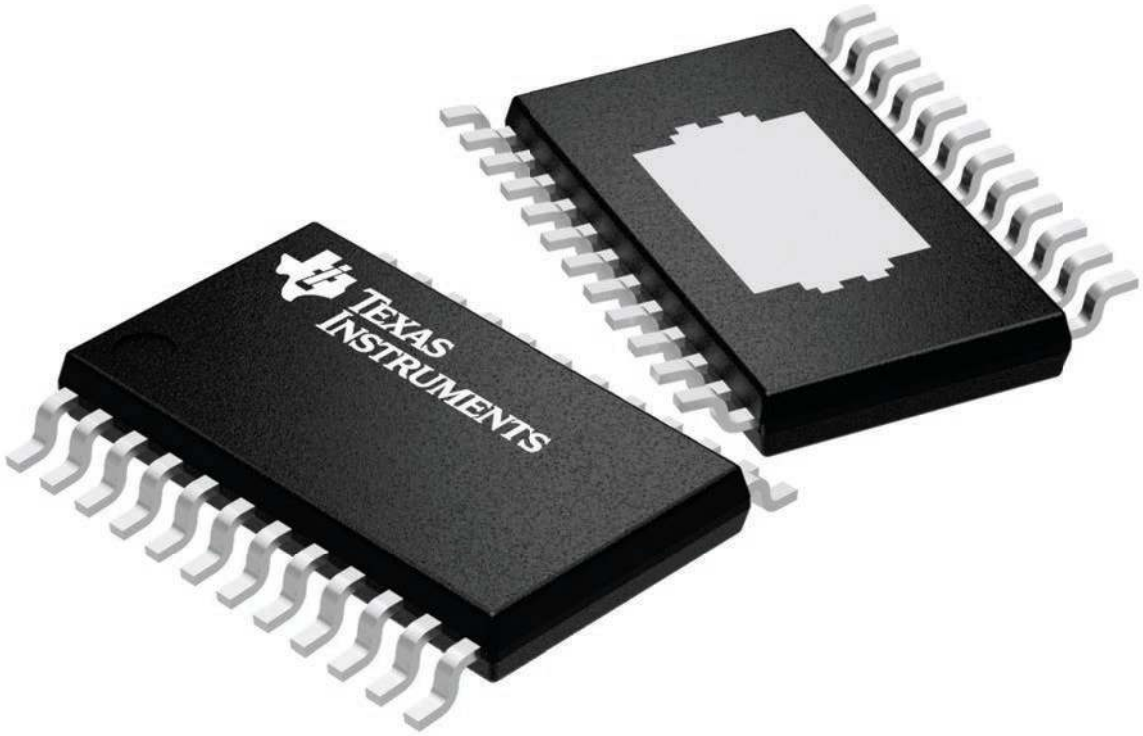
PWP 24

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 7.6, 0.65 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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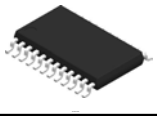
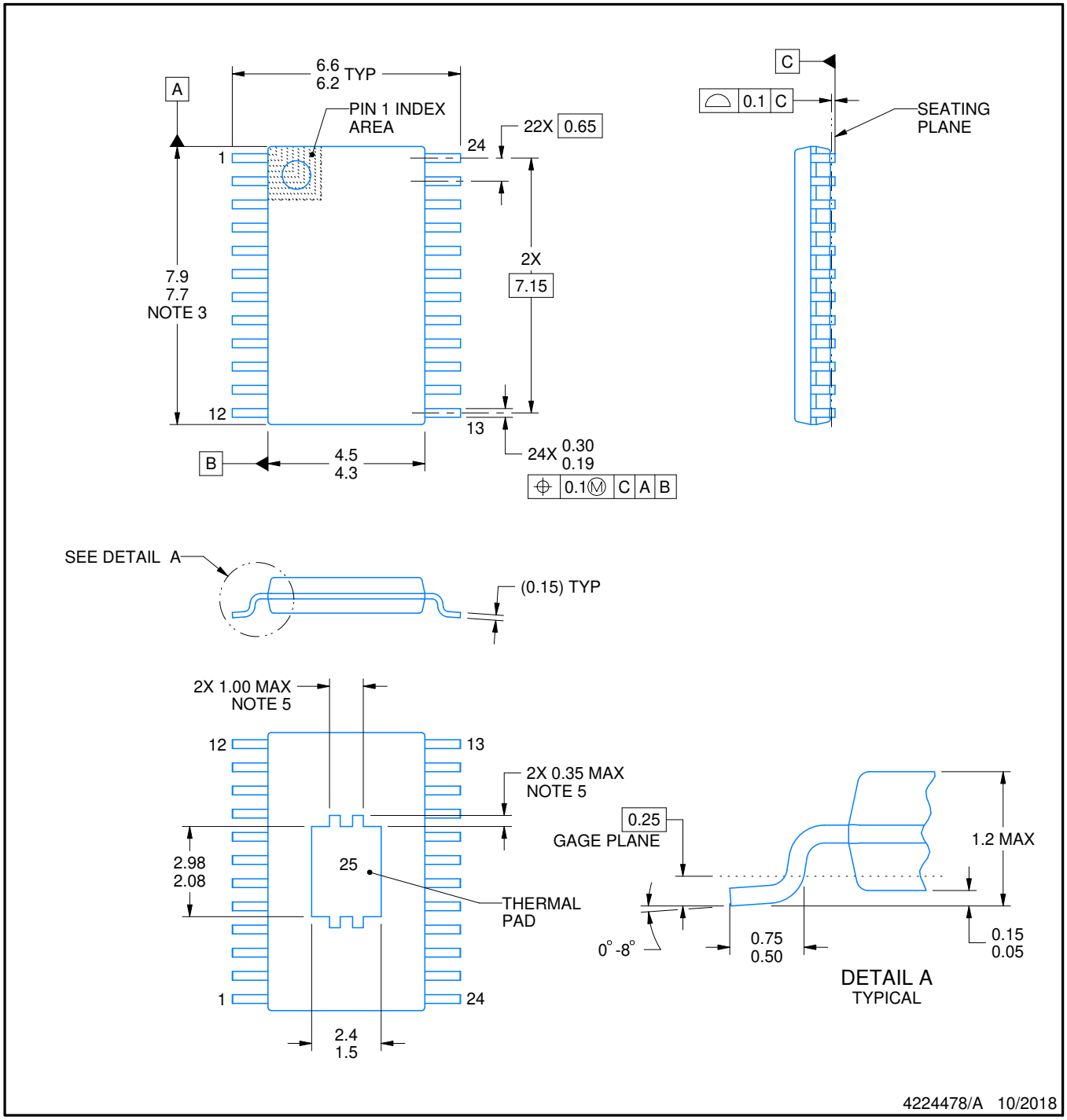
PACKAGE OUTLINE

PWP0024P



PowerPAD™ TSSOP - 1.2 mm max height

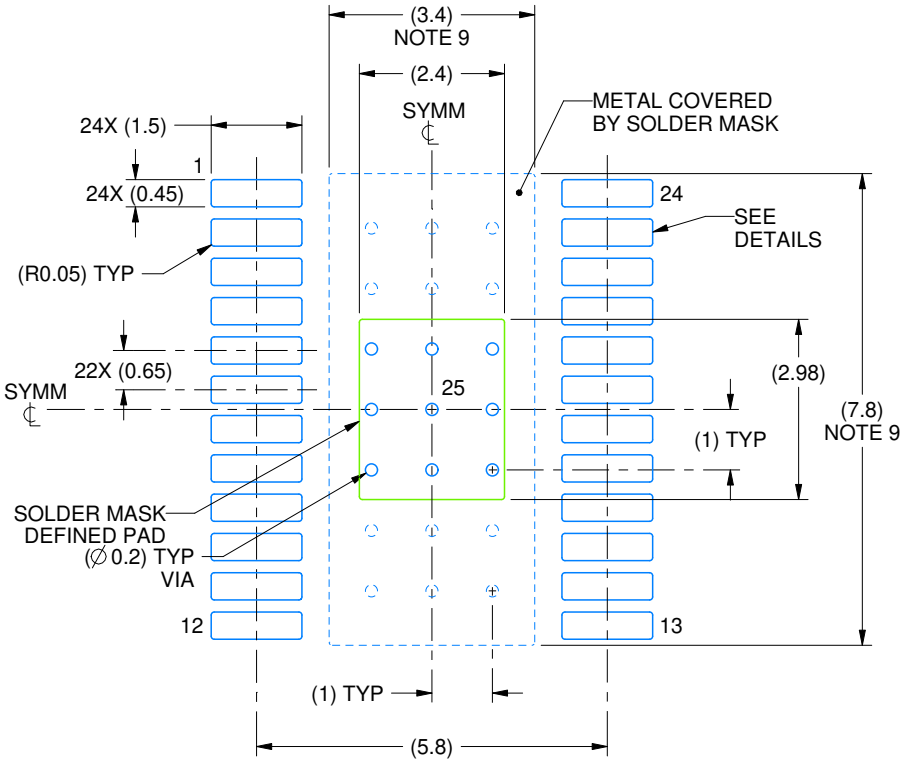
SMALL OUTLINE PACKAGE



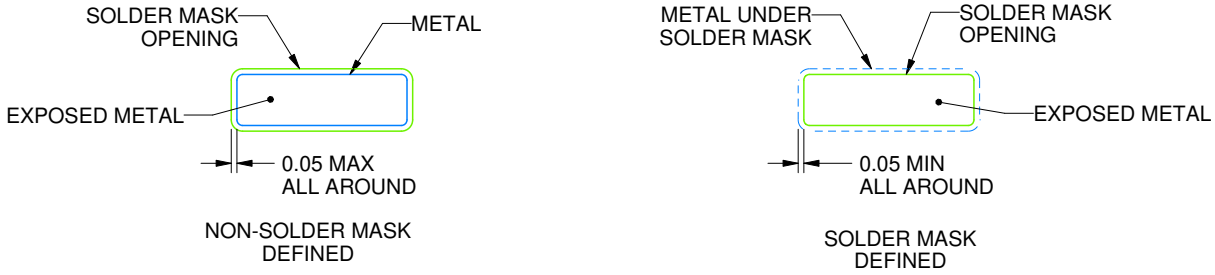
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X

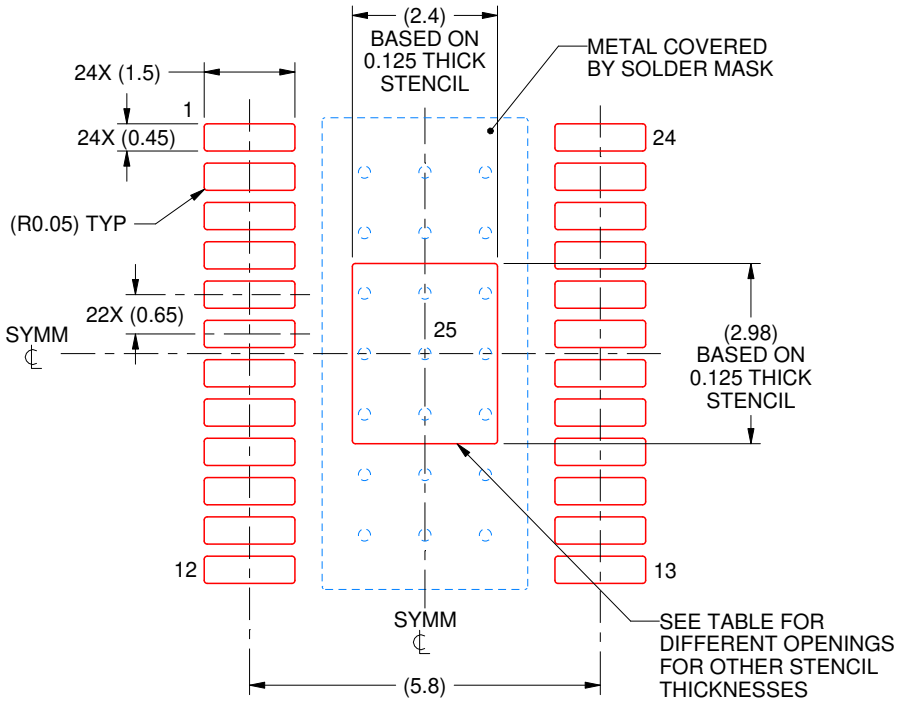


SOLDER MASK DETAILS

4224478/A 10/2018

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.68 X 3.33
0.125	2.40 X 2.98 (SHOWN)
0.15	2.19 X 2.72
0.175	2.03 X 2.52

4224478/A 10/2018

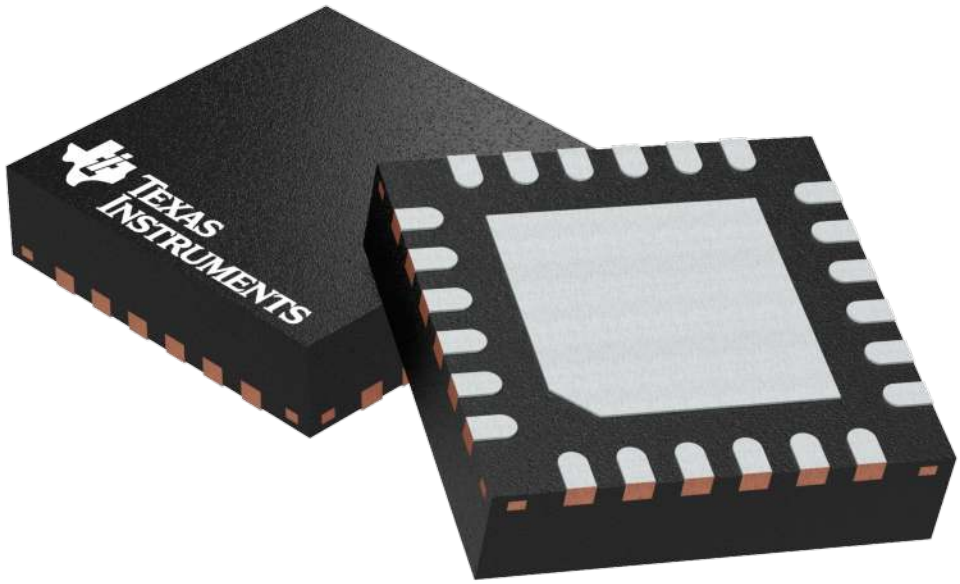
NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



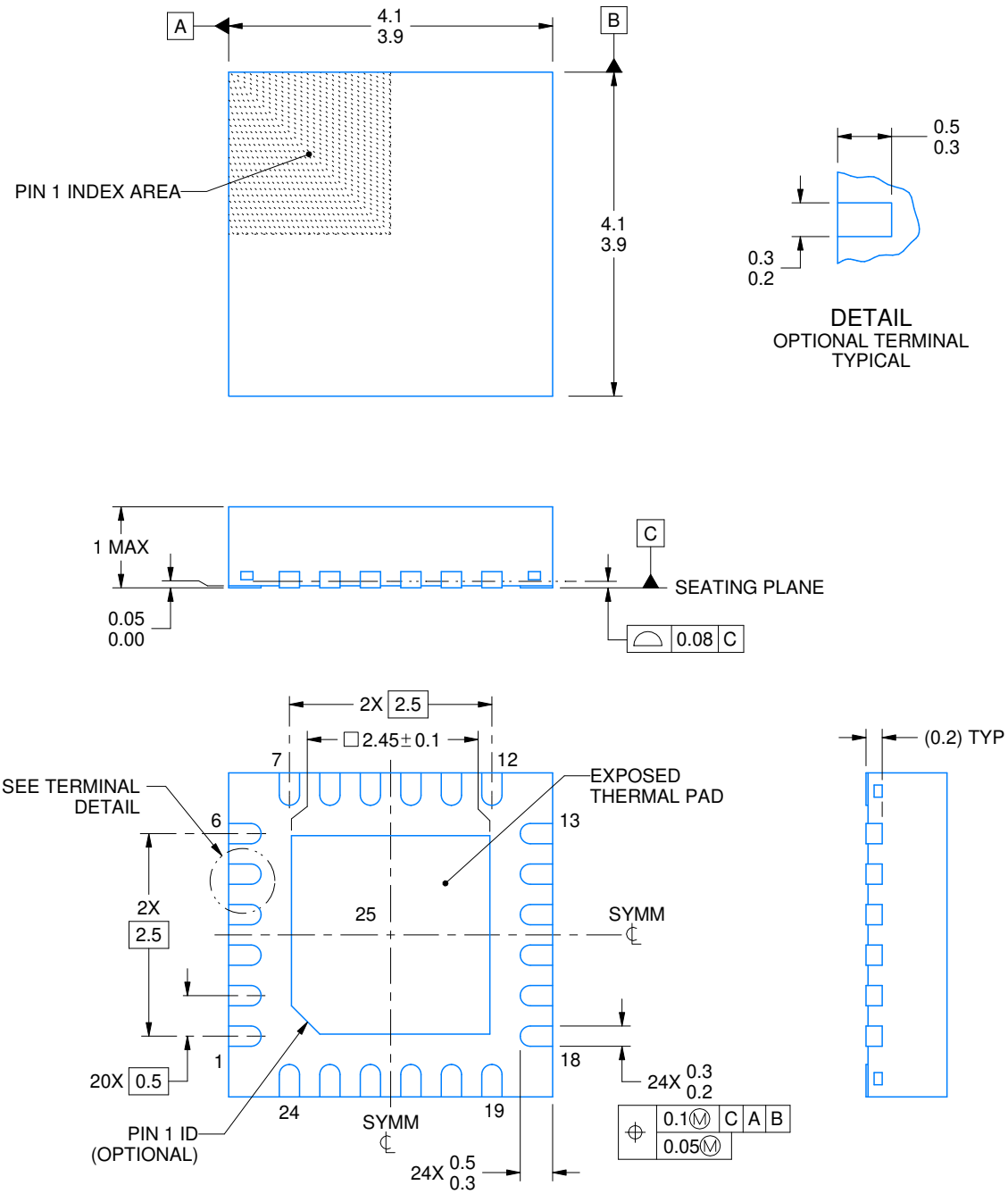
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

RGE0024B

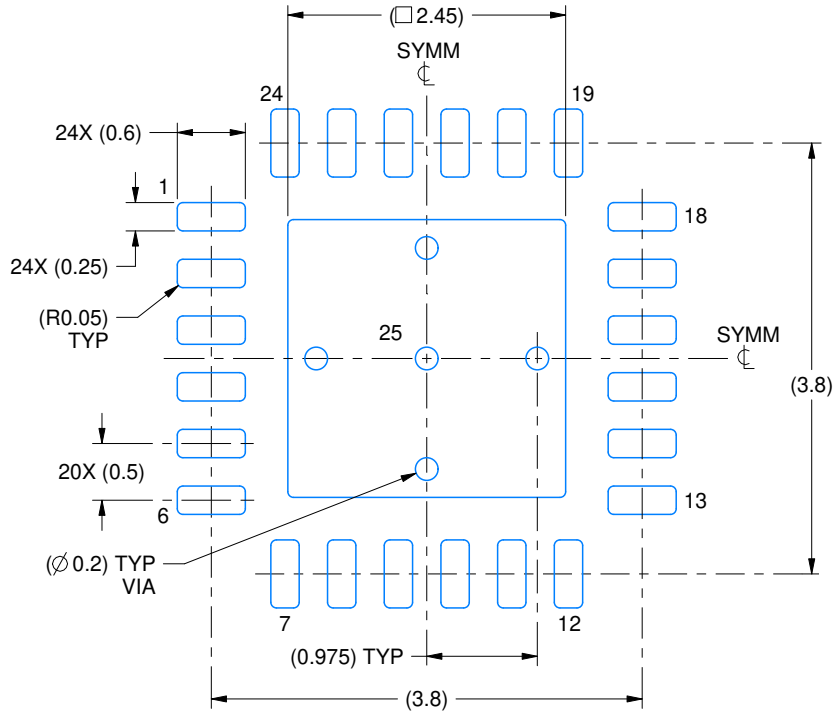
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

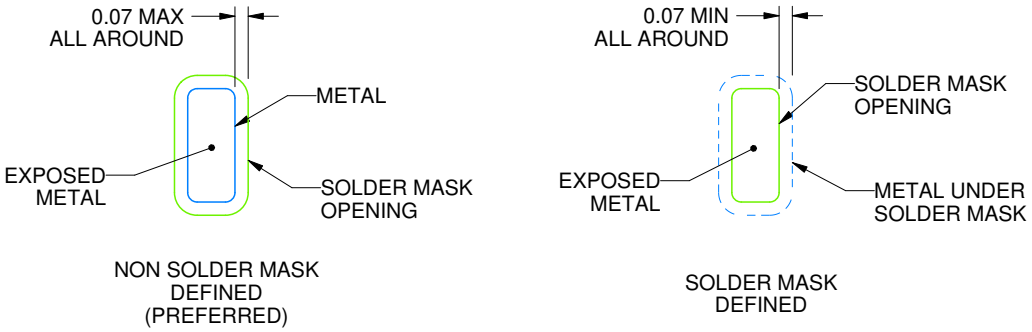


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4219013/A 05/2017

NOTES: (continued)

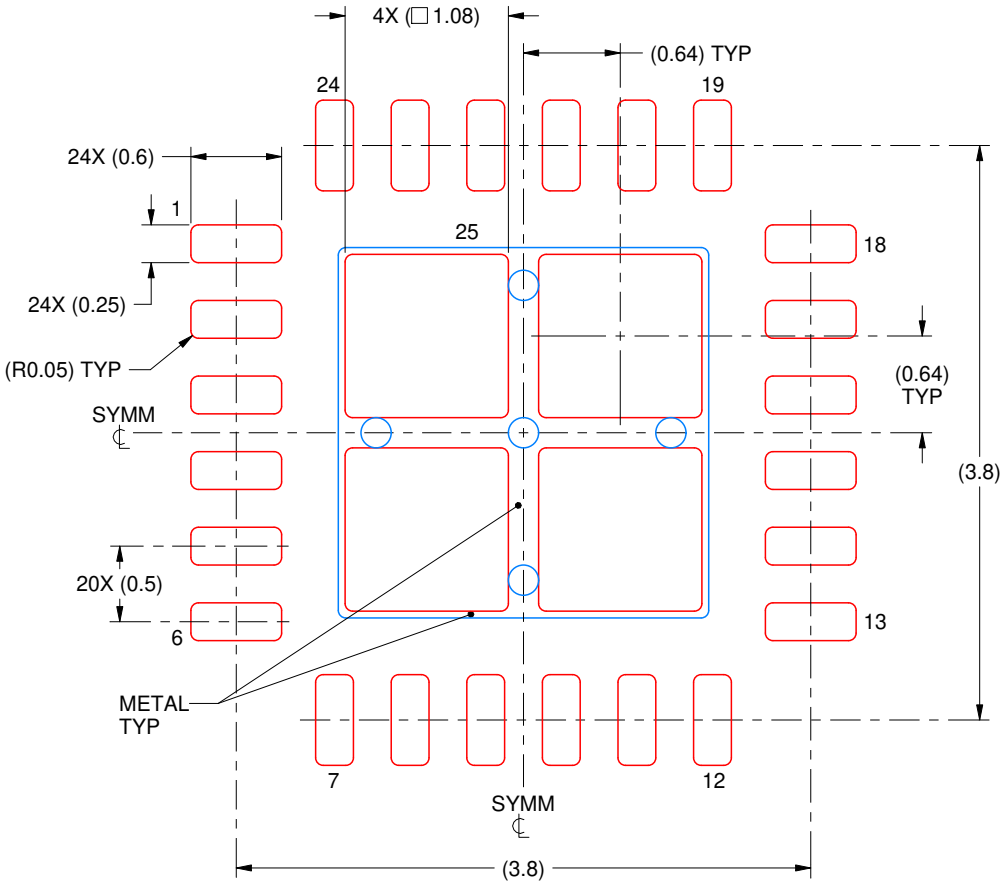
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGE0024B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219013/A 05/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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