# MC33664

## Isolated network high-speed transceiver

Rev. 1.0 — 23 May 2018 Short data sheet: technical data

## 1 General description

The MC33664 is a SMARTMOS transceiver physical layer transformer driver designed to interface a microcontroller conveniently to a high speed isolated communication network. MCU serial peripheral interface (SPI) data bits are directly converted to pulse bit information and transferred to the bus network.

Slave response messages use the same structure to send pulse bit information to the MC33664, which is converted and sent back to the MCU as a SPI bit stream.

## 2 Features and benefits

- 2.0 Mbit/s isolated network communication rate
- Dual SPI architecture for message confirmation
- Robust conducted and radiated immunity with wake-up
- 3.3 V and 5.0 V compatible logic thresholds
- Low sleep mode current with automatic bus wake-up
- Ultra-low radiated emissions

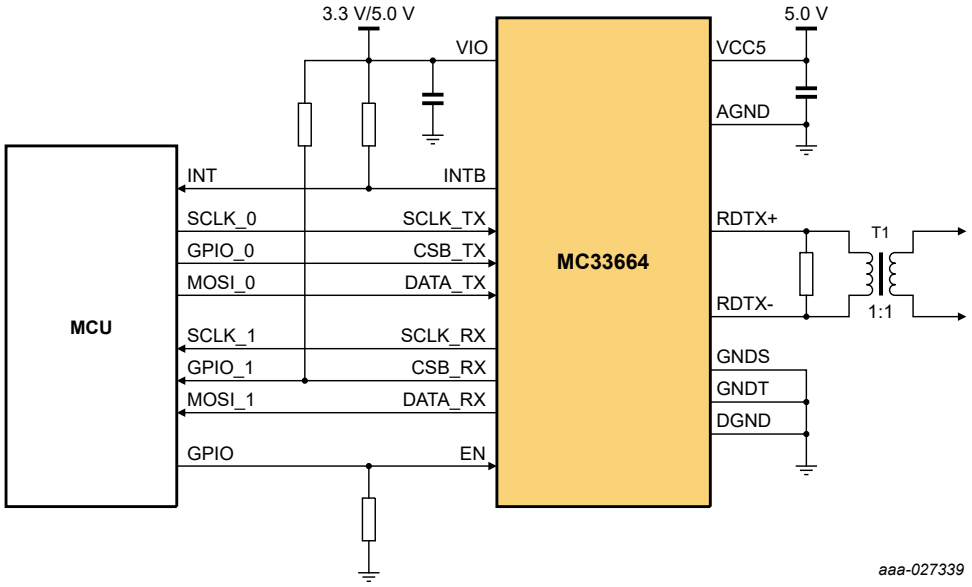



**Figure 1. Typical application circuit**

## 3 Applications

- Automotive communication network
- Industrial communication network
- Utility vehicle battery systems
- Forklift/mining battery systems
- Battery backup systems

## 4 Ordering information

**Table 1. Ordering information**

| Type number | Package | | | |
|---|---|---|---|---|
| | Name | Description | $T_{amb}$ [°C] | Version |
| MC33664ATL1EG[1] | SO16 | plastic small outline package; 16 leads; 1.27 mm pitch; body 9.9 mm × 3.9 mm × 1.75 mm | −40 to +125 | SOT109-5 |

[1] To order parts in tape and reel, add R2 suffix to the part number.

# 5 Pinning information

## 5.1 Pinning

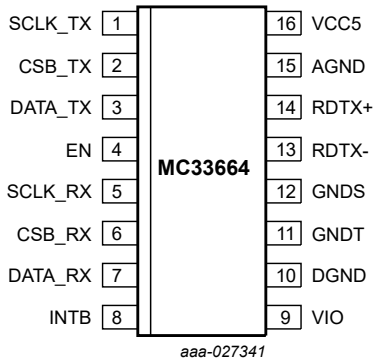



**Figure 2. Pin configuration for SO16**

## 5.2 Pin description

**Table 2. Pin description**

| Symbol | Pin | Type | Description |
|---|---|---|---|
| SCLK_TX | 1 | input | SPI transmit clock from the microcontroller to the MC33664 |
| CSB_TX | 2 | input | SPI transmit chip select from the microcontroller to the MC33664 |
| DATA_TX | 3 | input | SPI transmit data from the microcontroller to the MC33664 |
| EN | 4 | input | enable control pin for the MCU to control the MC33664 to Sleep mode or Normal mode |
| SCLK_RX | 5 | output | message receive SPI clock output to the microcontroller |
| CSB_RX | 6 | output | message receive SPI chip select output to the microcontroller |
| DATA_RX | 7 | output | message receive SPI data output to the microcontroller |
| INTB | 8 | output | digital interrupt pin used to trigger MCU wake-ups |
| VIO | 9 | power | digital 3.3 V/5.0 V power to the IC |
| DGND | 10 | ground | digital ground |
| GNDT | 11 | ground | terminate to ground |
| GNDS | 12 | ground | substrate ground; terminate to ground |
| RDTX- | 13 | I/O | transformer communication bi-directional bus |
| RDTX+ | 14 | I/O | transformer communication bi-directional bus |
| AGND | 15 | ground | analog ground |
| VCC5 | 16 | input | 5.0 V input supply |

# 6 Ratings and operating requirements relationship

The operating voltage range pertains to the VCC5 and VIO pins referenced to the AGND and DGND pins.

**Table 3. Ratings versus operating requirements**

| Fatal range | Lower limited operating range | Normal operating range | Upper limited operating range | Fatal range |
|---|---|---|---|---|
| $V_{PWR}$ < −0.3 V<br>**Permanent failure may occur** | 4.5 V ≤ $V_{CC5}$ ≤ 4.75 V<br>**no permanent failure, but IC functionality is not guaranteed** | 4.75 V ≤ $V_{CC5}$ ≤ 5.5 V<br>3.1 V ≤ $V_{IO}$ ≤ 5.5 V<br>**100 % functional** | 5.5 V ≤ $V_{CC5}$ ≤ 7.0 V<br>5.5 V ≤ $V_{IO}$ ≤ 7.0 V | 7.0 V ≤ $V_{CC5}$<br>7.0 V ≤ $V_{IO}$<br>**permanent failure may occur** |
| | 0 V ≤ $V_{CC5}$ ≤ 4.5 V<br>0 V ≤ $V_{IO}$ ≤ 3.1 V<br>**reset** | | | |
| | **handling range; no permanent failure** | | | |

# 7 Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

*All voltages are respect to reference ground (AGND and DGND) unless otherwise noted. Exceeding these ratings may cause malfunction or permanent damage to the device.*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{IO}$ | supply input voltage | | −0.3 | +7.0 | V |
| $V_{CC5}$ | supply input voltage | | −0.3 | +7.0 | V |
| EN | digital enable pin for Sleep or Normal mode | | −0.3 | $V_{IO}$ + 0.3 | V |
| RDTX+, RDTX− | communication bus | | −10 | +10 | V |
| INTB | interrupt pin | | −0.3 | $V_{IO}$ + 0.3 | V |
| SCLK_TX, SCLK_RX, CSB_TX, CSB_RX, DATA_TX, DATA_RX | serial peripheral interface communication ports | | −0.3 | $V_{IO}$ + 0.3 | V |
| $V_{ESD}$ | electrostatic discharge voltage | human body model (HBM) [1] | ±2000 | - | V |
| | | charge device model (CDM) | ±500 | - | V |
| | | CDM corner pins | ±750 | - | V |
| | | machine model (MM) | ±200 | - | V |
| | | RDTX+, RDTX−; HBM | ±4000 | - | V |
| | | RDTX+, RDTX−; MM | ±200 | - | V |

[1] Electrostatic discharge (ESD) testing is performed in accordance with the HBM ($C_{ZAP}$ = 100 pF, $R_{ZAP}$ = 1500 Ω).

# 8 Thermal characteristics

**Table 5. Thermal characteristics**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $T_{amb}$ | ambient temperature | | −40 | +125 | °C |
| $T_j$ | junction temperature | [1] | −40 | +150 | °C |
| $T_{stg}$ | storage temperature | | −55 | +150 | °C |
| $T_{reflow(peak)}$ | peak reflow temperature | [2] [3] | - | 260 | °C |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | single layer (1s) [4] | - | 125 | °C/W |
| $R_{th(j-pcb)}$ | thermal resistance from junction to printed-circuit board | multi layer (2s2p) [5] | - | 62 | °C/W |

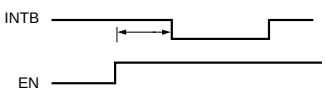
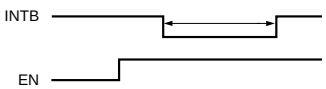
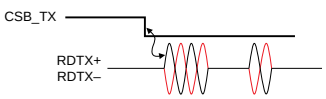
[1] Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
[2] Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
[3] Package reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For peak package reflow temperature and moisture sensitivity levels (MSL), go to http://www.nxp.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts (i.e. MC33xxxD enter 33xxx)], and review parametric.
[4] Per SEMI G38-87 and JEDEC standard JESD51-2 with the single-layer board horizontal.
[5] Indicates the maximum thermal resistance between the die and the exposed pad surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.

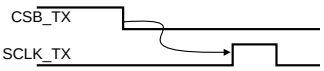
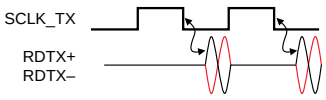
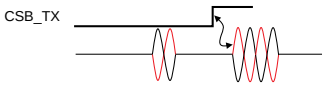
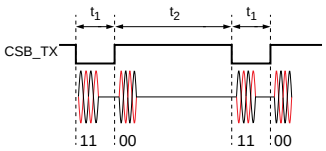
# 9 Characteristics

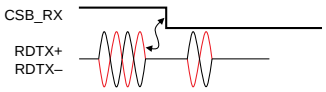
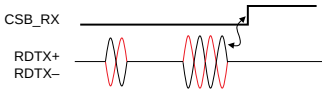
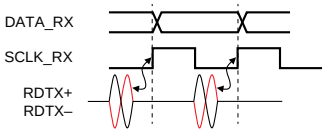
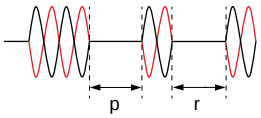
**Table 6. Characteristics**

*Characteristic noted under conditions 4.75 V ≤ $V_{CC5}$ ≤ 5.5 V, 3.1 V ≤ $V_{IO}$ ≤ 5.5 V, −40 °C ≤ $T_{amb}$ ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at $V_{CC5}$ = 5.0 V, $V_{IO}$ = 3.3 V/5.0 V, $T_{amb}$ = 25 °C and device operating under nominal conditions unless otherwise noted.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Power supply VCC5 | | | | | | |
| $V_{CC5}$ | supply voltage | fully operational | 4.75 | — | 5.5 | V |
| | | limited operation | 4.5 | — | 4.75 | V |
| $I_{VCC5(NORMAL)}$ | supply current | Normal mode; EN = 1; continuous transmit; 50 Ω load | | 40 | | mA |
| | | Normal mode; EN = 1; continuous receive | | 3.0 | | mA |
| $I_{VCC5(SLEEP)}$ | supply current | Sleep mode; EN = 0; INTB = 5.0 V | | 30 | | µA |
| $VCC5_{UV}$ | VCC5 undervoltage POR threshold | | 4.0 | — | 4.5 | V |
| $VCC5_{UV\_FLT}$ | VCC5 undervoltage POR filter | | | 2.5 | | µs |
| $VCC5_{UVHYS}$ | VCC5 undervoltage POR hysteresis | | | 100 | | mV |
| Power supply VIO | | | | | | |
| $V_{IO}$ | supply voltage | | 3.1 | — | 5.5 | V |
| $VIO_{UV}$ | VIO undervoltage POR threshold | | 2.2 | — | 3.1 | V |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $VIO_{UV\_FLT}$ | VIO undervoltage POR filter | | | 2.5 | | µs |
| $VIO_{UVHYS}$ | VIO undervoltage POR hysteresis | | | 100 | | mV |
| $I_{VIO(SLEEP)}$ | VIO sleep current | EN = 0; INTB = 1 | 0.1 | — | 4.5 | µA |
| $I_{VIO(NORMAL)}$ | VIO Normal mode current | EN = 1; continuous communication; SPI_1 open | | 1.0 | | mA |
| Logic transmit EN, CSB_TX, SCLK_TX, DATA_TX | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | | 1.7 | — | $V_{IO}$ + 0.3 | V |
| $V_{IL}$ | LOW-level input voltage | | — | — | 0.95 | V |
| $V_{hys}$ | hysteresis voltage | | | 150 | | mV |
| $R_{pd}$ | pull-down resistance | EN, SCLK_TX, DATA_TX | | 100 | | kΩ |
| $R_{pu}$ | pull-up resistance | CSB_TX | | 100 | | kΩ |
| $t_{READY}$ | Sleep mode to Normal mode | EN LOW to HIGH transition to device ready to transmit | — | — | 100 | µs |
| $t_{INTB\_PULSE\_DELAY}$ | EN LOW to HIGH transition to INTB verification pulse   | | — | — | 100 | µs |
| $t_{INTB\_PULSE}$ | INTB verification pulse duration   | | — | 100 | — | µs |
| $f_{SCLK\_TX}$ | SPI_0 frequency | SCLK_TX | | 2.0 | | MHz |
| a | SCLK_TX HIGH | see Figure 3 | | 250 | | ns |
| b | SCLK_TX LOW | see Figure 3 | | 250 | | ns |
| e | SCLK_TX to CSB_TX | see Figure 3 | — | 250 | — | ns |
| L | CSB_TX to start of message   | | — | — | 1.1 | µs |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| f | falling edge of CSB_TX to rising edge SCLK_TX   | see Figure 3 | 1.75 | — | — | µs |
| $t_{RDTX\_DLY}$ | propagation delay   | SCLK_TX LOW to sine out [1] | — | 80 | 150 | ns |
| g | SCLK_TX LOW to CSB_TX HIGH | see Figure 3 | 600 | — | — | ns |
| c | DATA_TX to SCLK_TX setup | see Figure 3 | 40 | — | — | ns |
| d | DATA_TX hold | see Figure 3 | 40 | — | — | ns |
| $t_{CSB\_TX\_HIGH\_EOM}$ | propagation delay   | CSB_TX LOW to HIGH to end of message [1] | — | — | 150 | ns |
| $t_1$ | CSB_TX wake#up pulse sequence timing   | CSB_TX LOW period | | 21 | | µs |
| $t_2$ | | CSB_TX HIGH period | | 600 | | µs |
| h | time between consecutive transmit messages | see Figure 3 | 1.0 | 3.0 | — | µs |
| Logic receive pins (CSB_RX, SCLK_RX, DATA_RX) | | | | | | |
| $V_{OH}$ | HIGH-level output voltage | $I_{OH}$ = −2.0 mA; $V_{IO}$ = 3.1 V | $V_{IO}$ − 0.4 | — | — | V |
| $V_{OL}$ | LOW-level output voltage | $I_{OL}$ = −2.0 mA; $V_{IO}$ = 3.1 V | — | — | 0.4 | V |
| $f_{SPI}$ | SPI_1 frequency | SCLK_RX | | 2.0 | | MHz |
| q | pulse frequency | see Figure 4 | | 4.0 | | MHz |
| o | start of message | see Figure 4 [1] | | 500 | | ns |
| a | SCLK_RX HIGH | [1] | | 250 | | ns |
| b | SCLK_RX LOW | [1] | | 250 | | ns |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{SOM\_CSB\_RX}$ | start of message to CSB_RX   | [1] | | 160 | | ns |
| $t_{EOM\_CSB\_RX}$ | end of message to CSB_RX   | [1] | | 60 | | ns |
| $t_{PDB\_SCLK\_DATA\_RX}$ | pulse data bit to DATA_RX and SCLK_RX   | [1] | | 280 | | ns |
| r | start of message to MSB (receive)   | see Figure 4 [1] | — | 250 | — | ns |
| p | | see Figure 4 [1] | — | 600 | — | ns |
| m | time between consecutive messages received | see Figure 4 | 1.0 | 3.0 | — | µs |
| Bus differential transmitter/receiver | | | | | | |
| $V_{RDTX(PK\_DIFF)}$ | RDTX± differential output voltage | $R_L$ = 50 Ω; $V_{CC5}$ = 4.75 V | | 2.5 | | V |
| $I_{RDTX}$ | RDTX± current limit | sinking/sourcing to 2.5 V | 65 | — | 300 | mA |
| $V_{RDTX\_IN(TH)}$ | RDTX± differential receiver threshold voltage | rising edge | | 0.74 | | V |
| | | falling edge | | 0.61 | 0.70 | V |
| $V_{RDTX\_IN\_HYST}$ | RDTX± differential receiver threshold voltage hysteresis | | | 130 | | mV |
| $V_{RDTX\_BIAS}$ | transformer bias voltage | transmitter in 3-state | | 2.5 | | V |
| $f_{RDTX}$ | transmit/receive pulse frequency | | | 4.0 | | MHz |
| Wake-up receiver | | | | | | |
| $V_{RDTXWU\_TH}$ | RDTX± wake#up differential receiver threshold voltage | rising edge | | 0.6 | | V |
| | | falling edge | | 0.6 | | V |
| $V_{RDTXWU\_TH\_HYS}$ | RDTX± wake#up differential receiver threshold hysteresis | | | 100 | | mV |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{RDTXWU\_FLT}$ | RDTX± wake#up filter | | | 50 | | ns |

[1] All bus network signals to SPI timing are referenced to 0.8 V differential threshold.

## 9.1 Timing diagrams

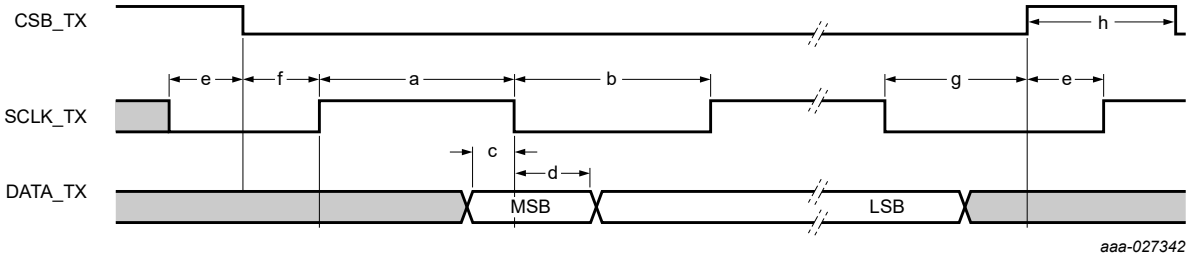



**Figure 3. SPI transmit timing**

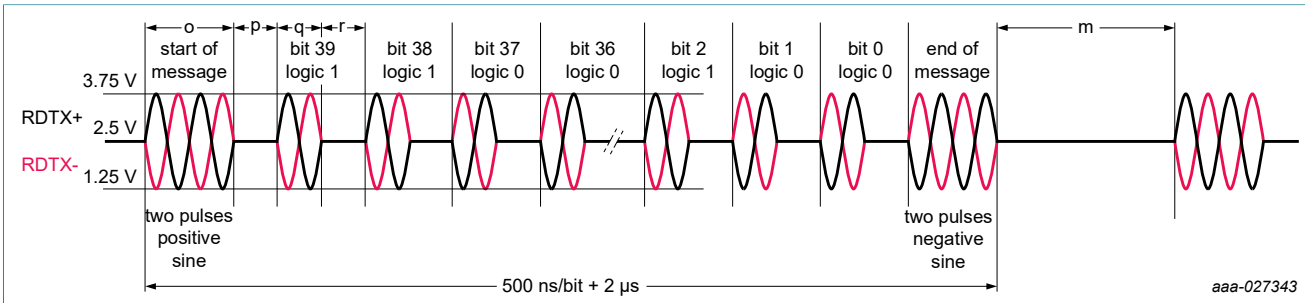



**Figure 4. Transformer receive communication timing**

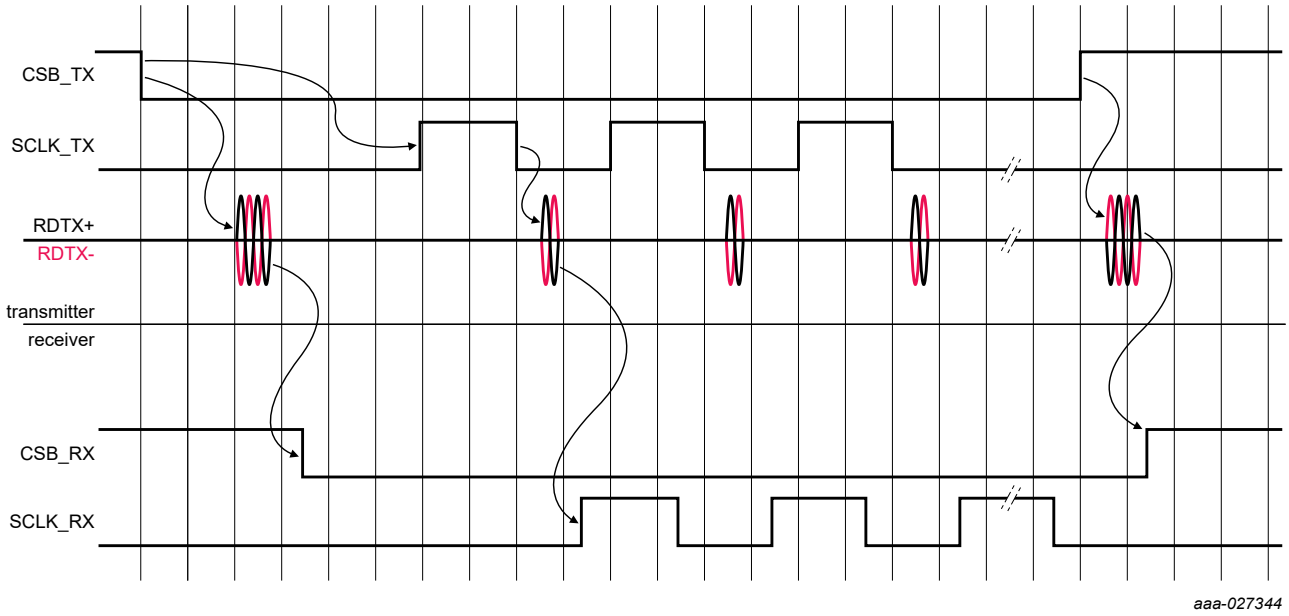



**Figure 5. Transmit/receive signal propagation**

## 10 Package outline

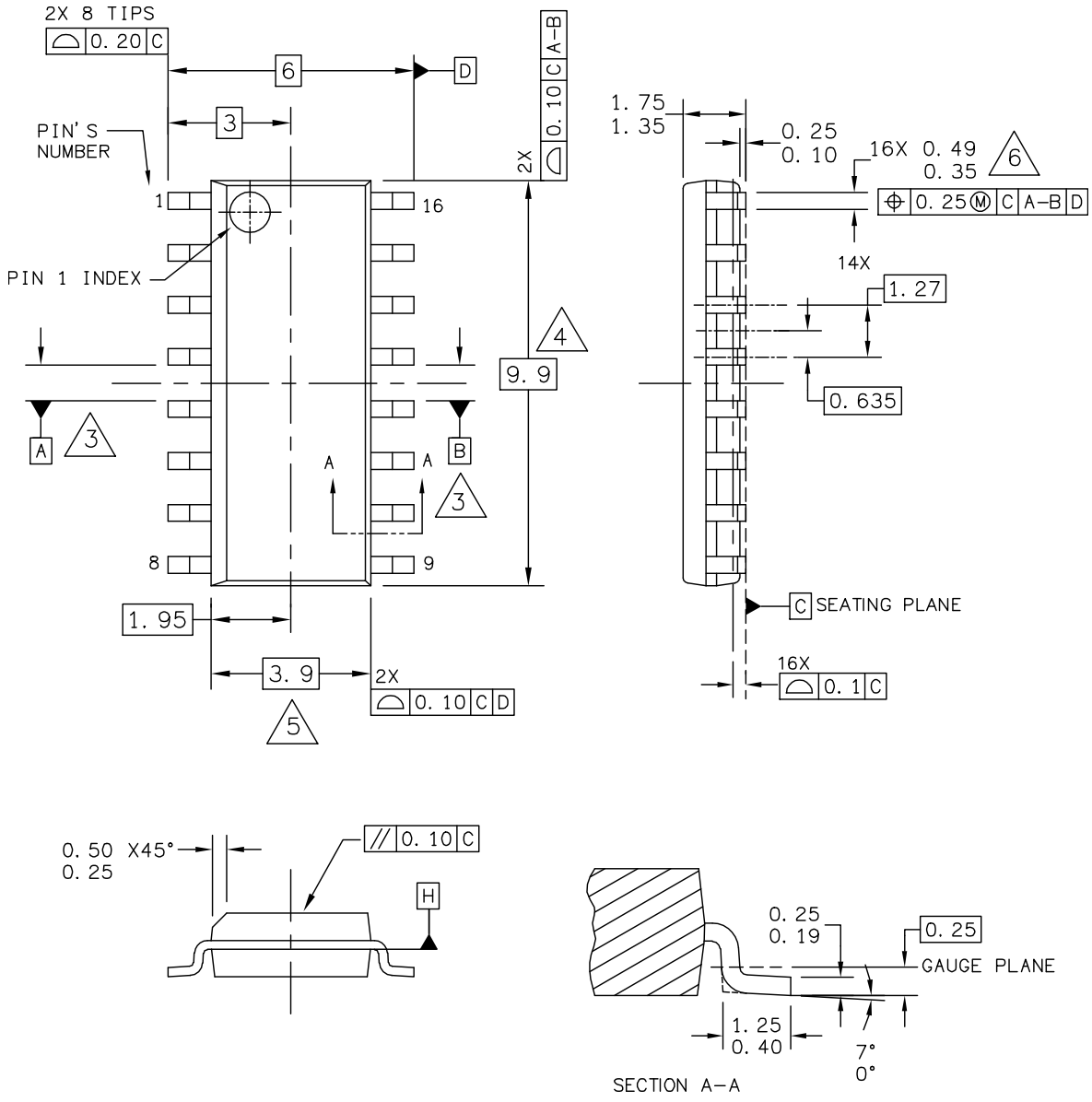



**Figure 6. Package outline SOT109-5 (SO16)**

## 11 Revision history

**Table 7. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| MC33664_SDS v.1.0 | 20180523 | Technical data | — | — |

# 12 Legal information

## 12.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| [short] Data sheet: product preview | Development | This document contains certain information on a product under development. NXP reserves the right to change or discontinue this product without notice. |
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