



PJW7N04-AU

40V N-Channel Enhancement Mode MOSFET

Voltage

40 V

Current

6.5 A

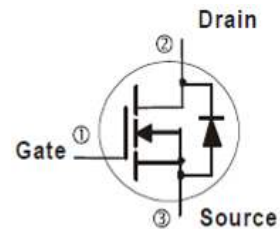
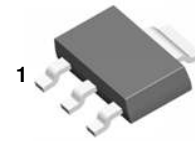
Features

- $R_{DS(ON)}$, $V_{GS}@10V$, $I_D@5A < 42m\Omega$
- $R_{DS(ON)}$, $V_{GS}@4.5V$, $I_D@4A < 51m\Omega$
- Advanced Trench Process Technology
- High density cell design for ultra low on-resistance
- AEC-Q101 qualified
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

Mechanical Data

- Case : SOT-223 Package
- Terminals : Solderable per MIL-STD-750, Method 2026
- Approx. Weight : 0.043 ounces, 0.123 grams

SOT-223



Maximum Ratings and Thermal Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNITS
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (Note 4)	$T_A=25^\circ\text{C}$	I_D	6.5	A
	$T_A=70^\circ\text{C}$		5	
Pulsed Drain Current (Note 1)		I_{DM}	26	
Power Dissipation	$T_A=25^\circ\text{C}$	P_D	3.7	W
	$T_A=70^\circ\text{C}$		2.6	
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55~175	$^\circ\text{C}$
Typical Thermal Resistance		$R_{\theta JA}$	40.3	$^\circ\text{C/W}$
- Junction to Ambient (Note 4,5)				

- Limited only By Maximum Junction Temperature



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Electrical Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	40	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1	1.5	2.5	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=5A$	-	35	42	m Ω
		$V_{GS}=4.5V, I_D=4A$	-	44	51	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=40V, V_{GS}=0V$	-	-	1	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
Dynamic (Note 6)						
Total Gate Charge	Q_g	$V_{DS}=20V, I_D=4.3A,$ $V_{GS}=4.5V$ (Note 1,2)	-	4.8	-	nC
Gate-Source Charge	Q_{gs}		-	1.4	-	
Gate-Drain Charge	Q_{gd}		-	1.8	-	
Input Capacitance	C_{iss}	$V_{DS}=20V, V_{GS}=0V,$ $f=1\text{MHZ}$	-	410	-	pF
Output Capacitance	C_{oss}		-	50	-	
Reverse Transfer Capacitance	C_{rss}		-	30	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD}=20V, I_D=3.5A,$ $V_{GS}=10V,$ $R_G=1\Omega$ (Note 1,2)	-	4	-	ns
Turn-On Rise Time	t_r		-	30	-	
Turn-Off Delay Time	$t_{d(off)}$		-	15	-	
Turn-Off Fall Time	t_f		-	8	-	
Drain-Source Diode						
Maximum Continuous Drain-Source Diode Forward Current	I_S	---	-	-	6.5	A
Diode Forward Voltage	V_{SD}	$I_S=1A, V_{GS}=0V$	-	0.78	1.2	V

NOTES :

1. Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$.
2. Essentially independent of operating temperature typical characteristics.
3. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}=150^\circ\text{C}$. Ratings are based on low frequency and duty cycles to keep initial $T_J=25^\circ\text{C}$.
4. The maximum current rating is package limited.
5. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch² with 2oz.square pad of copper.
6. Guaranteed by design, not subject to production testing.



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TYPICAL CHARACTERISTIC CURVES

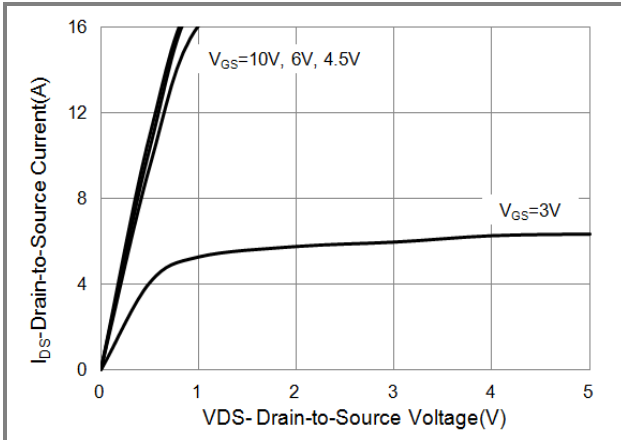


Fig.1 Output Characteristics

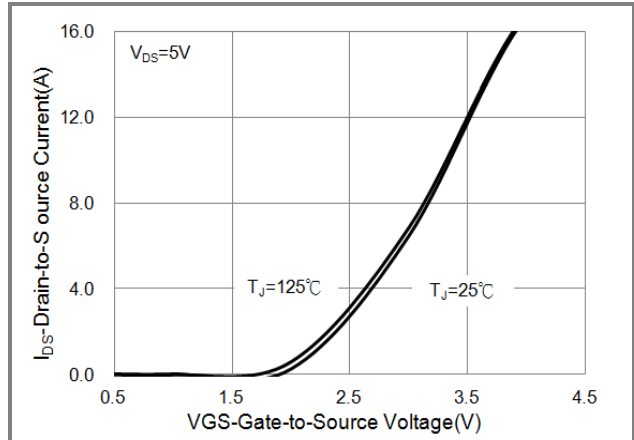


Fig.2 Transfer Characteristics

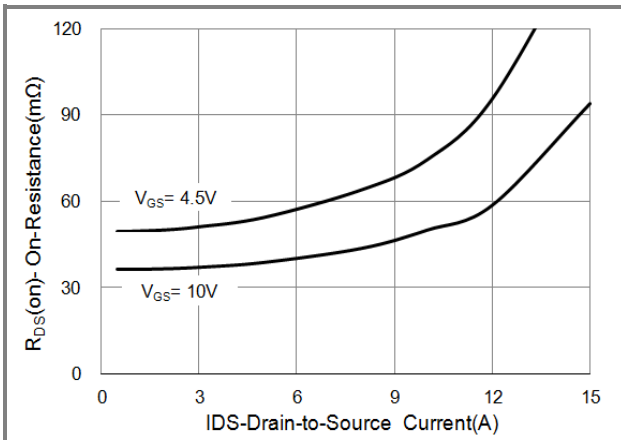


Fig.3 On-Resistance vs. Drain Current

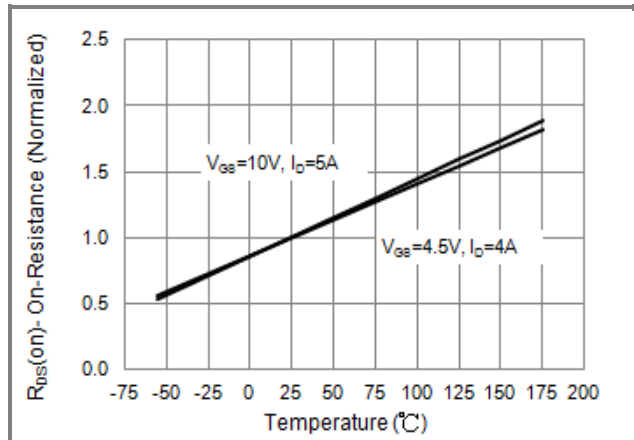


Fig.4 On-Resistance vs. Junction temperature

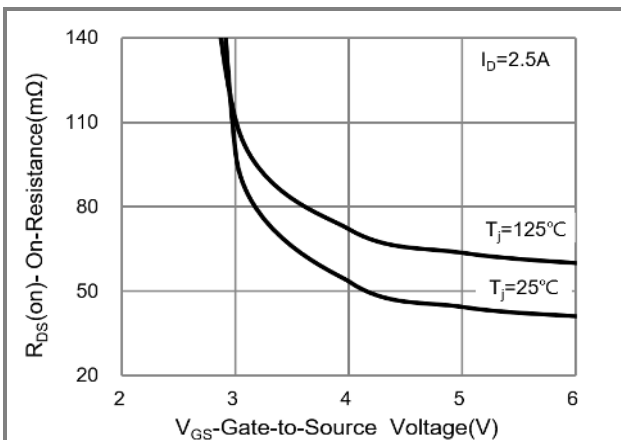


Fig.5 On-Resistance Variation with VGS

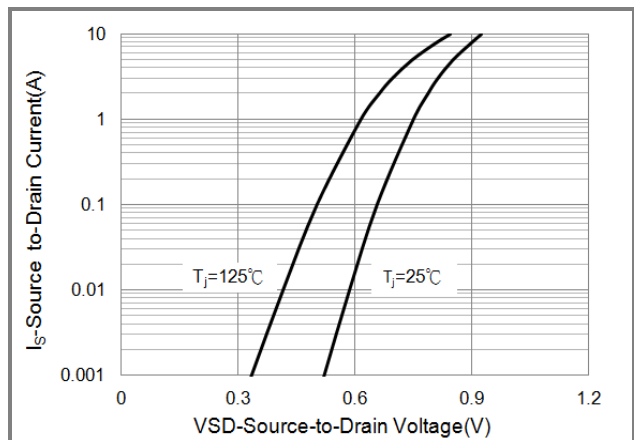


Fig.6 Source-Drain Diode Forward Voltage



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TYPICAL CHARACTERISTIC CURVES

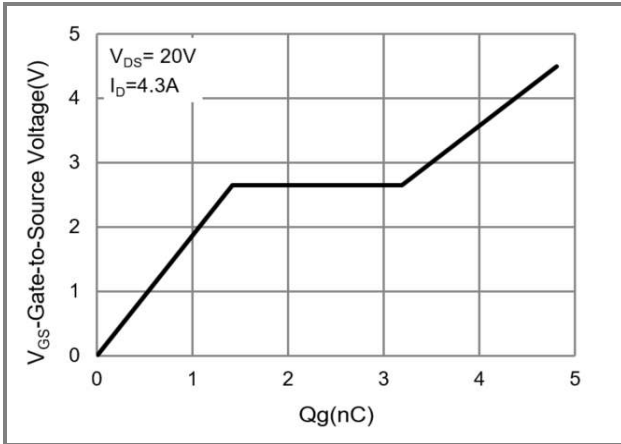


Fig.7 Gate-Charge Characteristics

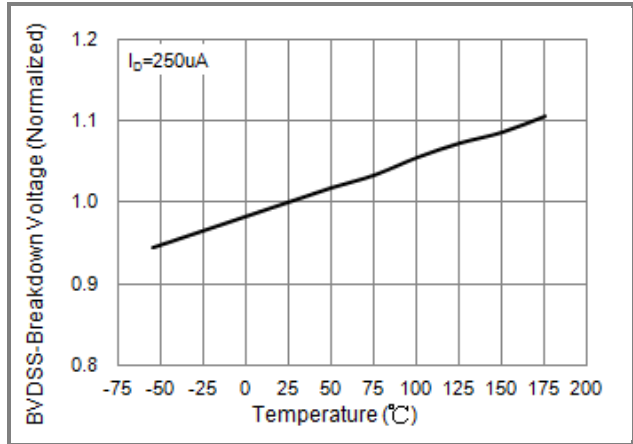


Fig.8 Breakdown Voltage Variation vs. Temperature

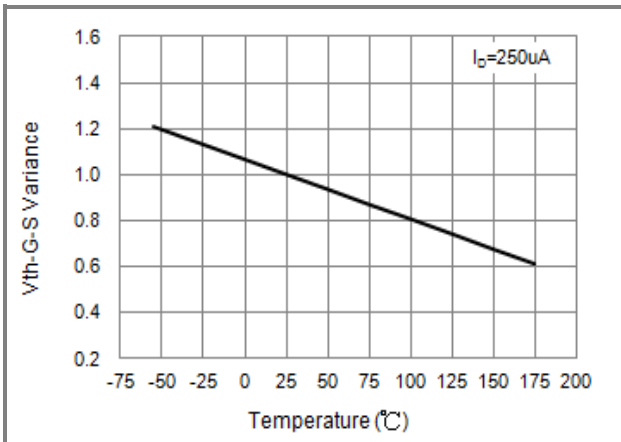


Fig.9 Threshold Voltage Variation with Temperature

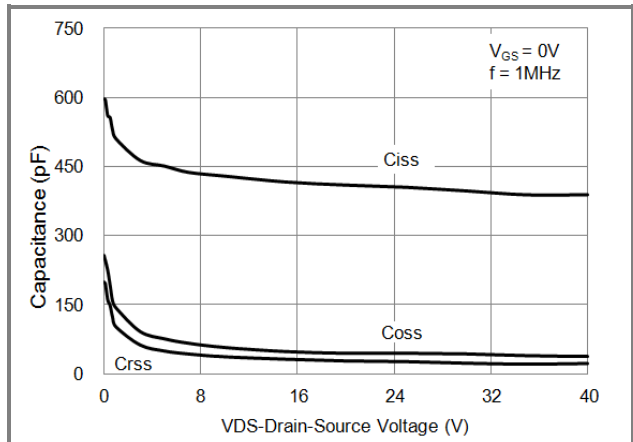


Fig.10 Capacitance vs. Drain-Source Voltage

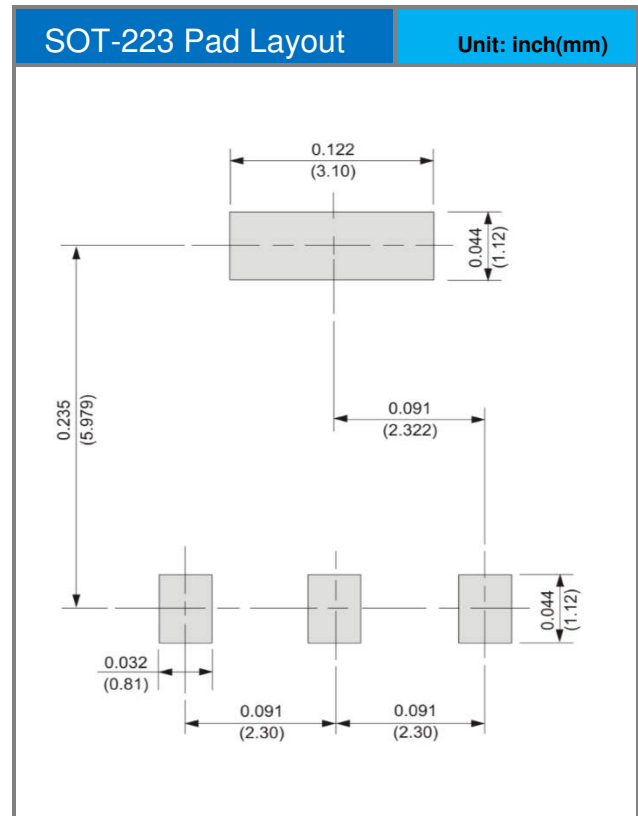
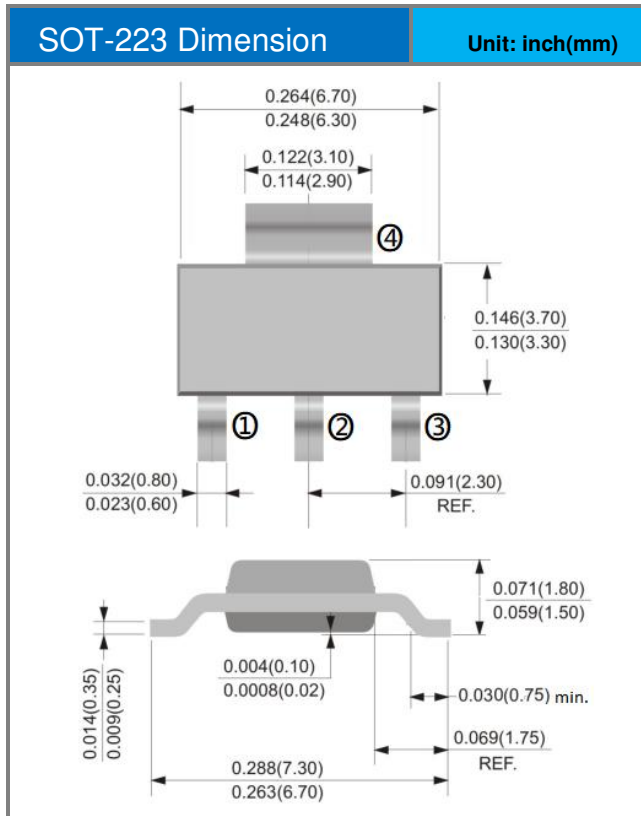


PJW7N04-AU

Part No Packing Code Version

Part No Packing Code	Package Type	Packing Type	Marking	Version
PJW7N04-AU_R2_000A1	SOT-223	2,500pcs / 13" reel	W7N04	Halogen free

Packaging Information & Mounting Pad Layout





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