CY7C1370S
CY7C1372S

18-Mbit (512K × 36/1M × 18) Pipelined SRAM with NoBL™ Architecture

Features

- Pin-compatible and functionally equivalent to ZBT™
- Supports 200-MHz bus operations with zero wait states
  - Available speed grades are 200, and 167 MHz
- Internally self-timed output buffer control to eliminate the need to use asynchronous $\overline{OE}$
- Fully registered (inputs and outputs) for pipelined operation
- Byte write capability
- 3.3 V core power supply (V_{DD})
- 3.3 V/2.5 V I/O power supply (V_{DDQ})
- Fast clock-to-output times
  - 3.0 ns (for 200-MHz device)
- Clock enable ($\overline{CEN}$) pin to suspend operation
- Synchronous self-timed writes
- Available in JEDEC-standard Pb-free 100-pin TQFP
- Burst capability – linear or interleaved burst order
- "ZZ" sleep mode option and stop clock option

Functional Description

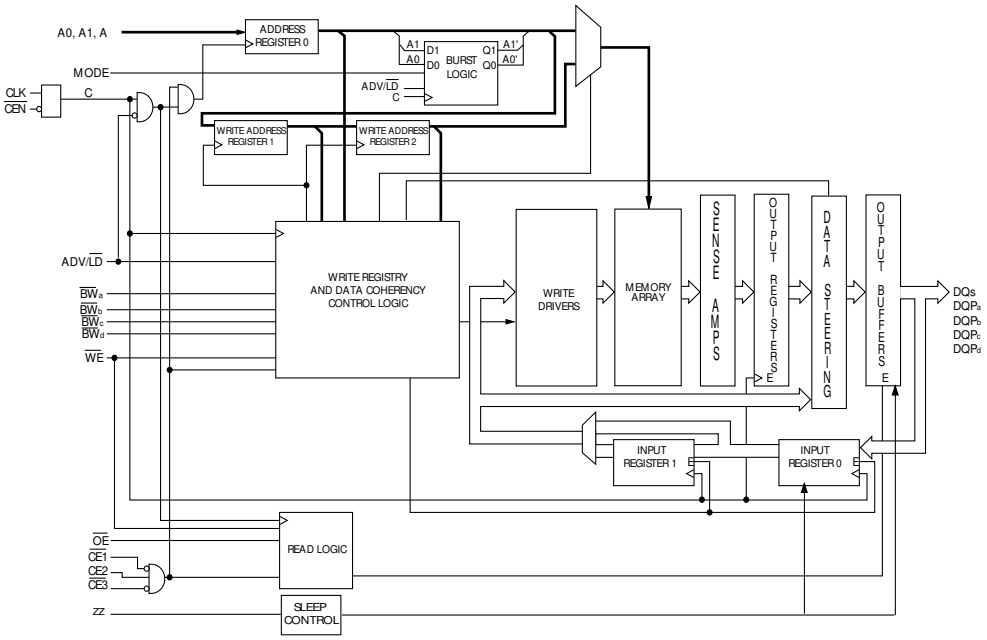
The CY7C1370S and CY7C1372S are 3.3 V, 512K × 36 and 1M × 18 synchronous pipelined burst SRAMs with No Bus Latency™ (NoBL™) logic, respectively. They are designed to support unlimited true back-to-back read/write operations with no wait states. The CY7C1370S and CY7C1372S are equipped with the advanced (NoBL) logic required to enable consecutive read/write operations with data being transferred on every clock cycle. This feature dramatically improves the throughput of data in systems that require frequent write/read transitions. The CY7C1370S and CY7C1372S are pin compatible and functionally equivalent to ZBT devices.

All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through output registers controlled by the rising edge of the clock. The clock input is qualified by the clock enable ($\overline{CEN}$) signal, which when deasserted suspends operation and extends the previous clock cycle.

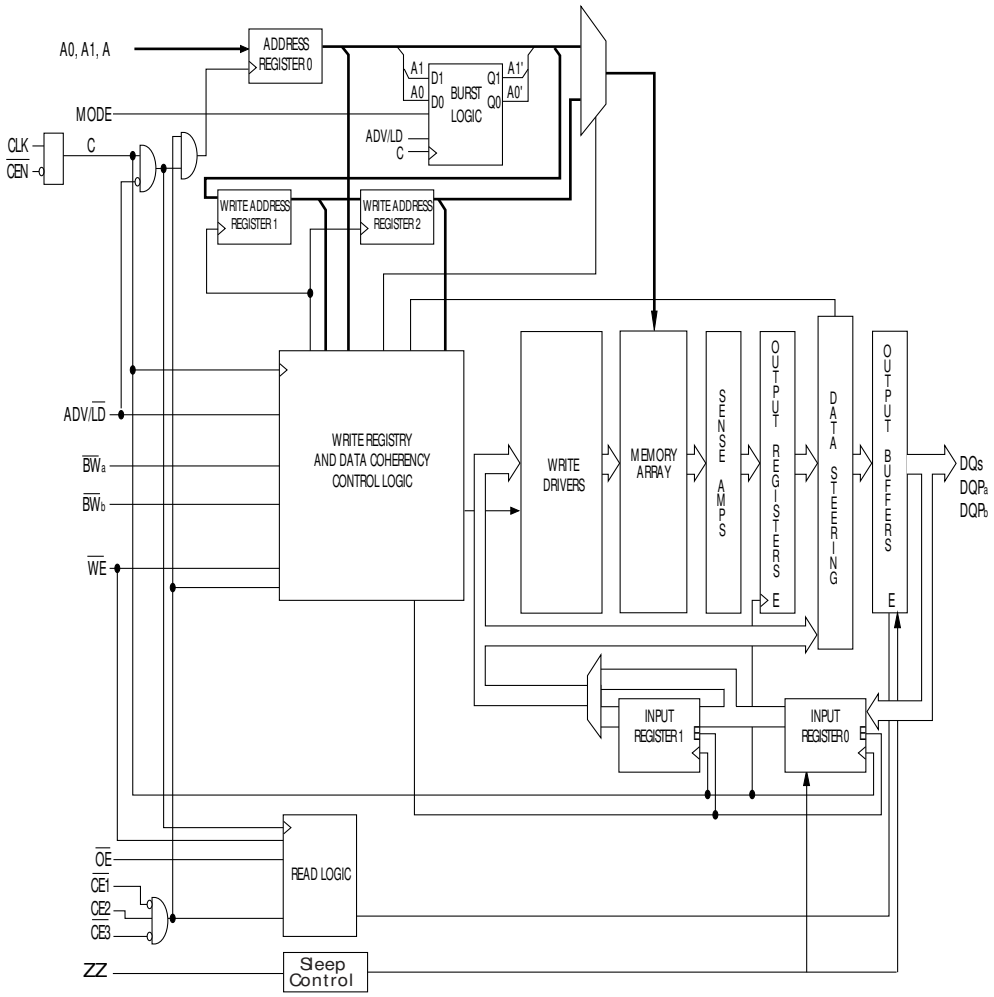
Write operations are controlled by the byte write selects ($\overline{BW_a}$–$\overline{BW_d}$ for CY7C1370S and $\overline{BW_a}$–$\overline{BW_b}$ for CY7C1372S) and a write enable ($\overline{WE}$) input. All writes are conducted with on-chip synchronous self-timed write circuitry.

Three synchronous chip enables ($\overline{CE_1}$, CE_2, $\overline{CE_3}$) and an asynchronous output enable ($\overline{OE}$) provide for easy bank selection and output tri-state control. In order to avoid bus contention, the output drivers are synchronously tri-stated during the data portion of a write sequence.

Logic Block Diagram – CY7C1370S



Logic Block Diagram – CY7C1372S



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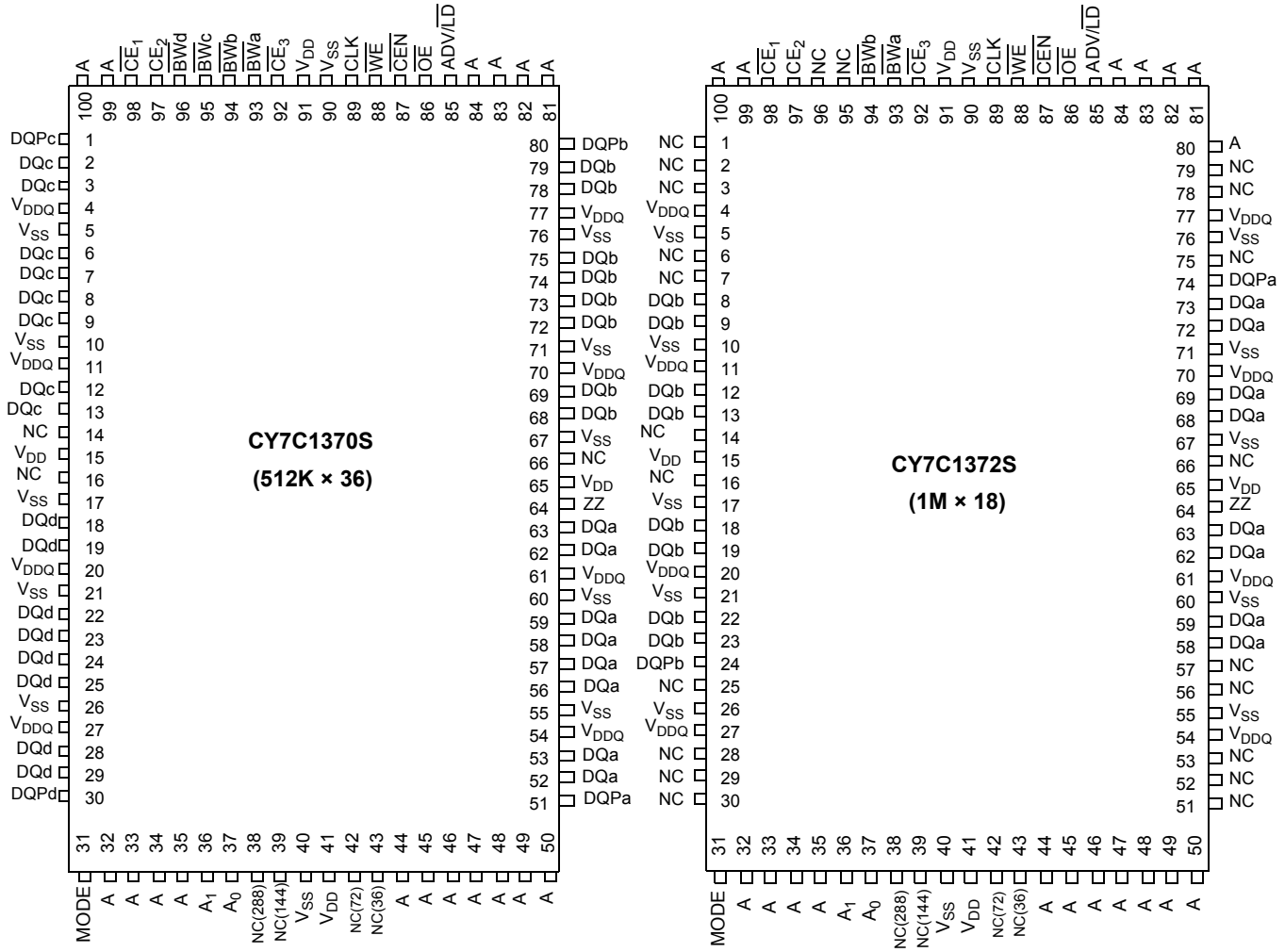
Selection Guide

Description	200 MHz	167 MHz	Unit
Maximum access time	3.0	3.4	ns
Maximum operating current	300	275	mA
Maximum CMOS standby current	70	70	mA

Pin Configurations

Figure 1. 100-pin TQFP (14 × 20 × 1.4 mm) pinout



Pin Definitions

Pin Name	I/O Type	Pin Description
A_0, A_1, A	Input-synchronous	**Address inputs used to select one of the address locations**. Sampled at the rising edge of the CLK.
$\overline{BW}_a$, $\overline{BW}_b$, $\overline{BW}_c$, $\overline{BW}_d$	Input-synchronous	**Byte write select inputs, active LOW**. Qualified with $\overline{WE}$ to conduct writes to the SRAM. Sampled on the rising edge of CLK. $\overline{BW}_a$ controls DQ_a and DQP_a, $\overline{BW}_b$ controls DQ_b and DQP_b, $\overline{BW}_c$ controls DQ_c and DQP_c, $\overline{BW}_d$ controls DQ_d and DQP_d.
$\overline{WE}$	Input-synchronous	**Write enable input, active LOW**. Sampled on the rising edge of CLK if $\overline{CEN}$ is active LOW. This signal must be asserted LOW to initiate a write sequence.
ADV/$\overline{LD}$	Input-synchronous	**Advance/load input used to advance the on-chip address counter or load a new address**. When HIGH (and $\overline{CEN}$ is asserted LOW) the internal burst counter is advanced. When LOW, a new address can be loaded into the device for an access. After being deselected, ADV/$\overline{LD}$ should be driven LOW in order to load a new address.
CLK	Input-clock	**Clock input**. Used to capture all synchronous inputs to the device. CLK is qualified with $\overline{CEN}$. CLK is only recognized if $\overline{CEN}$ is active LOW.
$\overline{CE}_1$	Input-synchronous	**Chip enable 1 input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with CE_2 and $\overline{CE}_3$ to select/deselect the device.
CE_2	Input-synchronous	**Chip enable 2 input, active HIGH**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $\overline{CE}_3$ to select/deselect the device.
$\overline{CE}_3$	Input-synchronous	**Chip enable 3 input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and CE_2 to select/deselect the device.
$\overline{OE}$	Input-asynchronous	**Output enable, active LOW**. Combined with the synchronous logic block inside the device to control the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When deasserted HIGH, I/O pins are tri-stated, and act as input data pins. $\overline{OE}$ is masked during the data portion of a write sequence, during the first clock when emerging from a deselected state and when the device has been deselected.
$\overline{CEN}$	Input-synchronous	**Clock enable input, active LOW**. When asserted LOW the clock signal is recognized by the SRAM. When deasserted HIGH the clock signal is masked. Since deasserting $\overline{CEN}$ does not deselect the device, $\overline{CEN}$ can be used to extend the previous cycle when required.
DQ_S	I/O-synchronous	**Bidirectional data I/O lines**. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by $A_{[17:0]}$ during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$ and the internal control logic. When $\overline{OE}$ is asserted LOW, the pins can behave as outputs. When HIGH, DQ_a–DQ_d are placed in a tri-state condition. The outputs are automatically tri-stated during the data portion of a write sequence, during the first clock when emerging from a deselected state, and when the device is deselected, regardless of the state of $\overline{OE}$.
DQP_X	I/O-synchronous	**Bidirectional data parity I/O lines**. Functionally, these signals are identical to DQ_s. During write sequences, DQP_a is controlled by $\overline{BW}_a$, DQP_b is controlled by $\overline{BW}_b$, DQP_c is controlled by $\overline{BW}_c$, and DQP_d is controlled by $\overline{BW}_d$.
MODE	Input strap pin	**Mode input**. Selects the burst order of the device. Tied HIGH selects the interleaved burst order. Pulled LOW selects the linear burst order. MODE should not change states during operation. When left floating MODE defaults HIGH, to an interleaved burst order.
V_{DD}	Power supply	**Power supply inputs to the core of the device**.
V_{DDQ}	I/O power supply	**Power supply for the I/O circuitry**.
V_{SS}	Ground	**Ground for the device**. Must be connected to ground of the system.
NC	–	**No connects**. This pin is not connected to the die.

Pin Definitions *(continued)*

Pin Name	I/O Type	Pin Description
NC/(36M, 72M, 144M, 288M, 576M, 1G)	–	**These pins are not connected**. They are used for expansion to the 36M, 72M, 144M, 288M, 576M, and 1G densities.
ZZ	Input-asynchronous	**ZZ "sleep" input**. This active HIGH input places the device in a non-time critical "sleep" condition with data integrity preserved. During normal operation, this pin can be connected to V_{SS} or left floating. ZZ pin has an internal pull down.

Functional Overview

The CY7C1370S and CY7C1372S are synchronous-pipelined burst NoBL SRAMs designed specifically to eliminate wait states during write/read transitions. All synchronous inputs pass through input registers controlled by the rising edge of the clock. The clock signal is qualified with the clock enable input signal ($\overline{CEN}$). If $\overline{CEN}$ is HIGH, the clock signal is not recognized and all internal states are maintained. All synchronous operations are qualified with $\overline{CEN}$. All data outputs pass through output registers controlled by the rising edge of the clock. Maximum access delay from the clock rise (t_{CO}) is 3.0 ns (200-MHz device).

Accesses can be initiated by asserting all three chip enables ($\overline{CE_1}$, CE_2, $\overline{CE_3}$) active at the rising edge of the clock. If clock enable ($\overline{CEN}$) is active LOW and ADV/LD is asserted LOW, the address presented to the device is latched. The access can either be a read or write operation, depending on the status of the write enable ($\overline{WE}$). BW_X can be used to conduct byte write operations.

Write operations are qualified by the write enable ($\overline{WE}$). All writes are simplified with on-chip synchronous self-timed write circuitry.

Three synchronous chip enables ($\overline{CE_1}$, CE_2, $\overline{CE_3}$) and an asynchronous output enable ($\overline{OE}$) simplify depth expansion. All operations (reads, writes, and deselects) are pipelined. ADV/LD must be driven LOW once the device has been deselected in order to load a new address for the next operation.

Single Read Accesses

A read access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{CEN}$ is asserted LOW, (2) $\overline{CE_1}$, CE_2, and $\overline{CE_3}$ are all asserted active, (3) the write enable input signal $\overline{WE}$ is deasserted HIGH, and (4) ADV/LD is asserted LOW. The address presented to the address inputs is latched into the address register and presented to the memory core and control logic. The control logic determines that a read access is in progress and allows the requested data to propagate to the input of the output register. At the rising edge of the next clock the requested data is allowed to propagate through the output register and onto the data bus within 3.0 ns (200-MHz device) provided $\overline{OE}$ is active LOW. After the first clock of the read access the output buffers are controlled by $\overline{OE}$ and the internal control logic. $\overline{OE}$ must be driven LOW in order for the device to drive out the requested data. During the second clock, a subsequent operation (read/write/deselect) can be initiated. Deselecting the device is also pipelined. Therefore, when the SRAM is deselected at clock rise by one of the chip enable signals, its output tri-states following the next clock rise.

Burst Read Accesses

The CY7C1370S and CY7C1372S have an on-chip burst counter that allows the user the ability to supply a single address and conduct up to four reads without reasserting the address inputs. ADV/LD must be driven LOW in order to load a new address into the SRAM, as described in the Single Read Accesses section. The sequence of the burst counter is determined by the MODE input signal. A LOW input on MODE selects a linear burst mode, a HIGH selects an interleaved burst sequence. Both burst counters use A0 and A1 in the burst sequence, and wraps around when incremented sufficiently. A HIGH input on ADV/LD increments the internal burst counter regardless of the state of chip enables inputs or $\overline{WE}$. $\overline{WE}$ is latched at the beginning of a burst cycle. Therefore, the type of access (read or write) is maintained throughout the burst sequence.

Single Write Accesses

Write access are initiated when the following conditions are satisfied at clock rise: (1) $\overline{CEN}$ is asserted LOW, (2) $\overline{CE_1}$, CE_2, and $\overline{CE_3}$ are all asserted active, and (3) the write signal $\overline{WE}$ is asserted LOW. The address presented is loaded into the address register. The write signals are latched into the control logic block.

On the subsequent clock rise the data lines are automatically tri-stated regardless of the state of the $\overline{OE}$ input signal. This allows the external logic to present the data on DQ and DQP ($DQ_{a,b,c,d}$/$DQP_{a,b,c,d}$ for CY7C1370S and $DQ_{a,b}$/$DQP_{a,b}$ for CY7C1372S). In addition, the address for the subsequent access (read/write/deselect) is latched into the address register (provided the appropriate control signals are asserted).

On the next clock rise the data presented to DQ and DQP ($DQ_{a,b,c,d}$/$DQP_{a,b,c,d}$ for CY7C1370S and $DQ_{a,b}$/$DQP_{a,b}$ for CY7C1372S) (or a subset for byte write operations, see Write Cycle Description table for details) inputs is latched into the device and the write is complete.

The data written during the write operation is controlled by $\overline{BW}$ ($\overline{BW_{a,b,c,d}}$ for CY7C1370S and $\overline{BW_{a,b}}$ for CY7C1372S) signals. The CY7C1370S/CY7C1372S provides byte write capability that is described in the Write Cycle Description table. Asserting the write enable input ($\overline{WE}$) with the selected byte write select ($\overline{BW}$) input selectively writes to only the desired bytes. Bytes not selected during a byte write operation remains unaltered. A synchronous self-timed write mechanism has been provided to simplify the write operations. Byte write capability has been included in order to greatly simplify read/modify/write

sequences, which can be reduced to simple byte write operations.

Because the CY7C1370S and CY7C1372S are common I/O devices, data must not be driven into the device while the outputs are active. The output enable ($\overline{OE}$) can be deasserted HIGH before presenting data to the DQ and DQP ($DQ_{a,b,c,d}$/$DQP_{a,b,c,d}$ for CY7C1370S and $DQ_{a,b}$/$DQP_{a,b}$ for CY7C1372S) inputs. Doing so tri-states the output drivers. As a safety precaution, DQ and DQP ($DQ_{a,b,c,d}$/$DQP_{a,b,c,d}$ for CY7C1370S and $DQ_{a,b}$/$DQP_{a,b}$ for CY7C1372S) are automatically tri-stated during the data portion of a write cycle, regardless of the state of $\overline{OE}$.

Burst Write Accesses

The CY7C1370S/CY7C1372S has an on-chip burst counter that allows the user the ability to supply a single address and conduct up to four write operations without reasserting the address inputs. ADV/$\overline{LD}$ must be driven LOW in order to load the initial address, as described in the section Single Write Accesses on page 6. When ADV/$\overline{LD}$ is driven HIGH on the subsequent clock rise, the chip enables ($\overline{CE_1}$, CE_2, and $\overline{CE_3}$) and $\overline{WE}$ inputs are ignored and the burst counter is incremented. The correct $\overline{BW}$ ($\overline{BW_{a,b,c,d}}$ for CY7C1370S and $\overline{BW_{a,b}}$ for CY7C1372S) inputs must be driven in each cycle of the burst write in order to write the correct bytes of data.

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation “sleep” mode. Two clock cycles are required to enter into or exit from this “sleep” mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the “sleep” mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the “sleep” mode. $\overline{CE_1}$, CE_2, and $\overline{CE_3}$, must remain inactive for the duration of t_{ZZREC} after the ZZ input returns LOW.

Interleaved Burst Address Table

(MODE = Floating or V_{DD})

First Address A1:A0	Second Address A1:A0	Third Address A1:A0	Fourth Address A1:A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

Linear Burst Address Table

(MODE = GND)

First Address A1:A0	Second Address A1:A0	Third Address A1:A0	Fourth Address A1:A0
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min	Max	Unit
I_{DDZZ}	Sleep mode standby current	ZZ $\geq$ V_{DD} – 0.2 V	–	80	mA
t_{ZZS}	Device operation to ZZ	ZZ $\geq$ V_{DD} – 0.2 V	–	$2t_{CYC}$	ns
t_{ZZREC}	ZZ recovery time	ZZ $\leq$ 0.2 V	$2t_{CYC}$	–	ns
t_{ZZI}	ZZ active to sleep current	This parameter is sampled	–	$2t_{CYC}$	ns
t_{RZZI}	ZZ inactive to exit sleep current	This parameter is sampled	0	–	ns

Truth Table

The truth table CY7C1370S and CY7C1372S follows. [1, 2, 3, 4, 5, 6, 7]

Operation	Address Used	$\overline{CE}$	ZZ	ADV/$\overline{LD}$	$\overline{WE}$	$\overline{BW_x}$	$\overline{OE}$	$\overline{CEN}$	CLK	DQ
Deselect cycle	None	H	L	L	X	X	X	L	L–H	Tri-state
Continue deselect cycle	None	X	L	H	X	X	X	L	L–H	Tri-state
Read cycle (begin burst)	External	L	L	L	H	X	L	L	L–H	Data out (Q)
Read cycle (continue burst)	Next	X	L	H	X	X	L	L	L–H	Data out (Q)
NOP/dummy read (begin burst)	External	L	L	L	H	X	H	L	L–H	Tri-state
Dummy read (continue burst)	Next	X	L	H	X	X	H	L	L–H	Tri-state
Write cycle (begin burst)	External	L	L	L	L	L	X	L	L–H	Data in (D)
Write cycle (continue burst)	Next	X	L	H	X	L	X	L	L–H	Data in (D)
NOP/write abort (begin burst)	None	L	L	L	L	H	X	L	L–H	Tri-state
Write abort (continue burst)	Next	X	L	H	X	H	X	L	L–H	Tri-state
Ignore clock edge (stall)	Current	X	L	X	X	X	X	H	L–H	–
Sleep mode	None	X	H	X	X	X	X	X	X	Tri-state

Notes
1. X = “Don't Care”, H = Logic HIGH, L = Logic LOW, $\overline{CE}$ stands for all chip enables active. $\overline{BW}$x = L signifies at least one byte write select is active, $\overline{BW}$x = valid signifies that the desired byte write selects are asserted, see Write Cycle Description table for details.
2. Write is defined by $\overline{WE}$ and $\overline{BW}_X$. See Write Cycle Description table for details.
3. When a write cycle is detected, all IOs are tri-stated, even during byte writes.
4. The DQ and DQP pins are controlled by the current cycle and the $\overline{OE}$ signal.
5. $\overline{CEN}$ = H inserts wait states.
6. Device powers up deselected and the IOs in a tri-state condition, regardless of $\overline{OE}$.
7. $\overline{OE}$ is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles.During a read cycle DQ_s and DQP_X = three-state when $\overline{OE}$ is inactive or when the device is deselected, and DQ_s = data when $\overline{OE}$ is active

Partial Write Cycle Description

The Partial Write Cycle Description table for CY7C1370S follows. [8, 9, 10, 11]

Function (CY7C1370S)	$\overline{WE}$	$\overline{BW_d}$	$\overline{BW_c}$	$\overline{BW_b}$	$\overline{BW_a}$
Read	H	X	X	X	X
Write – No bytes written	L	H	H	H	H
Write byte a – (DQ_a and DQP_a)	L	H	H	H	L
Write byte b – (DQ_b and DQP_b)	L	H	H	L	H
Write bytes b, a	L	H	H	L	L
Write byte c – (DQ_c and DQP_c)	L	H	L	H	H
Write bytes c, a	L	H	L	H	L
Write bytes c, b	L	H	L	L	H
Write bytes c, b, a	L	H	L	L	L
Write byte d – (DQ_d and DQP_d)	L	L	H	H	H
Write bytes d, a	L	L	H	H	L
Write bytes d, b	L	L	H	L	H
Write bytes d, b, a	L	L	H	L	L
Write bytes d, c	L	L	L	H	H
Write bytes d, c, a	L	L	L	H	L
Write bytes d, c, b	L	L	L	L	H
Write all bytes	L	L	L	L	L

Partial Write Cycle Description

The Partial Write Cycle Description table for CY7C1372S follows. [8, 9, 10, 11]

Function (CY7C1372S)	$\overline{WE}$	$\overline{BW_b}$	$\overline{BW_a}$
Read	H	X	X
Write – no bytes written	L	H	H
Write byte a – (DQ_a and DQP_a)	L	H	L
Write byte b – (DQ_b and DQP_b)	L	L	H
Write both bytes	L	L	L

Notes
8. X = "Don't Care", H = Logic HIGH, L = Logic LOW, $\overline{CE}$ stands for all chip enables active. $\overline{BW}$x = L signifies at least one byte write select is active, $\overline{BW}$x = valid signifies that the desired byte write selects are asserted, see Write Cycle Description table for details.
9. Write is defined by $\overline{WE}$ and $\overline{BW}_X$. See Write Cycle Description table for details.
10. When a write cycle is detected, all IOs are tri-stated, even during byte writes.
11. Table only lists a partial listing of the byte write combinations. Any Combination of $\overline{BW}_X$ is valid Appropriate write is done based on which byte write is active.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage on V_{DD} relative to GND .....–0.5 V to +4.6 V

Supply voltage on V_{DDQ} relative to GND ..... –0.5 V to +V_{DD}

DC to outputs in tri-state .....–0.5 V to V_{DDQ} + 0.5 V

DC input voltage .....–0.5 V to V_{DD} + 0.5 V

Current into outputs (LOW) ..... 20 mA

Static discharge voltage (per MIL-STD-883, method 3015) ..... > 2001 V

Latch-up current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Commercial	0 °C to +70 °C	3.3 V – 5% / + 10%	2.5 V – 5% to V_{DD}

Electrical Characteristics

Over the Operating Range

Parameter [12, 13]	Description	Test Conditions		Min	Max	Unit
V_{DD}	Power supply voltage			3.135	3.6	V
V_{DDQ}	I/O supply voltage	for 3.3 V I/O		3.135	V_{DD}	V
		for 2.5 V I/O		2.375	2.625	V
V_{OH}	Output HIGH voltage	for 3.3 V I/O, I_{OH} = –4.0 mA		2.4	–	V
		for 2.5 V I/O, I_{OH} = –1.0 mA		2.0	–	V
V_{OL}	Output LOW voltage	for 3.3 V I/O, I_{OL} = 8.0 mA		–	0.4	V
		for 2.5 V I/O, I_{OL} = 1.0 mA		–	0.4	V
V_{IH}	Input HIGH voltage[12]	for 3.3 V I/O		2.0	V_{DD} + 0.3	V
		for 2.5 V I/O		1.7	V_{DD} + 0.3	V
V_{IL}	Input LOW voltage[12]	for 3.3 V I/O		–0.3	0.8	V
		for 2.5 V I/O		–0.3	0.7	V
I_X	Input leakage current except ZZ and MODE	GND ≤ V_I ≤ V_{DDQ}		–5	5	µA
	Input current of MODE	Input = V_{SS}		–30	–	µA
		Input = V_{DD}		–	5	µA
	Input current of ZZ	Input = V_{SS}		–5	–	µA
		Input = V_{DD}		–	30	µA
I_{OZ}	Output leakage current	GND ≤ V_I ≤ V_{DDQ}, output disabled		–5	5	µA
I_{DD} [14]	V_{DD} operating supply	V_{DD} = Max, I_{OUT} = 0 mA, f = f_{MAX} = 1/t_{CYC}	5-ns cycle, 200 MHz	–	300	mA
			6-ns cycle, 167 MHz	–	275	mA
I_{SB1}	Automatic CE power-down current – TTL inputs	Max. V_{DD}, device deselected, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX} = 1/t_{CYC}	5-ns cycle, 200 MHz	–	150	mA
			6-ns cycle, 167 MHz	–	140	mA
I_{SB2}	Automatic CE power-down current – CMOS inputs	Max. V_{DD}, device deselected, V_{IN} ≤ 0.3 V or V_{IN} ≥ V_{DDQ} – 0.3 V, f = 0	All speed grades	–	70	mA

Notes
12. Overshoot: $V_{IH(AC)}$ < V_{DD} + 1.5 V (Pulse width less than $t_{CYC}/2$), undershoot: $V_{IL(AC)}$ > –2 V (Pulse width less than $t_{CYC}/2$).
13. $T_{Power-up}$: Assumes a linear ramp from 0 V to V_{DD} (min) within 200 ms. During this time V_{IH} < V_{DD} and V_{DDQ} ≤ V_{DD}.
14. The operation current is calculated with 50% read cycle and 50% write cycle.

Electrical Characteristics *(continued)*

Over the Operating Range

Parameter [12, 13]	Description	Test Conditions		Min	Max	Unit
I_{SB3}	Automatic CE power-down current – CMOS inputs	Max. V_{DD}, device deselected, $V_{IN} \le 0.3$ V or $V_{IN} \ge V_{DDQ} - 0.3$ V, $f = f_{MAX} = 1/t_{CYC}$	5-ns cycle, 200 MHz	–	130	mA
			6-ns cycle, 167 MHz	–	125	mA
I_{SB4}	Automatic CE power-down current – TTL inputs	Max. V_{DD}, device deselected, $V_{IN} \ge V_{IH}$ or $V_{IN} \le V_{IL}$, f = 0	All speed grades	–	80	mA

Capacitance

Parameter [15]	Description	Test Conditions	100-pin TQFP Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{DD} = 3.3 V, V_{DDQ} = 2.5 V	5	pF
C_{CLK}	Clock input capacitance		5	pF
C_{IO}	Input/Output capacitance		5	pF

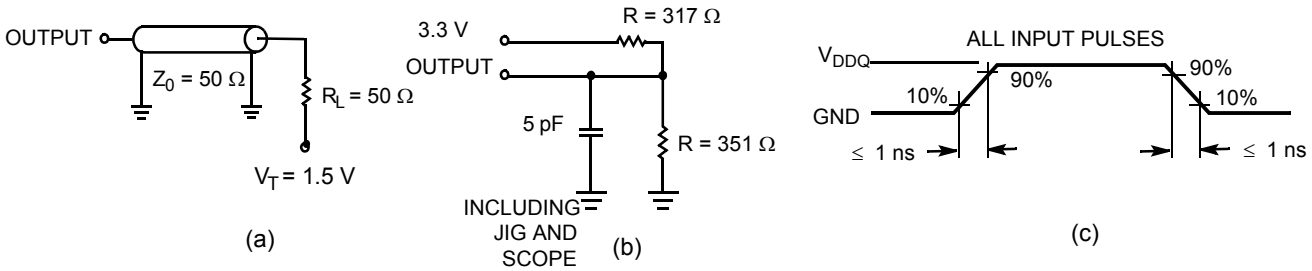
Thermal Resistance

Parameter [15]	Description	Test Conditions	100-pin TQFP Package	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	28.66	°C/W
Θ_{JC}	Thermal resistance (junction to case)		4.08	°C/W

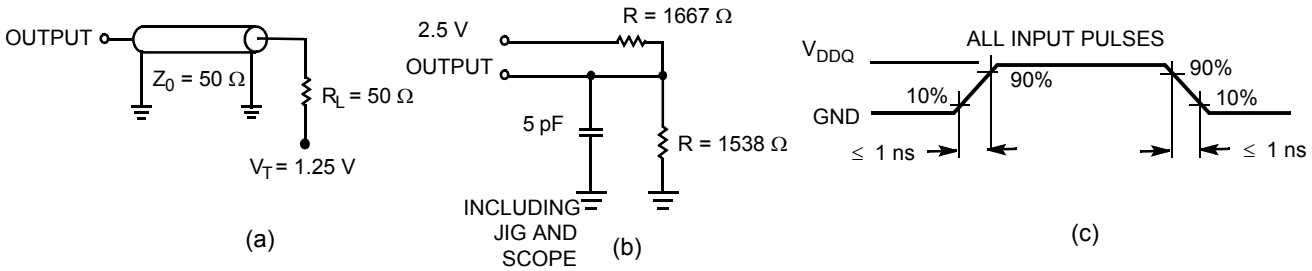
AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms

3.3 V I/O Test Load



2.5 V I/O Test Load



Note
15. Tested initially and after any design or process change that may affect these parameters.

Switching Characteristics

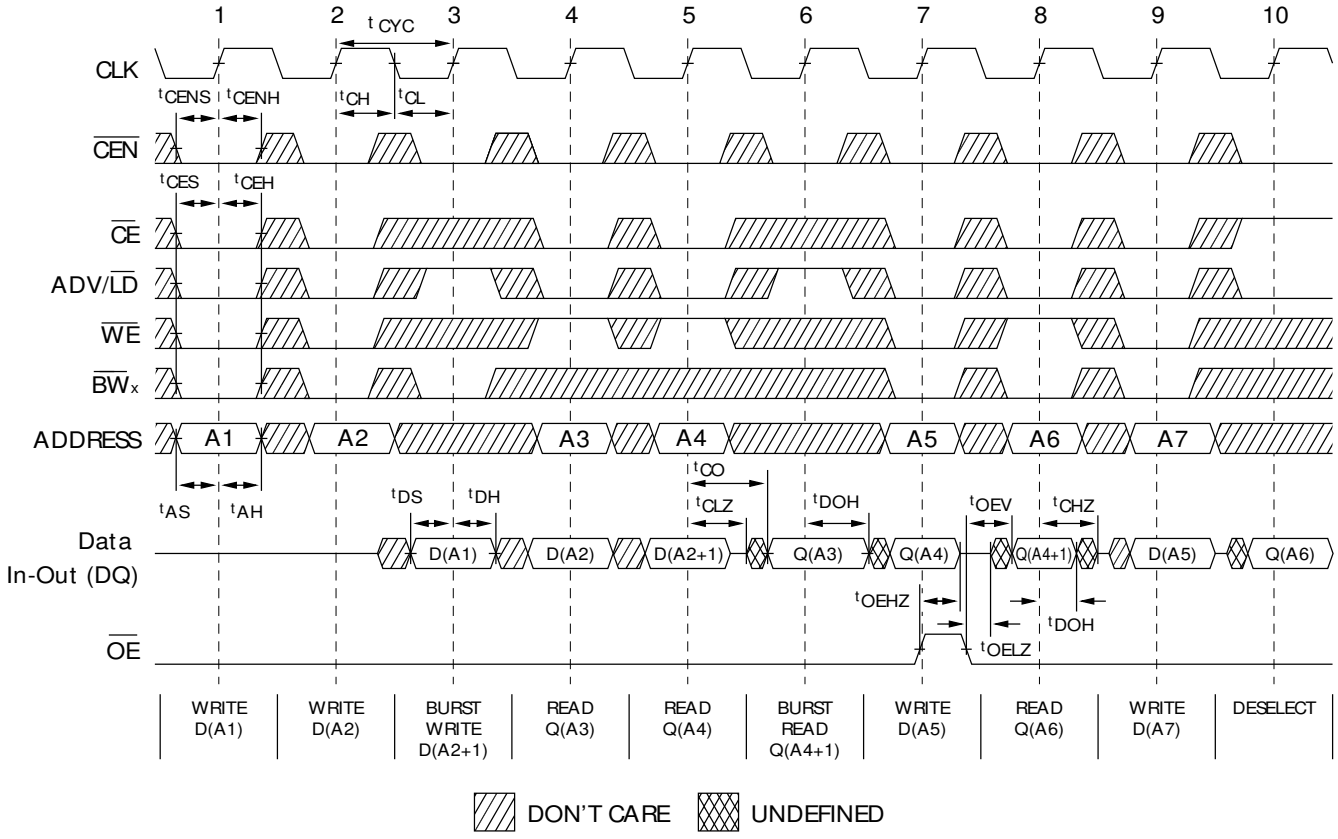
Over the Operating Range

Parameter [16, 17]	Description	-200		-167		Unit
		Min	Max	Min	Max	
t_{Power}[18]	V_{CC}(typical) to the first access read or write	1	–	1	–	ms
Clock						
t_{CYC}	Clock cycle time	5	–	6	–	ns
F_{MAX}	Maximum operating frequency	–	200	–	167	MHz
t_{CH}	Clock HIGH	2.0	–	2.2	–	ns
t_{CL}	Clock LOW	2.0	–	2.2	–	ns
Output Times						
t_{CO}	Data output valid after CLK rise	–	3.0	–	3.4	ns
t_{EOV}	$\overline{OE}$ LOW to output valid	–	3.0	–	3.4	ns
t_{DOH}	Data output hold after CLK rise	1.3	–	1.3	–	ns
t_{CHZ}	Clock to high Z[19, 20, 21]	–	3.0	–	3.4	ns
t_{CLZ}	Clock to low Z[19, 20, 21]	1.3	–	1.3	–	ns
t_{EOHZ}	$\overline{OE}$ HIGH to output high Z[19, 20, 21]	–	3.0	–	3.4	ns
t_{EOLZ}	$\overline{OE}$ LOW to output low Z[19, 20, 21]	0	–	0	–	ns
Setup Times						
t_{AS}	Address setup before CLK rise	1.4	–	1.5	–	ns
t_{DS}	Data input setup before CLK rise	1.4	–	1.5	–	ns
t_{CENS}	$\overline{CEN}$ setup before CLK rise	1.4	–	1.5	–	ns
t_{WES}	$\overline{WE}$, $\overline{BW_X}$ setup before CLK rise	1.4	–	1.5	–	ns
t_{ALS}	ADV/$\overline{LD}$ setup before CLK rise	1.4	–	1.5	–	ns
t_{CES}	Chip select setup	1.4	–	1.5	–	ns
Hold Times						
t_{AH}	Address hold after CLK rise	0.4	–	0.5	–	ns
t_{DH}	Data input Hold after CLK rise	0.4	–	0.5	–	ns
t_{CENH}	$\overline{CEN}$ hold after CLK rise	0.4	–	0.5	–	ns
t_{WEH}	$\overline{WE}$, $\overline{BW_X}$ hold after CLK rise	0.4	–	0.5	–	ns
t_{ALH}	ADV/$\overline{LD}$ hold after CLK rise	0.4	–	0.5	–	ns
t_{CEH}	Chip select hold after CLK rise	0.4	–	0.5	–	ns

Notes
16. Timing reference is 1.5 V when V_{DDQ} = 3.3 V and is 1.25 V when V_{DDQ} = 2.5 V.
17. Test conditions shown in (a) of Figure 2 on page 11 unless otherwise noted.
18. This part has a voltage regulator internally; t_{Power} is the time power is supplied above $V_{DD(minimum)}$ initially, before a read or write operation can be initiated.
19. t_{CHZ}, t_{CLZ}, t_{EOLZ}, and t_{EOHZ} are specified with AC test conditions shown in (b) of Figure 2 on page 11. Transition is measured ±200 mV from steady-state voltage.
20. At any voltage and temperature, t_{EOHZ} is less than t_{EOLZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve high Z prior to low Z under the same system conditions.
21. This parameter is sampled and not 100% tested.

Switching Waveforms

Figure 2. Read/Write/Timing [22, 23, 24]



Notes
22. For this waveform ZZ is tied LOW.
23. When $\overline{CE}$ is LOW, $\overline{CE}_1$ is LOW, CE_2 is HIGH and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH,$\overline{CE}_1$ is HIGH or CE_2 is LOW or $\overline{CE}_3$ is HIGH.
24. Order of the burst sequence is determined by the status of the MODE (0 = Linear, 1 = Interleaved). Burst operations are optional.

Switching Waveforms *(continued)*

Figure 3. NOP,STALL and DESELECT Cycles [25, 26, 27]

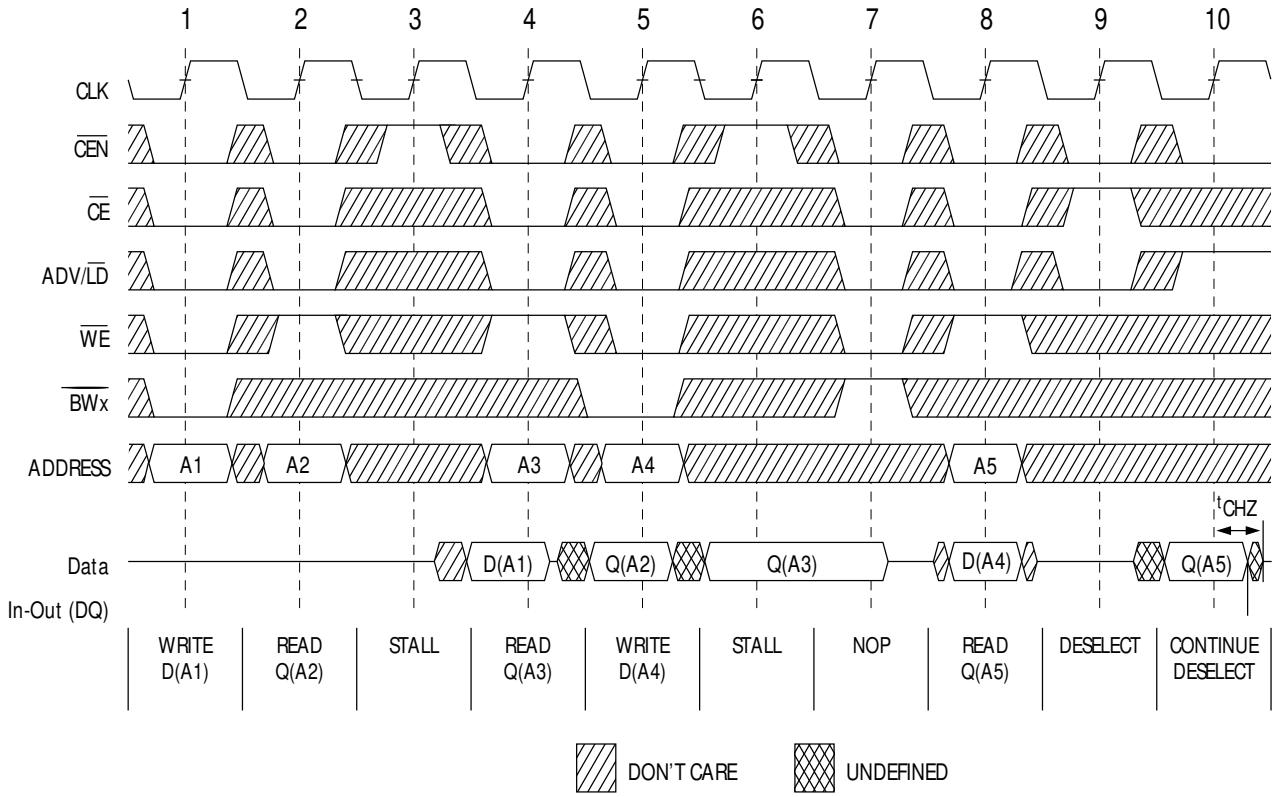
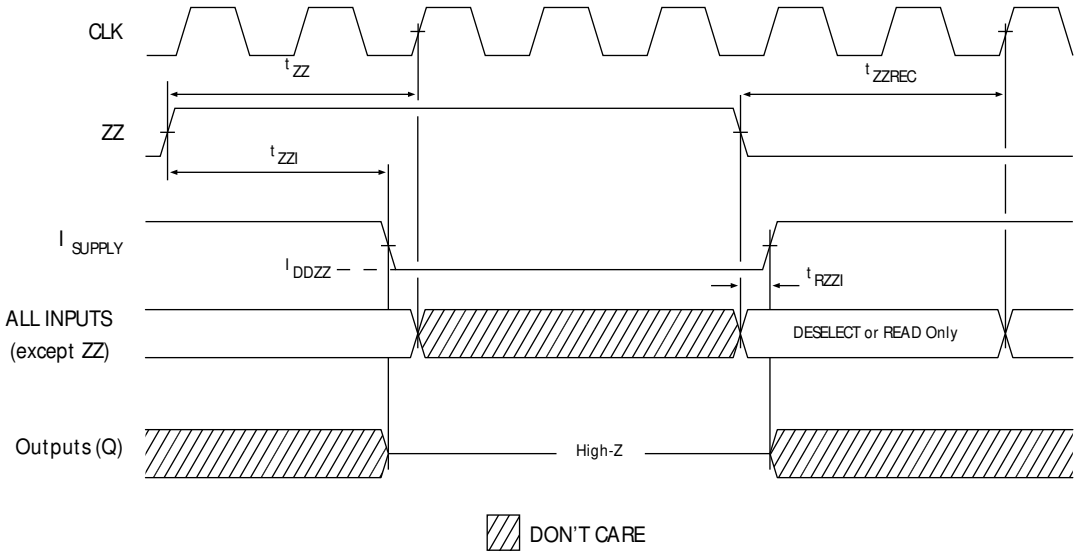


Figure 4. ZZ Mode Timing [28, 29]



Notes
25. For this waveform ZZ is tied LOW.
26. When $\overline{CE}$ is LOW, $\overline{CE_1}$ is LOW, CE_2 is HIGH and $\overline{CE_3}$ is LOW. When $\overline{CE}$ is HIGH, $\overline{CE_1}$ is HIGH or CE_2 is LOW or $\overline{CE_3}$ is HIGH.
27. The ignore clock edge or stall cycle (Clock 3) illustrated $\overline{CEN}$ being used to create a pause. A write is not performed during this cycle.
28. Device must be deselected when entering ZZ mode. See cycle description table for all possible signal conditions to deselect the device.
29. IOs are in high Z when exiting ZZ sleep mode.

Ordering Information

The following table contains only the list of parts that are currently available. If you do not see what you are looking for, contact your local sales representative. For more information, visit the Cypress website at www.cypress.com and refer to the product summary page at http://www.cypress.com/products.

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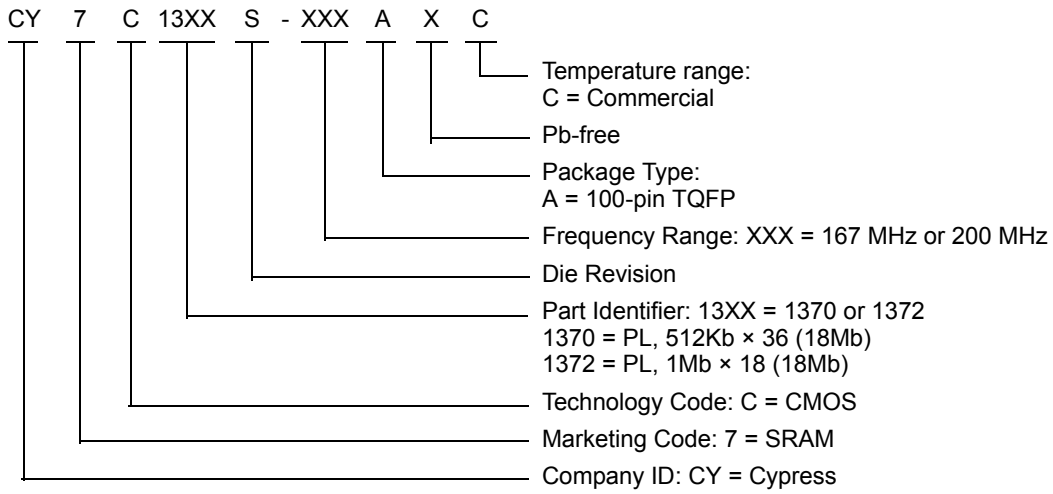
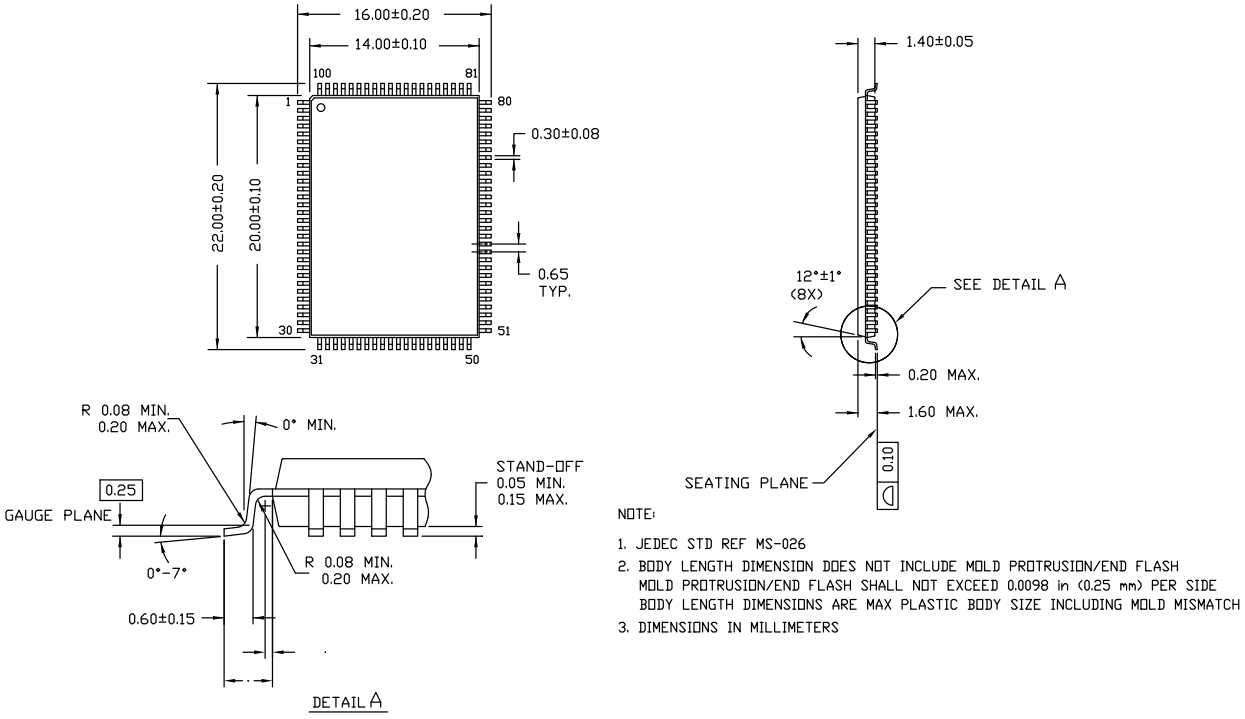
Speed (MHz)	Ordering Code	Package Diagram	Part and Package Type	Operating Range
167	CY7C1370S-167AXC	51-85050	100-pin TQFP (14 × 20 × 1.4 mm) Pb-free	Commercial
	CY7C1372S-167AXC			
200	CY7C1370S-200AXC	51-85050	100-pin TQFP (14 × 20 × 1.4 mm) Pb-free	Commercial

Ordering Code Definitions



Package Diagrams

Figure 5. 100-pin TQFP (14 × 20 × 1.4 mm) A100RA Package Outline, 51-85050



51-85050 *E

Acronyms

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
NoBL	No Bus Latency
$\overline{OE}$	Output Enable
SRAM	Static Random Access Memory
TTL	Transistor-Transistor Logic
TQFP	Thin Quad Flat Pack
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
mA	milliampere
mm	millimeter
ms	millisecond
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C1370S/CY7C1372S, 18-Mbit (512K × 36/1M × 18) Pipelined SRAM with NoBL™ Architecture Document Number: 001-43824				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	1897927	See ECN	VKN / AESA	New data sheet.
*A	2082246	See ECN	JASM	Changed status from Preliminary to Final.
*B	2896565	03/20/2010	NJY	Updated Ordering Information (Removed obsolete part numbers). Updated Package Diagrams.
*C	2906548	04/07/2010	NJY	Updated Ordering Information (Removed inactive parts).
*D	3050813	10/07/2010	AJU	Updated Ordering Information: Updated part numbers. Added Ordering Code Definitions. Added Acronyms and Units of Measure. Minor edits. Updated to new template.
*E	3196490	03/15/2011	NJY	Updated Package Diagrams.
*F	3572553	04/04/2012	PRIT	Updated Features (Removed 250 MHz frequency related information, removed 119-ball BGA package and 165-ball FBGA package related information). Updated Selection Guide (Removed 250 MHz frequency related information). Updated Pin Configurations (Removed 119-ball BGA package and 165-ball FBGA package related information). Updated Pin Definitions (Removed JTAG related information). Removed IEEE 1149.1 Serial Boundary Scan (JTAG). Removed TAP Controller State Diagram. Removed TAP Controller Block Diagram. Removed TAP Timing. Removed TAP AC Switching Characteristics. Removed 3.3 V TAP AC Test Conditions. Removed 3.3 V TAP AC Output Load Equivalent. Removed 2.5 V TAP AC Test Conditions. Removed 2.5 V TAP AC Output Load Equivalent. Removed TAP DC Electrical Characteristics and Operating Conditions. Removed Identification Register Definitions. Removed Scan Register Sizes. Removed Identification Codes. Removed Boundary Scan Order. Updated Operating Range (Removed Industrial Temperature Range). Updated Electrical Characteristics (Removed 250 MHz frequency related information). Updated Capacitance (Removed 119-ball BGA package and 165-ball FBGA package related information). Updated Thermal Resistance (Removed 119-ball BGA package and 165-ball FBGA package related information). Updated Switching Characteristics (Removed 250 MHz frequency related information). Updated Package Diagrams (Removed 119-ball BGA package and 165-ball FBGA package related information). Replaced all instances of IO with I/O across the document.
*G	3978217	04/22/2013	PRIT	No technical updates. Completing Sunset Review.
*H	5187232	03/23/2016	PRIT	Updated Package Diagrams: spec 51-85050 – Changed revision from *D to *E. Updated to new template. Completing Sunset Review.

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