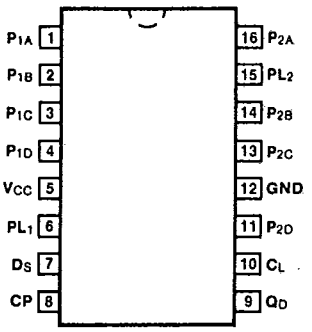
54/7494
4-BIT SHIFT REGISTER

DESCRIPTION — The '94 contains four dc coupled RS master/slave flip-flops with serial data entry into the first stage for synchronous Serial-in/Serial-out operation, and with a common asynchronous Clear and two sets of individual asynchronous Preset inputs. Preset inputs P_{1X} are enabled by a HIGH signal on PL_1 and Preset inputs P_{2X} are enabled by a HIGH signal on PL_2. The normal procedure for paralled entry of data consists of re-setting the flip-flops by applying a momentary HIGH signal to CL, followed by a HIGH signal on either PL_1, or PL_2, depending on which set of parallel data is desired. For serial operation the CL and both PL inputs must be LOW. Serial transfer is initiated by the rising edge of the clock.

CONNECTION DIAGRAM
PINOUT A



4

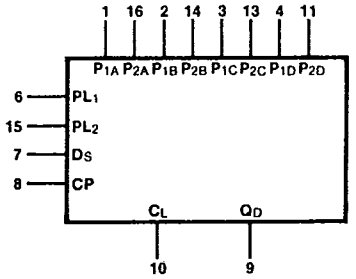
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7494PC		9B
Ceramic DIP (D)	A	7494DC	5494DM	7B
Flatpak (F)	A	7494FC	5494FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW
P_{1A} — P_{1D}	Source 1 Parallel Data Inputs	1.0/1.0
P_{2A} — P_{2D}	Source 2 Parallel Data Inputs	1.0/1.0
PL_1	Asynchronous Parallel Load Input (Source 1)	4.0/4.0
PL_2	Asynchronous Parallel Load Input (Source 2)	4.0/4.0
D_S	Serial Data Input	1.0/1.0
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0
CL	Asynchronous Clear Input (Active HIGH)	1.0/1.0
Q_D	Serial Data Output	10/10

LOGIC SYMBOL



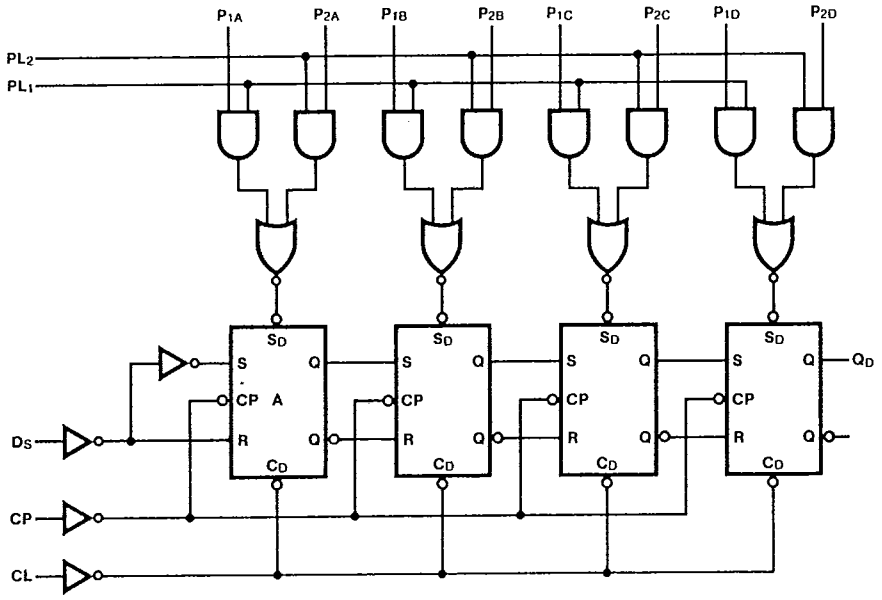
V_{CC} = Pin 5
GND = Pin 12

TRUTH TABLE

INPUTS CP	CL	$PL_1 \bullet P_{1D}$	$PL_2 \bullet P_{2D}$	OUTPUTS Q_D	RESPONSE
X	H	L	L	L	Clear
X	L	H	X	H	Preset
X	L	X	H	H	Preset
X	H	H	X	H	Indeterminate
X	H	X	H	H	Indeterminate
⎍	L	L	L	Q_C	Shift Right

NOTE: All four flip-flops respond in a similar manner.
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74 Min	54/74 Max	UNITS	CONDITIONS
I_{CC}	Power Supply Current	XM		50	mA	V_{CC} = Max
		XC		58		

AC CHARACTERISTICS: V_{CC} = 5.0 V, T_A = 25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF R_L = 400 Ω Min	54/74 Max	UNITS	CONDITIONS
f_{max}	Maximum Shift Frequency	10		MHz	Figs. 3-1, 3-8
t_{PLH}	Propagation Delay CP to Q_D		40	ns	Figs. 3-1, 3-8
t_{PHL}			40		
t_{PLH}	Propagation Delay, PL_n to Q_D		35	ns	Figs. 3-1, 3-17
t_{PHL}	Propagation Delay, CL to Q_D		40		

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74 Min	54/74 Max	UNITS	CONDITIONS
t_s (H)	Setup Time HIGH, D_s to CP	35		ns	Fig. 3-6
t_h (H)	Hold Time HIGH, D_s to CP	0		ns	
t_s (L)	Setup Time LOW, D_s to CP	25		ns	Fig. 3-6
t_h (L)	Hold Time LOW, D_s to CP	0		ns	
t_w (H)	CP Pulse Width HIGH	35		ns	Fig. 3-8
t_w (H)	CL Pulse Width HIGH	30		ns	Fig. 3-16
t_w (H)	PL_n Pulse Width HIGH	30		ns	Fig. 3-16

4