DSA20XX

Low Jitter Configurable Dual Output Oscillators for Automotive

Features

- Automotive AEC-Q100 Qualified
- Two Independent Outputs with Any Format Combination from LVPECL, LVDS, HCSL, and LVCMOS
- Wide Frequency Range:
  - 2.3 MHz to 460 MHz LVDS/HCSL/LVPECL Output
  - 2.3 MHz to 170 MHz CMOS Output
- Low RMS Phase Jitter: <1 ps (typical)
- High Stability: ±25 ppm, ±50 ppm
- Wide Temperature Range
  - Automotive Grade 2: –40° to +105°C
  - Automotive Grade 3: –40°C to +85°C
- High Supply Noise Rejection: –50 dBc
- Pin-Selectable Configurations
  - 3-bit Output Drive Strength (CMOS)
  - 3-bit Output Frequency Combinations
- Miniature Footprint of 3.2 mm x 2.5 mm
- Excellent Shock and Vibration Immunity
  - Qualified to MIL-STD-883
- High Reliability
  - 20x Better MTF Than Quartz Oscillators
- Supply Range of 2.25V to 3.6V
- Short Sample Lead Time: <2 weeks
- Lead Free & RoHS Compliant

Applications

- Automotive Infotainment
- Automotive ADAS
- Autonomous Driving
- In-Vehicle Network

General Description

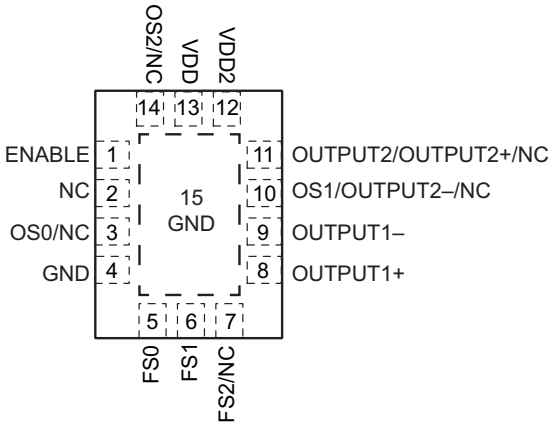
The DSA20xx family of high performance dual output oscillators utilizes proven silicon MEMS technology to provide excellent jitter and stability while incorporating additional device functionality. The two outputs are controlled by separate supply voltages to allow for independent voltage level control. The frequencies of the outputs can be identical or independently derived from a common PLL frequency source. The DSA20xx have provisions for up to eight user-defined pre-programmed, pin-selectable output frequency combinations. The DSA20x1 is also equipped with independent pin-selectable output drive strengths for the CMOS output to reduce EMI and noise.

Please visit the Microchip ClockWorks® Configurator website at http://clockworks.microchip.com/timing/ to configure the part number for customized frequencies.

All DSA20xx devices are packaged in a 14-lead 3.2 mm x 2.5 mm QFN package and is available in Automotive Grade 2 and Grade 3 temperatures.

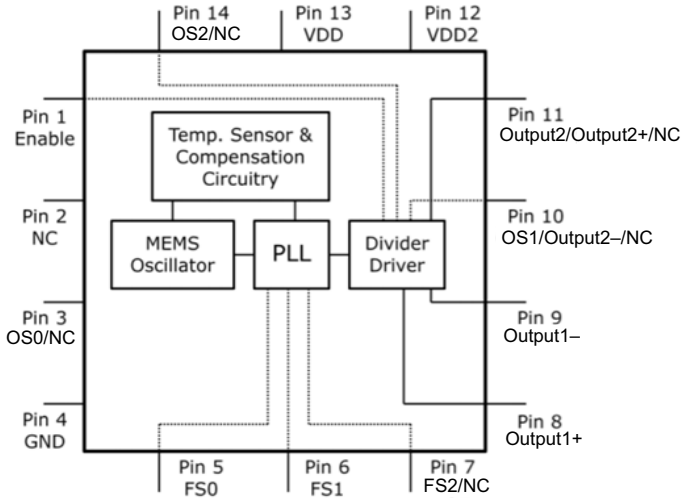
Package Type

DSA20xx
3.2 mm x 2.5 mm QFN
(Top View)



Block Diagram

DSA20xx



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Supply Voltage ..... –0.3V to +4.0V
Input Voltage (V_{IN}) ..... –0.3V to V_{DD} + 0.3V
ESD Protection ..... 4 kV HBM, 400V MM, 1.5 kV CDM

ELECTRICAL CHARACTERISTICS

Electrical Characteristics: Unless otherwise indicated, T = +25°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Supply Voltage	V_{DD}	2.25	—	3.6	V	Note 1
Supply Current	I_{DD}	—	21	23	mA	EN pin low, outputs are disabled
Supply Current (Note 2)	I_{DD}	—	49	—	mA	EN pin high, outputs are enabled; LVDS: R_L = 100Ω, F_{O1} = 125 MHz; CMOS: C_L = 15 pF, F_{O2} = 75 MHz
Frequency Stability	Δf	—	—	±25	ppm	Includes frequency variations due to initial tolerance, temperature, and power supply voltage.
		—	—	±50		
Aging	Δf	—	—	±5	ppm	First year
		—	—	±1		Subsequent years
Startup Time	t_{SU}	—	—	5	ms	T = +25°C, Note 3
Input Logic Level High	V_{IH}	0.75xV_{DD}	—	—	V	—
Input Logic Level Low	V_{IL}	—	—	0.25xV_{DD}		
Output Disable Time	t_{DA}	—	—	5	ns	Note 4
Output Enable Time	t_{EN}	—	—	20	ns	—
Pull-Up Resistor	R_{PU}	—	40	—	kΩ	Note 2, Pull-up exists on all digital I/Os
LVDS Outputs						
Output Offset Voltage	—	1.125	—	1.4	V	R_L = 100Ω differential
Delta Offset Voltage	—	—	—	50	mV	—
Peak-to-Peak Output Swing	—	—	350	—	mV	Single-ended
Output Rise/Fall Time	t_r/t_f	200	—	350	ps	20% to 80%, R_L = 100Ω, C_L = 2 pF (to GND)
Frequency	f_0	2.3	—	460	MHz	Single frequency
Output Duty Cycle	SYM	48	—	52	%	Differential

Note 1: Pin 4 V_{DD} should be filtered with 0.01 µF capacitor.
2: Output is enabled if Enable pad is floated or not connected
3: t_{SU} is time to stable output frequency after V_{DD} is applied and outputs are enabled.
4: Output Waveform and Test Circuit figures define the parameters.
5: Period Jitter include crosstalk from adjacent output.

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, T = +25°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Period Jitter (Note 5)	J_{PER}	—	2.5	—	ps_{RMS}	F_{O1} = 125 MHz
Integrated Phase Noise	J_{CC}	—	0.28	—	ps_{RMS}	200 kHz to 20 MHz @ 156.25 MHz
		—	0.4	—		100 kHz to 20 MHz @ 156.25 MHz
		—	1.7	2		12 kHz to 20 MHz @ 156.25 MHz
CMOS Output						
Output Logic Level High	V_{OH}	$0.9xV_{DD}$	—	—	V	I = ±6 mA
Output Logic Level Low	V_{OL}	—	—	$0.1xV_{DD}$		
Output Rise/Fall Time	t_r	—	1.1	2	ns	20% to 80%, C_L = 15 pF
	t_f	—	1.3	2		
Frequency	f_0	2.3	—	170	MHz	Commercial/Industrial temperature range
Output Duty Cycle	SYM	45	—	55	%	—
Period Jitter (Note 5)	J_{PER}	—	3	—	ps_{RMS}	F_{O2} = 125 MHz
Integrated Phase Noise	J_{CC}	—	0.3	—	ps_{RMS}	200 kHz to 20 MHz @ 125 MHz
		—	0.38	—		100 kHz to 20 MHz @ 125 MHz
		—	1.7	2		12 kHz to 20 MHz @ 125 MHz
LVPECL Outputs						
Output Logic Level High	V_{OH}	V_{DD} – 1.08	—	—	V	R_L = 50Ω
Output Logic Level Low	V_{OL}	—	—	V_{DD} – 1.55		
Peak to Peak Output Swing	—	—	800	—	mV	Single-Ended
Output Rise/Fall Time	t_r	—	250	—	ps	20% to 80%, R_L = 50Ω
	t_f					
Frequency	f_0	2.3	—	460	MHz	Single Frequency
Output Duty Cycle	SYM	48	—	52	%	Differential
Period Jitter (Note 5)	J_{PER}	—	2.5	—	ps_{RMS}	f_{01} = 125 MHz
Integrated Phase Noise	J_{CC}	—	0.25	—	ps_{RMS}	200 kHz to 20 MHz @ 156.25 MHz
		—	0.38	—		100 kHz to 20 MHz @ 156.25 MHz
		—	1.7	2		12 kHz to 20 MHz @ 156.25 MHz

Note 1: Pin 4 V_{DD} should be filtered with 0.01 µF capacitor.

2: Output is enabled if Enable pad is floated or not connected

3: t_{SU} is time to stable output frequency after V_{DD} is applied and outputs are enabled.

4: Output Waveform and Test Circuit figures define the parameters.

5: Period Jitter include crosstalk from adjacent output.

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, T = +25°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
HCSL Outputs						
Output Logic Level High	V_{OH}	0.725	—	—	V	R_L = 50Ω
Output Logic Level Low	V_{OL}	—	—	0.1		
Peak to Peak Output Swing	—	—	750	—	mV	Single-Ended
Output Rise/Fall Time (Note 4)	t_r / t_f	200	—	400	ps	20% to 80%, R_L = 50Ω, C_L = 2 pF
Frequency	f_0	2.3	—	460	MHz	Single Frequency
Output Duty Cycle	SYM	48	—	52	%	Differential
Period Jitter (Note 5)	J_{PER}	—	2.8	—	ps_{RMS}	f_{01} = f_{02} = 125 MHz
Integrated Phase Noise	J_{PH}	—	0.25	—	ps_{RMS}	200 kHz to 20 MHz @ 156.25 MHz
		—	0.37	—		100 kHz to 20 MHz @ 156.25 MHz
		—	1.7	2		12 kHz to 20 MHz @ 156.25 MHz

Note 1: Pin 4 V_{DD} should be filtered with 0.01 µF capacitor.

2: Output is enabled if Enable pad is floated or not connected

3: t_{SU} is time to stable output frequency after V_{DD} is applied and outputs are enabled.

4: Output Waveform and Test Circuit figures define the parameters.

5: Period Jitter include crosstalk from adjacent output.

TEMPERATURE SPECIFICATIONS (Note 1)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Junction Operating Temperature	T_J	—	—	+150	°C	—
Ambient Operating Temperature	T_A	–40	—	+105	°C	Automotive Grade 2
Ambient Operating Temperature	T_A	–40	—	+85	°C	Automotive Grade 3
Storage Ambient Temperature Range	T_A	–55	—	+150	°C	—
Soldering Temperature	T_S	—	+260	—	°C	40 sec. max.

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +150°C rating. Sustained junction temperatures above +150°C can impact the device reliability.

2.0 TYPICAL OPERATING CHARACTERISTICS

Unless specified otherwise, T = +25°C, V_{DD} = 3.3V

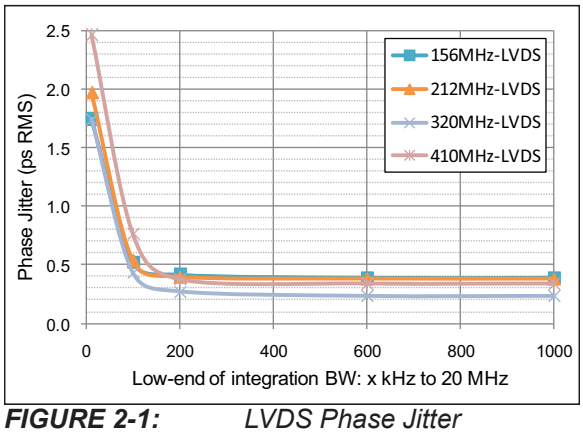


FIGURE 2-1: *LVDS Phase Jitter (Integrated Phase Noise).*

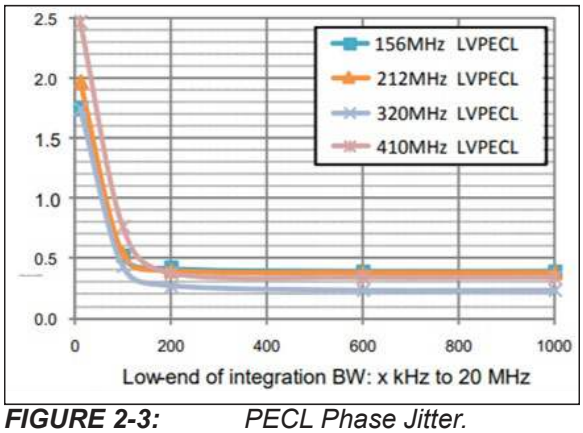


FIGURE 2-3: *PECL Phase Jitter.*

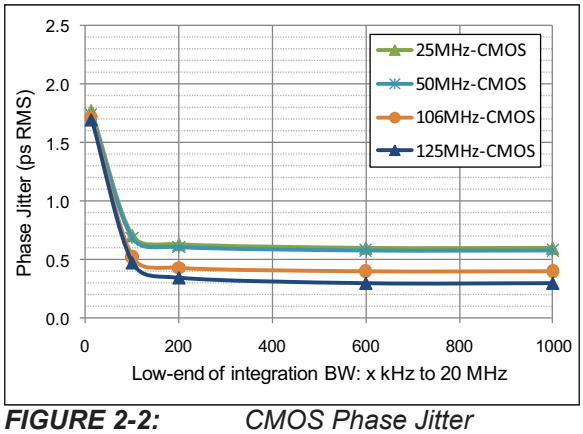


FIGURE 2-2: *CMOS Phase Jitter (Integrated Phase Noise).*

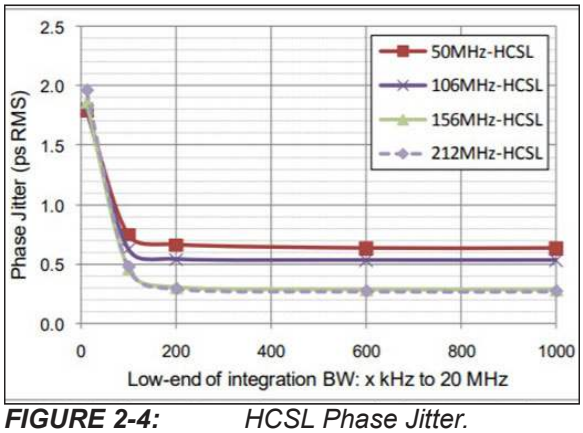


FIGURE 2-4: *HCSL Phase Jitter.*

3.0 OPERATIONAL DESCRIPTION

The DSA20xx are a family of dual output oscillators consisting of a MEMS resonator and a support PLL IC. The two outputs can be any LVPECL/LVDS/HCSL/LVCMOS combination. The “xx” represent the Output 1 and Output 2 logics. For example, DSA2031 offers LVDS-CMOS, DSA2032 offers LVPECL-LVDS, DSA2033 offers LVDS-LVDS, and DSA2030 offers a single LVDS output. The two outputs are generated through independent 8-bit programmable dividers from the output of the internal PLL. Two constraints are imposed on the output frequencies:

- $f_2 = M \times f_1/N$; where M and N are even integers between 4 and 254.
- $1.2\ GHz < N \times f_2 < 1.7\ GHz$

The actual frequencies output by the DSA20xx are controlled by an internal pre-programmed memory (OTP). This memory stores all coefficients required by the PLL for up to eight different frequency combinations. Three control pins (FS0, FS1, FS2) select the output frequency combination. Microchip supports customer-defined versions of the DSA20xx. Standard frequency options are described in the following sections.

The DSA20xx provides control of the output voltage levels of the CMOS output. VDD2 (pin 12) sets the high voltage level of Output 2 and must be equal to or less than VDD at all times to ensure proper operation. VDD2 can be as low as 1.65V.

When Enable (pin 1) is floated or connected to VDD, the DSA20xx is in operational mode. Driving Enable to ground will tri-state both output drivers (high-impedance mode).

The DSA20xx have programmable output drive strength for CMOS output. Using three control pins (OS0, OS1, OS2), the drive strength for the CMOS output can be adjusted to match circuit board impedances to reduce power supply noise, overshoot/undershoot, and EMI. Table 3-1 displays typical rise/fall times for the output with a 15 pF load capacitance as a function of these control pins at V_{DD} = 3.3V and at room temperature.

TABLE 3-1: RISE/FALL TIMES FOR DRIVE STRENGTHS

	Output Drive Strength Bits [OS0, OS1, OS2] – Default is 111							
	000	**001**	**010**	**011**	**100**	**101**	**110**	**111**
t_r	2.1 ns	1.7 ns	1.6 ns	1.4 ns	1.3 ns	1.3 ns	1.2 ns	1.1 ns
t_f	2.5 ns	2.4 ns	2.4 ns	2.0 ns	1.8 ns	1.6 ns	1.3 ns	1.3 ns

3.1 Output Clock Frequencies

Table 3-2 lists the standard frequency configurations and the associated ordering information to be used in conjunction with the ordering information in the Product Identification System section. Customer-defined combinations are available.

TABLE 3-2: PRE-PROGRAMMED PIN-SELECTABLE OUTPUT FREQUENCY COMBINATIONS

Ordering Code	Freq. (MHz)	Frequency Select Bits [FS0, FS1, FS2] – Default is 111							
		000	**001**	**010**	**011**	**100**	**101**	**110**	**111**
J0001	f_{OUT1}	148.25	74.25	156.25	150	125	125	100	100
	f_{OUT2}	74.25	74.25	125	125	25	50	50	75
J000X	f_{OUT1}	Contact Microchip for additional configurations.							
	f_{OUT2}								

Frequency select bits are weakly tied high. So if they are left unconnected, the default setting will be [111] and the device will output the associated frequencies in the table above.

4.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 4-1 and Table 4-2.

TABLE 4-1: DSA20XX PIN FUNCTION TABLE (GLOBAL)

Pin Number	Pin Name	Pin Type	Description
1	Enable	I	Enables all outputs when high and disables (tri-state) them when low.
2	NC	N/A	Leave unconnected or grounded.
3	O2S0/OS0/NC	I	Least significant bit for output strength selection for LVCMOS Output 2/Leave unconnected or grounded.
4	GND	Power	Ground.
5	FS0	I	Least significant bit for frequency selection.
6	FS1	I	Middle bit for frequency selection.
7	FS2/NC	I	Most significant bit for frequency selection/Leave unconnected or grounded.
8	Output1/Output1+	O	LVCMOS Output 1/True Output 1 for differential output.
9	O1SO/OS0/Output1–	I/O	Least significant bit for output strength selection for LVCMOS Output 1/Complementary Output 1 for differential output.
10	O1S1/OS1/Output2–/NC	I/O	Middle bit for output strength selection for LVCMOS Output/Complementary Output2 for differential output/Leave unconnected or grounded.
11	Output2/Output2+/NC	O	LVCMOS Output 2/True Output2 for differential output/Leave unconnected or grounded.
12	VDD2/VDD	Power	Power supply for Output 2/Connect to Power supply for configuration with only Output 1.
13	VDD	Power	Power supply.
14	O2S1/OS2/NC	I	Most significant bit for output strength selection for LVCMOS Output/Leave unconnected or grounded.
15	ePAD	Power	Connect to GND.

TABLE 4-2: PIN FUNCTION TABLE (SPECIFIC)

Pin No.	Part Number						
—	**DSA2010**	**DSA2011**	**DSA2020**	**DSA2021**	**DSA2022**	**DSA2023**	**DSA2024**
Output 1	**LVCMOS**	**LVCMOS**	**LVPECL**	**LVPECL**	**LVPECL**	**LVPECL**	**LVPECL**
Output 2	**OFF**	**LVCMOS**	**OFF**	**LVCMOS**	**LVPECL**	**LVDS**	**HCSL**
1	Enable	Enable	Enable	Enable	Enable	Enable	Enable
2	NC	NC	NC	NC	NC	NC	NC
3	NC	O2S0	NC	OS0	NC	NC	NC
4	GND	GND	GND	GND	GND	GND	GND
5	FS0	FS0	FS0	FS0	FS0	FS0	FS0
6	FS1	FS1	FS1	FS1	FS1	FS1	FS1
7	NC	FS2	NC	FS2	FS2	FS2	FS2
8	Output1	Output1	Output1+	Output1+	Output1+	Output1+	Output1+
9	OS0	O1S0	Output1–	Output1–	Output1–	Output1–	Output1–
10	OS1	O1S1	NC	OS1	Output2–	Output2–	Output2–
11	NC	Output2	NC	Output2	Output2+	Output2+	Output2+
12	VDD	VDD2	VDD	VDD2	VDD2	VDD2	VDD2
13	VDD	VDD	VDD	VDD	VDD	VDD	VDD
14	OS2	O2S1	NC	OS2	NC	NC	NC
15	ePad	ePad	ePad	ePad	ePad	ePad	ePad
—	**DSA2030**	**DSA2031**	**DSA2033**	**DSA2040**	**DSA2041**	**DSA2043**	**DSA2044**
Output 1	**LVDS**	**LVDS**	**LVDS**	**HCSL**	**HCSL**	**HCSL**	**HCSL**
Output 2	**OFF**	**LVCMOS**	**LVDS**	**OFF**	**LVCMOS**	**LVDS**	**HCSL**
1	Enable	Enable	Enable	Enable	Enable	Enable	Enable
2	NC	NC	NC	NC	NC	NC	NC
3	NC	OS0	NC	NC	OS0	NC	NC
4	GND	GND	GND	GND	GND	GND	GND
5	FS0	FS0	FS0	FS0	FS0	FS0	FS0
6	FS1	FS1	FS1	FS1	FS1	FS1	FS1
7	NC	FS2	FS2	NC	FS2	FS2	FS2
8	Output1+	Output1+	Output1+	Output1+	Output1+	Output1+	Output1+
9	Output1–	Output1–	Output1–	Output1–	Output1–	Output1–	Output1–
10	NC	OS1	Output2–	NC	OS1	Output2–	Output2–
11	NC	Output2	Output2+	NC	Output2	Output2+	Output2+
12	VDD	VDD2	VDD2	VDD	VDD2	VDD2	VDD2
13	VDD	VDD	VDD	VDD	VDD	VDD	VDD
14	NC	OS2	NC	NC	OS2	NC	NC
15	ePad	ePad	ePad	ePad	ePad	ePad	ePad

Please visit the ClockWorks® Configurator website at http://clockworks.microchip.com/timing to configure the part number for the eight customer-defined frequencies.

5.0 TERMINATION SCHEMES

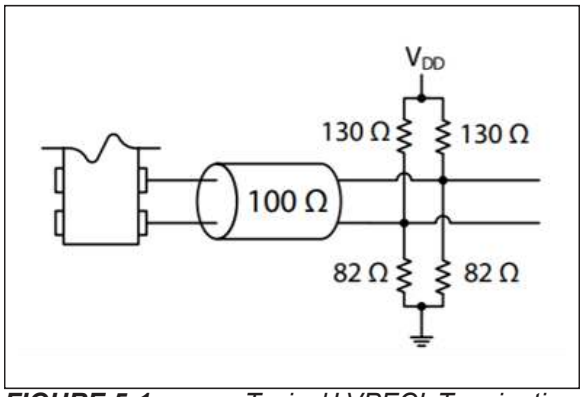


FIGURE 5-1: *Typical LVPECL Termination Scheme.*

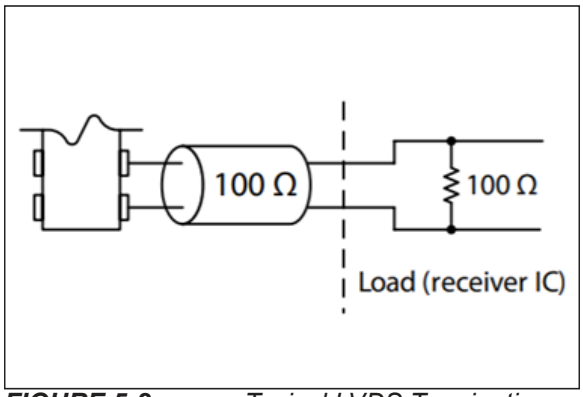


FIGURE 5-2: *Typical LVDS Termination Scheme.*

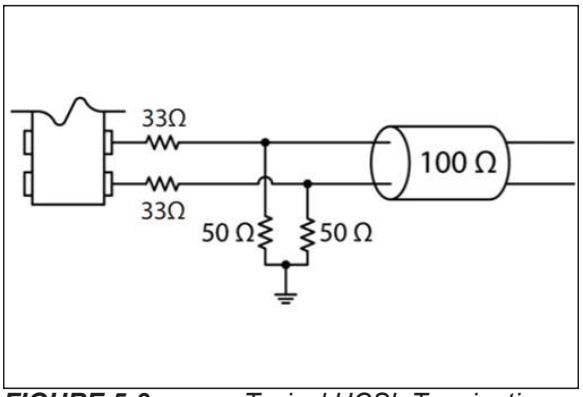


FIGURE 5-3: *Typical HCSL Termination Scheme.*

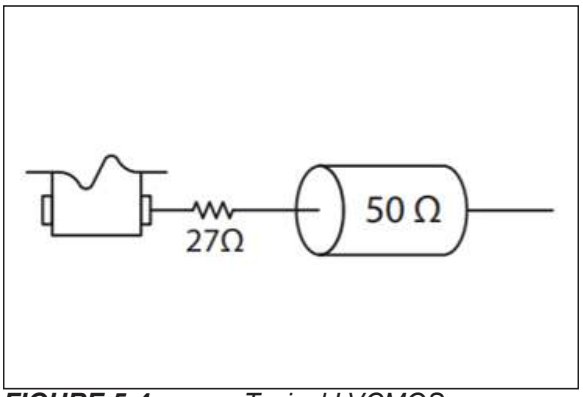


FIGURE 5-4: *Typical LVCMOS Termination Scheme.*

6.0 DIAGRAMS

Unless otherwise specified, T = +25°C, V_{DD} = 3.3V.

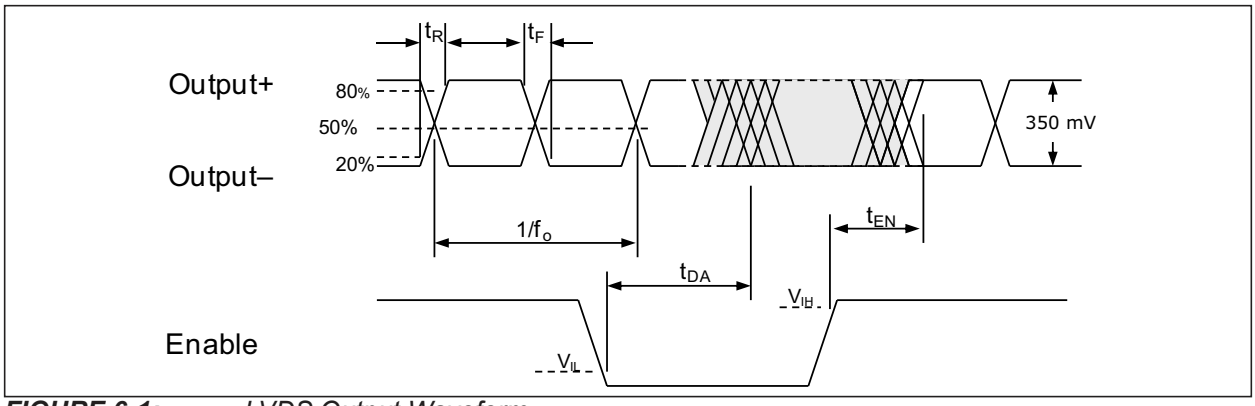


FIGURE 6-1: *LVDS Output Waveform.*

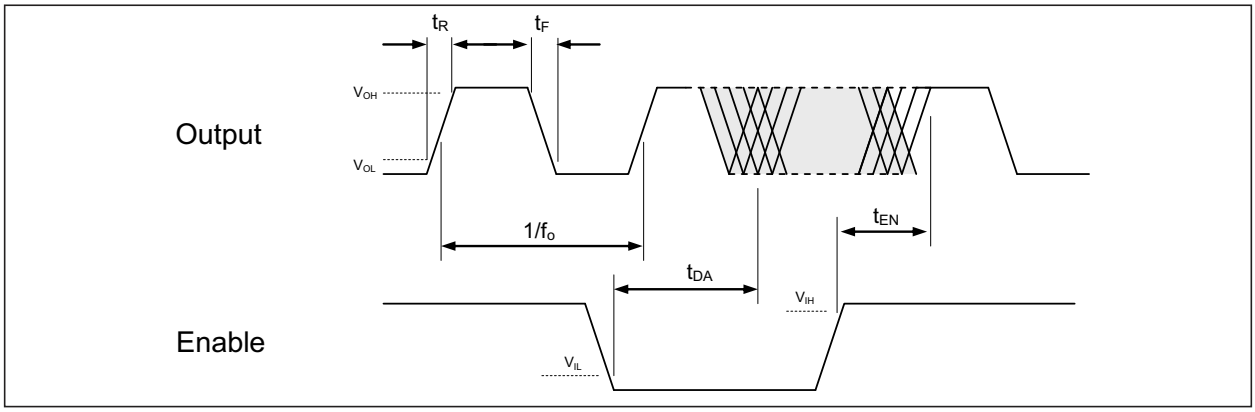


FIGURE 6-2: *CMOS Output Waveform.*

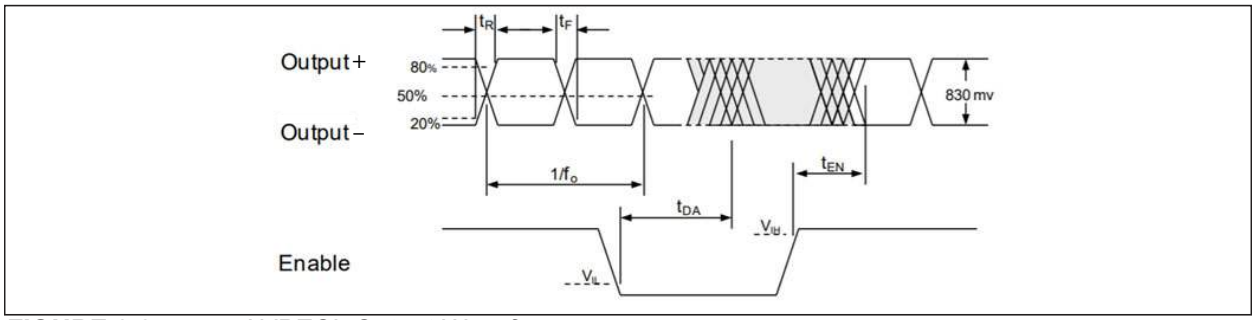


FIGURE 6-3: *LVPECL Output Waveform.*

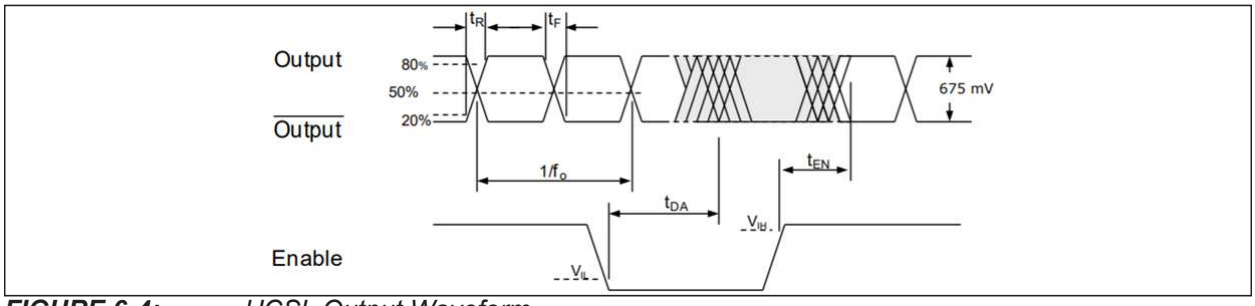


FIGURE 6-4: *HCSL Output Waveform.*

7.0 SOLDER REFLOW PROFILE

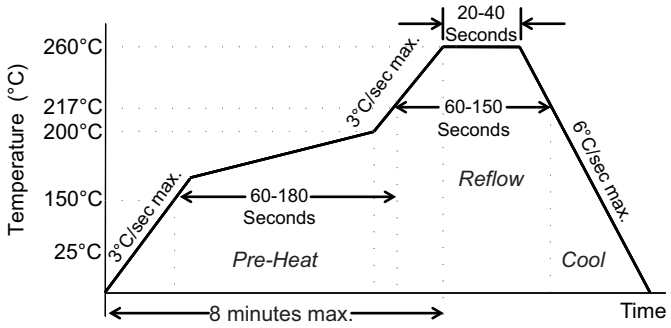


FIGURE 7-1: *Solder Reflow Profile.*

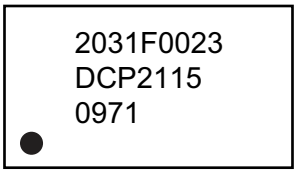
MSL 1 @ 260°C refer to JSTD-020C	
Ramp-Up Rate (200°C to Peak Temp)	3°C/sec. max.
Preheat Time 150°C to 200°C	60 to 180 sec.
Time maintained above 217°C	60 to 150 sec.
Peak Temperature	255°C to 260°C
Time within 5°C of actual Peak	20 to 40 sec.
Ramp-Down Rate	6°C/sec. max.
Time 25°C to Peak Temperature	8 minutes max.

8.0 PACKAGING INFORMATION

8.1 Package Marking Information

14-Lead QFN*

Example

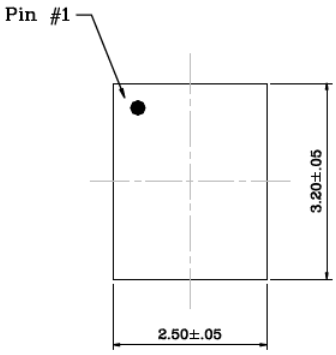


Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	SSS	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar (_) and/or Overbar (¯) symbol may not be to scale.	

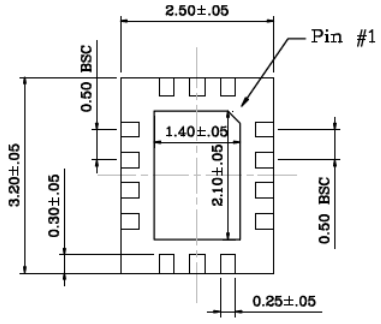
14-Lead 3.2 mm x 2.5 mm QFN Package Outline and Recommended Land Pattern

TITLE
14 LEAD QFN 2.5x3.2mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	QFN2532-14LD-PL-1	UNIT	MM

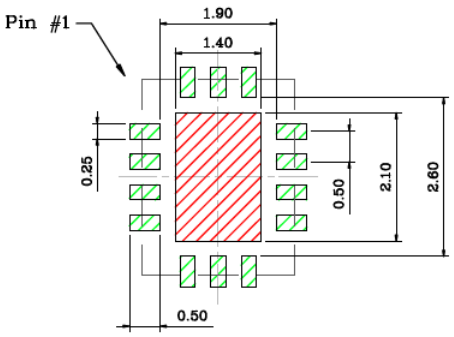


Top View



Bottom View

Side View



Recommended Land Pattern

NOTE:
1. Green shaded rectangles in Recommended Land Pattern are solder stencil opening.
2. Red shaded rectangle in Recommended Land Pattern is keep out area.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

APPENDIX A: REVISION HISTORY

Revision A (July 2020)

- Initial release of DSA20xx Microchip data sheet DS20006384A.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

Part No.	X	X	X	-XXXXX	X	XXX
Device	Package	Temp. Range	Freq. Stability	Frequency	Media Type	Automotive Suffix

Device: DSA20xx:

X	Output 1	Output 2
0	OFF	OFF
1	LVCMOS	LVCMOS
2	LVPECL	LVPECL
3	LVDS	LVDS
4	HCSL	HCSL

Package: F = 14-Lead 3.2 mm x 2.5 mm QFN

Temperature Range: L = –40°C to +105°C (Automotive Grade 2)
I = –40°C to +85°C (Automotive Grade 3)

Frequency Stability: 1 = ± 50 ppm
2 = ± 25 ppm

Frequency: xxxxx = User-Defined in the ClockWorks Configurator.

Media Type: <blank>= 110/Tube
T = 1,000/Reel

Automotive Suffix: Vxx = Automotive suffix in which “xx” is assigned by Microchip. Default value is “AO” for the standard automotive part.

Please visit Microchip’s ClockWorks® Configurator Website to configure the part number for customized frequency. http://clockworks.microchip.com/timing/.

Examples:

a) DSA2031FL2-F0023VAO:
Output 1 = LVDS; Output 2 = LVCMOS, 14-Lead QFN, –40°C to +105°C Temperature Range, ±25 ppm Stability, 110/Tube, Standard Automotive

b) DSA2011FI1-F0050TVAO:
Output 1 & Output 2 = LVCMOS, 14-Lead QFN, –40°C to +85°C Temperature Range, ±50 ppm Stability, 1,000/Reel, Standard Automotive

c) DSA2033FI2-F0004TVAO:
Output 1 & Output 2 = LVDS, 14-Lead QFN, –40°C to +85°C Temperature Range, ±25 ppm Stability, 1,000/Reel, Standard Automotive

d) DSA2030FL1-B0020VAO:
Output 1 = LVDS; Output 2 = OFF, 14-Lead QFN, –40°C to +105°C Temperature Range, ±50 ppm Stability, 110/Tube, Standard Automotive

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

Note the following details of the code protection feature on Microchip devices:

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