



PJA3412-AU

20V N-Channel Enhancement Mode MOSFET

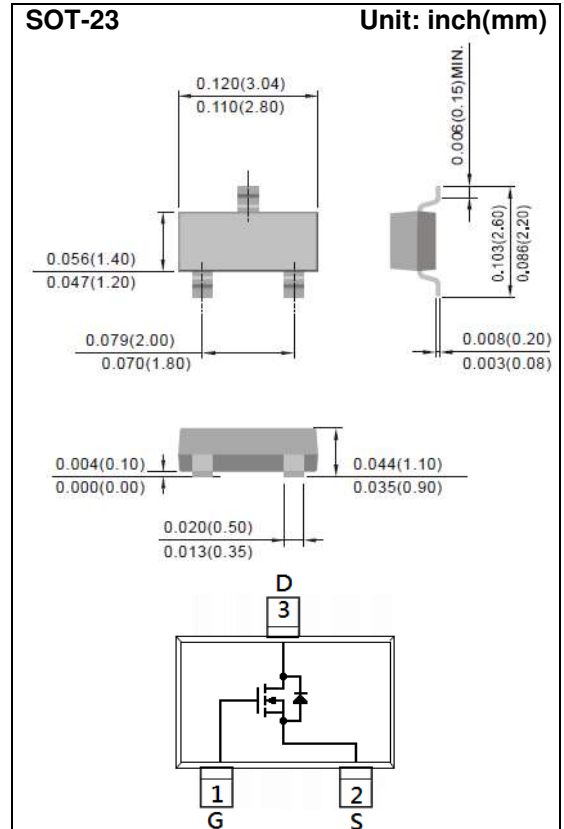
Voltage	20 V	Current	4.1 A
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Features

- $R_{DS(ON)}$, $V_{GS}@4.5V$, $I_D@4.1A < 56m\Omega$
- $R_{DS(ON)}$, $V_{GS}@2.5V$, $I_D@2.8A < 68m\Omega$
- $R_{DS(ON)}$, $V_{GS}@1.8V$, $I_D@1.5A < 95m\Omega$
- Advanced Trench Process Technology
- Specially Designed for Switch Load, PWM Application, etc
- AEC-Q101 qualified
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

Mechanical Data

- Case: SOT-23 Package
- Terminals: Solderable per MIL-STD-750, Method 2026
- Approx. Weight: 0.0003 ounces, 0.0084 grams



Maximum Ratings and Thermal Characteristics ($T_A=25^\circ C$ unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNITS
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	± 12	
Continuous Drain Current		I_D	4.1	A
Pulsed Drain Current		I_{DM}	16.4	
Power Dissipation	$T_a=25^\circ C$	P_D	1.25	W
	Derate above $25^\circ C$		10	mW/ $^\circ C$
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55~150	$^\circ C$
Typical Thermal Resistance		$R_{\theta JA}$	100	$^\circ C/W$
- Junction to Ambient ^(Note 3)				



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Electrical Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	20	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	0.4	0.66	1.2	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=4.5V, I_D=4.1A$	-	41	56	mΩ
		$V_{GS}=2.5V, I_D=2.8A$	-	50	68	
		$V_{GS}=1.8V, I_D=1.5A$	-	66	95	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=20V, V_{GS}=0V$	-	-	1	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 12V, V_{DS}=0V$	-	-	± 100	nA
Dynamic (Note 5)						
Total Gate Charge	Q_g	$V_{DS}=10V, I_D=4.1A,$ $V_{GS}=4.5V$ (Note 1,2)	-	4.6	-	nC
Gate-Source Charge	Q_{gs}		-	0.8	-	
Gate-Drain Charge	Q_{gd}		-	1	-	
Input Capacitance	C_{iss}	$V_{DS}=10V, V_{GS}=0V,$ $f=1.0MHz$	-	350	-	pF
Output Capacitance	C_{oss}		-	40	-	
Reverse Transfer Capacitance	C_{rss}		-	29	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD}=10V, I_D=4.1A,$ $V_{GS}=4.5V,$ $R_G=6\Omega$ (Note 1,2)	-	4	-	ns
Turn-On Rise Time	t_r		-	47	-	
Turn-Off Delay Time	$t_{d(off)}$		-	18	-	
Turn-Off Fall Time	t_f		-	10	-	
Drain-Source Diode						
Maximum Continuous Drain-Source Diode Forward Current	I_S	---	-	-	1.5	A
Diode Forward Voltage	V_{SD}	$I_S=1.0A, V_{GS}=0V$	-	0.75	1.2	V

NOTES :

1. Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$.
2. Essentially independent of operating temperature typical characteristics.
3. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins mounted on a 1 inch FR-4 with 2oz. square pad of copper.
4. The maximum current rating is package limited.
5. Guaranteed by design, not subject to production testing.



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TYPICAL CHARACTERISTIC CURVES

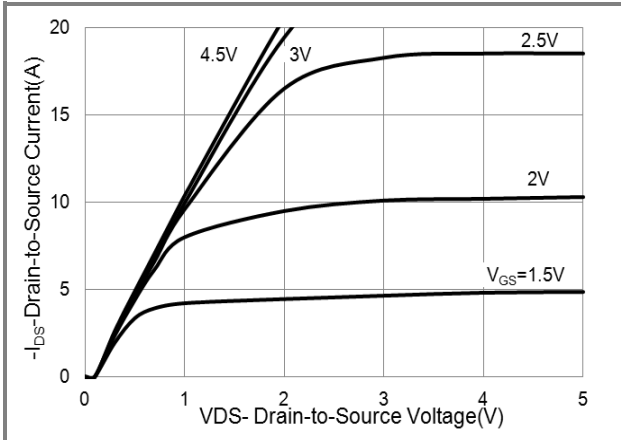


Fig.1 On-Region Characteristics

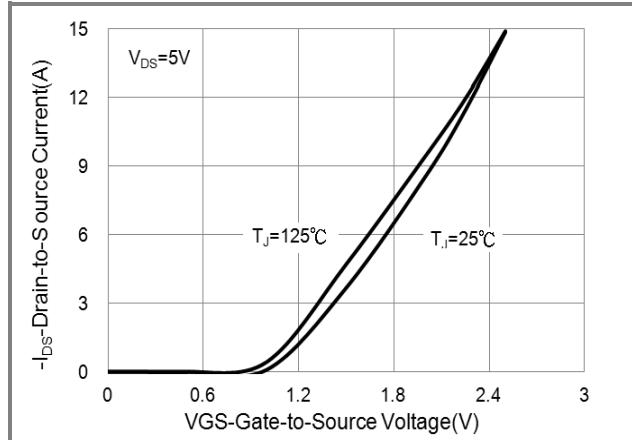


Fig.2 Transfer Characteristics

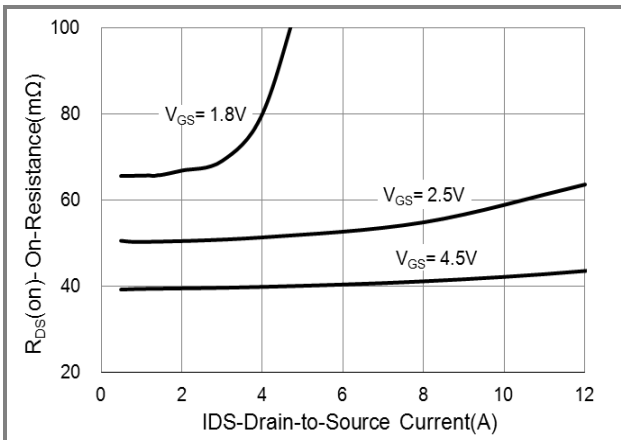


Fig.3 On-Resistance vs. Drain Current

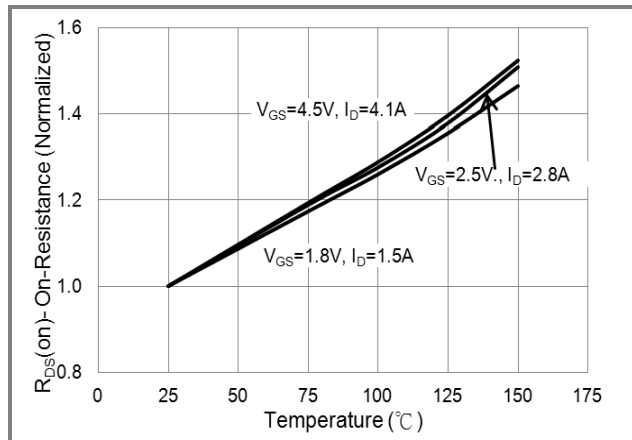


Fig.4 On-Resistance vs. Junction temperature

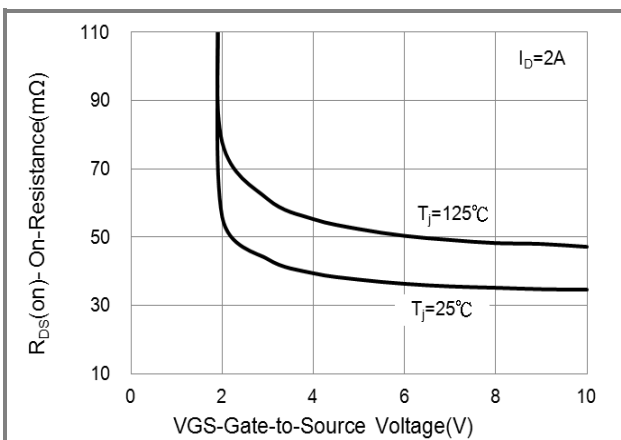


Fig.5 On-Resistance Variation with V_{GS}

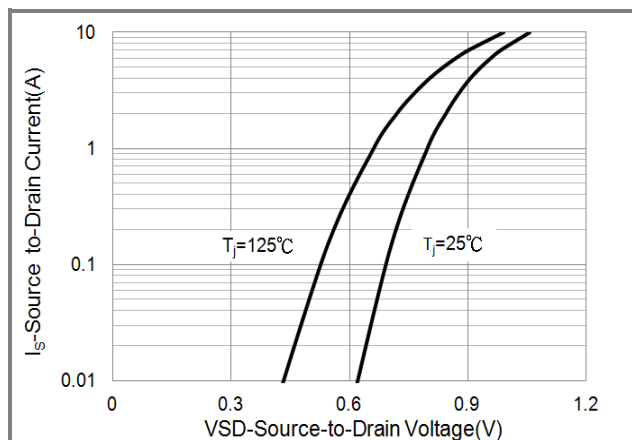


Fig.6 Body Diode Characteristics



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TYPICAL CHARACTERISTIC CURVES

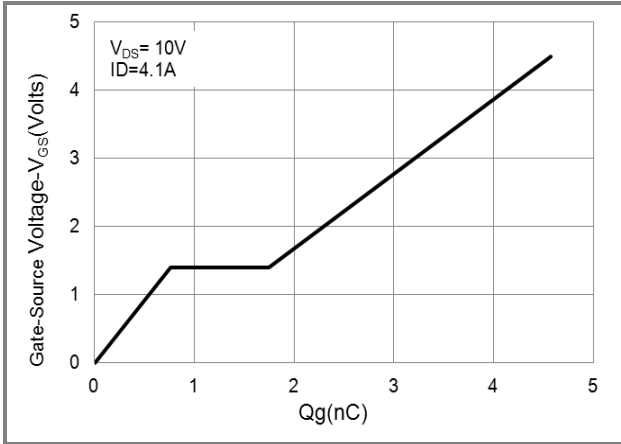


Fig.7 Gate-Charge Characteristics

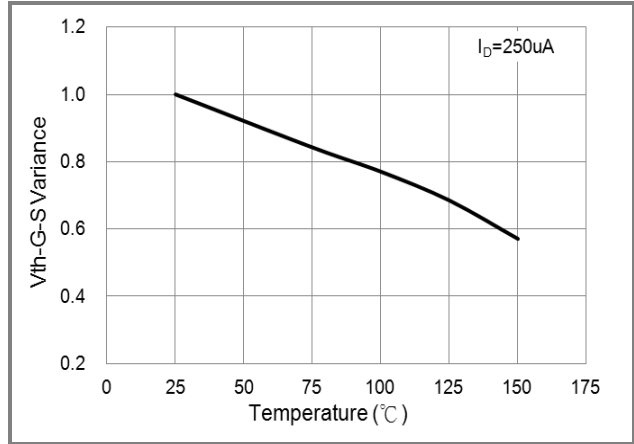


Fig.8 Threshold Voltage Variation with Temperature

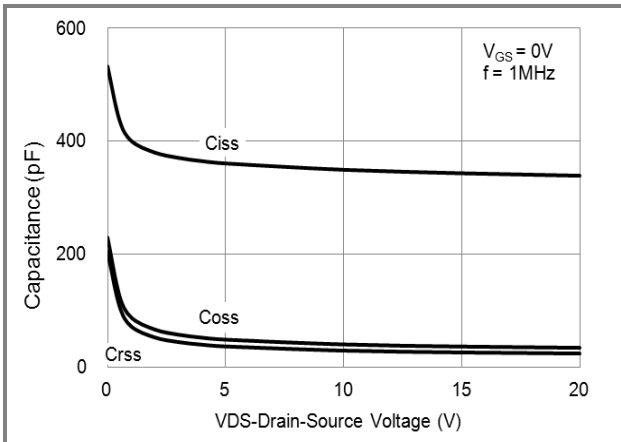


Fig.9 Capacitance vs. Drain-Source Voltage

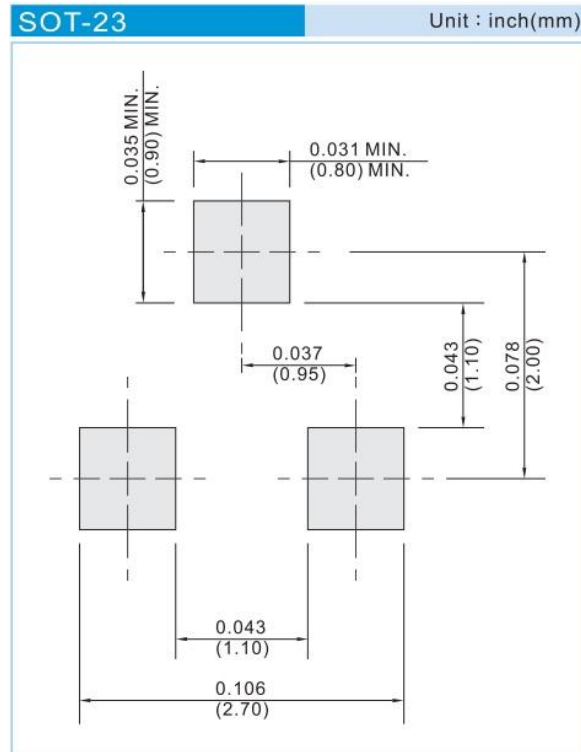


PJA3412-AU

Part No Packing Code Version

Part No Packing Code	Package Type	Packing Type	Marking	Version
PJA3412-AU_R1_000A1	SOT-23	3K pcs / 7" reel	A12	Halogen free

Mounting Pad Layout





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