QUALITY SEMICONDUCTOR, INC.

High-Speed CMOS 8-Bit Bus Interface Register Transceivers

QS29FCT52T
QS29FCT53T
QS29FCT2052T

FEATURES/BENEFITS

- Pin and function compatible to the Am2952/3 29FCT52/53 and 29FCT52/53T
- Industrial temperature –40°C to 85°C
- CMOS power levels: <7.5mW static
- Available in DIP, ZIP, SOIC, QSOP, HQSOP
- Undershoot clamp diodes on all inputs
- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Military product compliant to MIL-STD-883, Class B

FCT-T 2952T, 2953T

- JEDEC-FCT spec compatible
- A, B, and C speed grades with 5.5ns t_{PD} for C
- I_{OL} = 64mA Ind., 48mA Mil.

FCT-T 2052T

- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- A, B, and C speed grades with 5.5ns t_{PD} for C speed guaranteed with 50pF loads

DESCRIPTION

The QS29FCT52/53T are 8-bit high-speed CMOS TTL-compatible registered bus transceivers with three-state outputs that are ideal for driving high capacitance loads such as memory and address buses. The QS29FCT2052T device is a 25Ω resistor output version useful for driving transmission lines and reducing system noise. The FCT2052 series part can replace the FCT52/FCT53 series to reduce noise in an existing design. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression, and will not load an active bus when V_{CC} is removed from the device.

Figure 1. Functional Block Diagram

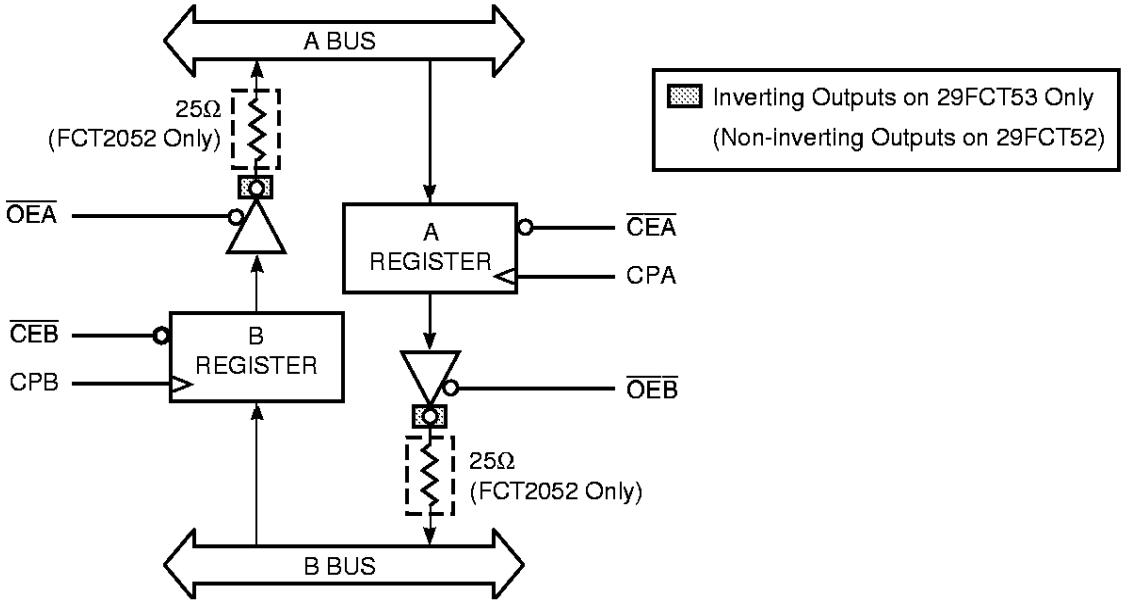
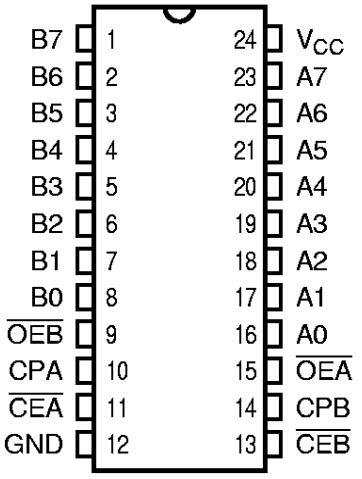


Figure 2. Pin Configurations (All Pins Top View)

PDIP, SOIC, QSOP, HQSOP



ZIP

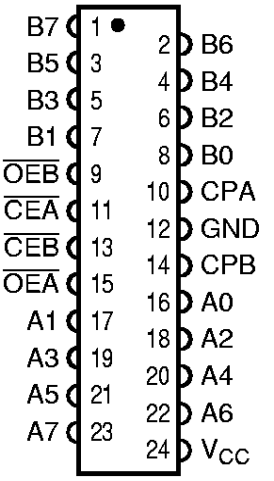


Table 1. Pin Description

Name	I/O	Description
A7-A0	I/O	A Bus
B7-B0	I/O	B Bus
CPA	I	Register A Clock Input
CPB	I	Register B Clock Input
$\overline{CEA}$	I	Register A Clock Enable
$\overline{CEB}$	I	Register B Clock Enable
$\overline{OEA}$	I	Output Enable, Reg. B to Bus A
$\overline{OEB}$	I	Output Enable, Reg. A to Bus B

Table 2. Function Tables

Inputs						Outputs	
CPA	CPB	$\overline{CEA}$	$\overline{CEB}$	$\overline{OEA}$	$\overline{OEB}$	A7-A0	B7-B0
X	X	X	X	H	L	Hi-Z	Reg. A
X	X	X	X	L	H	Reg. B	Hi-Z
X	X	X	X	H	H	Hi-Z	Hi-Z
X	X	X	X	L	L	Reg. B	Reg. A

Inputs				Outputs	
CPA	CPB	$\overline{CEA}$	$\overline{CEB}$	A7-A0	B7-B0
X	X	H	H	Hold	Hold
↑	X	L	H	Load	Hold
X	↑	H	L	Hold	Load
X	↑	L	L	X	Load
↑	X	L	L	Load	X

Table 3. Absolute Maximum Ratings

Supply Voltage to Ground	–0.5V to 7.0V
DC Output Voltage V_{OUT}	–0.5V to 7.0V
DC Input Voltage V_{IN}	–0.5V to 7.0V
AC Input Voltage (for a pulse width ≤ 20ns)	–3.0V
DC Input Diode Current with $V_{IN} < 0$	–20mA
DC Output Diode Current with $V_{OUT} < 0$	–50mA
DC Output Current Max. Sink Current/Pin	120mA
Maximum Power Dissipation	0.5 watts
T_{STG} Storage Temperature	–65° to 150°C

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to this device resulting in functional or reliability type failures.

Table 4. Capacitance(1)

T_A = 25°C, f = 1MHz, V_{IN} = 0V, V_{OUT} = 0V

Pins(2)	SOIC	QSOP	PDIP	ZIP	Unit
1-11, 13-23	8	8	9	10	pF

Notes:
1. Capacitance is characterized but not tested.
2. Pin reference for 24-pin package.

Table 5. DC Electrical Characteristics Over Operating Range

Industrial T_A = –40°C to 85°C, V_{CC} = 5.0V ±5% Military T_A = –55°C to 125°C, V_{CC} = 5.0V ±10%

Symbol	Parameter	Test Conditions	Min	Typ(1)	Max	Unit
V_{IH}	Input HIGH Voltage	Logic HIGH for All Inputs	2.0	—	—	V
V_{IL}	Input LOW Voltage	Logic LOW for All Inputs	—	—	0.8	V
ΔV_T	Input Hysteresis	$V_{TLH} - V_{THL}$ for All Inputs	—	0.2	—	V
$\lvert I_{IH} \rvert$ $\lvert I_{IL} \rvert$	Input Current Input HIGH or LOW	V_{CC} = Max., $0 \le V_{IN} < V_{CC}$	—	—	5	µA
$\lvert I_{OZ} \rvert$	Off-State Output Current (Hi-Z)	V_{CC} = Max., $0 \le V_{IN} \le V_{CC}$	—	—	5	µA
I_{OS}	Short Circuit Current (FCTXXX)	V_{CC} = Max., V_{OUT} = GND(2,3)	–60	—	—	mA
I_{OR}	Current Drive (FCT2XXX – 25Ω)	V_{CC} = Max., V_{OUT} = 2.0V(3)	50	—	—	mA
V_{IC}	Input Clamp Voltage	V_{CC} = Min., I_{IN} = –18mA, T_A = 25°C(3)	—	–0.7	–1.2	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –12mA (MIL) I_{OH} = –15mA (IND)	2.4 2.4	— —	— —	V
V_{OL}	Output LOW Voltage (FCTXXX)	V_{CC} = Min., I_{OL} = 48mA (MIL) I_{OL} = 64mA (IND)	— —	— —	0.55 0.55	V
V_{OL}	Output LOW Voltage (FCT2XXX – 25Ω)	V_{CC} = Min., I_{OL} = 12mA (MIL) I_{OL} = 12mA (IND)	— —	— —	0.50 0.50	V
R_{OUT}	Output Resistance (FCT2XXX – 25Ω)	V_{CC} = Min., I_{OL} = 12mA (MIL) I_{OL} = 12mA (IND)	— 20	25 28	— 40	Ω

Notes:
1. Typical values indicate V_{CC} = 5.0V and T_A = 25°C.
2. Not more than one output should be shorted and the duration is ≤1 second.
3. These parameters are guaranteed by design but not tested.

Table 6. Power Supply Characteristics

Symbol	Parameter	Test Conditions[1]	Min	Max	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., freq = 0 0V ≤ V_{IN} ≤ 0.2V or V_{CC}-0.2V ≤ V_{IN} ≤ V_{CC}	—	1.5	mA
ΔI_{CC}	Supply Current per Input @ TTL HIGH	V_{CC} = Max., V_{IN} = 3.4V, freq = 0[2]	—	2.0	mA
Q_{CCD}	Supply Current per Input per MHz	V_{CC} = Max., Outputs Open and Enabled One Bit Toggling @ 50% Duty Cycle Other Inputs at GND or V_{CC}[3,4]	—	0.25	mA/ MHz

Notes:
1. For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
2. Per TTL driven input (V_{IN} = 3.4V).
3. For flip-flops, Q_{CCD} is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4. I_C can be computed using the above parameters as explained in the Technical Overview section.

Table 7. Switching Characteristics Over Operating Range

Industrial T_A = –40°C to 70°C, V_{CC} = 5.0V ±5% Military T_A = –55°C to 125°C, V_{CC} = 5.0V ±10%
C_{LOAD} = 50pF, R_{LOAD} = 500Ω unless otherwise noted.

Symbol	Description		52/53A 2052A Min	52/53A 2052A Max	52/53B 2052B Min	52/53B 2052B Max	52/53C 2052C Min	52/53C 2052C Max	Unit
t_{PHL}	Propagation Delay[1]	Ind	2	10	2	6.5	2	5.8	ns
t_{PLH}	CP to Ai, Bi, 52/53	Mil	2	11	2	7.2	0	6.8	
t_{PHL}	Propagation Delay[1]	Ind	2	10	2	6.5	2	5.8	ns
t_{PLH}	CP to Ai, Bi, 2052	Mil	2	11	2	7.2	0	6.8	
t_{PZH}	Output Enable Time[1]	Ind	1.5	10.5	1.5	6.5	1.5	6.5	ns
t_{PZL}	$\overline{OE}$ to Ai, Bi, 52/53	Mil	1.5	13	1.5	7.5	1.5	7.5	
t_{PZH}	Output Enable Time[1]	Ind	1.5	10.5	1.5	7.0	1.5	7.0	ns
t_{PZL}	$\overline{OE}$ to Ai, Bi, 2052	Mil	1.5	13	1.5	7.5	1.5	7.5	
t_{PHZ}	Output Disable Time[1,2]	Ind	2	10	2	5.5	1.5	5.5	ns
t_{PLZ}	$\overline{OE}$ to Ai, Bi	Mil	2	11	2	6.5	1.5	6.5	
t_S	Data Setup Time	Ind	2	—	2	—	2	—	ns
	Ai, Bi, to CP	Mil	2.5	—	2	—	2	—	
t_H	Data Hold Time	Ind	2	—	1.5	—	1.5	—	ns
	Ai, Bi, to CP	Mil	2	—	1.5	—	1.5	—	
t_{SCE}	Clock Enable Setup	Ind	2	—	2	—	2	—	ns
	Time, $\overline{CE}$ to CP	Mil	2	—	2	—	2	—	
t_{HCE}	Clock Enable Hold	Ind	2	—	2	—	2	—	ns
	Time, $\overline{CE}$ to CP	Mil	2	—	2	—	2	—	
t_W	Clock Pulse Width[2]	Ind	3	—	3	—	3	—	ns
	HIGH or LOW	Mil	3	—	3	—	3	—	

Notes:
1. Minimums guaranteed but not tested.
2. This parameter is guaranteed by design but not tested.
3. See Test Circuit and Waveforms.