CY7C187

64K x 1 Static RAM

Features

- High Speed
  - 25 ns
- CMOS for Optimum Speed and Power
- Low Active Power
  - 385 mW
- Low Standby Power
  - 110 mW
- TTL Compatible Inputs and Outputs
- Automatic Power Down when Deselected
- Available in Pb-free 22-Pin (300-Mil) Molded DIP

Functional Description

The CY7C187 is a high performance CMOS static RAM organized as 65,536 words x 1 bit. Easy memory expansion is provided by an active LOW Chip Enable ($\overline{CE}$) and tristate drivers. The CY7C187 has an automatic power down feature, reducing the power consumption by 56% when deselected.

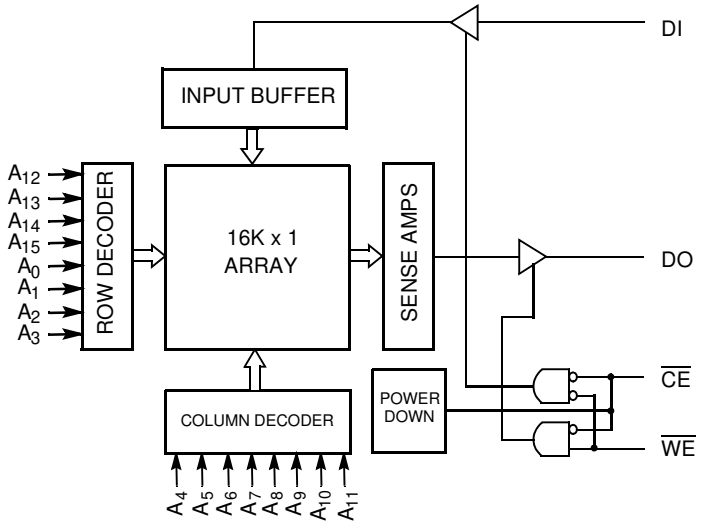
Writing to the device is possible when the Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs are both LOW. Data on the input pin (D_{IN}) is written into the memory location specified on the address pins (A_0 through A_{15}).

Reading the device is possible by taking the Chip Enable ($\overline{CE}$) LOW, while Write Enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified on the address pin appears on the data output (D_{OUT}) pin.

The output pin stays in high impedance state when $\overline{CE}$ is HIGH or $\overline{WE}$ is LOW.

The CY7C187 uses a die coat to insure alpha immunity.

Logic Block Diagram

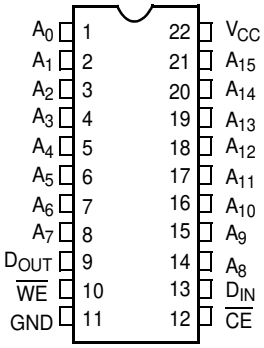


Selection Guide

Description	-25	-35
Maximum Access Time (ns)	25	35
Maximum Operating Current (mA)	70	70
Maximum CMOS Standby Current (mA)	20	20

Pin Configuration

Figure 1. Pin Diagram DIP - Top View



Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. User guidelines are not tested.

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage to Ground Potential (Pin 22 to Pin 11) .....–0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[1] .....–0.5V to +7.0V

DC Input Voltage[1] .....–0.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage..... >2001V (per MIL–STD–883, Method 3015)

Latch Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

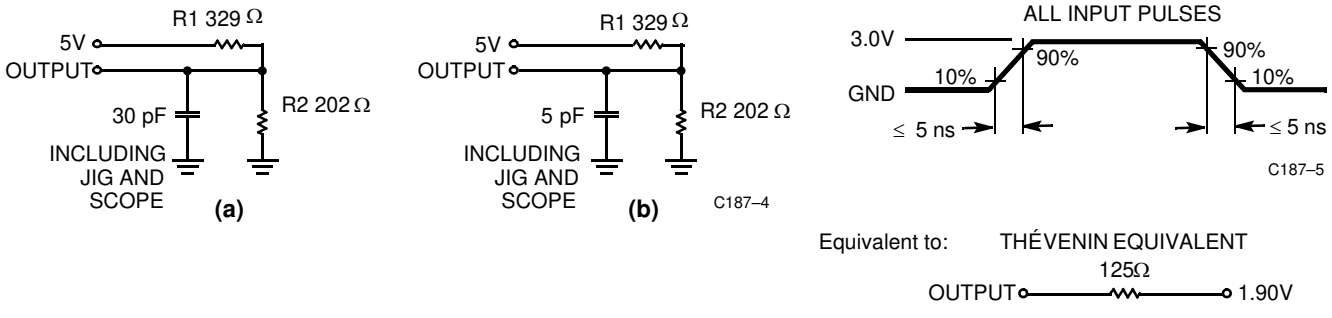
Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	-25 and -35		Unit
			Min	Max	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL}=12.0 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[1]		–0.5	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}	–5	+5	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	–5	+5	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA		70	mA
I_{SB1}	Automatic $\overline{CE}$ Power Down Current[3]	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}		20	mA
I_{SB2}	Automatic $\overline{C}$ Power Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3V, V_{IN} ≥ V_{CC} – 0.3V or V_{IN} ≤ 0.3V		20	mA

Capacitance[4]

Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

Figure 2. AC Test Loads and Waveforms



Notes
1. V_{IL} (min.) = –3.0V for pulse durations less than 30 ns.
2. Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
3. A pull up resistor to V_{CC} on the $\overline{CE}$ input is required to keep the device deselected during V_{CC} power up, otherwise I_{SB} exceeds values given.
4. Tested initially and after any design or process changes that may affect these parameters.

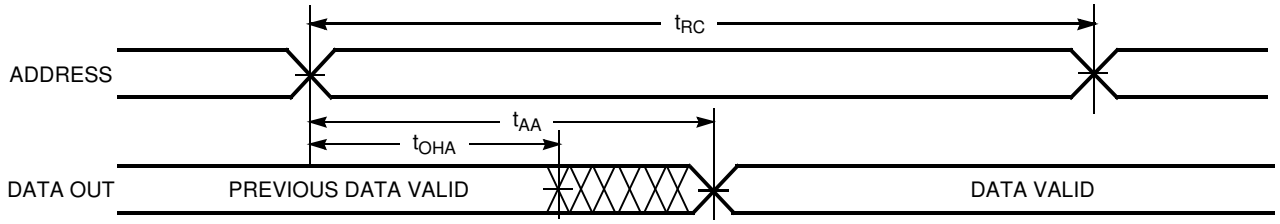
[+] Feedback

Switching Characteristics Over the Operating Range[5]

Parameter	Description	-25		-35		Unit
		Min	Max	Min	Max	
Read Cycle						
t_{RC}	Read Cycle Time	25		35		ns
t_{AA}	Address to Data Valid		25		35	ns
t_{OHA}	Output Hold from Address Change	5		5		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		25		35	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[6]	5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[6,7]		10		15	ns
t_{PU}	$\overline{CE}$ LOW to Power Up	0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power Down		20		20	ns
Write Cycle[8]						
t_{WC}	Write Cycle Time	20		25		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	20		25		ns
t_{AW}	Address Setup to Write End	20		25		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Setup to Write Start	0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	15		20		ns
t_{SD}	Data Setup to Write End	10		15		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7]		7		10	ns

Switching Waveforms

Figure 3. Read Cycle No. 1[9, 10]



Notes
5. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
6. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any device.
7. t_{HZCE} and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads and Waveforms on page 3. Transition is measured ±500 mV from steady-state voltage.
8. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
9. $\overline{WE}$ is HIGH for read cycle.
10. Device is continuously selected, $\overline{CE}$ = V_{IL}.

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Figure 4. Read Cycle No. 2[9, 11]

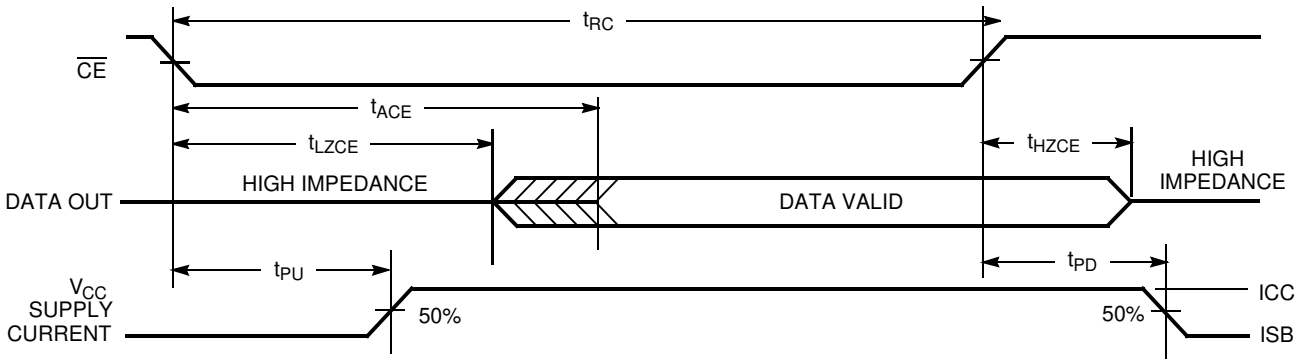


Figure 5. Write Cycle No. 1($\overline{WE}$ Controlled)[11]

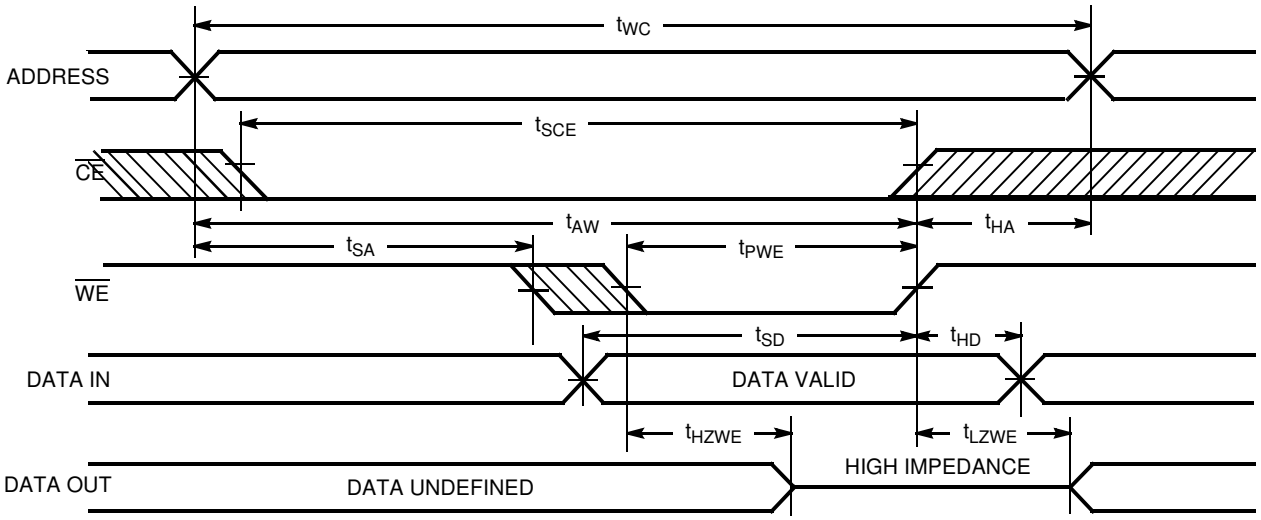
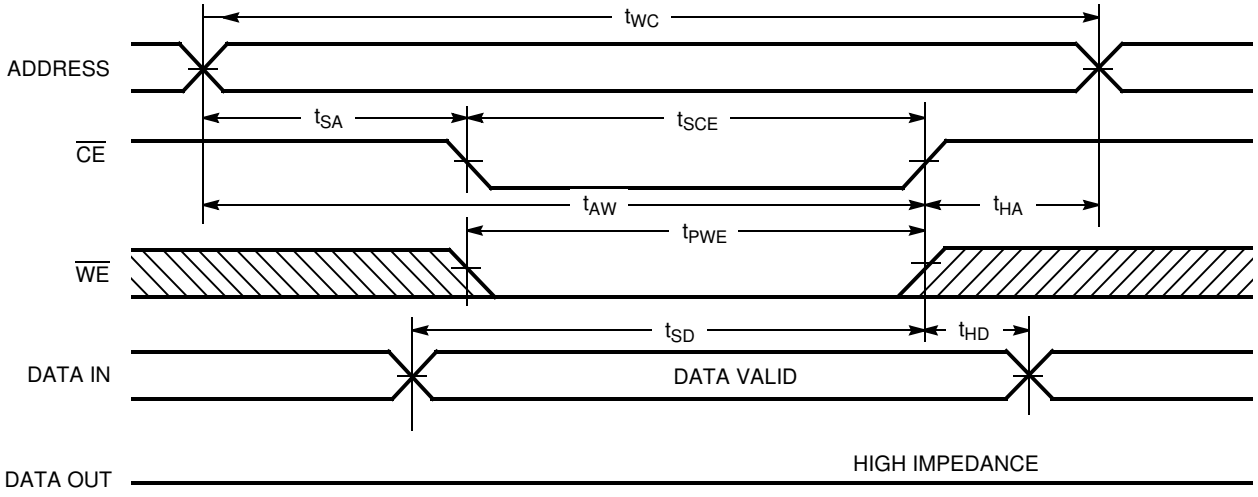


Figure 6. Write Cycle No. 2($\overline{CE}$ Controlled)[11,12]



Notes
11. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
12. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high impedance state

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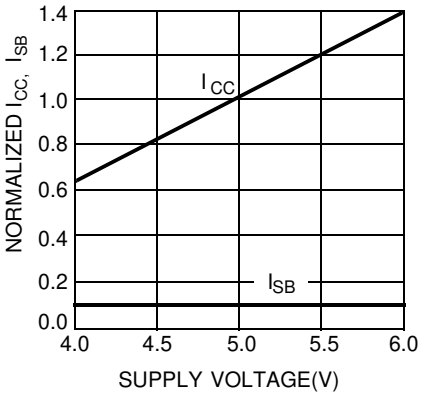
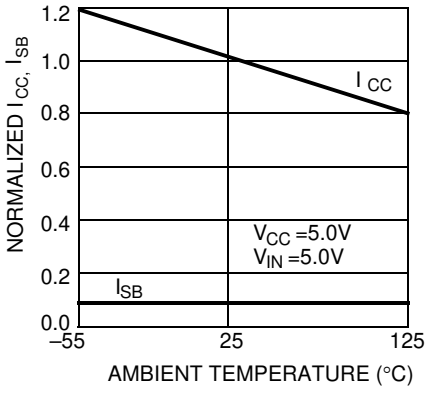
Typical DC and AC Characteristics

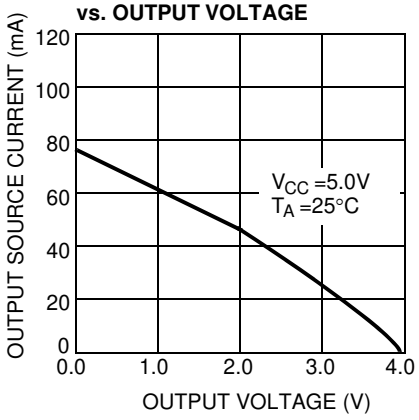
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



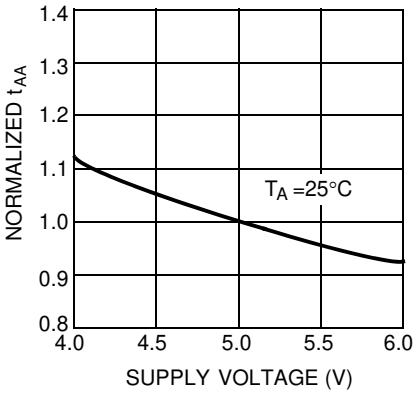
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



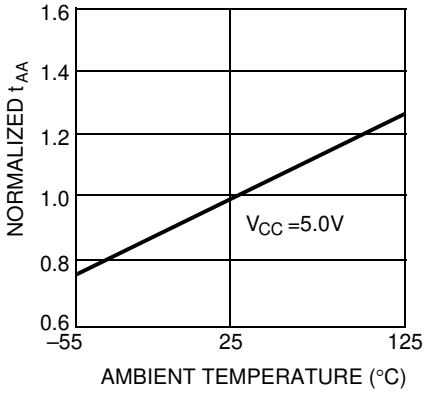
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



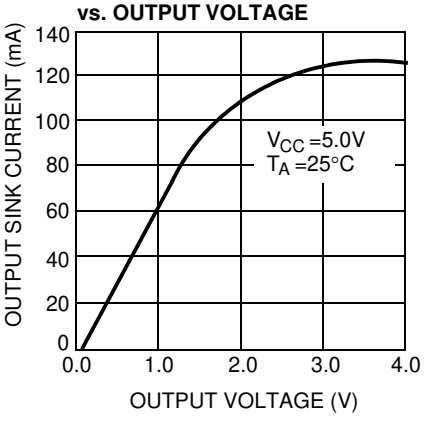
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



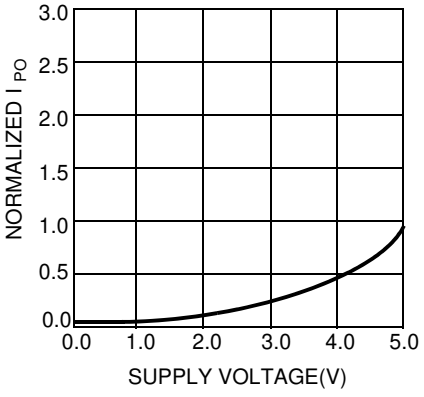
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



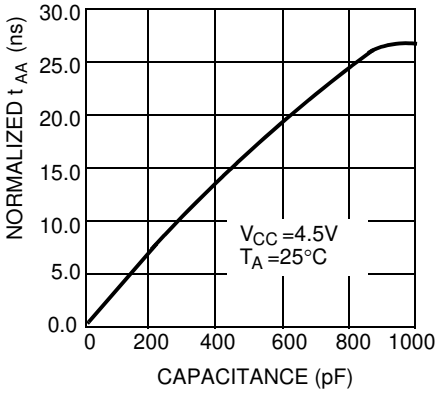
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



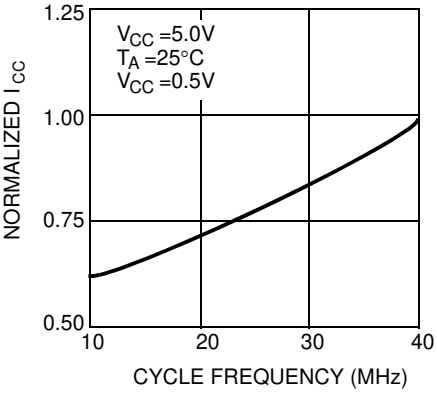
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Address Designators

Address Name	Address Function	Pin Number
A0	X3	1
A1	X4	2
A2	X5	3
A3	X6	4
A4	X7	5
A5	Y7	6
A6	Y6	7
A7	Y2	8
A8	Y3	14
A9	Y1	15
A10	Y0	16
A11	Y4	17
A12	Y5	18
A13	X0	19
A14	X1	20
A15	X2	21

Truth Table

$\overline{CE}$	$\overline{WE}$	Input/Output	Mode
H	X	High Z	Deselect/Power Down
L	H	Data Out	Read
L	L	Data In	Write

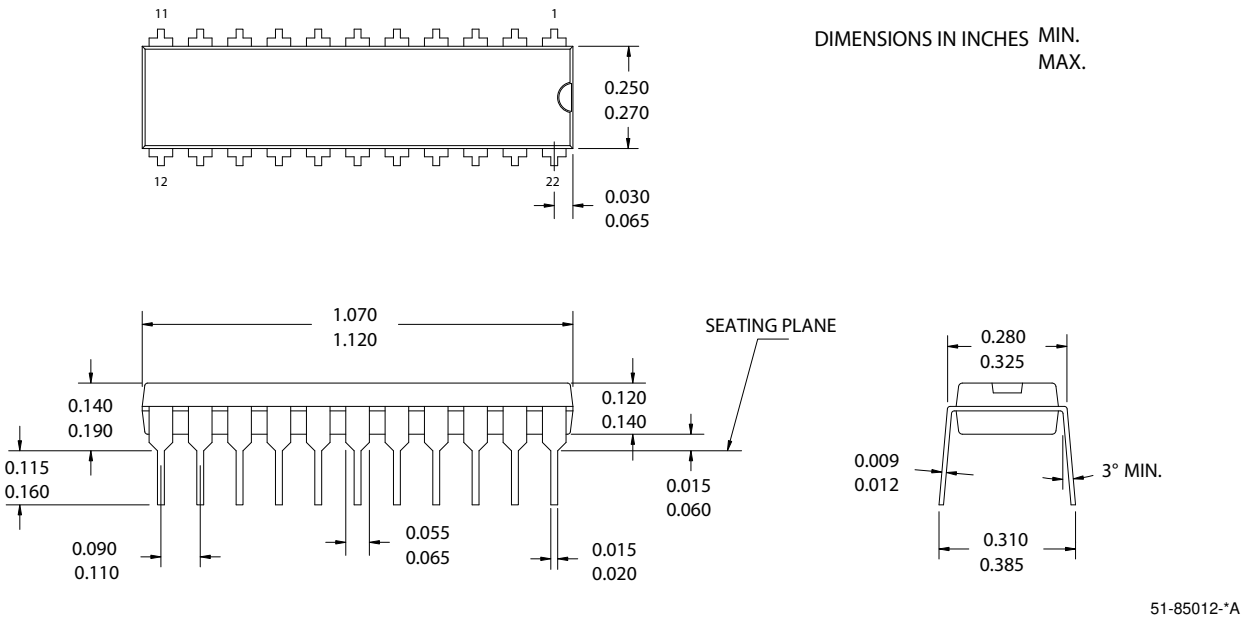
Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
25	CY7C187-25PXC	51-85012	22-Pin (300-Mil) Molded DIP	Commercial
35	CY7C187-35PXC	51-85012	22-Pin (300-Mil) Molded DIP	

Contact your local Cypress sales representatives for the availability of parts

Package Diagram

Figure 7. 22-Pin (300 Mil) PDIP



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Document History Page

Document Title: CY7C187 64K x 1 Static RAM Document Number: 38-05044				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	107146	SZV	09/10/01	Change from Spec number: 38-00038 to 38-05044
*A	486744	NXR	See ECN	Removed 20 ns speed bin Changed Low standby power from 220mW to 110mW Changed the description of I_{IX} from Input Load Current to Input Leakage Current in DC Electrical Characteristics table Updated the Ordering Information Table
*B	2753814	NXR	08/19/09	Removed SOJ package from product offering Updated the Ordering Information Table

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