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fido1100® Data Sheet

32-Bit Real-Time Communications Controller

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1. Overview

Innovasic Semiconductor's fido1100 is the first product in the fido™ family of real-time communication controllers. The fido communication controller architecture is uniquely optimized for solving memory bottlenecks, and is designed from the ground up for deterministic processing. Critical timing parameters, such as context switching and interrupt latency, are precisely predictable for real-time tasks. The fido1100 also incorporates the Universal I/O Controller (UIC™) that is configurable to support various communication protocols across multiple platforms. This flexibility relieves the designer of the task of searching product matrices to find the set of peripherals that most closely match the system interface needs. The Software Profiling and Integrated Debug EnviRonment (SPIDER™) has extensive real-time code debug capabilities without the burden of code instrumentation (see Table 1).

Figure 1 illustrates the top-level blocks of the fido1100 architecture.

Table 1. Key Features

Features	Benefits
Programmable UIC	• Provides the ability to customize peripherals to match user application. • Single chip can solve multiple end-product demands. • Reduces costs through optimized inventory management.
Five Hardware Contexts	• Runs tight-control loops in separate contexts while RTOS manages high level tasks in another context. • Provides context isolation with robust time-and-space partitioning.
Low-Jitter Execution	• Performs tasks at much lower clock rates (66MHz versus >200MHz), reducing power budget and simplifying board design.
SPIDER	• Reduces system integration and debug time through in-system, "what-if" testing without code changes. • Reduces firmware development time thus cutting costs. • Up to 1Mbyte of trace buffer.
Long-Life-Cycle Support	• Fulfills Innovasic's corporate policy of supporting products for the customer's entire life-cycle, eliminating product obsolescence concerns.

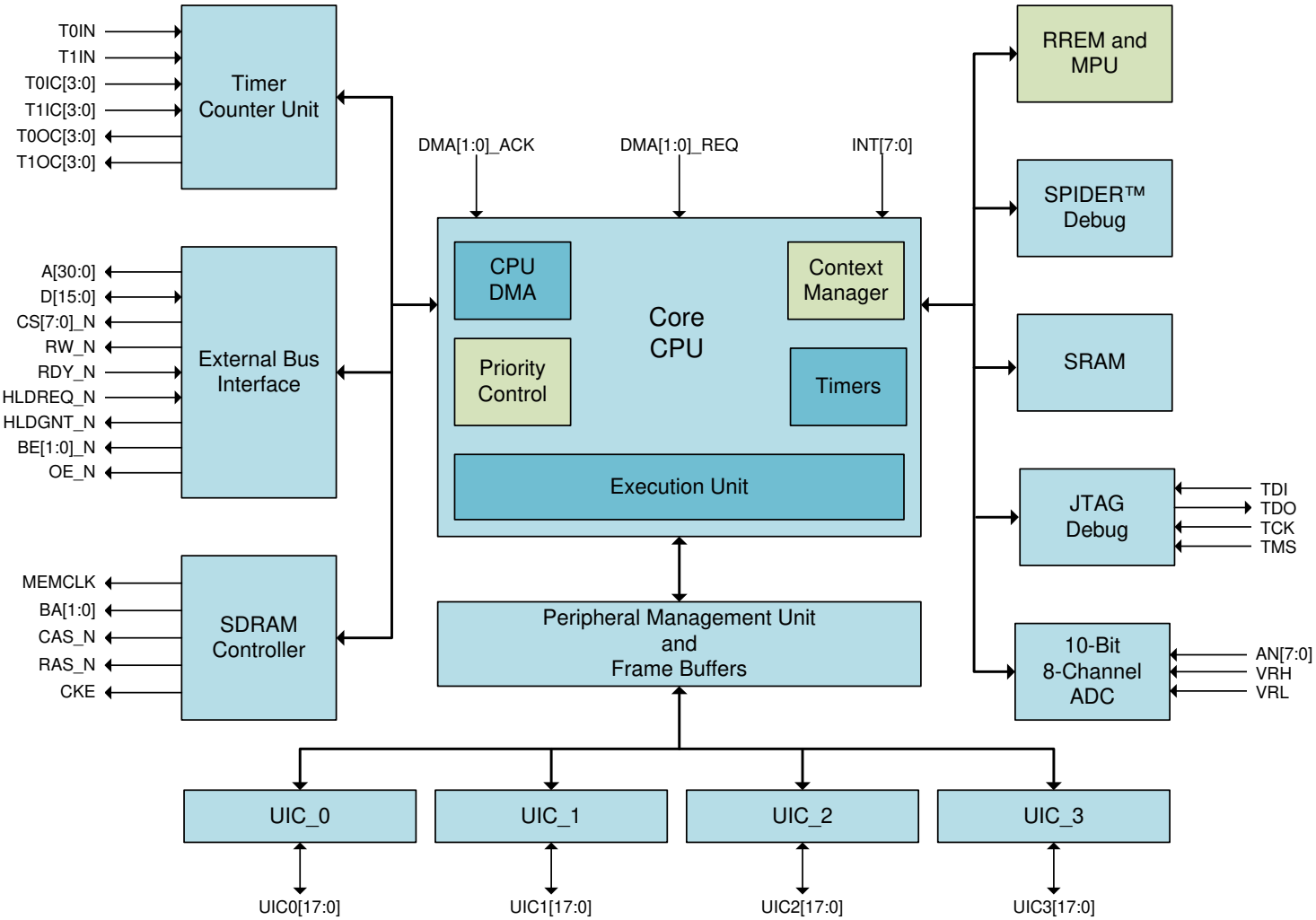


Figure 1. Block Diagram for the fido1100

2. Features

The fido1100 communication controller's features include:

- 32-bit Core CPU
- CISC architecture optimized for real time
- CPU32+ (Motorola® 68000) instruction-set compatible
- Five hardware contexts, each with its own register set and interrupt vector table
- An 8- or 16-bit external bus interface with programmable chip selects
- 24 Kbytes of high-speed internal user SRAM
- 32 Kbytes of high-speed internal user-mappable Relocatable Rapid Execution Memory (RREM)
- A Memory Protection Unit (MPU)
- An SDRAM controller
- Flat, contiguous memory space
- Non-aligned memory access support
- Dedicated Peripheral Management Unit (PMU)
- Four Universal I/O Controllers (UICs) capable of supporting the following protocols:
  - GPIO
  - 10/100 Ethernet with flexible MAC Address Filtering schemes
  - EIA-232
  - CAN
  - SPI
  - I^2C™ Bus
  - SMBus
  - HDLC
- Two channels of full-featured direct memory access (DMA) with deterministic arbitration
- Two Timer/Counter Units (TCU)
- A Watchdog timer, system timer, and context timers

- JTAG emulation and debug interface
- Available in 208-pin PQFP and BGA 15- by 15-mm packages
- 3.3V operation with 5V-tolerant I/O
- Industrial temperature grade
- Software development supported by libraries and tools including UIC firmware for various interface protocols and formats, as well as a customized GNU tool set.

2.1 Core CPU

The fido1100 core is based on the CPU32 architecture, and is compatible with the CPU32 instruction set. The fido1100 incorporates five independent hardware contexts. While all contexts share the same Execution Unit, each of the five hardware contexts in the fido1100 has its own register set, execution priority and exception vector table. From an application's view, this unique feature of the fido1100 allows it to operate as five independent machines in one:

- 32-bit address and data paths on-chip
- 66-MHz operation
- Instruction execution from external memory or fast internal memory.
- Each hardware context has its own copy of:
  - Eight 32-bit User Data Registers (D0-D7)
  - Seven 32-bit Address Registers (A0-A6)
  - Two 32-bit Stack Pointers (A7 and A7')
  - One 32-bit Program Counter
  - One 16-bit Status Register (SR)
  - One 32-bit Vector Base Register (VBR)

2.2 JTAG

The fido1100 is fully compliant with the IEEE 1149.1 Test Access Port and Boundary-Scan architecture (see Table 2). The fido1100 architecture is equipped with the TAP (Test Access Port) interface, TAP controller, instruction register, instruction decoder, boundary-scan register, and by-pass register.

Table 2. Test Pin Descriptions

Pin	Direction	Description
TDO	In	Test Data Output—The tri-state test data output changing on the falling edge of the TCK input. This is actively driven only in the shift-DR and shift-IR controller states.
TDI	In	Test Data Input—The test data input sampled on the rising edge of the TCK input.
TMS	In	Test Mode Select Input—The test mode select input used to sequence the TAP controller state machine. If TMS is a 1 for 5 clock cycles, it sends the TAP controller into reset. If TMS is 0, the TAP controller goes to IDLE.
TCK	In	Test Clock Input—All JTAG commands and serial data are synchronized by this signal.

The JTAG Interface is used for controlling the SPIDER Debug Features of the fido1100.

- Breakpoints—Eight hardware context-aware breakpoints that can be chained to set up if/then triggering conditions.
  - Hardware breakpoints are enabled in software or over JTAG
- Watchpoints—Eight hardware watchpoints.
- Trace—Follow program execution with trace buffers.
  - Single address, single buffer, and circular buffer trace modes
  - Trace buffer can be written anywhere in the address space or to a peripheral
- Debug Control—Hardware single-step and context status control.
  - Access to all memory and registers that are accessible to software
  - Byte, word, and long-word access in full-address mode or offset mode
  - Invalid address access (keystroke errors) over JTAG will not kill the session
  - Direct programming of FLASH on the evaluation board without target software support
  - Built-in hardware support to halt contexts and execute single instructions without software
  - JTAG access to registers, stack space, etc., even if the processor is halted
- Statistical Profiling—SPIDER provides statistical software profiling to identify critical pieces of code.

2.3 Internal Memory and Memory Management

- User SRAM—Internal 24-Kbyte memory that can be used by applications for general purpose data needs or as trace buffers.
- Relocatable Rapid Execution Memory (RREM)—Internal 32-Kbyte memory that can be used as an instruction source for code that requires maximum execution speed.

- Memory Protection Unit (MPU)—Access-control method for 16 user-configurable blocks of internal or external memory on a context basis. A block of memory may be inaccessible, read only or read/write accessible to a selectable set of contexts. The MPU provides the space partitioning needed in deterministic, real-time systems.

2.4 External Bus Interface

The interface to all external memory. It handles memory interface timing and arbitration of external bus requests. The external bus interfaces provide all address, data, and control line to implement either an 8- or 16-bit microcontroller system bus.

- Address/data bus
  - 31-bit address bus to access up to 2 Gbytes of memory space
  - 8- or 16-bit data bus
  - Zero-overhead Endian conversion

- Chip Selects—Eight programmable chip selects with programmable size, data width, and timing.

- SDRAM Controller—Supports 8- or 16-bit data interfaces to SDRAM and provides the necessary control signals to interface to external SDRAM. The interface to the external SDRAM uses the 16-bit-wide data bus and 13 bits of the address bus of the External Bus Interface. The dedicated clock signal for this interface (MEMCLK) operates at the same frequency as the internal master clock.
  - Operates at a maximum clock rate of 66 MHz
  - Executes read, write, pre-charge, auto refresh, power down, and initialize SDRAM modes
  - Fixed, 4-word bursts to/from SDRAM interface
  - Periodically issues auto refresh command to prevent SDRAM data loss

- External Bus Arbitration—The fido1100 provides signals to allow it to operate in a multi-bus master environment.

2.5 PMU/UIC/CPU DMA

The PMU, UIC, and CPU DMA work together as a fast data transport scheme that requires minimal Core CPU overhead or intervention.

- Peripheral Management Unit (PMU)—A set of user-configurable buffers for data transmission and reception via the UICs.

- Universal Input/Output Controller (UIC)—Programmable protocol engine.

The UIC is a very flexible hardware solution designed to support numerous interface requirements. When working in concert with the on-board Peripheral Management Unit (PMU) and on-board data buffers, the operation of the interfaces requires little core processor intervention. This allows the processor to use its bus bandwidth for more important functions than managing data traffic. The UIC design can support complex protocols such as Ethernet or GPIO functions.

- Four software-configurable UICs
- Each supports 10/100 Ethernet, CAN, UART, SPI, I^2C, HDLC, or GPIO functionality
- Software libraries are provided for various interface protocols and formats
- User-programmable integrated 256-location MAC address filter
- Dedicated PMU offloads main CPU bus traffic
- Large 1K × 32 transmit buffer and 2K × 32 receive buffers
- At a minimum, each UIC can support 1 Ethernet port (MII), 2 UARTs, or 18 GPIO
- CPU DMA—Two independent channels of DMA for data transfer

2.6 Internal Peripherals

The fido1100 incorporates the following set of internal peripherals:

2.6.1 Timer Counter Units (TCU)

- Two Timer Counter Units (TCU)—The fido1100 is equipped with two Timer Counter Units.
  - Four channels per timer; any channel can be either input capture or output compare.
  - Input captures can be either rising or falling edge.
  - External signal clocking can be rising edge, falling edge, or both edges of input signal.
  - Output compare can be assert high, assert low, or toggle mode.
  - Underflow, overflow, input-capture, or output-compare conditions can trigger an interrupt.
  - Timers can be programmed for auto-stop or auto-reload.
  - Timer can generate an internal interrupt to wake up the processor from sleep mode.
  - Timer periods in excess of 50 seconds are achievable.

2.6.2 Analog-to-Digital Converter (ADC)

- 8-channel, 10-bit ADC
- Maximum throughput rate of 200 Kbps
- High- and low-reference voltage pins ensure accuracy and temperature compensation
- Very low 5-mW power consumption and includes a built-in power-down mode
- Single- or multiple-channel conversion scan modes
- Interrupt generated at the end of conversion is assigned a priority and a context
- Interrupts from the analog-to-digital converter can be disabled

2.6.3 Timers

- System Timer.
  - Provides five periodic System Timer interrupts.
    - 16-bit counter with 16-bit prescale allows a range of System Timer interrupts from 80 nS to 50 seconds with a 66-MHz system clock.
    - These interrupts can be assigned to the fast-context switching hardware providing a zero overhead system executive or the System Timer interrupts can simply produce a traditional vectored interrupt request to provide a system with basic timing needs.

- Watchdog Timer
  - 16-bit counter with an 11-bit prescaler

- Context Timers
  - Each hardware context has a set of timing registers that can track, specify, and limit execution time.

2.7 Power Control

All internal peripherals can be put into a low-power consumption mode.

3. Libraries and Support Tools

- Full library support
- UIC libraries
- Embedded communication stacks
- TCP/IP
- GPIO sample programs
- Customized GNU tool set
- Eclipse IDE
- Sourcery G++ from Code Sourcery

4. Packaging, Pin Descriptions, and Physical Dimensions

Information on the packages and pin descriptions for the fido1100 communication controller PQFP and BGA 15- by 15-mm package is provided individually. Refer to sections, figures, and tables for information on the device of interest.

4.1 PQFP Package

4.1.1 PQFP Pinout

The pinout for the fido1100 communication controller PQFP package is as shown in Figure 2. The corresponding pinout is provided in Table 3.

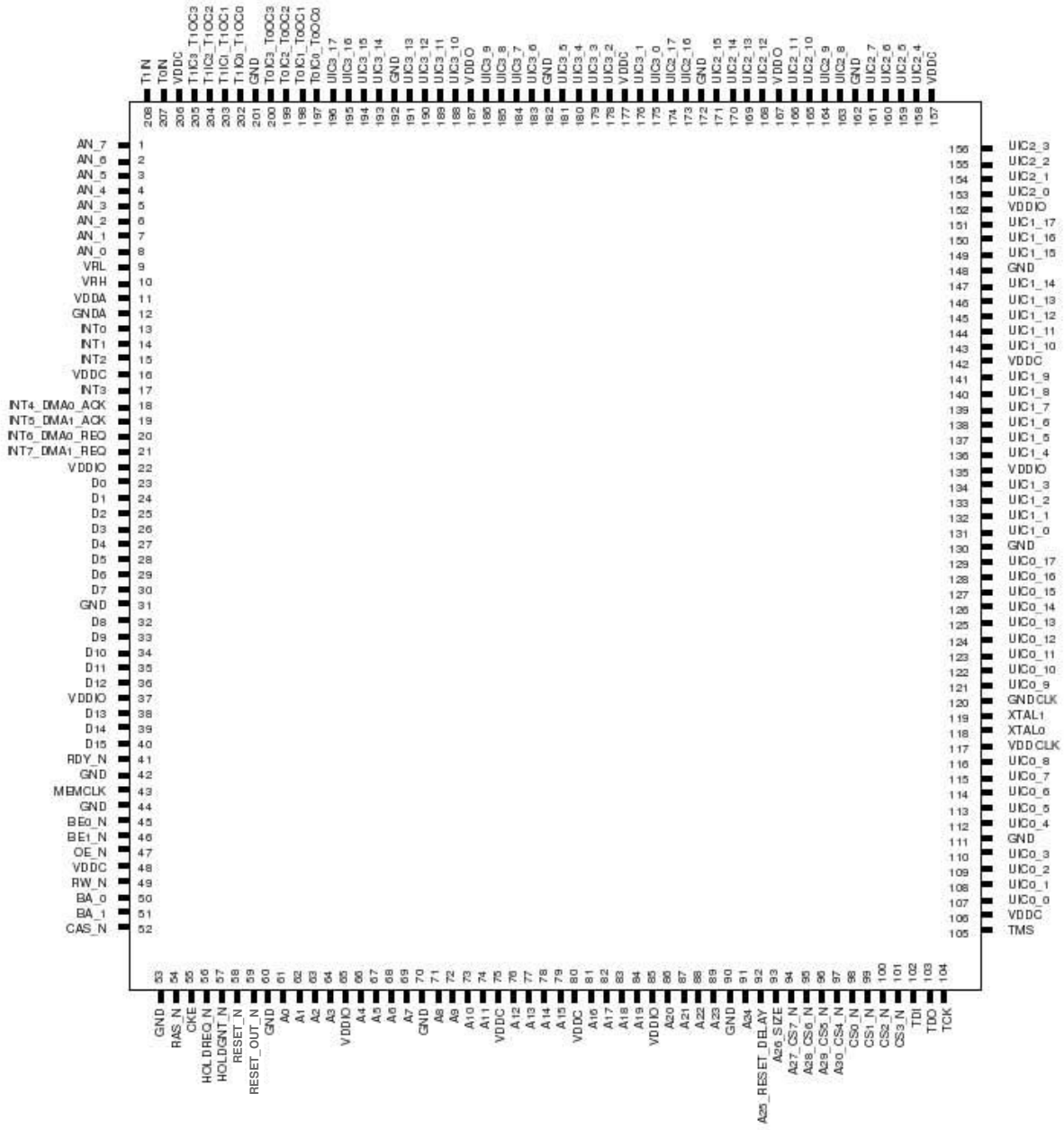


Figure 2. PQFP Package Diagram

Table 3. PQFP Pin Listing

Pin	Signal Name	Type	Description
1	AN_7	Input	Analog-to-digital converter input channel 7
2	AN_6	Input	Analog-to-digital converter input channel 6
3	AN_5	Input	Analog-to-digital converter input channel 5
4	AN_4	Input	Analog-to-digital converter input channel 4
5	AN_3	Input	Analog-to-digital converter input channel 3
6	AN_2	Input	Analog-to-digital converter input channel 2
7	AN_1	Input	Analog-to-digital converter input channel 1
8	AN_0	Input	Analog-to-digital converter input channel 0
9	VRL	Input	Analog-to-digital converter low-input reference
10	VRH	Input	Analog-to-digital converter high-input reference
11	VDDA	Power	Analog supply voltage (+3.3VDC)
12	GNDA	Ground	Analog ground
13	INT0	Input	Interrupt_0
14	INT1	Input	Interrupt_1
15	INT2	Input	Interrupt_2
16	VDDC	Power	Digital core supply voltage (+2.5VDC)
17	INT3	Input	Interrupt_3
18	INT4_DMA0_ ACK	Bidirectional	Muxed pin, Interrupt_4 or DMA channel 0 acknowledge
19	INT5_DMA1_ ACK	Bidirectional	Muxed pin, Interrupt_5 or DMA channel 1 acknowledge
20	INT6_DMA0_ REQ	Input	Muxed pin, Interrupt_6 or DMA channel 0 request
21	INT7_DMA1_ REQ	Input	Muxed pin, Interrupt_7 or DMA channel 1 request
22	VDDIO	Power	Digital I/O supply voltage (+3.3VDC)
23	D0	Bidirectional	External Bus Interface data Bit [0]
24	D1	Bidirectional	External Bus Interface data Bit [1]
25	D2	Bidirectional	External Bus Interface data Bit [2]
26	D3	Bidirectional	External Bus Interface data Bit [3]
27	D4	Bidirectional	External Bus Interface data Bit [4]
28	D5	Bidirectional	External Bus Interface data Bit [5]
29	D6	Bidirectional	External Bus Interface data Bit [6]
30	D7	Bidirectional	External Bus Interface data Bit [7]
31	GND	Ground	Digital ground
32	D8	Bidirectional	External Bus Interface data Bit [8]
33	D9	Bidirectional	External Bus Interface data Bit [9]
34	D10	Bidirectional	External Bus Interface data Bit [10]
35	D11	Bidirectional	External Bus Interface data Bit [11]

Table 3. PQFP Pin Listing *(Continued)*

Pin	Signal Name	Type	Description
36	D12	Bidirectional	External Bus Interface data Bit [12]
37	VDDIO	Power	Digital I/O supply voltage (+3.3VDC)
38	D13	Bidirectional	External Bus Interface data Bit [13]
39	D14	Bidirectional	External Bus Interface data Bit [14]
40	D15	Bidirectional	External Bus Interface data Bit [15]
41	RDY_N	Input	External Bus Interface External Ready Indication
42	GND	Ground	Digital ground
43	MEMCLK	Output	Memory clock used by external memory
44	GND	Ground	Digital ground
45	BE0_N	Output	Byte enable 0, active low
46	BE1_N	Output	Byte enable 1, active low
47	OE_N	Output	Output enable, active low
48	VDDC	Power	Digital core supply voltage (+2.5VDC)
49	RW_N	Output	Read or write control (active low write)
50	BA_0	Output	Bank Enable 0
51	BA_1	Output	Bank Enable 1
52	CAS_N	Output	Column activate signal, active low
53	GND	Ground	Digital Ground
54	RAS_N	Output	Row activate signal, active low
55	CKE	Output	Clock enable to be used in conjunction with MEMCLK
56	HOLDREQ_N	Input	External Bus hold request, active low
57	HOLDGNT_N	Output	External Bus grant request, active low
58	RESET_N	Input	Reset input
59	RESET_OUT_N	Output	Reset output
60	GND	Ground	Digital ground
61	A0	Output	External Bus Interface address Bit [0]
62	A1	Output	External Bus Interface address Bit [1]
63	A2	Output	External Bus Interface address Bit [2]
64	A3	Output	External Bus Interface address Bit [3]
65	VDDIO	Power	Digital I/O supply voltage (+3.3VDC)
66	A4	Output	External Bus Interface address Bit [4]
67	A5	Output	External Bus Interface address Bit [5]
68	A6	Output	External Bus Interface address Bit [6]
69	A7	Output	External Bus Interface address Bit [7]
70	GND	Ground	Digital ground
71	A8	Output	External Bus Interface address Bit [8]
72	A9	Output	External Bus Interface address Bit [9]
73	A10	Output	External Bus Interface address Bit [10]
74	A11	Output	External Bus Interface address Bit [11]

Table 3. PQFP Pin Listing *(Continued)*

Pin	Signal Name	Type	Description
75	VDDC	Power	Digital core supply voltage (+2.5VDC)
76	A12	Output	External Bus Interface address Bit [12]
77	A13	Output	External Bus Interface address Bit [13]
78	A14	Output	External Bus Interface address Bit [14]
79	A15	Output	External Bus Interface address Bit [15]
80	VDDC	Power	Digital core supply voltage (+2.5VDC)
81	A16	Output	External Bus Interface address Bit [16]
82	A17	Output	External Bus Interface address Bit [17]
83	A18	Output	External Bus Interface address Bit [18]
84	A19	Output	External Bus Interface address Bit [19]
85	VDDIO	Power	Digital I/O supply voltage (+3.3VDC)
86	A20	Output	External Bus Interface address Bit [20]
87	A21	Output	External Bus Interface address Bit [21]
88	A22	Output	External Bus Interface address Bit [22]
89	A23	Output	External Bus Interface address Bit [23]
90	GND	Ground	Digital ground
91	A24	Output	External Bus Interface address Bit [24]
92	A25_RESET_ DELAY	Internal Pull-up	Muxed pin, External Bus Interface address Bit [25] or POR counter bypass
93	A26_SIZE	Internal Pull-up	Muxed pin, External Bus Interface address Bit [26] or data bus size select (0 = 8-Bit, 1= 16=Bit)
94	A27_CS7_N	Output	Muxed pin, External Bus Interface address Bit [27] or Chip select 7 (chip select active low)
95	A28_CS6_N	Output	Muxed pin, External Bus Interface address Bit [28] or Chip select 6 (chip select active low)
96	A29_CS5_N	Output	Muxed pin, External Bus Interface address Bit [29] or Chip select 5 (chip select active low)
97	A30_CS4_N	Output	Muxed pin, External Bus Interface address Bit [30] or Chip select 4 (chip select active low)
98	CS0_N	Output	Chip select 0 (chip select active low)
99	CS1_N	Output	Chip select 1 (chip select active low)
100	CS2_N	Output	Chip select 2 (chip select active low)
101	CS3_N	Output	Chip select 3 (chip select active low)
102	TDI	Input	JTAG data input
103	TDO	Output	JTAG data output
104	TCK	Input	JTAG clock input
105	TMS	Input	JTAG control signal
106	VDDC	Power	Digital core supply voltage (+2.5VDC)
107	UIC0_0	Bidirectional	Universal I/O Controller 0, pin 0
108	UIC0_1	Bidirectional	Universal I/O Controller 0, pin 1

Table 3. PQFP Pin Listing *(Continued)*

Pin	Signal Name	Type	Description
109	UIC0_2	Bidirectional	Universal I/O Controller 0, pin 2
110	UIC0_3	Bidirectional	Universal I/O Controller 0, pin 3
111	GND	Ground	Digital ground
112	UIC0_4	Bidirectional	Universal I/O Controller 0, pin 4
113	UIC0_5	Bidirectional	Universal I/O Controller 0, pin 5
114	UIC0_6	Bidirectional	Universal I/O Controller 0, pin 6
115	UIC0_7	Bidirectional	Universal I/O Controller 0, pin 7
116	UIC0_8	Bidirectional	Universal I/O Controller 0, pin 8
117	VDDCLK	Power supply	Power Supply for the Crystal Oscillator (+2.5VDC)
118	XTAL0	Clock	Crystal input pin 0 (Osc. In)
119	XTAL1	Clock	Crystal input/output pin 1 (Osc. Out)
120	GNDCLK	Ground	Digital ground
121	UIC0_9	Bidirectional	Universal I/O Controller 0, pin 9
122	UIC0_10	Bidirectional	Universal I/O Controller 0, pin 10
123	UIC0_11	Bidirectional	Universal I/O Controller 0, pin 11
124	UIC0_12	Bidirectional	Universal I/O Controller 0, pin 12
125	UIC0_13	Bidirectional	Universal I/O Controller 0, pin 13
126	UIC0_14	Bidirectional	Universal I/O Controller 0, pin 14
127	UIC0_15	Bidirectional	Universal I/O Controller 0, pin 15
128	UIC0_16	Bidirectional	Universal I/O Controller 0, pin 16
129	UIC0_17	Bidirectional	Universal I/O Controller 0, pin 17
130	GND	Ground	Digital ground
131	UIC1_0	Bidirectional	Universal I/O Controller 1, pin 0
132	UIC1_1	Bidirectional	Universal I/O Controller 1, pin 1
133	UIC1_2	Bidirectional	Universal I/O Controller 1, pin 2
134	UIC1_3	Bidirectional	Universal I/O Controller 1, pin 3
135	VDDIO	Power	Digital I/O supply voltage (+3.3VDC)
136	UIC1_4	Bidirectional	Universal I/O Controller 1, pin 4
137	UIC1_5	Bidirectional	Universal I/O Controller 1, pin 5
138	UIC1_6	Bidirectional	Universal I/O Controller 1, pin 6
139	UIC1_7	Bidirectional	Universal I/O Controller 1, pin 7
140	UIC1_8	Bidirectional	Universal I/O Controller 1, pin 8
141	UIC1_9	Bidirectional	Universal I/O Controller 1, pin 9
142	VDDC	Power	Digital core supply voltage (+2.5VDC)
143	UIC1_10	Bidirectional	Universal I/O Controller 1, pin 10
144	UIC1_11	Bidirectional	Universal I/O Controller 1, pin 11
145	UIC1_12	Bidirectional	Universal I/O Controller 1, pin 12
146	UIC1_13	Bidirectional	Universal I/O Controller 1, pin 13
147	UIC1_14	Bidirectional	Universal I/O Controller 1, pin 14

Table 3. PQFP Pin Listing *(Continued)*

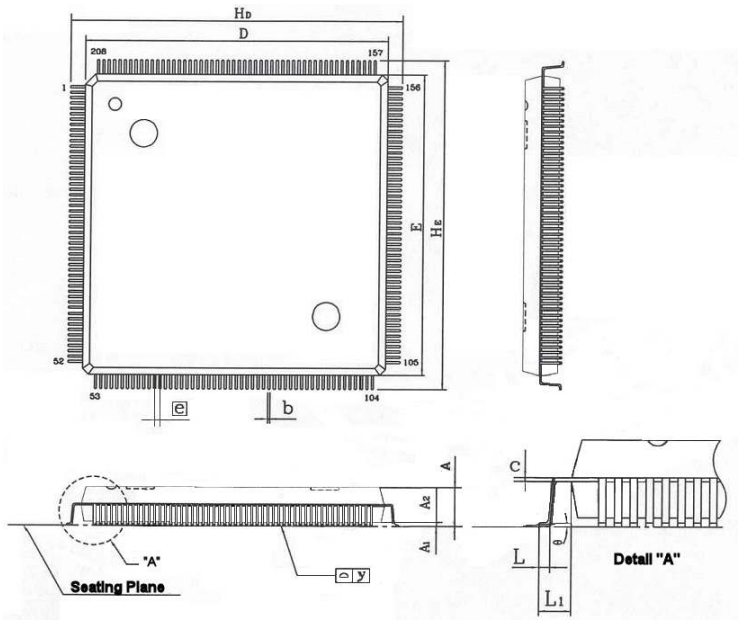
Pin	Signal Name	Type	Description
148	GND	Ground	Digital ground
149	UIC1_15	Bidirectional	Universal I/O Controller 1, pin 15
150	UIC1_16	Bidirectional	Universal I/O Controller 1, pin 16
151	UIC1_17	Bidirectional	Universal I/O Controller 1, pin 17
152	VDDIO	Power	Digital I/O supply voltage (+3.3VDC)
153	UIC2_0	Bidirectional	Universal I/O Controller 2, pin 0
154	UIC2_1	Bidirectional	Universal I/O Controller 2, pin 1
155	UIC2_2	Bidirectional	Universal I/O Controller 2, pin 2
156	UIC2_3	Bidirectional	Universal I/O Controller 2, pin 3
157	VDDC	Power	Digital core supply voltage (+2.5VDC)
158	UIC2_4	Bidirectional	Universal I/O Controller 2, pin 4
159	UIC2_5	Bidirectional	Universal I/O Controller 2, pin 5
160	UIC2_6	Bidirectional	Universal I/O Controller 2, pin 6
161	UIC2_7	Bidirectional	Universal I/O Controller 2, pin 7
162	GND	Ground	Digital ground
163	UIC2_8	Bidirectional	Universal I/O Controller 2, pin 8
164	UIC2_9	Bidirectional	Universal I/O Controller 2, pin 9
165	UIC2_10	Bidirectional	Universal I/O Controller 2, pin 10
166	UIC2_11	Bidirectional	Universal I/O Controller 2, pin 11
167	VDDIO	Power	Digital I/O supply voltage (+3.3VDC)
168	UIC2_12	Bidirectional	Universal I/O Controller 2, pin 12
169	UIC2_13	Bidirectional	Universal I/O Controller 2, pin 13
170	UIC2_14	Bidirectional	Universal I/O Controller 2, pin 14
171	UIC2_15	Bidirectional	Universal I/O Controller 2, pin 15
172	GND	Ground	Digital ground
173	UIC2_16	Bidirectional	Universal I/O Controller 2, pin 16
174	UIC2_17	Bidirectional	Universal I/O Controller 2, pin 17
175	UIC3_0	Bidirectional	Universal I/O Controller 3 pin 0
176	UIC3_1	Bidirectional	Universal I/O Controller 3 pin 1
177	VDDC	Power	Digital core supply voltage (+2.5VDC)
178	UIC3_2	Bidirectional	Universal I/O Controller 3 pin 2
179	UIC3_3	Bidirectional	Universal I/O Controller 3 pin 3
180	UIC3_4	Bidirectional	Universal I/O Controller 3 pin 4
181	UIC3_5	Bidirectional	Universal I/O Controller 3 pin 5
182	GND	Ground	Digital ground
183	UIC3_6	Bidirectional	Universal I/O Controller 3 pin 6
184	UIC3_7	Bidirectional	Universal I/O Controller 3 pin 7
185	UIC3_8	Bidirectional	Universal I/O Controller 3 pin 8
186	UIC3_9	Bidirectional	Universal I/O Controller 3 pin 9

Table 3. PQFP Pin Listing *(Continued)*

Pin	Signal Name	Type	Description
187	VDDIO	Power	Digital I/O supply voltage (+3.3VDC)
188	UIC3_10	Bidirectional	Universal I/O Controller 3 pin 10
189	UIC3_11	Bidirectional	Universal I/O Controller 3 pin 11
190	UIC3_12	Bidirectional	Universal I/O Controller 3 pin 12
191	UIC3_13	Bidirectional	Universal I/O Controller 3 pin 13
192	GND	Ground	Digital Ground
193	UIC3_14	Bidirectional	Universal I/O Controller 3 pin 14
194	UIC3_15	Bidirectional	Universal I/O Controller 3 pin 15
195	UIC3_16	Bidirectional	Universal I/O Controller 3 pin 16
196	UIC3_17	Bidirectional	Universal I/O Controller 3 pin 17
197	T0IC0_T0OC0	Bidirectional	Muxed pin, Timer Counter Unit 0 input capture 0 or output compare 0
198	T0IC1_T0OC1	Bidirectional	Muxed pin, Timer Counter Unit 0 input capture 1 or output compare 1
199	T0IC2_T0OC2	Bidirectional	Muxed pin, Timer Counter Unit 0 input capture 2 or output compare 2
200	T0IC3_T0OC3	Bidirectional	Muxed pin, Timer Counter Unit 0 input capture 3 or output compare 3
201	GND	Ground	Digital ground
202	T1IC0_T1OC0	Bidirectional	Muxed pin, Timer Counter Unit 1 input capture 0 or output compare 0
203	T1IC1_T1OC1	Bidirectional	Muxed pin, Timer Counter Unit 1 input capture 1 or output compare 1
204	T1IC2_T1OC2	Bidirectional	Muxed pin, Timer Counter Unit 1 input capture 2 or output compare 2
205	T1IC3_T1OC3	Bidirectional	Muxed pin, Timer Counter Unit 1 input capture 3 or output compare 3
206	VDDC	Power	Digital core supply voltage (+2.5VDC)
207	T0IN	Input	Timer Counter Unit 0 external clock source
208	T1IN	Input	Timer Counter Unit 1 external clock source

4.1.2 PQFP Physical Dimensions

The physical dimensions for the 208-pin PQFP package are as shown in Figure 3.



Legend:

Symbol	Dimension in mm			Dimension in Inches		
	Min	Nom	Max	Min	Nom	Max
A	–	–	4.07	–	–	0.160
A1	0.25	–	–	0.010	–	–
A2	3.15	3.23	3.30	0.124	0.127	0.130
b	0.18	–	0.28	0.007	–	0.011
c	0.13	–	0.23	0.005	–	0.009
D	27.90	28.00	28.10	1.098	1.102	1.106
E	27.90	28.00	28.10	1.098	1.102	1.106
e	0.50 BSC			0.020 BSC		
H_D	30.35	30.60	30.85	1.195	1.205	1.215
H_E	30.35	30.60	30.85	1.195	1.205	1.215
L	0.35	0.50	0.65	0.014	0.020	0.026
L1	1.30 REF			0.051 REF		
y	–	–	0.19	–	–	0.004
Θ	0°	–	7°	0°	–	7°

Notes:
1. Dimension D & E do not include interlead flash.
2. Dimension B does not include damper protrusion/intrusion.
3. Controlling dimension: mm
4. General appearance spec. should be based on visual inspection spec.

Figure 3. PQFP Physical Package Dimensions

4.2 BGA 15- by 15-mm Package

4.2.1 BGA 15- by 15-mm Pinout

The pinout for the fido1100™ communication controller BGA 15- by 15-mm package is as shown in Figure 4. The corresponding pinout is provided in Table 4.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
A	T1IC1_ T1OC1	T0IC2_ T0OC2	T0IC0_ T0OC0	UIC3_15	UIC3_13	UIC3_12	UIC3_9	UIC3_7	UIC3_4	UIC3_1	UIC3_0	UIC2_15	UIC2_13	UIC2_10	UIC2_7	UIC2_6	UIC1_17	A
B	AN_2	T1IC2_ T1OC2	T1IC0_ T1OC0	T0IC1_ T0OC1	UIC3_16	GND	UIC3_11	UIC3_8	UIC3_5	UIC3_2	UIC2_17	UIC2_14	UIC2_11	UIC2_8	UIC2_5	UIC2_0	UIC1_14	B
C	AN_0	AN_5	T0IN	T1IC3_ T1OC3	T0IC3_ T0OC3	UIC3_17	UIC3_14	UIC3_10	UIC3_6	UIC3_3	UIC2_16	UIC2_12	UIC2_9	UIC2_4	UIC2_1	UIC1_16	UIC1_12	C
D	VDDA	AN_1	AN_6	GND	GND	T1IN	VDDC	VDDC	VDDC	VDDIO	VDDIO	VDDIO	GND	GND	UIC2_2	UIC1_13	UIC1_9	D
E	GNDA	VRH	AN_3	GND										GND	UIC1_15	UIC1_10	UIC1_6	E
F	INT2	INT0	VRL	AN_7										UIC2_3	UIC1_11	UIC1_8	UIC1_5	F
G	INT4_ DMA0_ ACK	INT3	INT1	AN_4										VDDIO	UIC1_7	UIC1_4	UIC1_2	G
H	INT7_ DMA1_ REQ	INT6_ DMA0_ REQ	INT5_ DMA1_ ACK	VDDC										VDDIO	UIC1_3	UIC1_1	UIC1_0	H
J	D0	D1	D2	VDDIO										VDDIO	UIC0_17	UIC0_16	UIC0_15	J
K	D3	D4	D6	VDDIO										VDDC	UIC0_14	UIC0_13	UIC0_12	K
L	D5	D7	D11	OE_N										VDDC	UIC0_10	UIC0_9	UIC0_11	L
M	D8	D10	D15	CAS_N										GNDCLK	VDDCLK	UIC0_8	XTAL1	M
N	D9	D13	BE1_N	GND										GND	UIC0_5	UIC0_7	XTAL0	N
P	D12	RDY_N	BA_1	GND	GND	GND	RESET_N	VDDIO	VDDC	VDDC	A21	A26_SIZE	GND	GND	UIC0_0	UIC0_4	UIC0_6	P
R	D14	BE0_N	BA_0	RAS_N	HOLDGNT_N	A3	A6	A10	A15	A18	A22	A27_CS7_N	A29_CS5_N	CS3_N	CS2_N	UIC0_2	UIC0_3	R
T	GND	RW_N	CKE	RESET_ OUT_N	A2	A5	A8	A11	A14	A17	A20	A24	A28_CS6_N	CS0_N	CS1_N	TCK	UIC0_1	T
U	MEMCLK	HOLDREQ_N	A0	A1	A4	A7	A9	A12	A13	A16	A19	A23	A25_RESET_ DELAY	A30_CS4_N	TDI	TDO	TMS	U
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	

= Signals.
= Indicates power.
= Indicates ground.

Figure 4. BGA 15- by 15-mm Package Diagram

Table 4. BGA 15- by 15-mm Package Pin Listing

Pin	Signal Name	Type	Description
F4	AN_7	Input	Analog-to-digital converter input channel 7
D3	AN_6	Input	Analog-to-digital converter input channel 6
C2	AN_5	Input	Analog-to-digital converter input channel 5
G4	AN_4	Input	Analog-to-digital converter input channel 4
E3	AN_3	Input	Analog-to-digital converter input channel 3
B1	AN_2	Input	Analog-to-digital converter input channel 2
D2	AN_1	Input	Analog-to-digital converter input channel 1
C1	AN_0	Input	Analog-to-digital converter input channel 0
F3	VRL	Input	Analog-to-digital converter low-input reference
E2	VRH	Input	Analog-to-digital converter high-input reference
D1	VDDA	Power	Analog supply voltage (+3.3VDC)
E1	GNDA	Ground	Analog ground
F2	INT0	Input	Interrupt_0
G3	INT1	Input	Interrupt_1
F1	INT2	Input	Interrupt_2
D7	VDDC	Power	Digital core supply voltage (+2.5VDC)
G2	INT3	Input	Interrupt_3
G1	INT4_DMA0_ ACK	Bidirectional	Muxed pin, Interrupt_4 or DMA channel 0 acknowledge
H3	INT5_DMA1_ ACK	Bidirectional	Muxed pin, Interrupt_5 or DMA channel 1 acknowledge
H2	INT6_DMA0_ REQ	Input	Muxed pin, Interrupt_6 or DMA channel 0 request
H1	INT7_DMA1_ REQ	Input	Muxed pin, Interrupt_7 or DMA channel 1 request
D10	VDDIO	Power	Digital I/O supply voltage (+3.3VDC)
J1	D0	Bidirectional	External Bus Interface data Bit [0]
J2	D1	Bidirectional	External Bus Interface data Bit [1]
J3	D2	Bidirectional	External Bus Interface data Bit [2]
K1	D3	Bidirectional	External Bus Interface data Bit [3]
K2	D4	Bidirectional	External Bus Interface data Bit [4]
L1	D5	Bidirectional	External Bus Interface data Bit [5]
K3	D6	Bidirectional	External Bus Interface data Bit [6]
L2	D7	Bidirectional	External Bus Interface data Bit [7]
D4	GND	Ground	Digital ground
M1	D8	Bidirectional	External Bus Interface data Bit [8]
N1	D9	Bidirectional	External Bus Interface data Bit [9]
M2	D10	Bidirectional	External Bus Interface data Bit [10]
L3	D11	Bidirectional	External Bus Interface data Bit [11]

Table 4. BGA 15- by 15-mm Package Pin Listing *(Continued)*

Pin	Signal Name	Type	Description
P1	D12	Bidirectional	External Bus Interface data Bit [12]
D11	VDDIO	Power	Digital I/O supply voltage (+3.3VDC)
N2	D13	Bidirectional	External Bus Interface data Bit [13]
R1	D14	Bidirectional	External Bus Interface data Bit [14]
M3	D15	Bidirectional	External Bus Interface data Bit [15]
P2	RDY_N	Input	External Bus Interface External Ready Indication
T1	GND	Ground	Digital ground
U1	MEMCLK	Output	Memory clock used by external memory
D5	GND	Ground	Digital ground
R2	BE0_N	Output	Byte enable 0, active low
N3	BE1_N	Output	Byte enable 1, active low
L4	OE_N	Output	Output enable, active low
D8	VDDC	Power	Digital core supply voltage (+2.5VDC)
T2	RW_N	Output	Read or write control (active low write)
R3	BA_0	Output	Bank Enable 0
P3	BA_1	Output	Bank Enable 1
M4	CAS_N	Output	Column activate signal, active low
P6	GND	Ground	Digital Ground
R4	RAS_N	Output	Row activate signal, active low
T3	CKE	Output	Clock enable to be used in conjunction with MEMCLK
U2	HOLDREQ_N	Input	External Bus hold request, active low
R5	HOLDGNT_N	Output	External Bus grant request, active low
P7	RESET_N	Input	Reset input
T4	RESET_OUT_N	Output	Reset output
D13	GND	Ground	Digital ground
U3	A0	Output	External Bus Interface address Bit [0]
U4	A1	Output	External Bus Interface address Bit [1]
T5	A2	Output	External Bus Interface address Bit [2]
R6	A3	Output	External Bus Interface address Bit [3]
D12	VDDIO	Power	Digital I/O supply voltage (+3.3VDC)
U5	A4	Output	External Bus Interface address Bit [4]
T6	A5	Output	External Bus Interface address Bit [5]
R7	A6	Output	External Bus Interface address Bit [6]
U6	A7	Output	External Bus Interface address Bit [7]
D14	GND	Ground	Digital ground
T7	A8	Output	External Bus Interface address Bit [8]
U7	A9	Output	External Bus Interface address Bit [9]
R8	A10	Output	External Bus Interface address Bit [10]

Table 4. BGA 15- by 15-mm Package Pin Listing *(Continued)*

Pin	Signal Name	Type	Description
T8	A11	Output	External Bus Interface address Bit [11]
D9	VDDC	Power	Digital core supply voltage (+2.5VDC)
U8	A12	Output	External Bus Interface address Bit [12]
U9	A13	Output	External Bus Interface address Bit [13]
T9	A14	Output	External Bus Interface address Bit [14]
R9	A15	Output	External Bus Interface address Bit [15]
H4	VDDC	Power	Digital core supply voltage (+2.5VDC)
U10	A16	Output	External Bus Interface address Bit [16]
T10	A17	Output	External Bus Interface address Bit [17]
R10	A18	Output	External Bus Interface address Bit [18]
U11	A19	Output	External Bus Interface address Bit [19]
G14	VDDIO	Power	Digital I/O supply voltage (+3.3VDC)
T11	A20	Output	External Bus Interface address Bit [20]
P11	A21	Output	External Bus Interface address Bit [21]
R11	A22	Output	External Bus Interface address Bit [22]
U12	A23	Output	External Bus Interface address Bit [23]
E4	GND	Ground	Digital ground
T12	A24	Output	External Bus Interface address Bit [24]
U13	A_25_RESET_ DELAY	Internal Pull-up	Muxed pin, External Bus Interface address Bit [25] or POR counter bypass
P12	A_26_SIZE	Internal Pull-up	Muxed pin, External Bus Interface address Bit [26] or data bus size select (0 = 8-Bit, 1= 16=Bit)
R12	A27_CS7_N	Output	Muxed pin, External Bus Interface address Bit [27] or Chip select 7 (chip select active low)
T13	A28_CS6_N	Output	Muxed pin, External Bus Interface address Bit [28] or Chip select 6 (chip select active low)
R13	A29_CS5_N	Output	Muxed pin, External Bus Interface address Bit [29] or Chip select 5 (chip select active low)
U14	A30_CS4_N	Output	Muxed pin, External Bus Interface address Bit [30] or Chip select 4 (chip select active low)
T14	CS0_N	Output	Chip select 0 (chip select active low)
T15	CS1_N	Output	Chip select 1 (chip select active low)
R15	CS2_N	Output	Chip select 2 (chip select active low)
R14	CS3_N	Output	Chip select 3 (chip select active low)
U15	TDI	Input	JTAG data input
U16	TDO	Output	JTAG data output
T16	TCK	Input	JTAG clock input
U17	TMS	Input	JTAG control signal
K14	VDDC	Power	Digital core supply voltage (+2.5VDC)

Table 4. BGA 15- by 15-mm Package Pin Listing *(Continued)*

Pin	Signal Name	Type	Description
P15	UIC0_0	Bidirectional	Universal I/O Controller 0, pin 0
T17	UIC0_1	Bidirectional	Universal I/O Controller 0, pin 1
R16	UIC0_2	Bidirectional	Universal I/O Controller 0, pin 2
R17	UIC0_3	Bidirectional	Universal I/O Controller 0, pin 3
E14	GND	Ground	Digital ground
P16	UIC0_4	Bidirectional	Universal I/O Controller 0, pin 4
N15	UIC0_5	Bidirectional	Universal I/O Controller 0, pin 5
P17	UIC0_6	Bidirectional	Universal I/O Controller 0, pin 6
N16	UIC0_7	Bidirectional	Universal I/O Controller 0, pin 7
M16	UIC0_8	Bidirectional	Universal I/O Controller 0, pin 8
M15	VDDCLK	Power supply	Power Supply for the Crystal Oscillator (+2.5VDC)
N17	XTAL0	Clock	Crystal input pin 0 (Osc. In)
M17	XTAL1	Clock	Crystal input/output pin 1 (Osc. Out)
M14	GNDCLK	Ground	Digital ground
L16	UIC0_9	Bidirectional	Universal I/O Controller 0, pin 9
L15	UIC0_10	Bidirectional	Universal I/O Controller 0, pin 10
L17	UIC0_11	Bidirectional	Universal I/O Controller 0, pin 11
K17	UIC0_12	Bidirectional	Universal I/O Controller 0, pin 12
K16	UIC0_13	Bidirectional	Universal I/O Controller 0, pin 13
K15	UIC0_14	Bidirectional	Universal I/O Controller 0, pin 14
J17	UIC0_15	Bidirectional	Universal I/O Controller 0, pin 15
J16	UIC0_16	Bidirectional	Universal I/O Controller 0, pin 16
J15	UIC0_17	Bidirectional	Universal I/O Controller 0, pin 17
N4	GND	Ground	Digital ground
H17	UIC1_0	Bidirectional	Universal I/O Controller 1, pin 0
H16	UIC1_1	Bidirectional	Universal I/O Controller 1, pin 1
G17	UIC1_2	Bidirectional	Universal I/O Controller 1, pin 2
H15	UIC1_3	Bidirectional	Universal I/O Controller 1, pin 3
J4	VDDIO	Power	Digital I/O supply voltage (+3.3VDC)
G16	UIC1_4	Bidirectional	Universal I/O Controller 1, pin 4
F17	UIC1_5	Bidirectional	Universal I/O Controller 1, pin 5
E17	UIC1_6	Bidirectional	Universal I/O Controller 1, pin 6
G15	UIC1_7	Bidirectional	Universal I/O Controller 1, pin 7
F16	UIC1_8	Bidirectional	Universal I/O Controller 1, pin 8
D17	UIC1_9	Bidirectional	Universal I/O Controller 1, pin 9
L14	VDDC	Power	Digital core supply voltage (+2.5VDC)
E16	UIC1_10	Bidirectional	Universal I/O Controller 1, pin 10
F15	UIC1_11	Bidirectional	Universal I/O Controller 1, pin 11

Table 4. BGA 15- by 15-mm Package Pin Listing *(Continued)*

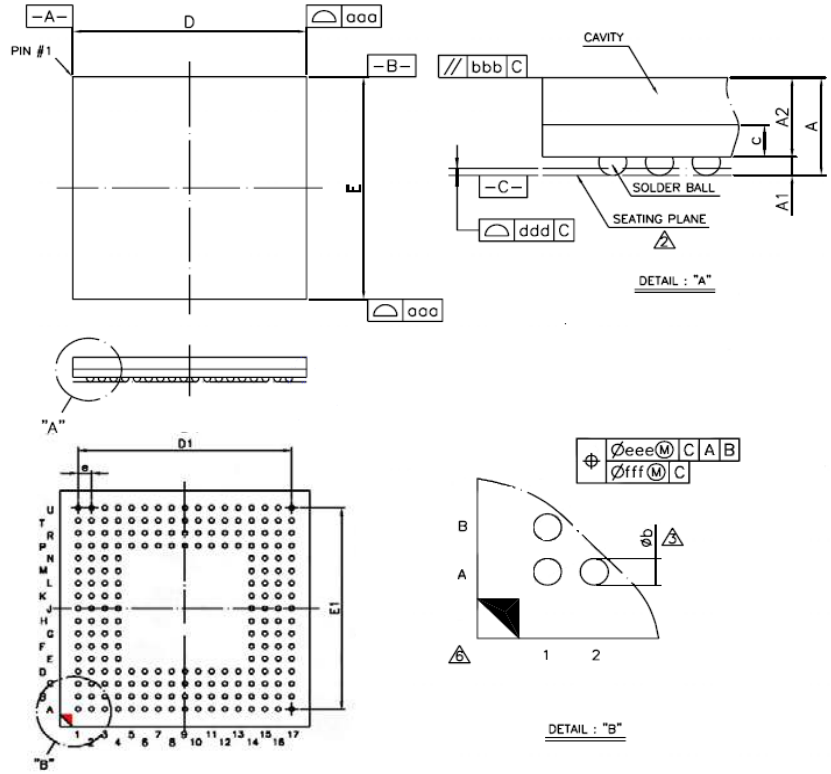
Pin	Signal Name	Type	Description
C17	UIC1_12	Bidirectional	Universal I/O Controller 1, pin 12
D16	UIC1_13	Bidirectional	Universal I/O Controller 1, pin 13
B17	UIC1_14	Bidirectional	Universal I/O Controller 1, pin 14
N14	GND	Ground	Digital ground
E15	UIC1_15	Bidirectional	Universal I/O Controller 1, pin 15
C16	UIC1_16	Bidirectional	Universal I/O Controller 1, pin 16
A17	UIC1_17	Bidirectional	Universal I/O Controller 1, pin 17
J14	VDDIO	Power	Digital I/O supply voltage (+3.3VDC)
B16	UIC2_0	Bidirectional	Universal I/O Controller 2, pin 0
C15	UIC2_1	Bidirectional	Universal I/O Controller 2, pin 1
D15	UIC2_2	Bidirectional	Universal I/O Controller 2, pin 2
F14	UIC2_3	Bidirectional	Universal I/O Controller 2, pin 3
P9	VDDC	Power	Digital core supply voltage (+2.5VDC)
C14	UIC2_4	Bidirectional	Universal I/O Controller 2, pin 4
B15	UIC2_5	Bidirectional	Universal I/O Controller 2, pin 5
A16	UIC2_6	Bidirectional	Universal I/O Controller 2, pin 6
A15	UIC2_7	Bidirectional	Universal I/O Controller 2, pin 7
P4	GND	Ground	Digital ground
B14	UIC2_8	Bidirectional	Universal I/O Controller 2, pin 8
C13	UIC2_9	Bidirectional	Universal I/O Controller 2, pin 9
A14	UIC2_10	Bidirectional	Universal I/O Controller 2, pin 10
B13	UIC2_11	Bidirectional	Universal I/O Controller 2, pin 11
K4	VDDIO	Power	Digital I/O supply voltage (+3.3VDC)
C12	UIC2_12	Bidirectional	Universal I/O Controller 2, pin 12
A13	UIC2_13	Bidirectional	Universal I/O Controller 2, pin 13
B12	UIC2_14	Bidirectional	Universal I/O Controller 2, pin 14
A12	UIC2_15	Bidirectional	Universal I/O Controller 2, pin 15
P5	GND	Ground	Digital ground
C11	UIC2_16	Bidirectional	Universal I/O Controller 2, pin 16
B11	UIC2_17	Bidirectional	Universal I/O Controller 2, pin 17
A11	UIC3_0	Bidirectional	Universal I/O Controller 3 pin 0
A10	UIC3_1	Bidirectional	Universal I/O Controller 3 pin 1
P10	VDDC	Power	Digital core supply voltage (+2.5VDC)
B10	UIC3_2	Bidirectional	Universal I/O Controller 3 pin 2
C10	UIC3_3	Bidirectional	Universal I/O Controller 3 pin 3
A9	UIC3_4	Bidirectional	Universal I/O Controller 3 pin 4
B9	UIC3_5	Bidirectional	Universal I/O Controller 3 pin 5

Table 4. BGA 15- by 15-mm Package Pin Listing *(Continued)*

Pin	Signal Name	Type	Description
C9	UIC3_6	Bidirectional	Universal I/O Controller 3 pin 6
A8	UIC3_7	Bidirectional	Universal I/O Controller 3 pin 7
B8	UIC3_8	Bidirectional	Universal I/O Controller 3 pin 8
A7	UIC3_9	Bidirectional	Universal I/O Controller 3 pin 9
P8	VDDIO	Power	Digital I/O supply voltage (+3.3VDC)
C8	UIC3_10	Bidirectional	Universal I/O Controller 3 pin 10
B7	UIC3_11	Bidirectional	Universal I/O Controller 3 pin 11
A6	UIC3_12	Bidirectional	Universal I/O Controller 3 pin 12
A5	UIC3_13	Bidirectional	Universal I/O Controller 3 pin 13
B6	GND	Ground	Digital Ground
C7	UIC3_14	Bidirectional	Universal I/O Controller 3 pin 14
A4	UIC3_15	Bidirectional	Universal I/O Controller 3 pin 15
B5	UIC3_16	Bidirectional	Universal I/O Controller 3 pin 16
C6	UIC3_17	Bidirectional	Universal I/O Controller 3 pin 17
A3	T0IC0_T0OC0	Bidirectional	Muxed pin, Timer Counter Unit 0 input capture 0 or output compare 0
B4	T0IC1_T0OC1	Bidirectional	Muxed pin, Timer Counter Unit 0 input capture 1 or output compare 1
A2	T0IC2_T0OC2	Bidirectional	Muxed pin, Timer Counter Unit 0 input capture 2 or output compare 2
C5	T0IC3_T0OC3	Bidirectional	Muxed pin, Timer Counter Unit 0 input capture 3 or output compare 3
P13	GND	Ground	Digital ground
B3	T1IC0_T1OC0	Bidirectional	Muxed pin, Timer Counter Unit 1 input capture 0 or output compare 0
A1	T1IC1_T1OC1	Bidirectional	Muxed pin, Timer Counter Unit 1 input capture 1 or output compare 1
B2	T1IC2_T1OC2	Bidirectional	Muxed pin, Timer Counter Unit 1 input capture 2 or output compare 2
C4	T1IC3_T1OC3	Bidirectional	Muxed pin, Timer Counter Unit 1 input capture 3 or output compare 3
C3	T0IN	Input	Timer Counter Unit 0 external clock source
D6	T1IN	Input	Timer Counter Unit 1 external clock source
P14	GND	Ground	Digital Ground
H14	VDDIO	Power	Digital I/O supply voltage (+3.3VDC)

4.2.2 BGA 15- by 15-mm Physical Package Dimensions

The physical dimensions for the BGA 15- by 15-mm package are as shown in Figure 5.



Notes:

1. Controlling dimension: Millimeter.

2. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.

3. Dimension b is measured at the maximum solder-ball diameter, parallel to primary datum C.

4. There will be a minimum clearance of 0.25 mm between the edge of the solder ball and the body edge.

5. Special Characteristics C Class: bbb ddd.

6. The pattern of Pin 1 fiducial is for reference only.

Legend:

Symbol	Dimension in mm			Dimension in Inches		
	MIN	NOM	MAX	MIN	NOM	MAX
A	–	–	1.20	–	–	0.047
A1	0.16	0.21	0.26	0.006	0.008	0.010
A2	0.84	0.89	0.94	0.033	0.035	0.037
c	0.32	0.36	0.40	0.013	0.014	0.016
D	14.90	15.00	15.10	0.587	0.591	0.594
E	14.90	15.00	15.10	0.587	0.591	0.594
D1	–	12.80	–	–	0.504	–
E1	–	12.80	–	–	0.504	–
e	–	0.80	–	–	0.031	–
b	0.25	0.30	0.35	0.010	0.012	0.014
aaa	0.10			0.004		
bbb	0.10			0.004		
ddd	0.12			0.005		
eee	0.15			0.006		
fff	0.08			0.003		
MD/ME	17/17			17/17		

Figure 5. BGA 15- by 15-mm Physical Package Dimensions

4.2.3 BGA 15- by 15-mm Signal Routing

The 15- by15-mm BGA can be easily routed using economical and readily available PCB fabrication design rules. In order to route all signals from the fido1100 BGA, 2 layers in addition to power and ground are required, using 0.1mm trace/space technology. Since 0.1mm = 3.937mil, most PCB fabricators will consider this 4mil trace/space.

The PCB land pattern for the BGA should use 0.3mm round pads. Since the BGA pitch is 0.8mm, this leaves 0.5mm of space between pads. Using 0.1mm trace/space, 2 signals may be routed between each pair of pads (2 traces + 3spaces = 0.5mm). Figure 8 shows how this is accomplished.

Referring to Figure 6, signal layer 1 is shown in black, signal layer 2 is shown in red, and the vias are shown in blue. Signal layer 1 is the top side with the BGA pads, while signal layer 2 may be any other layer, but is typically the bottom side. All vias with no trace routed out from the BGA are power or ground.

Note that the innermost row of pads is all power and ground, except for 9 pads which are signals. Three of these signals are easily routed on signal layer 1, but 6 of them require the use of vias and signal layer 2. If all of the signals are not required for a given design, it may be possible to route all of the used signals on signal layer 1.

It may be beneficial to place more vias and to route more signals on layers other than signal layer 1. This could produce a better PCB layout, but care should be exercised to not include an excessive number of vias. The use of too many vias can lead to inadequate copper on the power/ground plane layers surrounding the center area of the BGA, resulting in relative isolation of the BGA power/ground via connections.

Note the open space between pads M17 and N17 (A1 is upper left corner). These signals are XTAL1 and XTAL0. It is best not to route other signals between these pads, especially if a crystal is used for the clock source.

The power connections to the inner ring of pads have 4 vias for +3.3V and 4 vias for +2.5V. The use of a single bypass capacitor for each via, and alternating 0.1uF and 0.01uF values on each supply, provide reasonable bypass capacitance for the fido1100. Using 8 capacitors in this manner allows the use of capacitors in the 0603 package for economical PCB assembly.

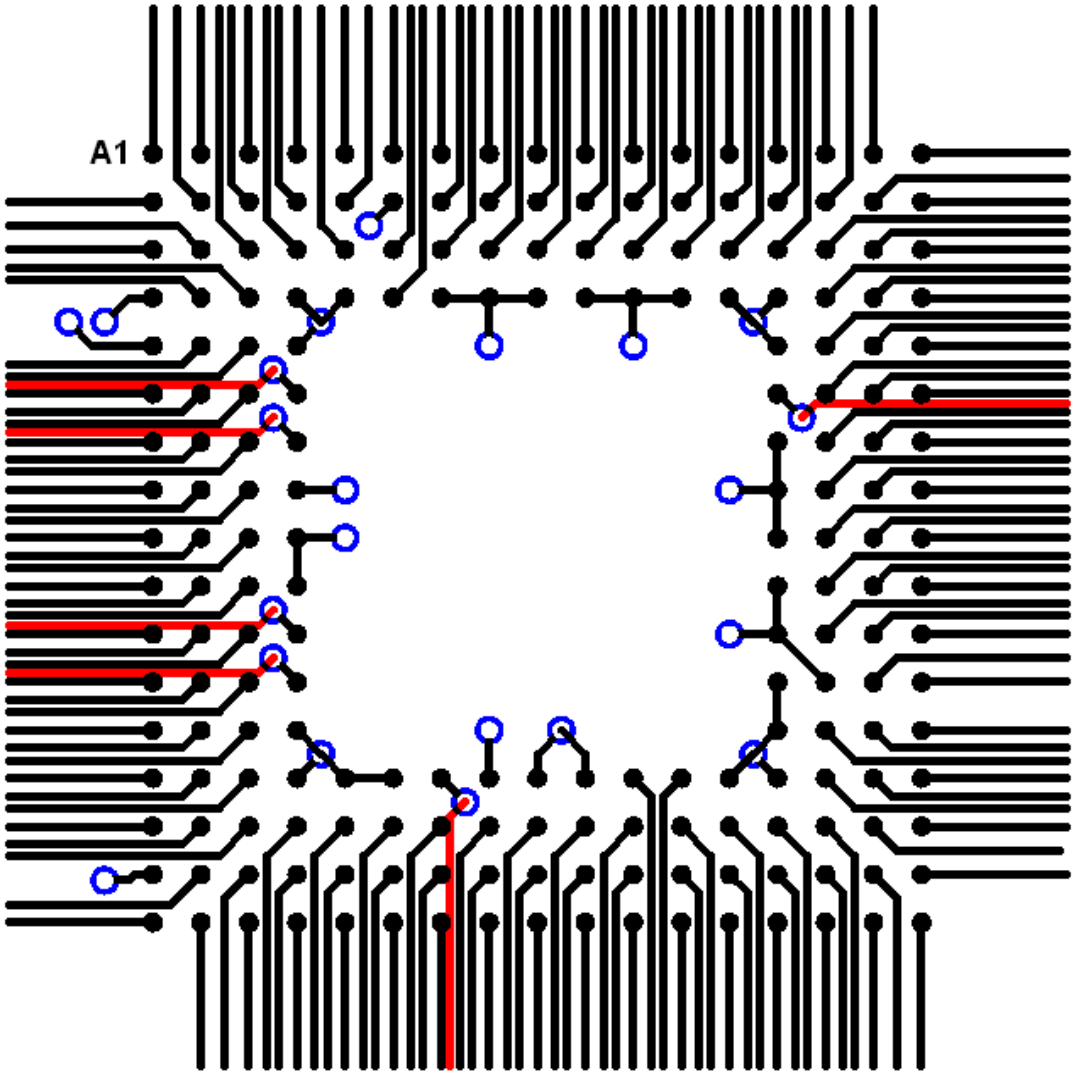


Figure 6. BGA 15- by 15-mm Signal Routing

4.3 Power and Ground Signals

Tables 5 - 9 provide analog power and ground signals, crystal oscillator power and ground signals, 2.5 VDC digital core power signals, 3.3 VDC digital IO power signals, and digital ground signals, respectively.

The recommended bypass capacitors for the fido1100 are:

- Use a mix of 0.1 µf and 0.01 µf capacitors.
- Bypass capacitors should be located as close as possible to power pins they are connected to.

Table 5. Analog Power and Ground Signals

PQFP	BGA 15 x 15	Signal Name	Type	Description
11	D1	VDDA	Power	Analog supply voltage (+3.3VDC)
12	E1	GNDA	Ground	Analog ground

Table 6. Crystal Oscillator Power and Ground Signals

PQFP	BGA 15 x 15	Signal Name	Type	Description
117	M15	VDDCLK	Power supply	Power Supply for the Crystal Oscillator (+2.5VDC)
120	M14	GNDCLK	Ground	Digital ground

Table 7. 2.5 VDC Digital Core Power Signals

PQFP	BGA 15 x 15	Signal Name	Type	Description
16	D7	VDDC	Power	Digital core supply voltage (+2.5VDC)
48	D8	VDDC	Power	Digital core supply voltage (+2.5VDC)
75	D9	VDDC	Power	Digital core supply voltage (+2.5VDC)
80	H4	VDDC	Power	Digital core supply voltage (+2.5VDC)
106	K14	VDDC	Power	Digital core supply voltage (+2.5VDC)
142	L14	VDDC	Power	Digital core supply voltage (+2.5VDC)
157	P9	VDDC	Power	Digital core supply voltage (+2.5VDC)
177	P10	VDDC	Power	Digital core supply voltage (+2.5VDC)
206	–	VDDC	Power	Digital core supply voltage (+2.5VDC)
–	–	VDDC	Power	Digital core supply voltage (+2.5VDC)

Table 8. 3.3 VDC Digital IO Power Signals

PQFP	BGA 15 x 15	Signal Name	Type	Description
22	D10	VDDIO	Power	Digital I/O supply voltage (+3.3VDC)
37	D11	VDDIO	Power	Digital I/O supply voltage (+3.3VDC)
65	D12	VDDIO	Power	Digital I/O supply voltage (+3.3VDC)
85	G14	VDDIO	Power	Digital I/O supply voltage (+3.3VDC)
135	J4	VDDIO	Power	Digital I/O supply voltage (+3.3VDC)
152	J14	VDDIO	Power	Digital I/O supply voltage (+3.3VDC)
167	K4	VDDIO	Power	Digital I/O supply voltage (+3.3VDC)
187	P8	VDDIO	Power	Digital I/O supply voltage (+3.3VDC)
–	H14	VDDIO	Power	Digital I/O supply voltage (+3.3VDC)

Table 9. Digital Ground Signals

PQFP	BGA 15 x 15	Signal Name	Type	Description
31	D4	GND	Ground	Digital ground
42	T1	GND	Ground	Digital ground
44	D5	GND	Ground	Digital ground
53	P6	GND	Ground	Digital Ground
60	D13	GND	Ground	Digital ground
70	D14	GND	Ground	Digital ground
90	E4	GND	Ground	Digital ground
111	E14	GND	Ground	Digital ground
130	N4	GND	Ground	Digital ground
148	N14	GND	Ground	Digital ground
162	P4	GND	Ground	Digital ground
172	P5	GND	Ground	Digital ground
182	B6	GND	Ground	Digital ground
192	P13	GND	Ground	Digital Ground
201	P14	GND	Ground	Digital ground
–	–	GND	Ground	Digital Ground

5. Electrical Characteristics

Tables 10 - 14 show the absolute maximum ratings, ESD and latch-up characteristics, recommended operating conditions, DC characteristics, and input impedance, respectively.

Table 10. Absolute Maximum Ratings

Symbol	Parameter Name	Conditions	Min	Typ	Max	Units
V_{DDC}	Digital core supply voltage	–	-0.3	–	3.05	V
V_{DDIO}	Digital I/O supply voltage	–	-0.3	–	5.5	V
V_{AIN}	Analog input voltage with respect to ground	–	-0.3	–	3.9	V
T_A	Ambient temperature	–	-40	–	+85	°C
T_S	Storage temperature	–	-55	–	+150	°C
T_J	Junction Temperature	–	-40	–	+125	°C

Note: Operation of the fido1100 outside of maximum operating ratings may result in failure of the device.

Table 11. ESD and Latch-Up Characteristics

Symbol	Parameter Name	Conditions	Min	Typ	Max	Units
V_{HBM}	Human body model	–	2000	–	–	V
V_{MM}	Machine model	–	200	–	–	V
I_{LATP}	Positive latch-up current	–	–	–	50	µA
I_{LATN}	Negative latch-up current	–	–	–	-50	µA

Table 12. Recommended Operating Conditions

Symbol	Parameter Name	Conditions	Min	Typ	Max	Units
V_{DDC}	Digital core supply voltage	–	2.25	2.5	2.75	V
V_{DDIO}	Digital I/O supply voltage	–	3.0	3.3	3.6	V
f_{XTAL}	Crystal frequency	–	–	–	66	MHz
T_A	Ambient temperature	–	-40	–	+85	°C
V_{DDA}	Analog supply voltage	–	3.0	3.3	3.6	V
V_{RH}	ADC reference voltage—high	–	–	3.0	–	V
V_{RL}	ADC reference voltage—low	–	–	0	–	V
C_L	Digital output load capacitance	See note	–	3.1	–	pF

Note: This parameter is guaranteed by design and not tested in production.

Table 13. DC Characteristics

T_A = –40°C and +85°C; V_{DDC} = 2.5V ± 10%; V_{DDIO} = 3.3V ± 10%; F_{CLK} = 66MHz

Symbol	Parameter Name	Conditions	Min	Typ	Max	Units
V_{IH}	Input high voltage	–	2.0	–	–	V
V_{IL}	Input low voltage	–	–	–	0.8	V
I_{LKG}	Input leakage current	–	-10	1	10	µA
C_{IN}	Input capacitance	–	–	3.6	–	pF
V_{OH}	Output high voltage	|IOH| = 8 mA	2.4	–	–	V
V_{OL}	Output low voltage	|IOL| = 8 mA	–	–	0.4	V
I_{OZ}	Tri-state leakage	–	-10	1	10	µA
C_{OUT}	Package output capacitance	–	–	3.6	–	pF

Table 14. Input Impedance

Input leakage current:	± 10 µA with no pull-up/pull-down
Tristate leakage current:	± 10 µA
Pin capacitance (input or output):	~3.5 pF not including package contribution

Table 15. AC Characteristics of Crystal Oscillator

Symbol	Parameter	Conditions	Typ	Max	Units
f_{OSC}	Crystal oscillator range	TA = 25ºC	–	66	MHz
t_{ST}	Startup time	TA = 25ºC	20	–	ms

Table 16. Analog-to-Digital Converter Characteristics

Symbol	Parameter Name	Conditions	Min	Typ	Max	Units
V_{INA}	Input voltage range	–	$0.1V_{DDA}$	-	$0.9V_{DDA}$	V
C_{INA}	Input capacitance	–	–	20	–	pF
Res	Resolution	–	–	10	–	Bits
INL	Integral non-linearity	–	–	± 2	–	Lsb
DNL	Differential non-linearity	guaranteed no missing codes	–	± 1	–	Lsb
SINAD	Signal to noise plus distortion	Fin = 10 KHz	–	54	–	dB
FSMPL	Sample clock frequency	–	0.5	–	2.6	MHz
P_D	Power dissipation	TA = 25ºC	–	5	–	mW
SMP	Sample rate	–	–	–	200	Ksps

Notes:
1. The ADC in the fido1100 uses its own VDD (VDDA) and GND (GNDA) connections along with VREF High (VRH) and VREF Low (VRL) signals.
2. VRH must be less than or equal to VDDA.
3. VRL must be greater than or equal to GNDA.
4. To ensure maximum conversion accuracy, VDDA, GNDA, VRH, and VRL should be as clean and free of noise as possible.

Table 17. Power Consumption

Conditions	Core Voltage 2.5 VDC		I/O Voltage 3.3 VDC		Total
	Current	Power	Current	Power	Power
Halted after a Reset	109.240 mA	273.100 mW	2.500 mA	8.25 mW	281.35 mW
Light Processing Load	214.000 mA	535.000 mW	7.700 mA	25.41 mW	560.41 mW
Heavy Processing Load	227.000 mA	567.500 mW	17.000 mA	56.1 mW	623.60 mW
Sleep Mode					320.90 mW
Stop Mode					302.91 mW
Low Power Stop Mode (LPSTOP)					8.68 mW

6. Thermal Characteristics

The thermal resistance characteristics for the 28 x 28 mm PQFP and the 15 x 15 mm BGA packages are provided in Table 18. All data is simulated based on the 2S2P board type. The board type is defined by JEDEC standard JESD51-7 for the PQFP package and by JESD51-9 for the BGA package.

Table 18. Thermal Resistance Characteristics

Name	Description	Airflow (m/S)	15 x 15 mm BGA	28 x 28 mm PQFP
θ_{JC} (°C/W)	Junction to Case	0	7.2	16.3
θ_{JA} (°C/W)	Junction to Ambient	0	56.8	35.1
θ_{JA} (°C/W)	Junction to Ambient	1	51.1	30.9
θ_{JA} (°C/W)	Junction to Ambient	2	48.8	28.7
θ_{JA} (°C/W)	Junction to Ambient	3	47.2	27.5

7. Reset

7.1 Overview

This section describes the reset signal considerations and the reset timing. The Power On Reset Register has a control bit to determine whether Major Reset or Minor Reset processing is performed after reset is asserted. The section below presents the hardware signal characteristics. See *The fido1100 User Guide* for more details on the Power On Reset Control Register.

7.2 Signal Considerations and Reset Timing

The fido1100 requires the RESET_N signal to be asserted LOW for a minimum of 100 µS after VDDIO and VDDC are at their nominal values and stable. The RESET_N signal must have a rise time of less than 100 nS. Table 19 presents the hardware signals involved or affected and should be considered when asserting reset.

Table 19. Hardware Signals Involved When Asserting Reset

Signal Name	Type	Description
RESET_N	Input	Reset input
RESET_OUT_N	Output	Reset output
A_25_RESET_DELAY	Muxed, Internal Pull-up	Muxed pin, External Bus Interface address Bit [25] or POR counter bypass
A_26_SIZE	Muxed, Internal Pull-up	Muxed pin, External Bus Interface address Bit [26] or data bus size select (0 = 8-bit, 1 = 16-bit)
A27_CS7_N	Muxed	Muxed pin, External Bus Interface address Bit [27] or Chip select 7 (chip select active low)
A28_CS6_N	Muxed	Muxed pin, External Bus Interface address Bit [28] or Chip select 6 (chip select active low)
A29_CS5_N	Muxed	Muxed pin, External Bus Interface address Bit [29] or Chip select 5 (chip select active low)
A30_CS4_N	Muxed	Muxed pin, External Bus Interface address Bit [30] or Chip select 4 (chip select active low)
CS0_N	Output	Chip select 0 (chip select active low)

When RESET_N is asserted, the following sequence occurs:

- The A25_Reset_Delay signal is sampled to determine the length of the reset clock delay
  - Low—reset clock delay → 100 µsecs
  - High—reset clock delay → 20 msecs

  Note: After this delay, the part performs major or minor reset processing and is released to run.
- The A_26_SIZE pin is sampled for the external bus interface size
  - Low—8-bit width
  - High—16-bit width

- The RESET_OUT_N signal is driven low for the determined clock delay

Figures 7 and 8 present the reset timing and extended reset timing diagrams, respectively. The A_26_SIZE signal is not shown, but it is sampled.

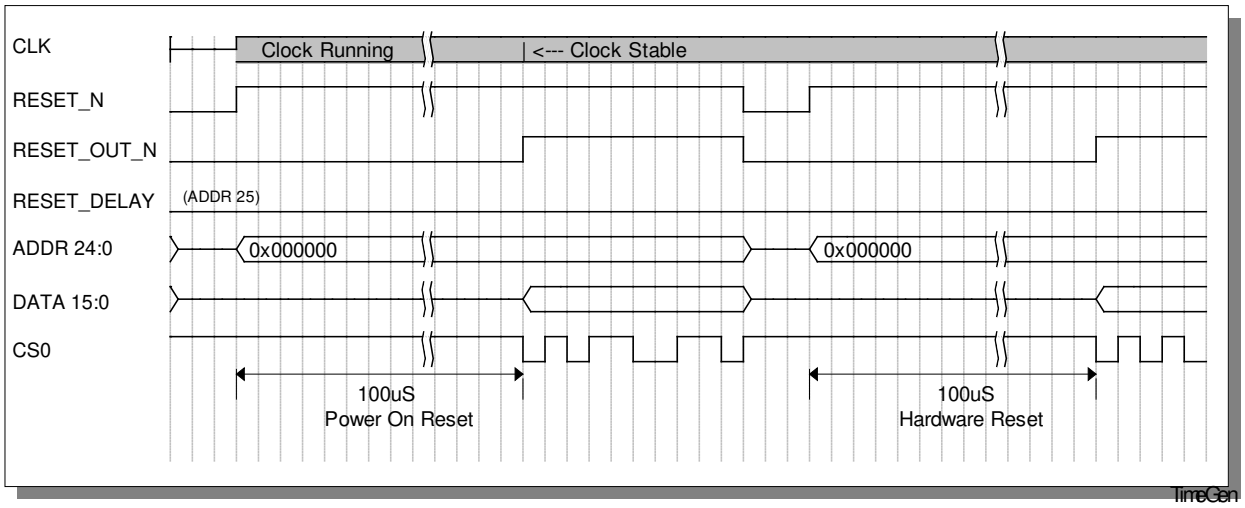


Figure 7. Reset Timing

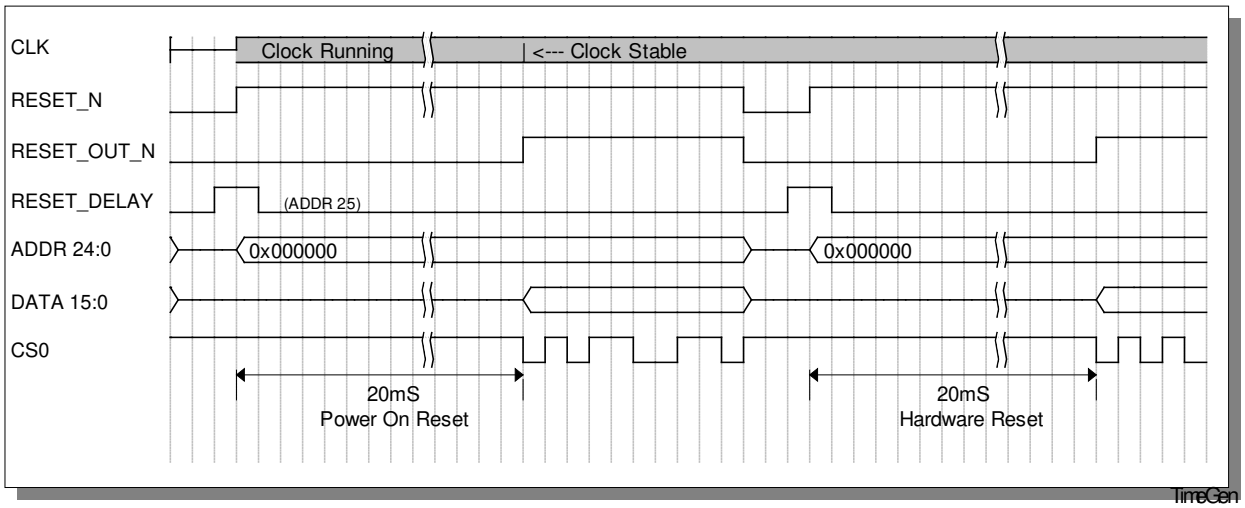


Figure 8. Extended Reset Timing

Note: If A25_RESET_DELAY is high at the rising edge of RESET_N, internal reset and RESET_OUT_N are extended from 100 µs to 20 mS.

The following multiplexed signals are tri-stated during reset and should be pulled high if being used as chip selects or pulled low if being used as address lines (the fido1100 boots at address 0x00000000). If not being used, they can be pulled either high or low.

- A27_CS7_N
- A28_CS6_N
- A29_CS5_N
- A30_CS4_N

At Reset, the CS0_N signal defaults to low for external memory access, supporting the boot sequence from address 0x00000000.

7.3 Clock Signals

7.4 Typical Clock Source Implementations

The fido1100 can operate in one of two modes: (1) Normal or driven clock source input or (2) using an external crystal to set the operating frequency of the internal oscillator.

> *Note: VDDCLK and GNDCLK must be connected even when not using an external crystal.*

7.4.1 Normal or Driven Clock Source

System configuration—Drive external clock source into XTAL0 (see Figure 9). XTAL1 is left unconnected. XTAL0 is effectively a Schmitt trigger input. Target frequency should have a duty cycle of approximately 40% to 60%.

7.4.2 Using an External Crystal

- System Configuration (third overtone)—Crystal across XTAL0/XTAL1 (see Figure 10), 36 pF load caps to ground, 0.1-µF cap, and 0.33-µH inductor in series from XTAL1 to ground.

- System Configuration (fundamental tone)—Crystal across XTAL0/XTAL1 (see Figure 11) and 20-pF load caps to ground.

> *Note: Load capacitor and inductor values may be different based on crystal used. Please consult with your crystal supplier for more information.*

Third overtone configuration is recommended for 24- to 66-MHz operation and fundamental tone configuration is recommended for 1- to 24-MHz operation.

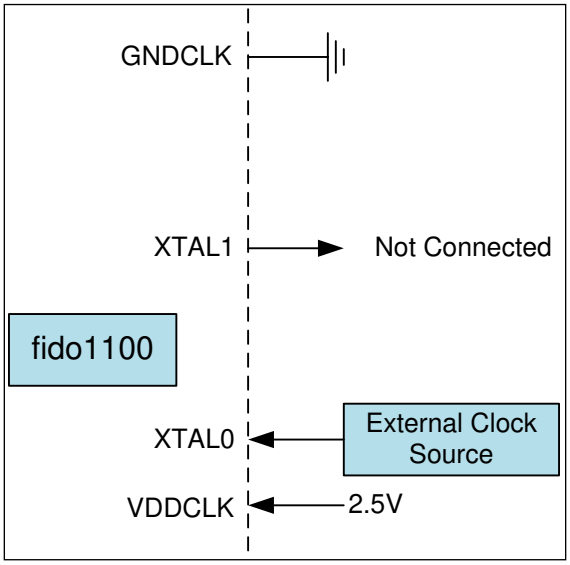


Figure 9. Driven Clock Source

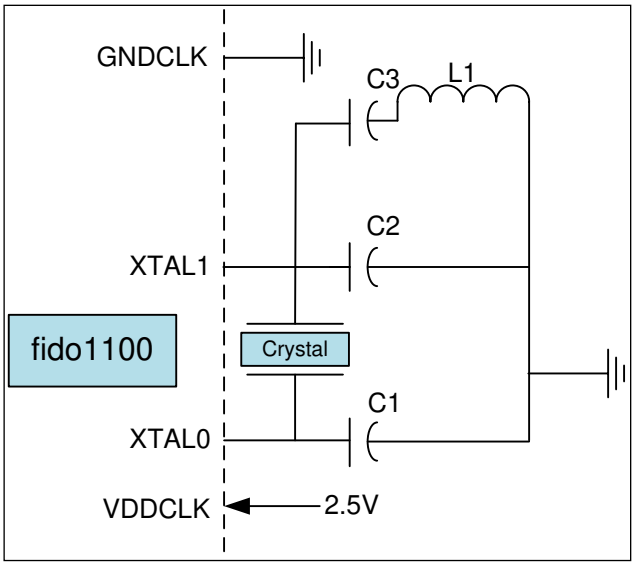


Figure 10. Crystal Oscillator Third Overtone Off-Chip Components

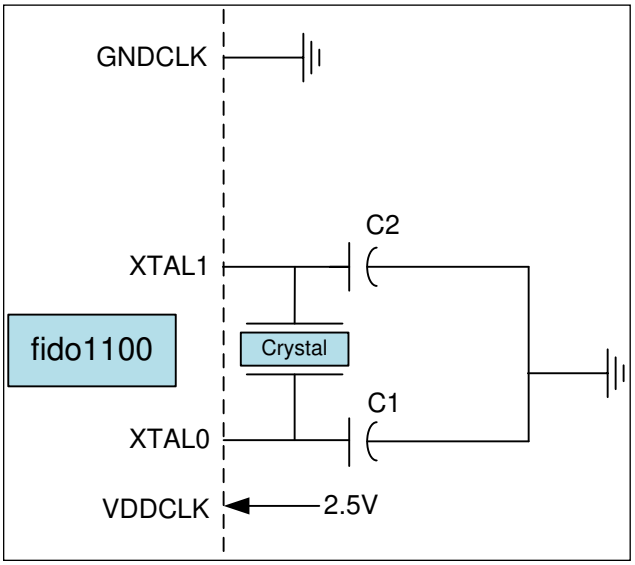


Figure 11. Crystal Oscillator Fundamental Overtone Off-Chip Components

7.5 Off-Chip Component Value

Table 20 shows the suggested off-chip component values:

Table 20. Suggested Off-Chip Component Values

Operating frequency	C1	C2	C3	L1
66MHz	36pF	36pF	0.1µF	330nH
20 MHZ	20pF	20pF	NA	NA

Notes:
1. Different C1, C2 values lead to different oscillation characteristics and should be selected based on system (board) level considerations.
2. Using C1 = C2 is recommended.

8. Signals

8.1 External Bus Operation

8.1.1 Overview

The fido1100 interfaces to external memory and peripherals through a set of programmable chip-select and bus-timing registers. It also has a built-in SDRAM controller to interface to SDRAM. This chapter provides timing diagrams for hardware considerations.

For definitions of registers that control external bus timing and the SDRAM timing, please see *The fido1100 User Guide*.

The external address bus of the fido1100 is 31-bit, and the external data bus is configurable to support either an 8- or 16-bit bus. In this section, timing diagrams are provided for the following:

- General Setup and Hold Timing
- External Bus Timing
  - 32-bit transfer without external ready (RDY_N)
  - 32-bit transfer with external ready (RDY_N)
  - 8-bit/16-bit single cycle without external ready (RDY_N)
  - 8-bit/16-bit cycle with external ready (RDY_N)
- SDRAM Timing
  - SDRAM CAS Timing
  - SDRAM Row Activation Timing
  - SDRAM Read Operation Timing
  - SDRAM Read Burst Timing
  - SDRAM Write Operation, Write Burst, Write-to-Write Operation, and Write-to-Precharge Timing

8.2 General Setup and Hold Timing

All timing delays are characterized at the 50% to 50% point. This includes propagation delay times through combinatorial functions as well as setup, hold time, and release-time definitions for sequential elements (see Chapter 9, Setup and Hold Timing, for diagrams).

8.3 External Bus Timing

Signals listed on the External Bus Timing diagrams are described below.

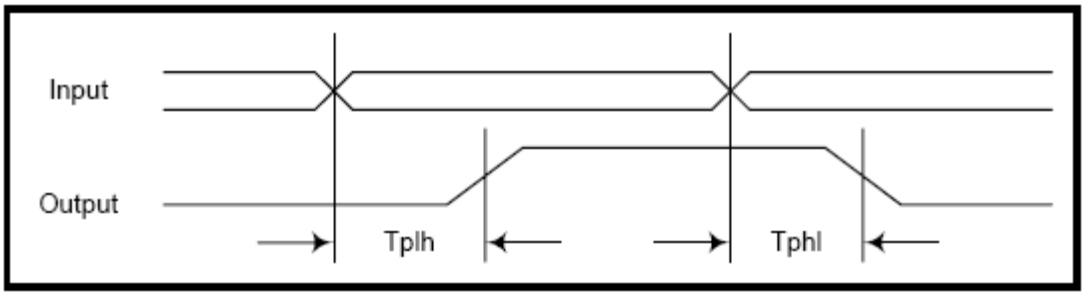
- TwWAIT
  - If RDY_ENABLE=0, specifies the width of the chip select active period for the non-burst-mode write cycle. The allowed range is 0–31, resulting in a wait time of 1–32 clocks.
  - If RDY_ENABLE=1, specifies the wait time before the RDY_N line is first sampled for the write cycle. This provides a max wait time of 484 nS at 66 MHz. Anything greater than this will require the external RDY_N line and external logic.

- TrWAIT
  - If RDY_ENABLE=0, specifies the width of the chip select active period for the non-burst-mode read cycle. The allowed range is 0–31, resulting in a wait time of 1–32 clocks.
  - If RDY_ENABLE=1, specifies the wait time before the RDY_N line is first sampled for the read cycle. This provides a max wait time of 484 nS at 66 MHz. Anything greater than this will require the external RDY_N line and external logic.

9. Setup and Hold Timing

All timing delays are characterized at the 50% to 50% point. This includes propagation delay times through combinatorial functions as well as setup, hold-time, and release-time definitions for sequential elements.

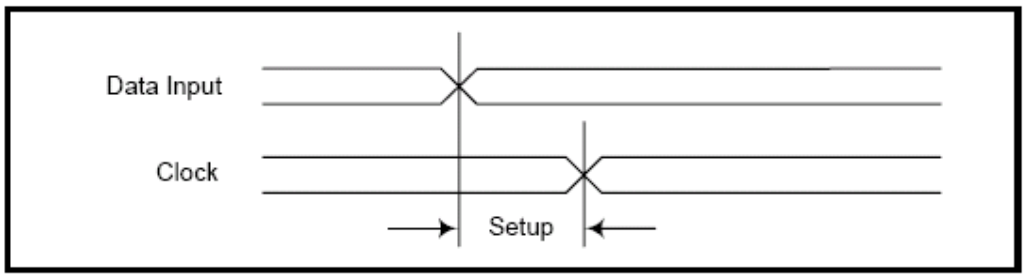
- Propagation Delay—Time between an input signal transition and the resultant output signal transition (see Figure 12).



Tplh = 14ns.
Tphl = 14ns.

Figure 12. Propagation Delay

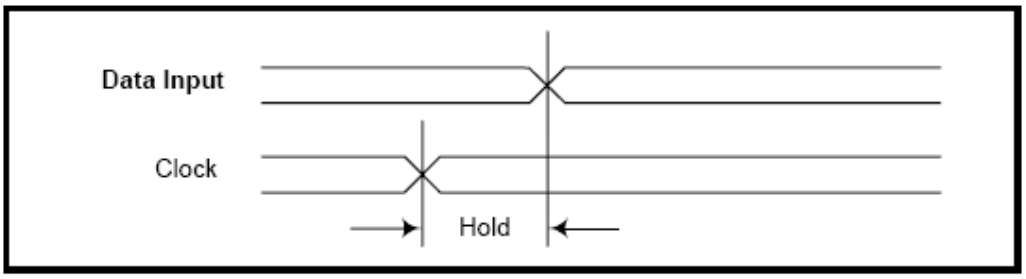
- Setup Time—The minimum time that input data must remain unchanged prior to an active clock transition (see Figure 13).



Setup = 2ns.

Figure 13. Setup Time

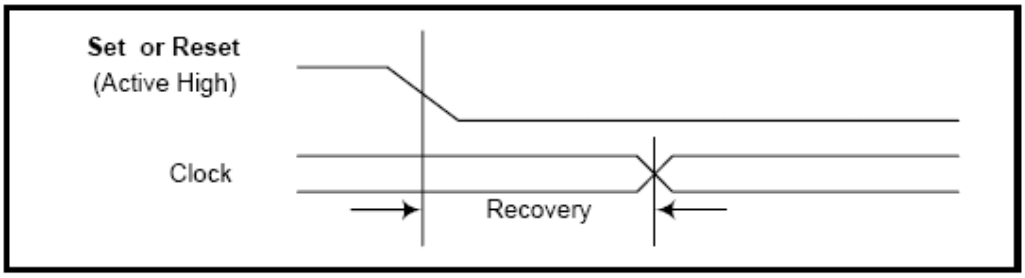
- Hold Time—The minimum time that input data must remain unchanged subsequent to an active clock transition (see Figure 14).



Hold = 2ns.

Figure 14. Hold Time

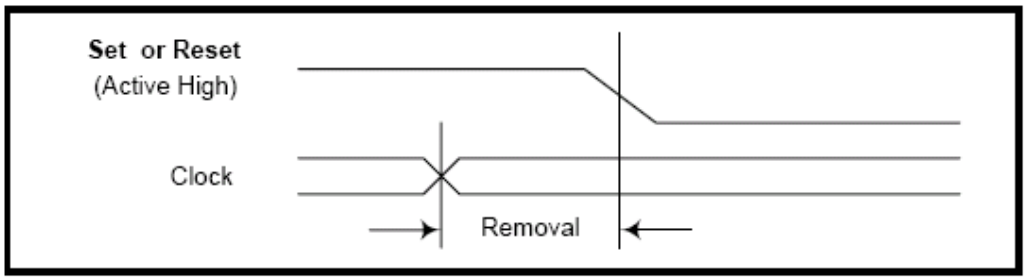
- Recovery Time—The minimum time that the Set or Reset input must remain unactivated prior to an active clock transition (see Figure 15).



Recovery = 3ns.

Figure 15. Recovery Time

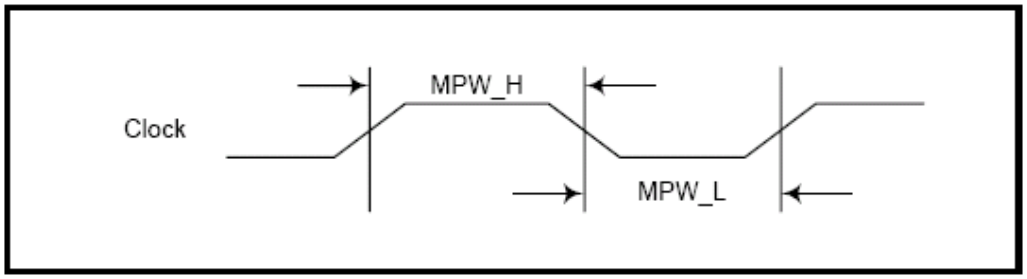
- Removal Time—The minimum time that the Set or Reset input must remain activated subsequent to an active clock transition (see Figure 16).



Removal = 3ns.

Figure 16. Removal Time

- Minimum Pulse Width—The minimum length of time between the leading and trailing edges of a pulse (see Figure 17).



Timings are based on a 66-MHz clock yielding 15-ns cycles.
MPW_H = 7ns.
MPW_L = 7ns.

Figure 17. Minimum Pulse Width

- THLD—Specifies the time between when the CSn_N and BEn_N signals go inactive (hi) and the address is removed, 0–7 clocks.
- TCS—Specifies the time between when the address bus is driven and the CSn_N and BEn_N signals go active (low), 0–3 clocks.
- TOE—Specifies the time between when the CSn_N and BEn_N signals go active (low) and the OE signal goes active (low), 0–3 clocks.
- TWEF—Specifies the time between when the CSn_N and BEn_N signals go active (low) and the WE_N signal goes active (low), 0–3 clocks.
- TWER—Specifies the time between when the WE_N signal goes inactive (hi) and the CSn_N and BEn_N signals go inactive (hi), 0–3 clocks.

9.1.1 External Bus Timing for a 32-Bit Transfer (without RDY_N)

This timing is programmable via the External Bus Chip Select Timing Register (see Figure 18).

- All timing is relative to the rising edge of the clock.
- The chip-select and byte-enable signals (CSn_N and BEn_N) go active (low) 0–3 clocks (TCS) after the address bus is driven.
- The chip-select, output-enable, and byte-enable signals (CSn_N, BEn_N, and OE_N) go inactive (hi) 0–7 clocks (THLD) before the address is removed (on the last cycle).

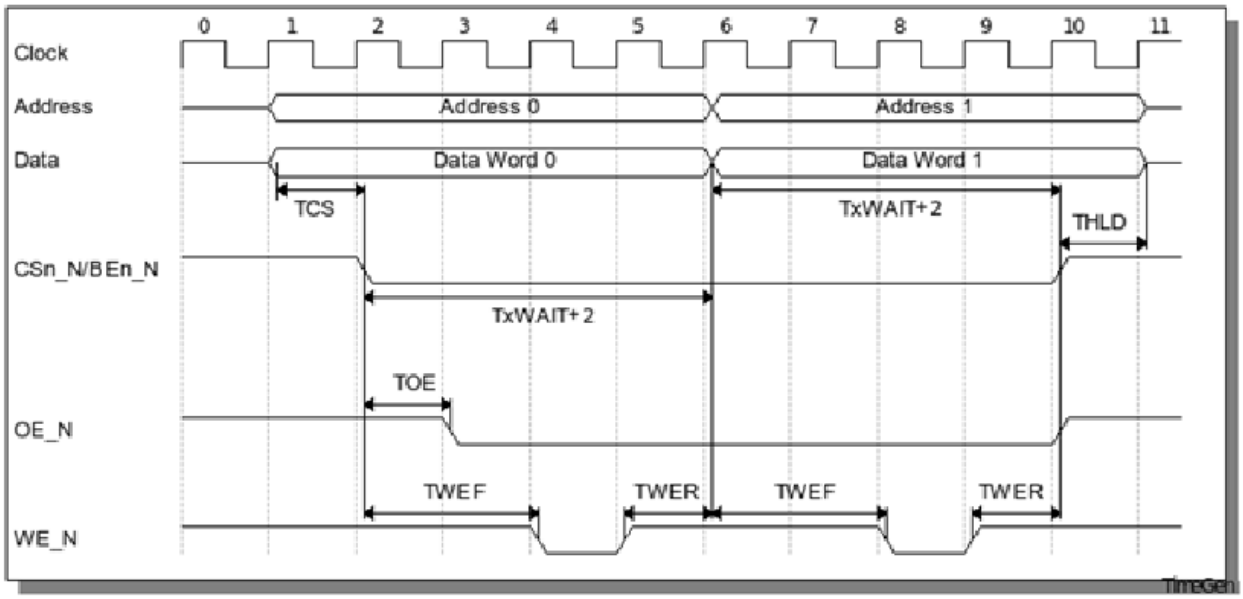


Figure 18. External Bus Timing for a Single, 32-Bit Cycle (without RDY_N)

- The write-cycle timing is controlled by TwWAIT setting (shown as TxWAIT in the diagram), 2-33 clocks.The read-cycle timing is controlled by TrWAIT setting (shown as TxWAIT in the diagram), 2-33 clocks.
- The output-enable signal (OE_N) goes active (low) 0–3 clocks (TOE) after the chip select.
- The output-enable signal (OE_N) goes inactive (hi) coincident with the chip select.
- The write-enable signal (WE_N) goes active (low) 0–3 clocks (TWEF) after the chip select (first cycle only). For subsequent cycles, the WE_N line will go active (low) 0–3 clocks (TWEF) after the address bus changes.
- The write-enable signal (WE_N) goes inactive (hi) 0–3 clocks (TWER) before the end of the wait time and hence before the address bus changes (subsequent cycles). This is when the data is considered "written."

9.1.2 External Bus Timing for a 32-Bit Transfer (with RDY_N)

This timing is programmable via the External Bus Chip Select Timing Register (see Figure 19).

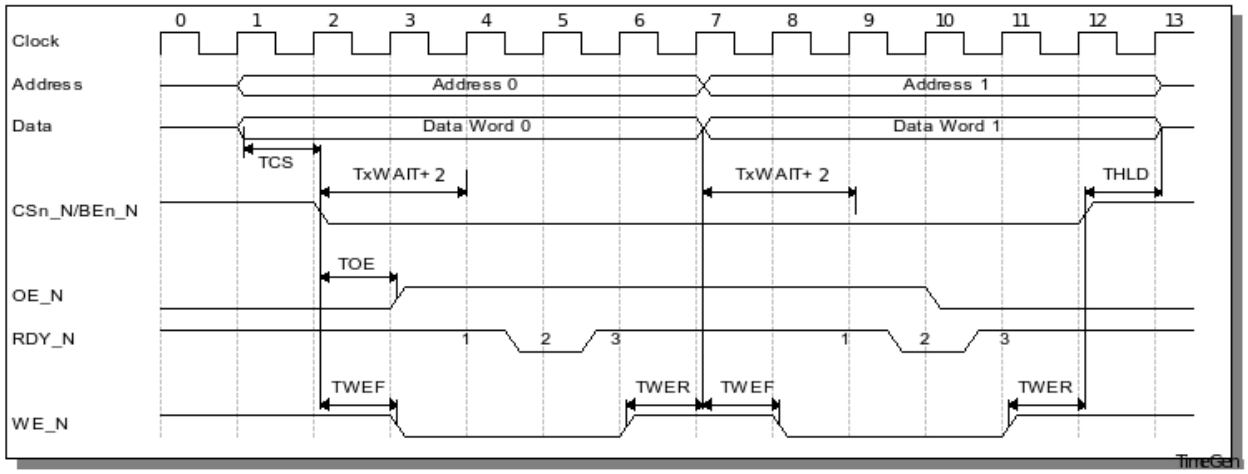


Figure 19. External Bus Timing for a 32-Bit Transfer (with RDY_N)

- The TxWAIT setting determines when first to start sampling the low active RDY_N line (labeled with an arrow marked “1” in the diagram).
- In the case of a write transfer after the low active RDY_N line is first sampled low (labeled with an arrow marked “2” in the diagram), the write cycle will complete on the next rising edge of the clock as shown (labeled with an arrow marked “3” in the diagram).
- In the case of a read transfer once the low active RDY_N line is first sampled low (labeled with an arrow marked “2” in the diagram), the read data will be sampled on the second rising edge of the clock.
- The write-cycle timing is controlled by TwWAIT setting (shown as TxWAIT in the diagram), 2-33 clocks.
- The read-cycle timing is controlled by TrWAIT setting (shown as TxWAIT in the diagram), 2-33 clocks.
- If the RDY_N line never goes low, the cycle will end (as a bus error) after a timeout of TxWAIT + 256 clocks.
- If the RDY_N line is unused (tied low via an internal pull down) or goes low immediately, the cycle will be controlled by TxWAIT as described above.
- In the case of a write transfer, the write-enable signal (WE_N) goes active (low) 0–3 clocks after the CS_N goes low.

- The write-enable signal (WE_N) goes inactive (hi) 0–3 clocks (TWER) before the end of the chip-select time.

9.1.3 External Bus Timing for 8-Bit/16-Bit Transfer (without RDY_N)

This timing is programmable via the External Bus Chip Select Control Register (see Figure 20).

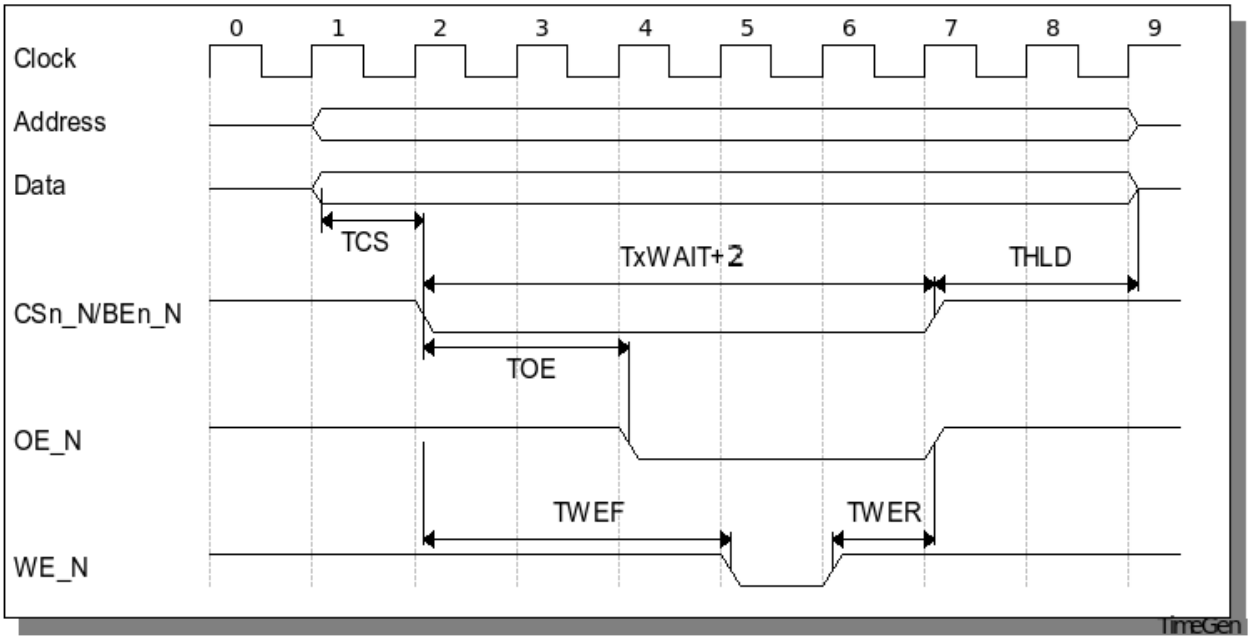


Figure 20. External Bus Timing for 8-Bit/16-Bit Transfer (without RDY_N)

- All timing is relative to the rising edge of the clock.
- The chip-select and byte-enable signals (CSn_N and BEn_N) go active (low) 0–3 clocks (TCS) after the address bus is driven.
- The chip-select and byte-enable signals (CSn_N and BEn_N) go inactive (hi) 0–7 clocks (THLD) before the address is changed.
- The write-cycle timing is controlled by TwWAIT setting (shown as TxWAIT in the diagram), 2-33 clocks.
- The read-cycle timing is controlled by TrWAIT setting (shown as TxWAIT in the diagram), 2-33 clocks.
- The output-enable signal (OE_N) goes active (low) 0–3 clocks (TOE) after the chip select.

- The output-enable signal (OE_N) goes inactive (hi) coincident with the chip select. This is also when the read data is sampled.
- The write-enable signal (WE_N) goes active (low) 0–3 clocks (TWEF) after the chip select.
- The write-enable signal (WE_N) goes inactive (hi) 0–3 clocks (TWER) before the end of the cycle (CSn_N is removed).

9.1.4 External Bus Timing for 8-Bit/16-Bit Transfer (with RDY_N)

This timing is programmable via the External Bus Chip Select Control Register (see Figure 21).

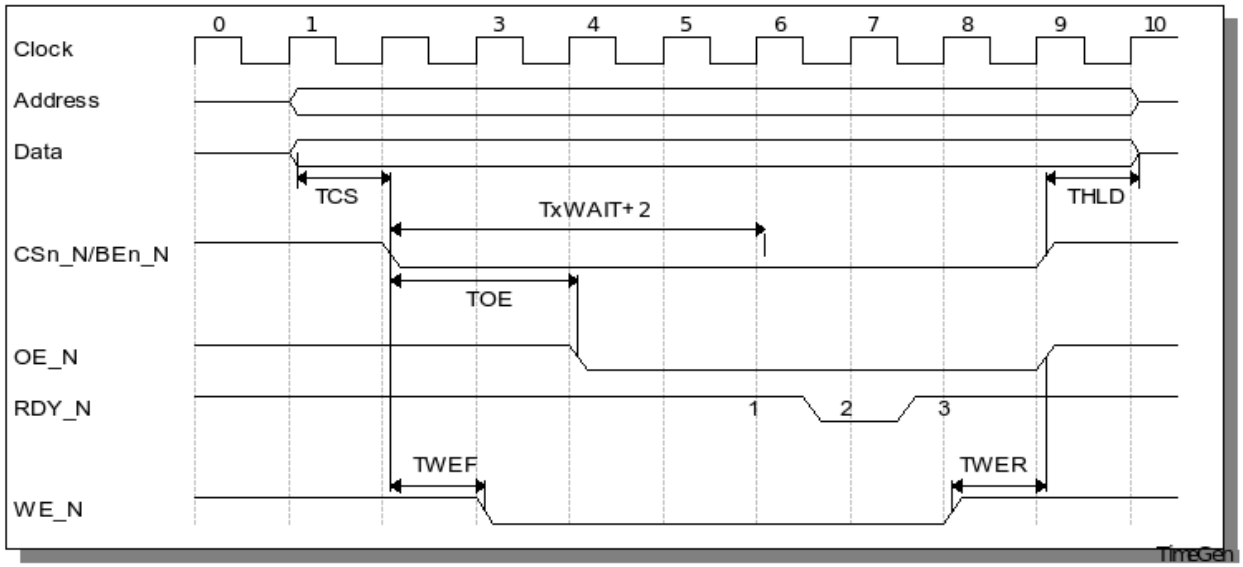


Figure 21. External Bus Timing for 8-Bit/16-Bit Transfer (with RDY_N)

- The write-cycle timing is controlled by TwWAIT setting (shown as TxWAIT in the diagram), 2-33 clocks.
- The read-cycle timing is controlled by TrWAIT setting (shown as TxWAIT in the diagram), 2-33 clocks.
- The TxWAIT setting determines when first to start sampling the low active RDY_N line (labeled with an arrow marked “1” in the diagram).
- In the case of a write transfer, once the low active RDY_N line is first sampled low (labeled with an arrow marked “2” in the diagram), the write cycle will complete on the

next rising edge of the clock as shown (labeled with an arrow marked "3" in the diagram).

- In the case of a read transfer, once the low active RDY_N line is first sampled low (labeled with an arrow marked "2" in the diagram), the read data will be sampled on the second rising edge of the clock.
- If the RDY_N line never goes low, the cycle will end (as a bus error) after a timeout of TxWAIT + 256 clocks.
- If the RDY_N line is unused (tied low via an internal pull down) or goes low immediately, the cycle will be controlled by TxWAIT as shown above.
- In the case of a write transfer, the write enable signal (WE_N) goes active (low) 0–3 clocks after the CS_N goes low.
- The write enable signal (WE_N) goes inactive (hi) 0–3 clocks (TWER) before the end of the chip-select time.

Note: This timing picture also reflects the default bus timing for all memory addresses not decoded by the internal chip-select unit. In this case, the timing is controlled by the External Bus Default Timing Register.

9.2 SDRAM Timing

9.2.1 SDRAM CAS Timing

The CAS latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first piece of output data. The latency can be set to two or three clocks. If a READ command is registered at clock edge *n*, and the latency is *m* clocks, the data will be available by clock edge $n + m$. The DQs will start driving because of the clock edge one cycle earlier ($n + m - 1$) and, provided the relevant access times are met, the data will be valid by clock edge $n + m$. For example, assuming the clock cycle time is such that all relevant access times are met, if a READ command is registered at T0 and the latency is programmed to two clocks, the DQs will start driving after T1 and the data will be valid by T2, as shown in Figure 22.

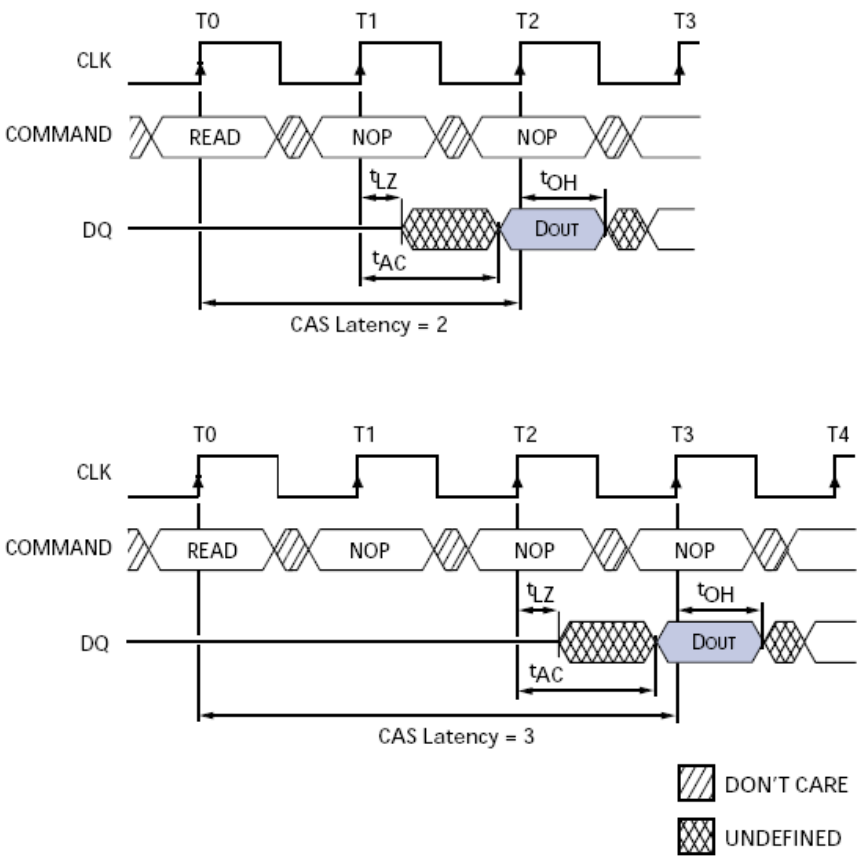


Figure 22. SDRAM CAS Timing

9.2.2 SDRAM Row Activation Timing

Before any READ or WRITE commands can be issued to a bank within the SDRAM, a row in that bank must be "opened." This is accomplished via the ACTIVE command, which selects both the bank and the row to be activated (see Figure 23). After opening a row (issuing an ACTIVE command), a READ or WRITE command may be issued to that row, subject to the tRCD specification. The tRCD (MIN) should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVE command on which a READ or WRITE command can be entered. For example, a tRCD specification of 20ns with a 125-MHz clock (8-ns period) results in 2.5 clocks, rounded to 3. This is reflected in Figure 24, which covers any case where $2 < \text{tRCD (MIN)/tCK} \leq 3$. (The same procedure is used to convert other specification limits from time units to clock cycles.)

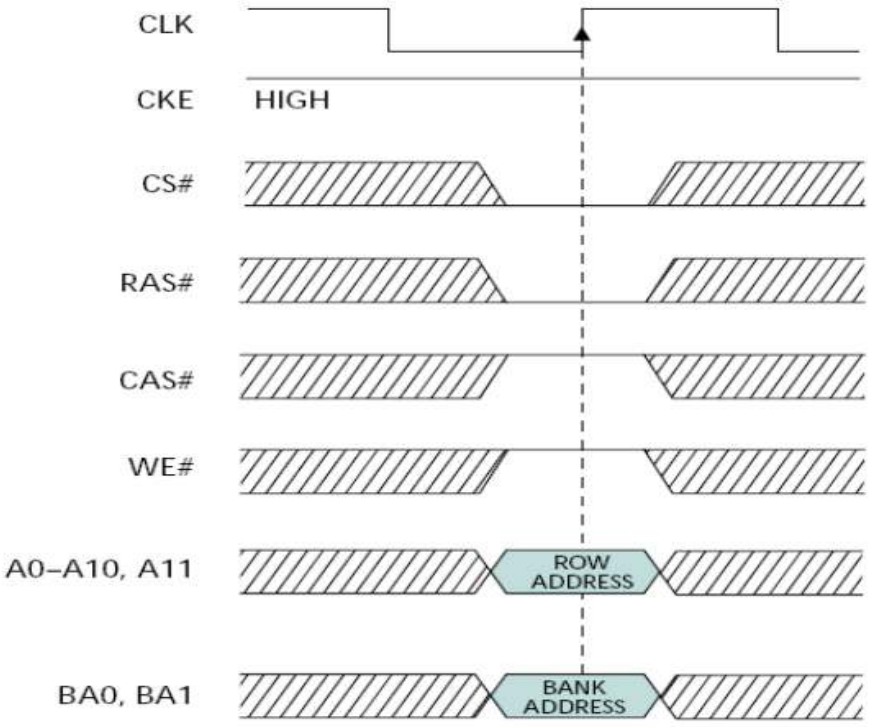


Figure 23. Specific Row Activation Timing

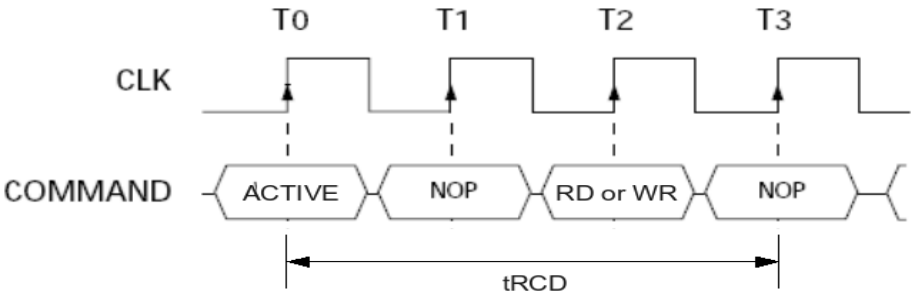


Figure 24. Meeting tRCD (min) When 2 < tRCD (min)/tCK ≤ 3

9.2.3 SDRAM Read Operation Timing

READ bursts are initiated with a READ command.

The starting column and bank addresses are provided with the READ command, and auto precharge is either enabled or disabled for that burst access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. For the generic READ commands used in the following illustrations, auto precharge is disabled (see Figure 25).

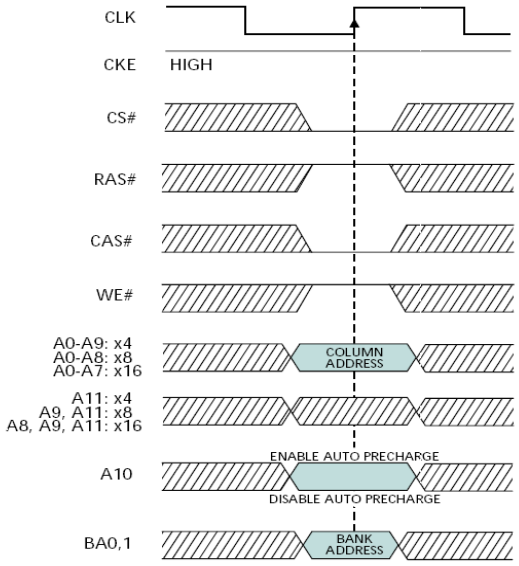


Figure 25. SDRAM Read Operation Timing

During READ bursts, the valid data-out element from the starting column address will be available following the CAS latency after the READ command. Each subsequent data-out element will be valid by the next positive clock edge.

Upon completion of a burst, assuming no other commands have been initiated, the DQs will go high, and full-page burst will continue until terminated. (At end of the page, it will wrap to column 0 and continue.)

9.2.4 SDRAM Read Burst Timing

Data from any READ burst may be truncated with subsequent READ command, and data from a fixed-length READ burst may be immediately followed by data from a READ command. In either case, a continuous flow of data can be maintained. The first data element from the new burst follows either the last element of a completed burst or the last desired data element of a

longer burst that is being truncated. The new READ command should be issued *x* cycles before the clock edge at which the last desired data element is valid, where *x* equals the CAS latency minus one (see Figure 26). For CAS latencies of two and three, data element *n* + 3 is either the last of a burst of four or the last desired of a longer burst. The 64 Mbyte SDRAM uses a pipelined architecture and therefore does not require the 2*n* rule associated with a prefetch architecture. A READ command can be initiated on any clock cycle following a previous READ command. Full-speed random read accesses can be performed to the same bank, as shown in Figure 16 or each subsequent READ may be performed to a different bank.

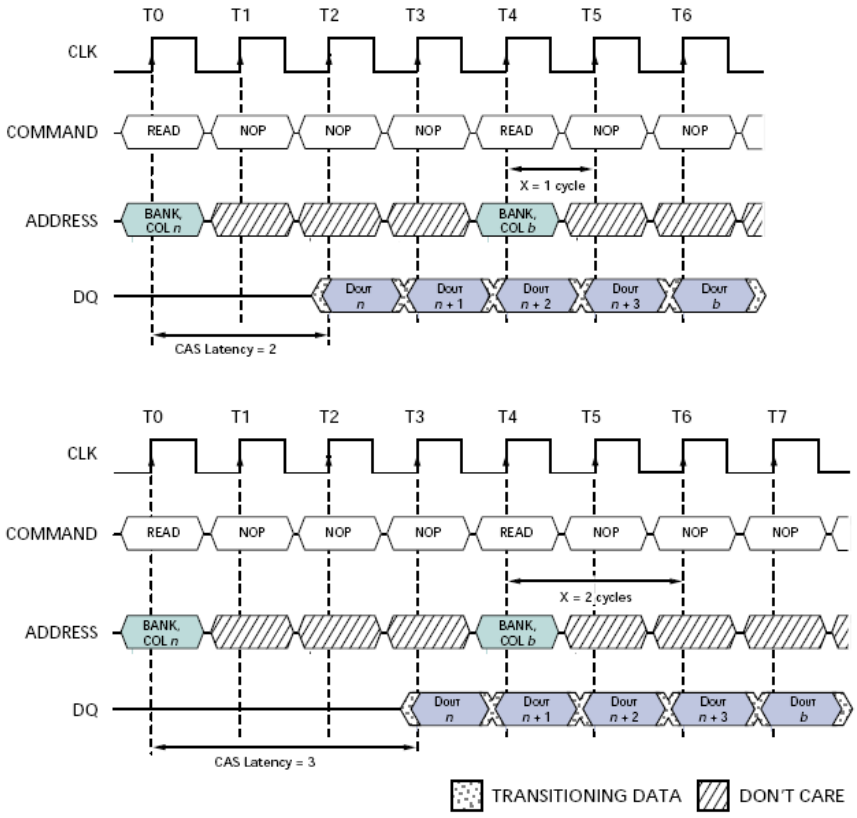


Figure 26. SDRAM Read Burst Timing

9.2.5 SDRAM Write Operation, Write Burst, Write-to-Write, and Write-to-Precharge Timing

WRITE bursts are initiated with a WRITE command.

The starting column and bank addresses are provided with the WRITE command, and auto precharge is either enabled or disabled for that access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. For the generic WRITE commands used in the following illustrations, auto precharge is disabled.

During WRITE bursts, the first valid data-in element will be registered coincident with the WRITE command. Subsequent data elements will be registered on each successive positive clock edge. Upon completion of a fixed-length burst, assuming no other commands have been initiated, the DQs will remain High-Z, and any additional input data will be ignored. A full-page burst will continue until terminated. (At the end of the page, it will wrap to column 0 and continue.)

Data for any WRITE burst may be truncated with a subsequent WRITE command, and data for a fixed length WRITE burst may be immediately followed by data for a WRITE command. The new WRITE command can be issued on any clock following the previous WRITE command, and the data provided coincident with the new command applies to the new command (see Figures 27 - 30).

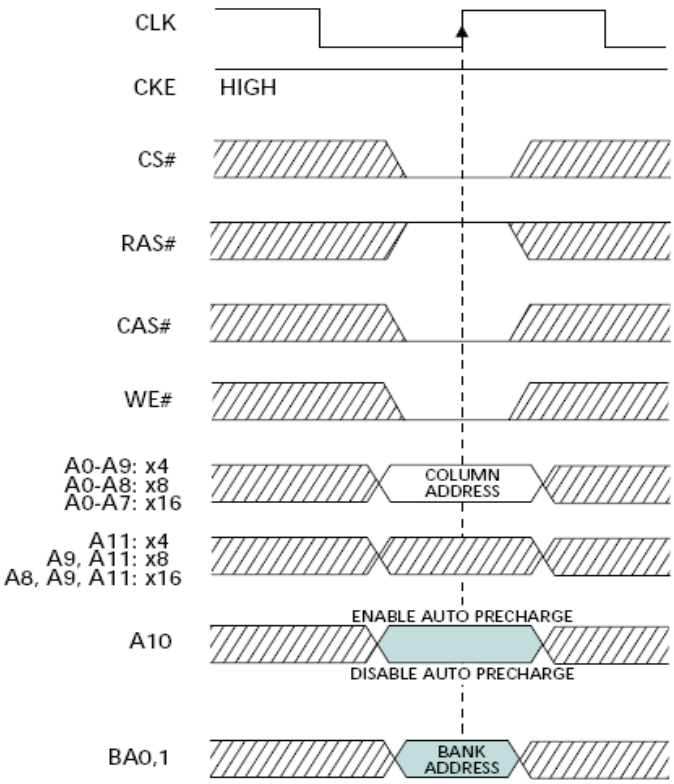


Figure 27. SDRAM Write Operation Timing

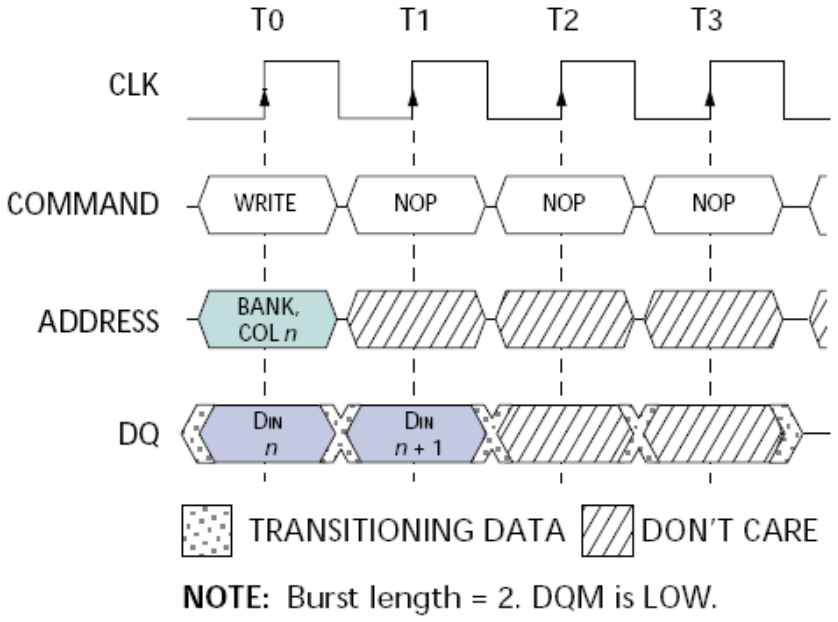


Figure 28. SDRAM Write Burst Timing

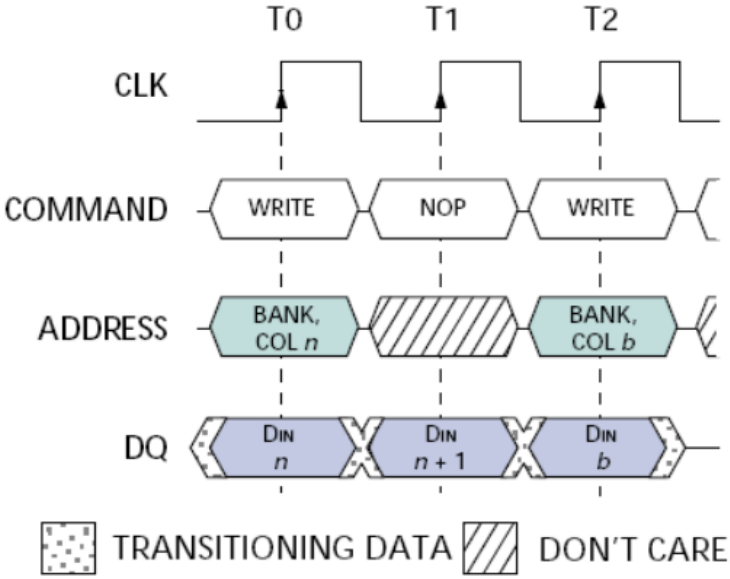


Figure 29. SDRAM Write-to-Write Timing

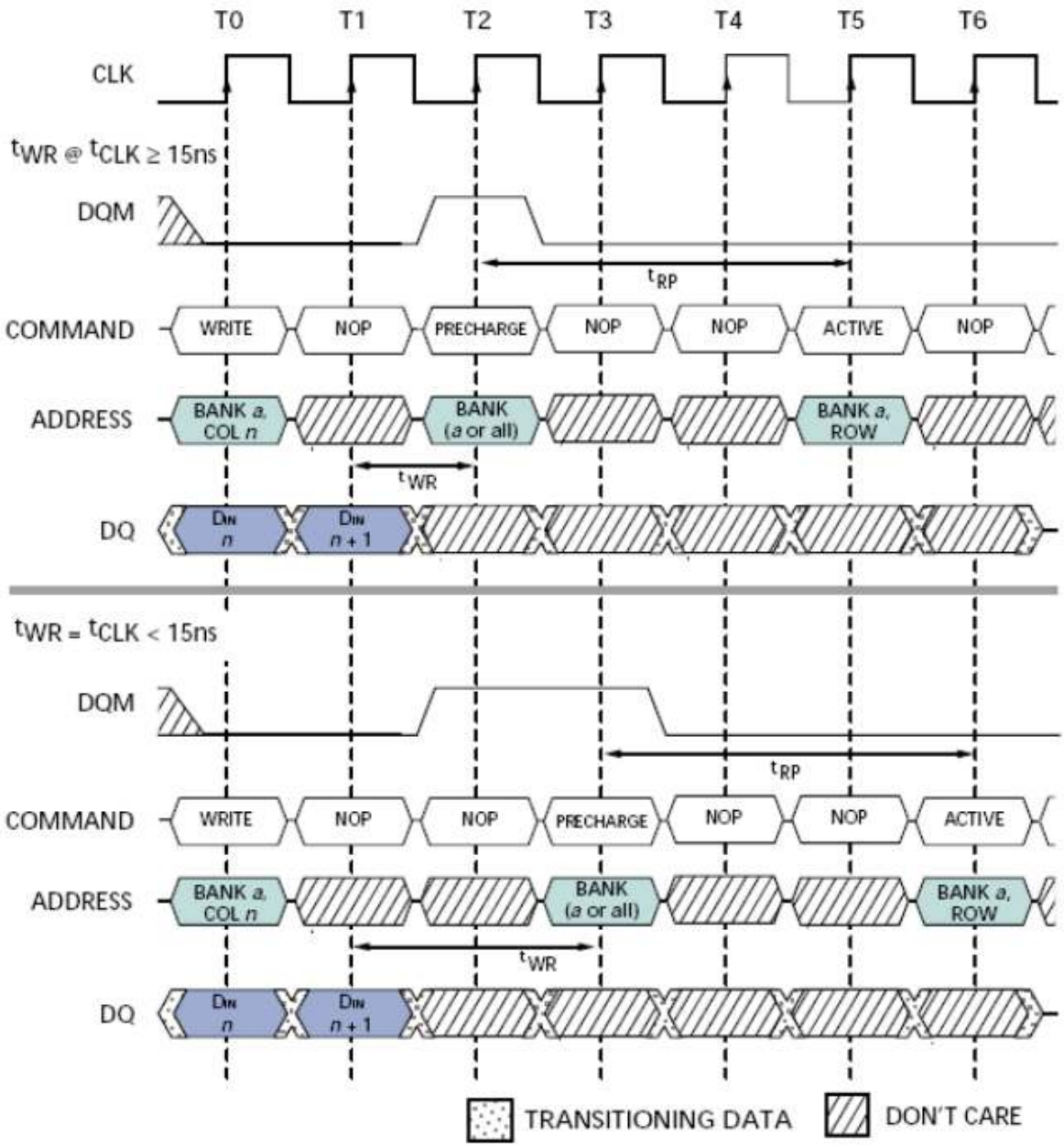


Figure 30. SDRAM Write-to-Precharge Timing

10. JTAG

The TAP controller is a synchronous Finite State Machine and responds to changes in the TMS and TCK signals. States transition occurs on the rising edge of TCK. Values shown to the side of each state represent the state of TMS at the time of the rising edge of TCK (see Figure 31).

There are two paths through the state machine. The instruction path captures and loads the JTAG instructions into the instruction register. The data path captures and loads data into the other three registers. The TAP controller executes the last instruction decode until a new instruction is entered at the Update-IR state or until a reset is sent to the controller.

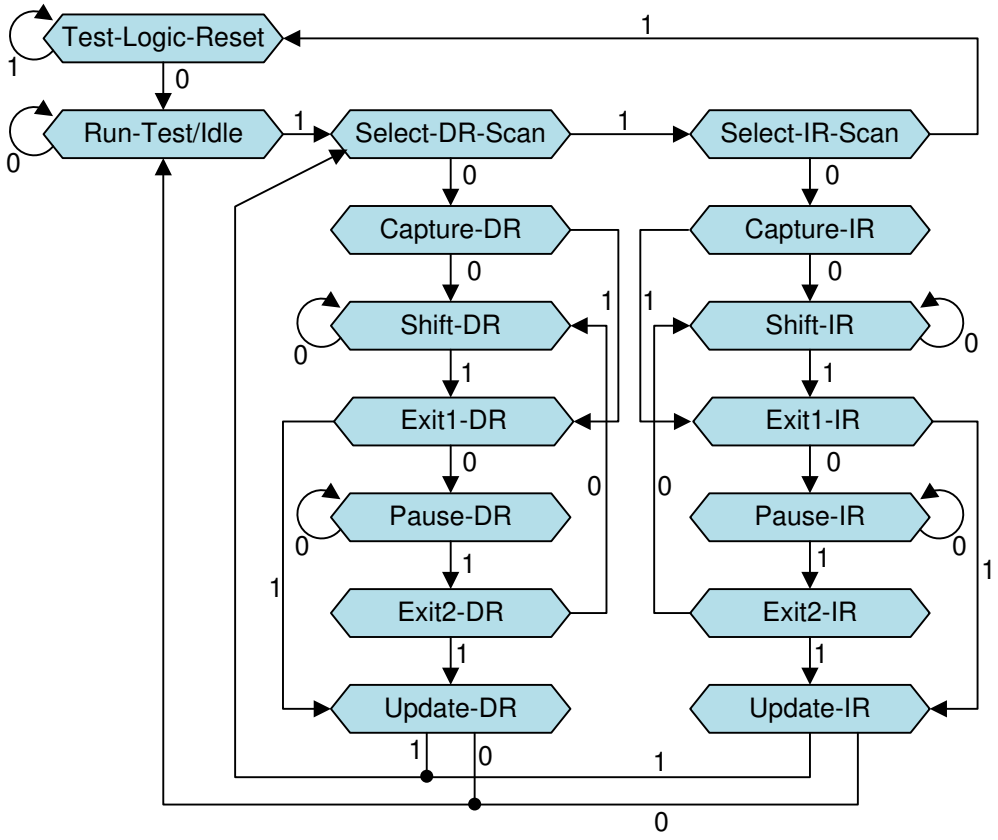


Figure 31. JTAG State Machine

The JTAG port has four Read/Write registers. An ID register, By-Pass Register, Boundary Scan, and Instruction Register (see Figure 32).

The TDO pin remains in the high impedance state except during a shift-DR or shift-IR controller state. In the shift-DR and shift-IR controller states, TDO is updated on the falling edge of TCK. TMS and TDI are sampled on the rising edge of TCK.

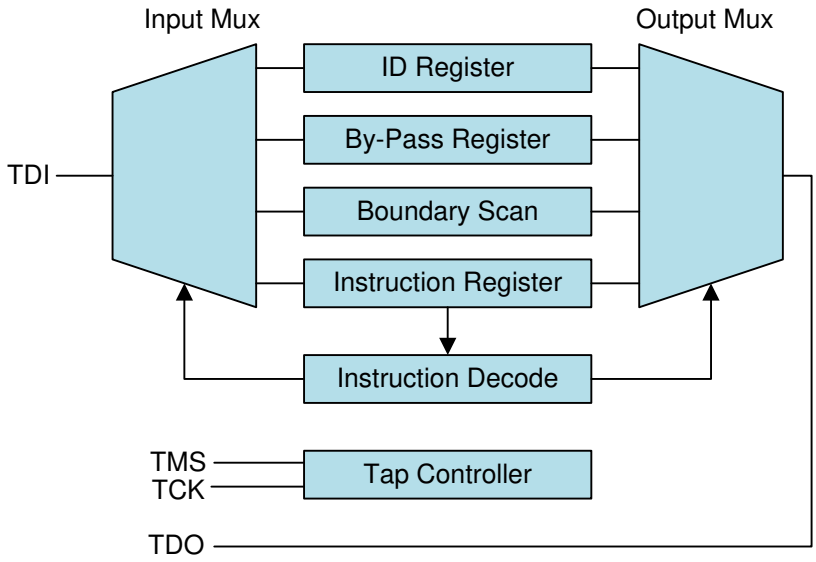


Figure 32. JTAG Port Register Interface

The timing of the JTAG signals is shown in Figure 33. The TDO pin remains in the high impedance state except during a shift-DR or shift-IR controller state. In the shift-DR and shift-IR controller states, TDO is updated on the falling edge of TCK. TMS and TDI are sampled on the rising edge of TCK.

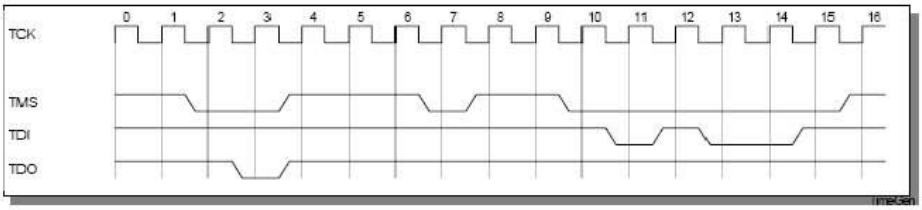


Figure 33. Timing of JTAG Signals

10.1 JTAG Scan Chain Debug Functionality

The JTAG port contains an 8-bit-wide instruction register. Instructions are transferred to this register during the shift-IR state of the TAP state machine and are decoded by entering the Update-IR state of the TAP. The JTAG controller executes the last decoded instruction until another new one is entered and decoded. The instructions and data are entered serially through the TDI pin, LSB first.

The JTAG Test Access Port (TAP) instruction shift register will support the debug scan chain commands shown in Table 21.

Table 21. Debug Scan Chain Commands Supported by the JTAG TAP

JTAG Instruction	Scan Chain Function	Scan Chain Length	Scan Chain Reference Number	Public or Private
00010000	READWRITEADDRCMD (Read/Write Memory/Registers Address and Command)	37 bits	1	Private
00010001	READDATA (Read Memory/Registers Data)	32 bits	2	Private
00010010	WRITEDATA (Write Memory/Registers Data)	32 bits	7	Private
00010011	READPC_ANDCONTEXT (Read Program Counter and Active context)	37 bits	4	Private
00010100	READWRITEDRBUGREG (Read/Write Debug Control Register)	15 bits	5	Private
11111110	IDCODE (Read Device ID Register)	32 bits	3	Public
11111000	EXTEST (IO Boundary Scan)	n bits (I/O Pins)	6	Public
11111010	SAMPLE/PRELOAD (Sample Boundary Scan chain on “Capture-DR” state, Load Boundary Scan chain on ‘Update-DR’ state)	N bits (I/O Pins)	6	Public
11111111	BYPASS (Use TDI/TDO Bypass Register)	1 bit	9	Public
00000111	RUNBIST (Run Built in Self-Test)	16 bits	8	Public
00001111	ENABLEATPG (Enable ATPG Mode for Manufacturing Test)	N/A	N/A	Private

Notes:
1. The boundary-scan scan chain is selected via the EXETEST, SAMPLE, and PRELOAD instructions.
2. The SAMPLE and PRELOAD instructions have the SAME binary code. (They are identified as separate instructions in the JTAG Spec, but are allowed to have the same binary code for backwards compatibility with previous version of spec.)
3. Any undefined bit pattern that is shifted into the Instruction Register will perform the same function as the BYPASS instruction.
4. On Power-on Reset, or when the JTAG state machine enters the “Test Logic Reset” the instruction register will reset its value to operate as the IDCODE Instruction (per JTAG Spec).

11. Ordering Information

The fido1100 parts currently available are listed in Table 22.

Table 22. Part Numbers by Package Types

Innovasic Part Number	Package Type	Temperature Grade
fido1100PQF208IR1 Lead-free (RoHS-compliant)	208-Lead QFP 28- by 28-mm Package	Industrial
fido1100BGB208IR1 Lead-free (RoHS-compliant)	208-Ball BGA, .8mm pitch 15- by 15-mm Package	Industrial

12. Errata

This chapter addresses issues discovered by our internal testing organization that may affect the implementation of the fido1100. This information should be used in conjunction with *The fido1100 User Guide* and *The fido1100 Instruction Set Reference Guide* to circumvent problems during the design process and is not intended as a standalone design guide. Although fido1100-specific terms are clearly described, in the interest of conciseness, many terms already familiar to designers and developers are left undefined.

12.1 Summary

Table 23 presents a summary of errata.

Table 23. Summary of Errata

Errata No.	Problem	Ver. 1
1	ADC Start Register Bit 0 (START) does not self-clear when non-scanning mode conversion for single channel or multi-channel is selected.	Exists
2	Fatal fault recovery sequence can be disturbed by interrupts.	Exists
3	The vectors are reversed when a trapx instruction is executed coincident with an interrupt to a higher priority context.	Exists
4	When using the RDY_N signal to insert wait states (chip select timing register RDY_ENABLE bit = 1), the Address bus timing is incorrect.	Exists
5	When using a JMP or JSR instruction in PC indirect with base displacement addressing mode in assembly code projects, the CPU does not execute the instruction correctly.	Exists

12.2 Detail

Errata No. 1

Problem: ADC Start Register Bit 0 (START) does not self-clear when non-scanning mode conversion for single channel or multi-channel is selected.

Description:

- Scanning mode is controlled by ADC Control Register Bit 6 (SCAN).

- ADC Control Register Bit 4 (CD-Conversion Done) will correctly indicate that conversion(s) are done.
- An ADC interrupt will be issued if ADC interrupts are enabled. ADC interrupts are enabled by setting ADC Control Register Bit 3 (IRQ_En) to 1.
- ADC Data Available Register will correctly indicate which channels have updated results in their Data Registers.

Workaround: When using non-scanning mode conversions, enable the ADC between each commanded conversion (single channel or multi-channel):

- Clear ADC Control Register Bit 7 (EN) to 0.
- Set ADC Control Register Bit 7 (EN) to 1.
- Set ADC Start Register Bit 0 (START) to 1 to start the conversion process.
- ADC Conversion complete will be indicated by:
  - An ADC interrupt, if ADC Control Register Bit 3 (IRQ_En) is set to 1.
  - ADC Control Register Bit 4 (CD-Conversion Done) will set to indicate that conversion(s) are done.

Errata No. 2

Problem: Fatal fault recovery sequence can be disturbed by interrupts.

Description:

Context Fatal Faults can occur if a context's stack pointer becomes corrupted. It is a feature of the hardware to detect this "Fatal Fault" and allow a graceful recovery by directing an exception to the Master Context. This operation can be disturbed if, by chance, an interrupt is triggered during a bus cycle leading to a Fatal Fault. This problem occurs no matter which context the interrupt is directed to. It need not be the faulting context. Furthermore, since neither interrupt timing nor fatal faults are predictable, there is no way to guarantee this cannot happen. The effect of this error depends on the interrupt mode of the context to which the interrupt is directed. If the interrupted context is running in Fast Single Threaded mode, when an interrupt targeted to it occurs during a faulting bus cycle (caused by another context) the CPU will lock up after the faulting bus cycle completes. If the interrupted context is in Standard or Fast Vectored mode the CPU will not lock up but the normal fault handling process will be disrupted. The effect is:

- Both the interrupted and the faulting context will be set to Halted.
- The fatal fault exception will be directed to the interrupted context rather than the Master.

- The expected interrupt will be directed (queued behind the fatal fault exception) to the interrupted context.
- The Master context will be moved to the ready state, with no modification of its program counter, thus it will start running from where it left off previously.
- All other contexts are unaffected.

Errata No. 3

Problem: The vectors are reversed when a trapx instruction is executed coincident with an interrupt to a higher priority context.

Description: Given a low priority context currently executing and the master context and a higher priority context sleeping, if an interrupt comes in for the higher priority context simultaneously with the execution of a trapx instruction in the low priority context, it can happen that the interrupt handler is executed by the master context (even though intended for the higher priority context), while the trapx handler is executed by the higher priority context.

Workaround:

The workaround involves several issues:

1. Any interrupt handlers intended for other than the lowest priority context should be executable by the master context.
2. The master context must have a valid vector to the appropriate interrupt handlers. Either the master context and the other contexts share a vector table or the vectors are duplicated on the master context's table. If the master context is executed in a different mode than the other contexts (e.g. master in standard mode, other context in fast-vectored mode), then a second interrupt handler must be coded that is compatible with the master context's operating mode.
3. Trapx handlers should verify that they are being executed in the master context. This assumes that they are performing some action that can only be executed in the master context, and if so, then they should execute and set a flag to alert the caller that they executed. If not, then they should return without setting the flag. Also, trapx handlers must be present (in the appropriate execution mode) on all vector tables.
4. The routine executing a trapx instruction should check the handshake flag from the trapx handler after execution of the instruction. If it is not set appropriately, the trapx should be executed again.

The approach given in 3 and 4 above, while more complex than simply having the trapx handler issue a trapx instruction if not executed in the master context, avoids the issue of

trapx handlers that rely on the Faulted Context register to determine what specific action to take.

Errata No. 4

Problem: When using the RDY_N signal to insert wait states (chip select timing register RDY_ENABLE bit = 1), the Address bus timing is incorrect.

Description: When used in this way, the Address bus will change states coincident with, or in some cases, before the end of the bus cycle. This can cause data corruption in memory.

Workaround: There is no work around for this problem. It is recommended to avoid use of the RDY_N signal and the RDY_ENABLE bit of the chip select timing registers.

Errata No. 5

Problem: When using a JMP or JSR instruction in PC indirect with base displacement addressing mode in assembly code projects, the CPU does not execute the instruction correctly.

Description: Instead of jumping indirectly to the location pointed to by the effective address, execution jumps to the effective address directly.

Workaround: There is no workaround for this problem. For assembly code projects, avoiding use of the PC indirect addressing with base displacement mode is recommended.

13. Revision History

Table 24 presents the sequence of revisions to document IA211080807.

Table 24. Revision History

Date	Revision	Description	Page(s)
August 8, 2007	00	First edition released.	NA
September 11, 2008	01	Reformatted to meet publication standards. Technical data updated. Errata added.	NA
October 9, 2008	02	Changed “RESET” to “RESET_N” and “RESET_OUT” to “RESET_OUT_N” in text, figures, and tables.	17, 19, 26, 28, 35, 37, 50, 51
		In Table 5, changed pin numbers in data row 14 from “F3” to “G3”and in data row 19 from “G3” to “H3.”	36
		In Table 5, changed pin numbers in data row 11 from “M14” to “M15” and in data row 14 from “M15” to “M14.”	39
		Deleted last row of Table 5 (duplicate).	40
		In Table 7, changed numbers in data row 1 from “M14” to “M15” and in data row 2 from “M15” to “M14.”	43
		In Table 10, changed numbers in data rows 13, 14, 15, and 16 to “B6,” “P13,” “P14,” and “–,” from “P5,” “B6,” “P13,” and “P14,” respectively, for column labeled “BGA 15 x 15.”	44
		Added 2 new sentences at beginning of Section 7.2, “Signal Considerations and Reset Timing.”	50
		Changed “CLKVDD” to “VDDCLK” and “CLKGND” to “GNDCLK” in note and Figures 11, 12, and 13.	52, 53
		Updated errata chapter to reflect errata for Version 01.	76 through 87
October 10, 2008	03	To conform to publication standards, removed illustration from cover. Changed Table 24, “Part Numbers by Package Types,” to reflect Version 01 part numbers.	1, 75
March 12, 2009	04	Revised ordering information – package information; Added Errata 2.	75 - 78
July 28, 2009	05	Revised description of when bus cycle terminates in a Read cycle; Added two errata.	61, 64, 76, 78, 79
November 20, 2009	06	Updated LPSTOP power consumption.	49
April 15, 2010	07	Added BGA signal routing guidance.	43, 44
April 25, 2012	08	Added Errata 5	81

Date	Revision	Description	Page(s)
December 11, 2012	09	Removed references to 10x10 BGA package; Added thermal characteristics data.	10, 41
April 10, 2013	10	Corrected oscillator startup time (t_{ST})	39
September 10, 2014	11	Modified timing information for TwWait and TrWait.	61-66

14. For Additional Information

Innovasic's fido1100 is the first product in the fido™ family of real-time communication controllers. The fido communication controller architecture is uniquely optimized for solving memory bottlenecks, and is designed from the ground up for deterministic processing. Critical timing parameters, such as context switching and interrupt latency, are precisely predictable for real-time tasks. The fido1100 also incorporates the Universal I/O Controller (UIC™) that is configurable to support various communication protocols across multiple platforms. This flexibility relieves the designer of the task of searching product matrices to find the set of peripherals that most closely match the system interface needs. The Software Profiling and Integrated Debug EnviRonment (SPIDER™) has extensive real-time code debug capabilities without the burden of code instrumentation.

The fido1100 User Guide and *The fido1100 Instruction Set Reference Guide* as well as other helpful tools and files are available. For example, the GDB debugger supports both profiling and tracing of executing code.

The Innovasic Support Team is continually planning and creating tools for your use. Visit http://www.innovasic.com for up-to-date documentation and software. Our goal is to provide timely, complete, accurate, useful, and easy-to-understand information. Please feel free to contact our experts at Innovasic at any time with suggestions, comments, or questions.

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