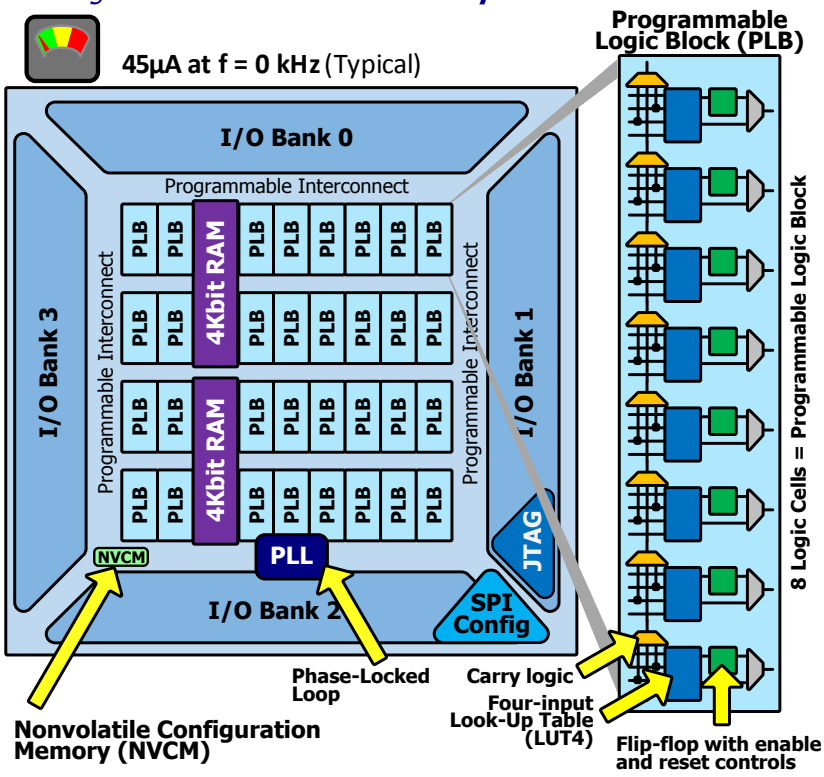
iCE65™ P-Series Ultra Low-Power mobileFPGA™ Family

SiliconBlue®

April 22, 2011 (1.31) **Data Sheet**

- **High-density, ultra low-power single-chip, SRAM mobileFPGA family specifically designed for hand-held applications and long battery life**
- **Integrated Phase-Locked Loop (PLL)**
  - Clock multiplication/division for display, serializer/deserializer (SerDes) , and memory interface applications
- **Up to 533 MHz PLL Output**
- **Reprogrammable from a variety of methods and sources**
  - Self configuration from external, commodity SPI serial Flash PROM
  - Slave configuration by a processor using SPI-like serial interface in as little as 20 us.
  - Self configuration from embedded, secure Nonvolatile Configuration Memory (NVCM)
    - ideal for volume production
    - superior design security: no exposed data
- **Proven, high-volume 65 nm, low-power CMOS technology**

Figure 1: **iCE65P P-Series Family Architectural Features**



- **Flexible programmable logic and programmable interconnect fabric**
  - Over 12K look-up tables (LUT4) and flip-flops
  - Low-power logic and interconnect
- **Flexible I/O pins to simplify system interfaces**
  - Up to 174 programmable I/O pins
  - Four independently-powered I/O banks; support for 3.3V, 2.5V, 1.8V, and 1.5V voltage standards
  - LVCMOS, MDDR, LVDS, and SubLVDS I/O standards
- **Plentiful, fast, on-chip 4Kbit RAM blocks**
- **Low-cost, space-efficient packaging options**
  - DiePlus™ known-good die (KGD) options available
- **Complete iCEcube™ development system**
  - Windows® and Linux® support
  - VHDL and Verilog logic synthesis
  - Place and route software
  - Design and IP core libraries
  - Low-cost iCEman65P development board

Table 1: **iCE65P Ultra Low-Power Programmable Logic Family Summary**

	iCE65P04	iCE65P08	iCE65P12
Logic Cells (LUT + Flip-Flop)	3,520		
Approximate System Gate Count	200K		
Typical Equivalent Macrocells	2,700		
RAM4K Memory Blocks	20		
RAM4K RAM bits	80K		
Phase-Locked Loops (PLLs)	1		
Configuration bits (maximum)	533 Kb		
Core Operating Current at 0 KHz	**45 µA**		
Maximum Programmable I/O Pins	174		
Maximum Differential Input Pairs	20		

Overview

The SiliconBlue Technologies iCE65P P-Series programmable logic family is specifically designed to deliver the lowest static and dynamic power consumption of any comparable CPLD or FPGA device. iCE65P FPGAs are designed specifically for cost-sensitive, high-volume applications. iCE65P FPGA are fully user-programmable and can self-configure from a configuration image stored in on-chip, nonvolatile configuration memory (NVCM) or stored in an external commodity SPI serial Flash PROM or downloaded from an external processor over an SPI-like serial port.

The three iCE65P components, highlighted in Table 1, deliver from approximately 3,500 to 12,000 logic cells and flip-flops while consuming a fraction of the power of comparable programmable logic devices. Each iCE65P device includes between 20 or more RAM blocks, each with 4Kbits of storage, for on-chip data storage and data buffering.

As pictured in Figure 1, each iCE65P device consists of five primary architectural elements.

- An array of Programmable Logic Blocks (PLBs)
  - Each PLB contains eight Logic Cells (LCs); each Logic Cell consists of …
    - A fast, four-input look-up table (LUT4) capable of implementing any combinational logic function of up to four inputs, regardless of complexity
    - A 'D'-type flip-flop with an optional clock-enable and set/reset control
    - Fast carry logic to accelerate arithmetic functions such as adders, subtracters, comparators, and counters.
  - Common clock input with polarity control, clock-enable input, and optional set/reset control input to the PLB is shared among all eight Logic Cells
- Two-port, 4Kbit RAM blocks (RAM4K)
  - 256x16 default configuration; selectable data width using programmable logic resources
  - Simultaneous read and write access; ideal for FIFO memory and data buffering applications
  - RAM contents pre-loadable during configuration
- Four I/O banks with independent supply voltage, each with multiple Programmable Input/Output (PIO) blocks
  - LVCMOS I/O standards and LVDS outputs supported in all banks
  - I/O Bank 3 supports additional SSTL, MDDR, LVDS, and SubLVDS I/O standards
- One or more Phase-Locked Loops (PLL)
  - Very low power
  - Clock multiplication and division
  - Phase shifting in fixed 90° increments
  - Static or dynamic phase shifting
- Programmable interconnections between the blocks
  - Flexible connections between all programmable logic functions
  - Eight dedicated low-skew, high-fanout clock distribution networks

Packaging Options

iCE65P components are available in a variety of package options to support specific application requirements. The available options, including the number of available user-programmable I/O pins (PIOs), are listed in Table 2. Fully-tested Known-Good Die (KGD) DiePlus™ are available for die stacking and highly space-conscious applications. All iCE65P devices are provided exclusively in Pb-free, RoHS-compliant packages.

Table 2: **iCE65P Family Packaging Options, Maximum I/O per Package**

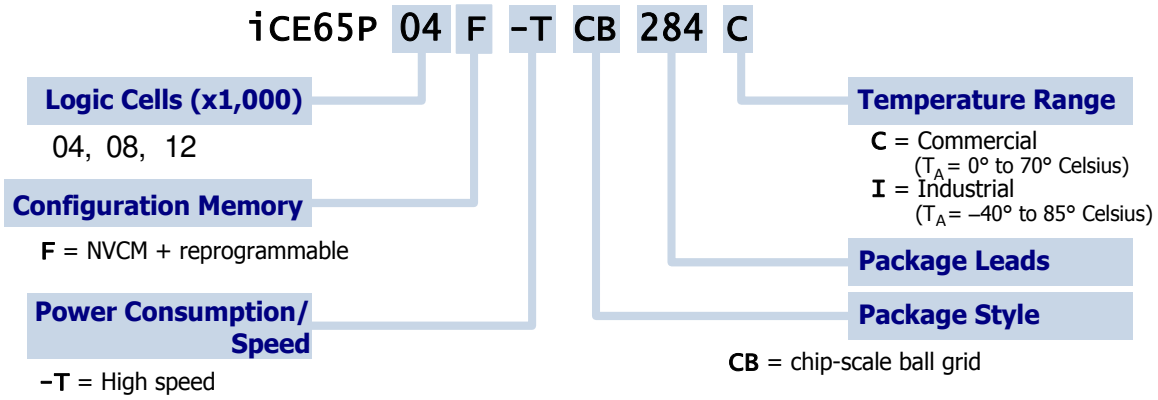
Package	Board Area (mm)	Package Code	Ball/Lead Pitch (mm)	iCE65P04	iCE65P08	iCE65P12
121-ball chip-scale BGA	6 x 6	CB121	0.5	95 *(13)*		
196-ball chip-scale BGA	8 x 8	CB196		148 *(18)*		
284-ball chip-scale BGA	12 x 12	CB284		174 *(20)*		
DiePlus known good die	See die data sheet	DI	—	174 *(20)*		

Feature-rich versions of the end application mount a larger iCE65P device on the circuit board. Low-end versions mount a smaller iCE65P device.

Ordering Information

Figure 2 describes the iCE65P ordering codes for all packaged components. See the separate DiePlus data sheets when ordering die-based products.

Figure 2: **iCE65P Ordering Codes (packaged, non-die components)**



iCE65P devices come standard in the higher speed "**-T**" version.

iCE65P devices are available in two operating temperature ranges, one for typical commercial applications, the other with an extended temperature range for industrial and telecommunications applications. The ordering code also specifies the device package option, as described further in Table 2.

Programmable Logic Block (PLB)

Generally, a logic design for an iCE65P component is created using a high-level hardware description language such as Verilog or VHDL. The SiliconBlue Technologies development software then synthesizes the high-level description into equivalent functions built using the programmable logic resources within each iCE65P device. Both sequential and combinational functions are constructed from an array of Programmable Logic Blocks (PLBs). Each PLB contains eight Logic Cells (LCs), as pictured in Figure 3, and share common control inputs, such as clocks, reset, and enable controls.

PLBs are connected to one another and other logic functions using the rich Programmable Interconnect resources.

Logic Cell (LC)

Each iCE65P device contains thousands of Logic Cells (LCs), as listed in Table 1. Each Logic Cell includes three primary logic elements, shown in Figure 3.

- A four-input Look-Up Table (LUT4) builds any combinational logic function, of any complexity, of up to four inputs. Similarly, the LUT4 element behaves as a 16x1 Read-Only Memory (ROM). Combine and cascade multiple LUT4s to create wider logic functions.
- A 'D'-style Flip-Flop (DFF), with an optional clock-enable and reset control input, builds sequential logic functions. Each DFF also connects to a global reset signal that is automatically asserted immediately following device configuration.
- Carry Logic boosts the logic efficiency and performance of arithmetic functions, including adders, subtracters, comparators, binary counters and some wide, cascaded logic functions.

The output from a Logic Cell is available to all inputs to all eight Logic Cells within the Programmable Logic Block. Similarly, the Logic Cell output feeds into the **Error! Reference source not found.** fabric to connect to other eatures on the iCE65P device.

Look-Up Table (LUT4)

The four-input Look-Up Table (LUT4) function implements any and all combinational logic functions, regardless of complexity, of between zero and four inputs. Zero-input functions include "High" (1) and "Low" (0). The LUT4 function has four inputs, labeled I0, I1, I2, and I3. Three of the four inputs are shared with the Carry Logic function, as shown in Figure 3. The bottom-most LUT4 input connects either to the I3 input or to the Carry Logic output from the previous Logic Cell.

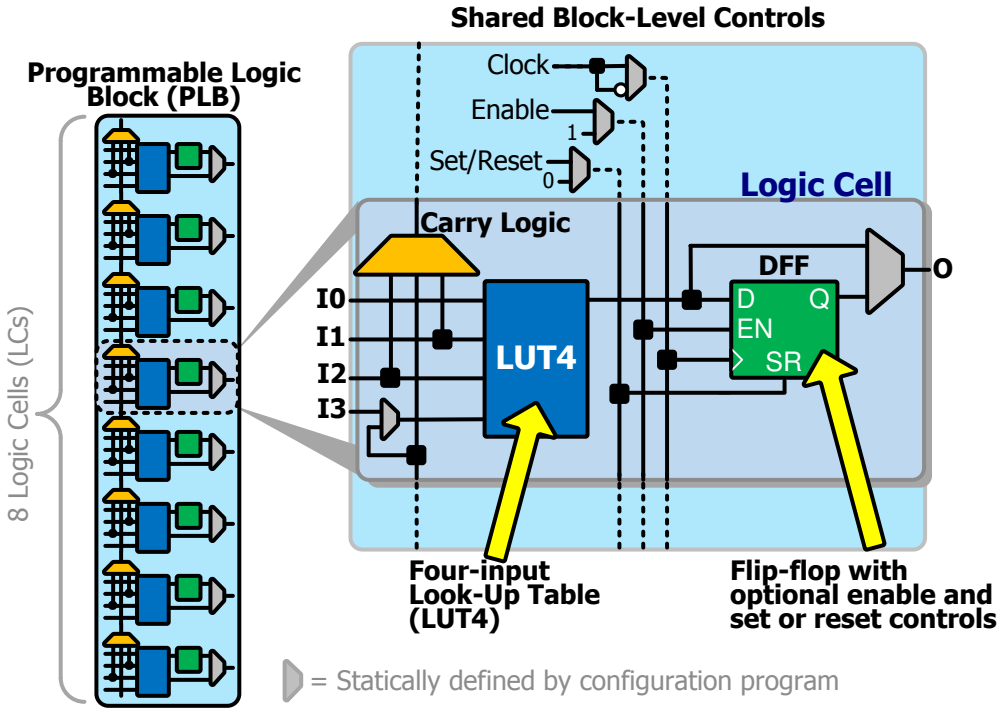
The output from the LUT4 function connects to the flip-flop within the same Logic Cell. The LUT4 output or the flip-flop output then connects to the programmable interconnect.

For detailed LUT4 internal timing, see Table 57.

'D'-style Flip-Flop (DFF)

The 'D'-style flip-flop (DFF) optionally stores state information for the application.

Figure 3: **Programmable Logic Block and Logic Cell**



The flip-flop has a data input, 'D', and a data output, 'Q'. Additionally, each flip-flop has up to three control signals that are shared among all flip-flops in all Logic Cells within the PLB, as shown in Figure 3. Table 3 describes the behavior of the flip-flop based on inputs and upon the specific DFF design primitive used or synthesized.

Table 3: **'D'-Style Flip-Flop Behavior**

DFF Primitive	Operation	Flip-Flop Mode	Inputs				Output
			D	**EN**	**SR**	**CLK**	**Q**
All	Cleared Immediately after Configuration	X	X	X	X	X	0
	Hold Present Value (Disabled)		X	0	X	X	Q
	Hold Present Value (Static Clock)		X	X	X	1 or 0	Q
	Load with Input Data		D	1*	0*	↑	D
SB_DFFR	Asynchronous Reset	Asynchronous Reset	X	X	1	X	0
SB_DFFS	Asynchronous Set	Asynchronous Set	X	X	1	X	1
SB_DFFSR	Synchronous Reset	Synchronous Reset	X	1*	1	↑	0
SB_DFFSS	Synchronous Set	Synchronous Set	X	1*	1	↑	1

X = don't care, ↑ = rising clock edge (default polarity), 1* = High or unused, 0* = Low or unused

The CLK clock signal is not optional and is shared among all flip-flops in a Programmable Logic Block. By default, flip-flops are clocked by the rising edge of the PLB clock input, although the clock polarity can be inverted for all the flip-flops in the PLB.

The CLK input optionally connects to one of the following clock sources.

- The output from any one of the eight Global Buffers, or
- A connection from the general-purpose interconnect fabric

The EN clock-enable signal is common to all Logic Cells in a Programmable Logic Block. If the enable signal is not used, then the flip-flop is always enabled. This condition is indicated as "1*" in Table 3. The asterisk indicates that this is the default state if the control signal is not connected in the application.

Similarly, the SR set/reset signal is common to all Logic Cells in a Programmable Logic Block. If not used, then the flip-flop is never set/reset, except when cleared immediately after configuration or by the Global Reset signal. This condition is indicated as "0*" in Table 3. The asterisk indicates that this is the default state if the control signal is not connected in the application.

Each flip-flop has an additional control that defines its set or reset behavior. As defined in the configuration image, the control defines whether the set or reset operation is synchronized to the active CLK clock edge or whether it is completely asynchronous.

- The SB_DFFR and SB_DFFS primitives are asynchronously controlled, solely by the SR input. If the SR input is High, then an SB_DFFR primitive is asynchronously reset and an SB_DFFS primitive is asynchronously set.
- The SB_DFFSR and SB_DFFRSS primitives are synchronously controlled by both the SR input and the clock input. If the SR input is High at a rising edge of the clock input, then an SB_DFFSR primitive is synchronously reset and an SB_DFFSS primitive is synchronously set.

The LUT4 output or the flip-flop output then connects to the programmable interconnect.

Because of the shared control signals, the design software can pack flip-flops with common control inputs into a single PLB block, as described by Table 4. There are eight total packing options.

Table 4: **Flip-flop Packing/Sharing within a PLB**

Group	Active Clock Edge	Clock Enable	Set or Reset Control (Sync. or Async)
1	↑	None (always enabled)	None
2	↓		
3	↑		PLB set/reset control
4	↓		
5	↑	Selective (controlled by PLB clock enable)	None
6	↓		
7	↑		PLB set/reset control
8	↓		

For detailed flip-flop internal timing, see Table 57.

Carry Logic

The dedicated Carry Logic within each Logic Cell primarily accelerates and improves the efficiency of arithmetic logic such as adders, accumulators, subtracters, incrementers, decrementers, counters, ALUs, and comparators. The Carry Logic also supports wide combinational logic functions.

$$COUT = I1 \bullet I2 + CIN \bullet I1 + CIN \bullet I2 \qquad \text{[Equation 1]}$$

Equation 1 and Figure 4 describe the Carry Logic structure within a Logic Cell. The Carry Logic shares inputs with the associated Look-Up Table (LUT4). The LUT4's I1 and I2 inputs directly feed the Carry Logic; inputs I0 and I3 do not. A signal cascades between Logic Cells within the Programmable Logic Block. The carry input from the previous adjacent Logic Cell optionally provides an alternate input to the LUT4 function, supplanting the I3 input.

Low-Power Disable

To save power and prevent unnecessary signal switching, the Carry Logic function within a Logic Cell is disabled if not used. The output of a Logic Cell's Carry Logic is forced High.

PLB Carry Input and Carry Output Connections

As shown in Figure 4, each Programmable Logic Block has a carry input signal that can be initialized High, Low, or come from the carry output signal from PLB immediately below.

Similarly, the Carry Logic output from the Programmable Logic Block connects to the PLB immediately above, which allows the Carry Logic to span across multiple PLBs in a column. As shown in Figure 5, the Carry Logic chain can be tapped mid-way through a chain or a PLB by feeding the value through a LUT4 function.

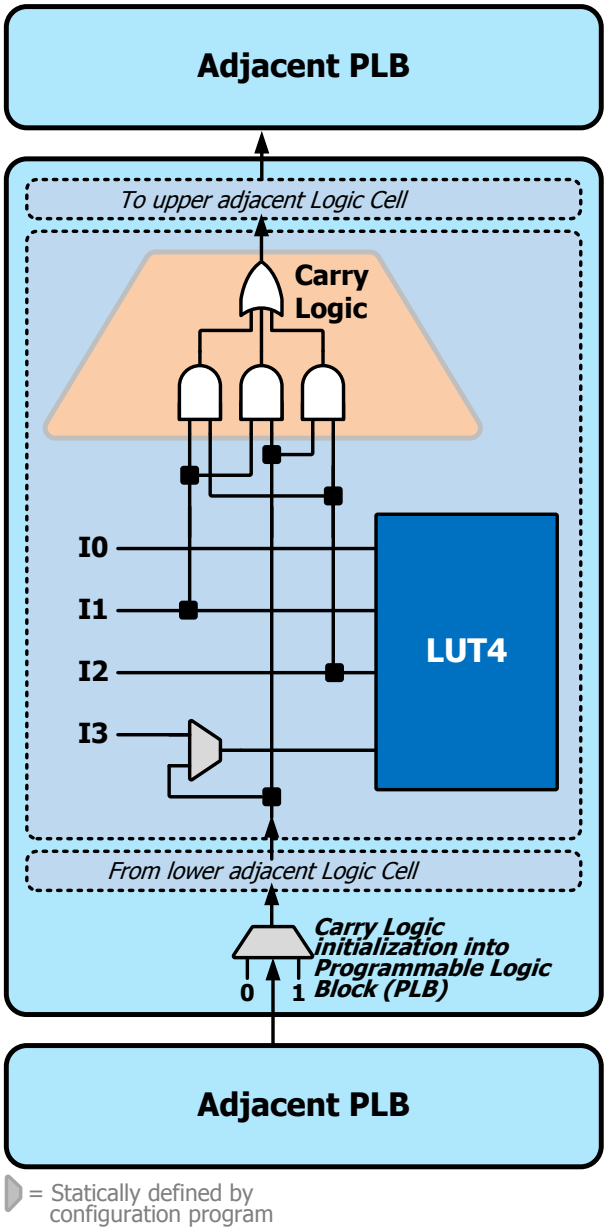
Adder Example

Figure 5 shows an example design that uses the Carry Logic. The example is a 2-bit adder, which can be expanded into an adder of arbitrary size. The LUT4 function within a Logic Cell is programmed to calculate the sum of the two input values and the carry input, `A[i] + B[i] + CARRY_IN[i-1] = SUM[i]`.

The Carry Logic generates the carry value to feed the next bit in the adder. The calculated carry value replaces the I3 input to the next LUT4 in the upper Logic Cell.

If required by the application, the carry output from the final stage of the adder is available by passing it through the final LUT4.

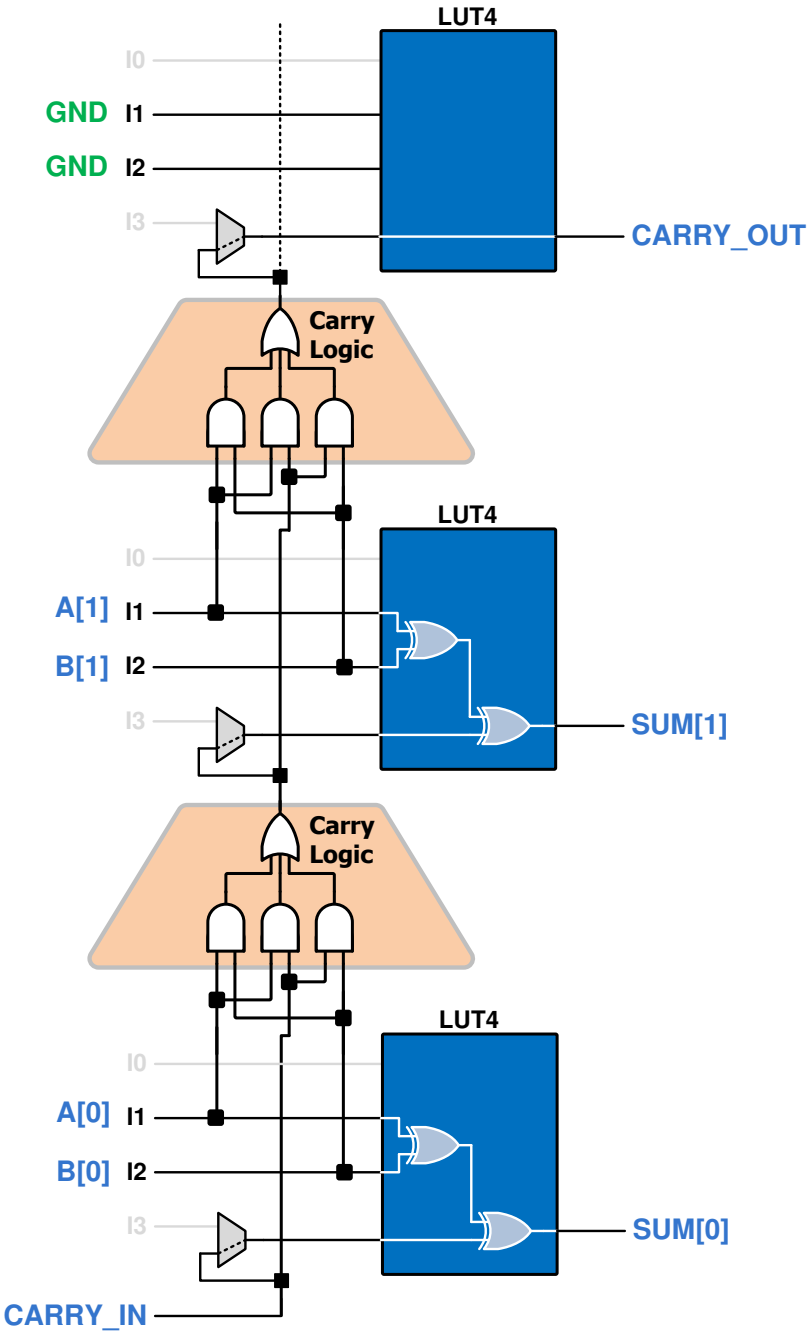
Figure 4: **Carry Logic Structure within a Logic Cell and between PLBs**



Implementing Subtracters, Decrementers

As mentioned earlier, the Carry Logic generates a High output whenever the sum of `I1 + I2 + CARRY_IN` generates a carry. The Carry Logic does not specifically have a subtract mode. To implement a subtract function or decrement function, logically invert either the I1 or I2 input and invert the initial carry input. This performs a 2s complement subtract operation.

Figure 5: **Two-bit Adder Example**

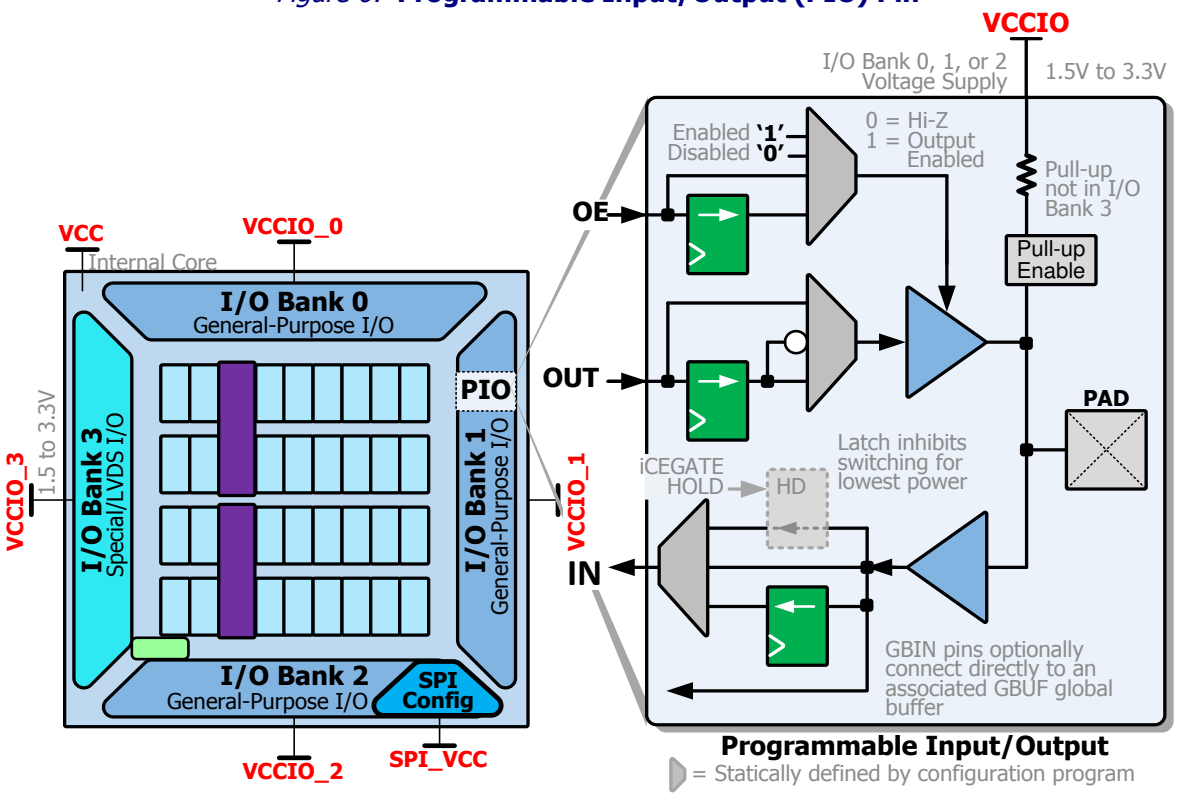


Programmable Input/Output Block (PIO)

Programmable Input/Output (PIO) blocks surround the periphery of the device and connect external components to the Programmable Logic Blocks (PLBs) and RAM4K blocks via programmable interconnect. Individual PIO pins are grouped into one of four I/O banks, as shown in Figure 6. I/O Bank 3 has additional capabilities, including LVDS differential I/O and the ability to interface to Mobile DDR memories.

Figure 6 also shows the logic within a PIO pin. When used in an application, a PIO pin becomes a signal input, an output, or a bidirectional I/O pin with a separate direction control input.

Figure 6: **Programmable Input/Output (PIO) Pin**



I/O Banks

PIO blocks are organized into four separate I/O banks, each with its own voltage supply input, as shown in Table 5. The voltage applied to the VCCIO pin on a bank defines the I/O standard used within the bank. Table 53 and Table 54 describe the I/O drive capabilities and switching thresholds by I/O standard. I/O Bank 3, along the left edge of the die, is different than the others and supports specialized I/O standards.

Because each I/O bank has its own voltage supply, iCE65P components become the ideal bridging device between different interface standards. For example, the iCE65P device allows a 1.8V-only processor to interface cleanly with a 3.3V bus interface. The iCE65P device replaces external voltage translators.

Table 5: **Supported Voltages by I/O Bank**

Bank	Device Edge	Supply Input	3.3V	2.5V	1.8V	1.5V
0	Top	VCCIO_0	Yes	Yes	Yes	Outputs only
1	Right	VCCIO_1	Yes	Yes	Yes	Outputs only
2	Bottom	VCCIO_2	Yes	Yes	Yes	Outputs only
3	Left	VCCIO_3	Yes	Yes	Yes	Yes
SPI	Bottom Right	SPI_VCC	Yes	Yes	Yes	No

If not connected to an external SPI PROM, the four pins associated with the SPI Master Configuration Interface can be used as PIO pins, supplied by the SPI_VCC input, essentially forming a fifth "mini" I/O bank. If using an SPI Flash PROM, then connect SPI_VCC to 3.3V.

Table 6 highlights the available I/O standards when using an iCE65P device, indicating the drive current options, and in which bank(s) the standard is supported. I/O Banks 0, 1, 2 and SPI interface support the same standards. I/O Bank 3 has additional capabilities, including support for MDDR memory standards and LVDS differential I/O.

Table 6: **I/O Standards for I/O Banks 0, 1, 2 and SPI Interface Bank**

I/O Standard	Supply Voltage	Drive Current (mA)	Attribute Name
5V Input Tolerance	3.3V	N/A	N/A
LVCMOS33	3.3V	±11	SB_LVCMOS
LVCMOS25	2.5V	±8	
LVCMOS18	1.8V	±5	
LVCMOS15 outputs	1.5V	±4	

I/O Bank 3

I/O Bank 3, located along the left edge of the die, has additional special I/O capabilities to support memory components and differential I/O signaling (LVDS). Table 7 lists the various I/O standards supported by I/O Bank 3. The SSTL2 and SSTL18 I/O standards require the VREF voltage reference input pin which is only available on the CB284 package. Also see Table 54 for electrical characteristics.

Table 7: **I/O Standards for I/O Bank 3 Only**

I/O Standard	Supply Voltage	VREF Pin (CB284 or iCE DiCE) Required?	Target Drive Current (mA)	Attribute Name
LVCMOS33	3.3V	No	±8	SB_LVCMOS33_8
LVCMOS25	2.5V	No	±16	SB_LVCMOS25_16
			±12	SB_LVCMOS25_12
			±8	SB_LVCMOS25_8
			±4	SB_LVCMOS25_4
LVCMOS18	1.8V	No	±10	SB_LVCMOS18_10
			±8	SB_LVCMOS18_8
			±4	SB_LVCMOS18_4
			±2	SB_LVCMOS18_2
LVCMOS15	1.5V	No	±4	SB_LVCMOS15_4
			±2	SB_LVCMOS15_2
SSTL2_II	2.5V	Yes	±16.2	SB_SSTL2_CLASS_2
SSTL2_I			±8.1	SB_SSTL2_CLASS_1
SSTL18_II	1.8V	Yes	±13.4	SB_SSTL18_FULL
SSTL18_I			±6.7	SB_SSTL18_HALF
MDDR	1.8V	No	±10	SB_MDDR10
			±8	SB_MDDR8
			±4	SB_MDDR4
			±2	SB_MDDR2
LVDS	2.5V	No	N/A	SB_LVDS_INPUT

Table 8 lists the I/O standards that can co-exist in I/O Bank 3, depending on the VCCIO_3 voltage.

Table 8: **Compatible I/O Standards in I/O Bank 3**

VCCIO_3 Voltage	3.3V	2.5V	1.8V	1.5V
Compatible I/O Standards	SB_LVCMOS33_8	Any SB_LVCMOS25 SB_SSTL2_Class_2 SB_SSTL2_Class_1 SB_LVDS_INPUT	Any SB_LVCMOS18 SB_SSTL18_FULL SB_SSTL18_HALF SB_MDDR10 SB_MDDR8 SB_MDDR4 SB_MDDR2 SB_LVDS_INPUT	Any SB_LVCMOS15

Programmable Output Drive Strength

Each PIO in I/O Bank 3 offers programmable output drive strength, as listed in Table 8. For the LVCMOS and MDDR I/O standards, the output driver has settings for static drive currents ranging from 2 mA to 16 mA output drive current, depending on the I/O standard and supply voltage.

The SSTL18 and SSTL2 I/O standards offer full- and half-strength drive current options

Differential Inputs and Outputs

All PIO pins support "single-ended" I/O standards, such as LVCMOS. However, iCE65P FPGAs also support differential I/O standards where a single data value is represented by two complementary signals transmitted or received using a pair of PIO pins. The PIO pins in I/O Bank 3 support Low-Voltage Differential Swing (LVDS) and SubLVDS inputs as shown in Figure 7. Differential outputs are available in all four I/O banks.

Differential Inputs Only on I/O Bank 3

Differential receivers are required for popular applications such as LVDS and LVPECL clock inputs, camera interfaces, and for various telecommunications standards.

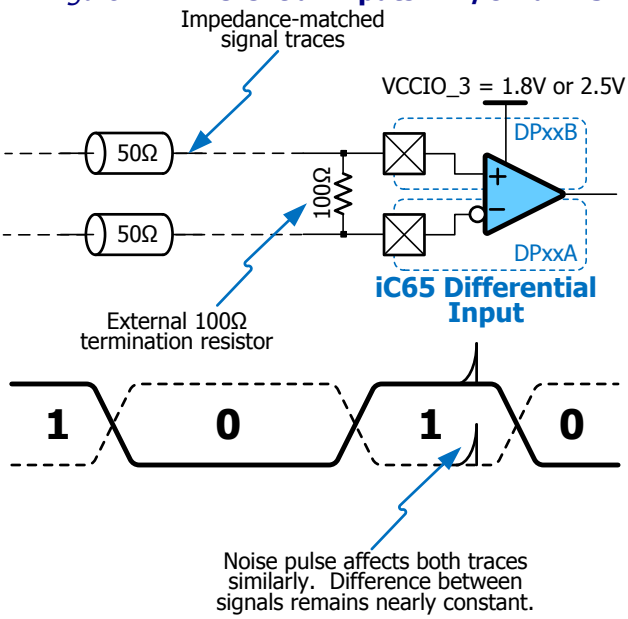
Specific pairs of PIO pins in I/O Bank 3 form a differential input. Each pair consists of a DPxxA and DPxxB pin, where "xx" represents the pair number. The DPxxB receives the true version of the signal while the DPxxA receives the complement of the signal. Typically, the resulting signal pair is routed on the printed circuit board (PCB) with matched 50Ω signal impedance. The differential signaling, the low voltage swing, and the matched signal routing are ideal for communicating very-high frequency signals. Differential signals are generally also more tolerant of system noise and generate little EMI themselves.

The LVDS input circuitry requires 2.5V on the VCCIO_3 voltage supply. Similarly, the SubLVDS input circuitry requires 1.8V on the VCCIO_3 voltage supply. For electrical specifications, see "Differential Inputs" on page 75.

Each differential input pair requires an external 100 Ω termination resistor, as shown in Figure 7.

The PIO pins that make up a differential input pair are indicated with a blue bounding box in the footprint diagrams and in the pinout tables.

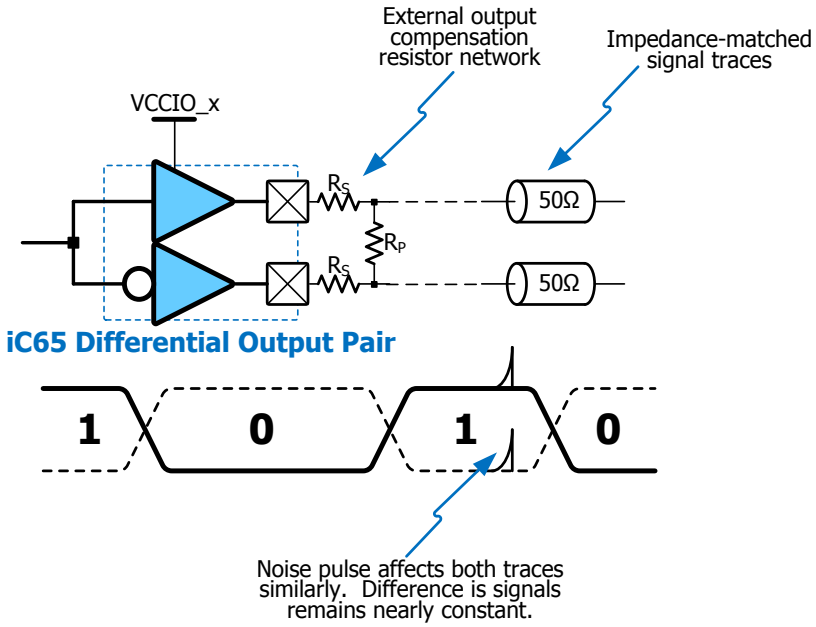
Figure 7: **Differential Inputs in I/O Bank 3**



Differential Outputs in Any Bank

Differential outputs are built using a pair of single-ended PIO pins as shown in Figure 8. Each differential I/O pair requires a three-resistor termination network to adjust output characteristic to match those for the specific differential I/O standard. The output characteristics depend on the values of the parallel resistors (RP) and series resistor (RS). Differential outputs must be located in the same I/O tile.

Figure 8: **Differential Output Pair**



For electrical characteristics, see "Differential Outputs" on page 75.

The PIO pins that make up a differential output pair are indicated with a blue bounding box in the in the tables in "Die Cross Reference" starting on page 67.

Input Signal Path

As shown in Figure 6, a signal from a package pin optionally feeds directly into the device, or is held in an input register. The input signal connects to the programmable interconnect resources through the IN signal. Table 9 describes the input behavior, assuming that the output path is not used or if a bidirectional I/O, that the output driver is in its high-impedance state (Hi-Z). Table 9 also indicates the effect of the Power-Saving I/O Bank iCEgate Latch and the Input Pull-Up Resistors on I/O Banks 0, 1, and 2.

See Input and Output Register Control per PIO Pair for information about the registered input path.

Power-Saving I/O Bank iCEgate Latch

To save power, the optional iCEgate latch can selectively freeze the state of individual, non-registered inputs within an I/O bank. Registered inputs are effectively frozen by their associated clock or clock-enable control. As shown in Figure 9, the iCEgate HOLD control signal captures the external value from the associated asynchronous input. The HOLD signal prevents switching activity on the PIO pad from affecting internal logic or programmable interconnect. Minimum power consumption occurs when there is no switching. However, individual pins within the I/O bank can bypass the iCEgate latch and directly feed into the programmable interconnect, remaining active during low-power operation. This behavior is described in Table 9. The decision on which asynchronous inputs use the iCEgate feature and which inputs bypass it is determined during system design. In other words, the iCEgate function is part of the source design used to create the iCE65P configuration image.

Figure 9: **Power-Saving iCEgate Latch**

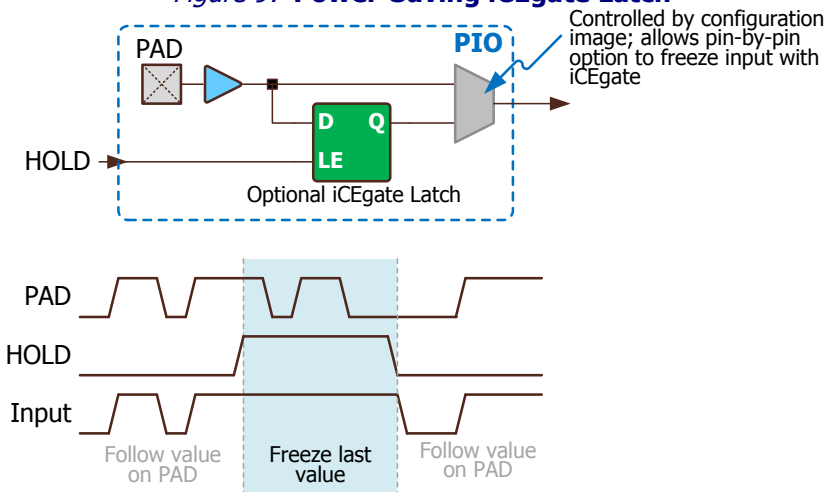


Table 9: **PIO Non-Registered Input Operations**

Operation	HOLD	Bitstream Setting		PAD	IN
	iCEgate Latch	Controlled by iCEgate?	Input Pull-Up Enabled?	Pin Value	Input Value to Interconnect
Data Input	0	X	X	PAD	PAD Value
Pad Floating, No Pull-up	0	X	No	Z	(Undefined)
Pad Floating, Pull-up	0	X	Yes	Z	1
Data Input, Latch Bypassed	X	No	X	PAD	PAD Value
Pad Floating, No Pull-up, Latch Bypassed	X	No	No	Z	(Undefined)
Pad Floating, Pull-up, Latch Bypassed	X	No	Yes	Z	1
Low Power Mode, Hold Last Value	1	Yes	X	X	Last Captured PAD Value

There are four iCEgate HOLD controls, one per each I/O bank. The iCEgate HOLD control input originates within the interconnect fabric, near the middle of the I/O edge. Consequently, the HOLD signal is optionally controlled externally through a PIO pin or from other logic within the iCE65P device.

For best possible performance, the global buffer inputs (GBIN[7:0]) connect directly to the their associated global buffers (GBUF[7:0]), bypassing the PIO logic and iCEgate circuitry as shown in Figure 6. Consequently, the direct GBIN-to-GBUF connection cannot be blocked by the iCEgate circuitry. However, it is possible to use iCEgate to block PIO-to-GBUF clock connections.

For additional information on using the iCEgate feature, please refer to the following application note.

AN002: Using iCEgate Blocking for Ultra-Low Power
www.siliconbluetech.com/media/AN2iCEGATErev1.1.pdf

Input Pull-Up Resistors on I/O Banks 0, 1, and 2

The PIO pins in I/O Banks 0, 1, and 2 have an optional input pull-up resistor. Pull-up resistors are not provided in I/O Bank 3.

During the iCE65P configuration process, the input pull-up resistor is unconditionally enabled and pulls the input to within a diode drop of the associated I/O bank supply voltage (VCCIO_#). This prevents any signals from floating on the circuit board during configuration.

After iCE65P configuration is complete, the input pull-up resistor is optional, defined by a configuration bit. The pull-up resistor is also useful to tie off unused PIO pins. The SiliconBlue iCEcube development software defines all unused PIO pins in I/O Banks 0, 1 and 2 as inputs with the pull-up resistor turned on.

The pull-up resistor value depends on the VCCIO voltage applied to the bank, as shown in Table 52.

No Input Pull-up Resistors on I/O Bank 3

The PIO pins associated with I/O Bank 3 do not have an internal pull-up resistor. To minimize power consumption, tie unused PIO pins in Bank 3 to a known logic level or drive them as a disabled high-impedance output.

Input Hysteresis

Inputs typically have about 50 mV of hysteresis, as indicated in Table 52.

Output and Output Enable Signal Path

As shown in Figure 6, a signal from programmable interconnect feeds the OUT signal on a Programmable I/O pad. This output connects either directly to the associated package pin or is held in an optional output flip-flop. Because all flip-flops are automatically reset after configuration, the output from the output flip-flop can be optionally inverted so that an active-Low output signal is held in the disabled (High) state immediately after configuration.

Similarly, each Programmable I/O pin has an output enable or three-state control called OE. When OE = High, the OUT output signal drives the associated pad, as described in Table 10. When OE = Low, the output driver is in the high-impedance (Hi-Z) state. The OE output enable control signal itself connects either directly to the output buffer or is held in an optional register. The output buffer is optionally permanently enabled or permanently disabled, either to unconditionally drive output signals, or to allow input-only signals.

Table 10: **PIO Output Operations (non-registered operation, no inversions)**

Operation	OUT	OE	PAD
	Data Output	Enable	
Three-State	X	0	Hi-Z
Drive Output Data	OUT	1*	OUT

X = don't care, 1* = High or unused, Hi-Z = high-impedance, three-stated, floating.

See Input and Output Register Control per PIO Pair for information about the registered input path.

Input and Output Register Control per PIO Pair

PIO pins are grouped into pairs for synchronous control. Registers within pairs of PIO pins share common input clock, output clock, and I/O clock enable control signals, as illustrated in Figure 10. The combinational logic paths are removed from the drawing for clarity.

The INCLK clock signal only controls the input flip-flops within the PIO pair.

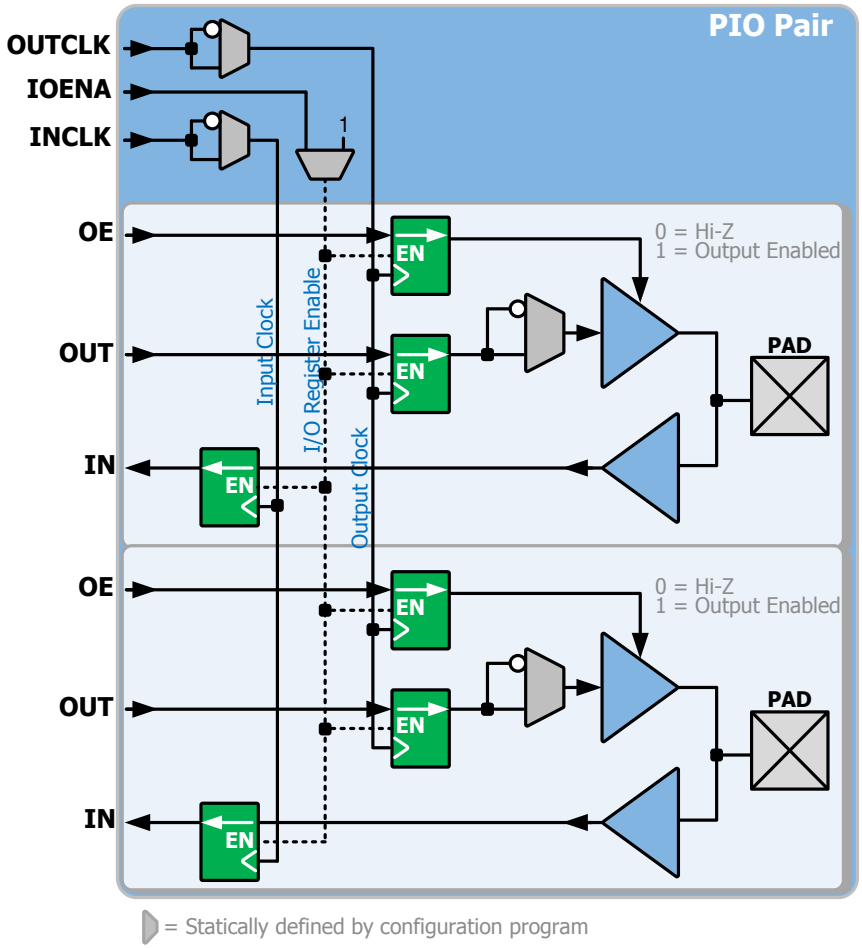
The OUTCLK clock signal controls the output flip-flops and the output-enable flip-flops within the PIO pair.

If desired in the iCE65P application, the INCLK and OUTCLK signals can be connected together using **Error! eference source not found.**.

The IOENA clock-enable input, if used, enables all registers in the PIO pair, as shown in Figure 10. By default, the registers are always enabled.

Before laying out your printed-circuit board, run the design through the iCEcube development software to verify that your selected pinout complies with these I/O register pairing requirements. See tables in "Die Cross Reference" starting on page 67.

Figure 10: **PIO Pairs Share Clock and Clock Enable Controls (only registered paths shown for clarity)**

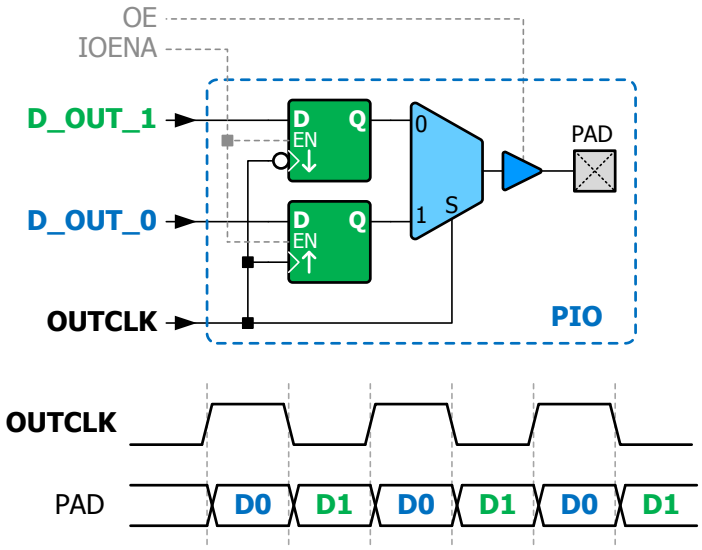


The pairing of PIO pairs is most evident in the tables in "Die Cross Reference" starting on page 67.

Double Data Rate (DDR) Flip-Flops

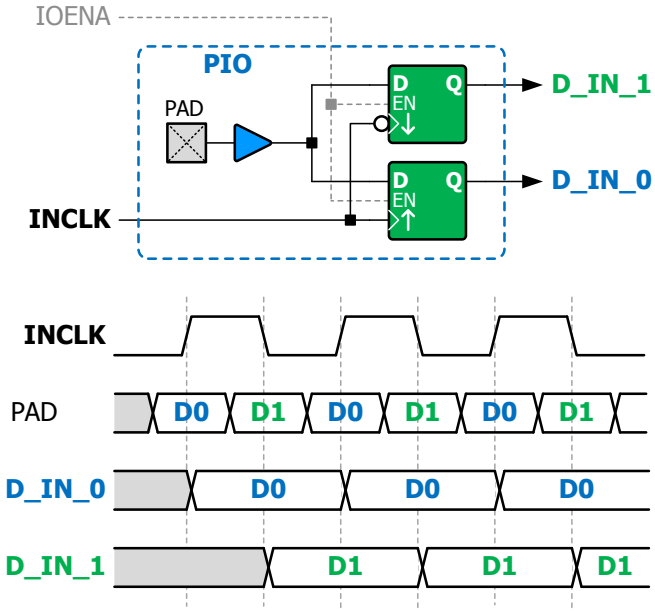
Each individual PIO pin optionally has two sets of double data rate (DDR) flip-flops; one input pair and one output pair. Figure 11 demonstrates the functionality of the output DDR flip-flop. Two signals from within the iCE65P device drive the DDR output flip-flop. The D_OUT_0 signal is clocked by the rising edge of the OUTCLK signal while the D_OUT_1 signal is clocked by the falling edge of the OUTCLK signal, assuming no optional clock polarity inversion. Internally, the two individual flip-flops are multiplexed together before the data appears at the pad, effectively doubling the output data rate.

Figure 11: **DDR Output Flip-Flop**



Similarly, Figure 12 demonstrates the DDR input flip-flop functionality. A double data rate (DDR) signal arrives at the pad. Internally, one value is clocked by the rising edge of the INCLK signal and another value is clocked by the falling edge of the INCLK signal. The DDR data stream is effectively de-multiplexed within the PIO pin and presented to the programmable interconnect on D_IN_0 and D_IN_1.

Figure 12: **DDR Input Flip-Flop**



The DDR flip-flops provide several design advantages. Internally within the iCE65P device, the clock frequency is half the effective external data rate. The lower clock frequency eases internal timing, doubling the clock period, and slashes the clock-related power in half.

Global Routing Resources

Global Buffers

Each iCE65P component has eight global buffer routing connections, illustrated in Figure 13.

There are eight high-drive buffers, connected to the eight low-skew, global lines. These lines are designed primarily for clock distribution but are also useful for other high-fanout signals such as set/reset and enable signals. The global buffers originate either from the Global Buffer Inputs (GBINx) or from programmable interconnect. The associated GBINx pin represents the best pin to drive a global buffer from an external source. However, the application with an iCE65P FPGA can also drive a global buffer via any other PIO pin or from internal logic using the programmable interconnect.

If not used in an application, individual global buffers are turned off to save power.

Figure 13: **High-drive, Low-skew, High-fanout Global Buffer Routing Resources**

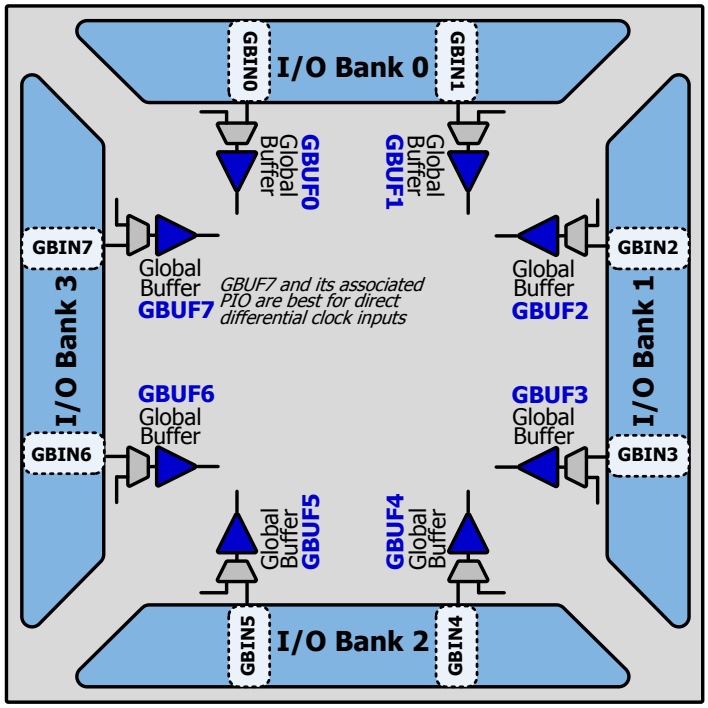


Table 11 lists the connections between a specific global buffer and the inputs on a Programmable Logic Block (PLB). All global buffers optionally connect to all clock inputs. Any four of the eight global buffers can drive logic inputs to a PLB. Even-numbered global buffers optionally drive the Reset input to a PLB. Similarly, odd-numbered buffers optionally drive the PLB clock-enable input.

Table 11: **Global Buffer (GBUF) Connections to Programmable Logic Block (PLB)**

Global Buffer	LUT Inputs	Clock	Clock Enable	Reset
GBUF0	Yes, any 4 of 8 GBUF buffers	Yes	Yes	No
GBUF1		Yes	No	Yes
GBUF2		Yes	Yes	No
GBUF3		Yes	No	Yes
GBUF4		Yes	Yes	No
GBUF5		Yes	No	Yes
GBUF6		Yes	Yes	No
GBUF7		Yes	No	Yes

Table 12 and Table 13 list the connections between a specific global buffer and the inputs on a Programmable I/O (PIO) pair. Although there is no direct connection between a global buffer and a PIO output, such a connection is possible by first connecting through a PLB LUT4 function. Again, all global buffers optionally drive all clock inputs. However, even-numbered global buffers optionally drive the clock-enable input on a PIO pair.

Table 12: **iCE65P04: Global Buffer (GBUF) Connections to Programmable I/O (PIO) Pair**

Global Buffer	Output Connections	Input Clock	Output Clock	Clock Enable
GBUF0	No (connect through PLB LUT)	Yes	Yes	No
GBUF1		Yes	Yes	Yes
GBUF2		Yes	Yes	No
GBUF3		Yes	Yes	Yes
GBUF4		Yes	Yes	No
GBUF5		Yes	Yes	Yes
GBUF6		Yes	Yes	No
GBUF7		Yes	Yes	Yes

Table 13: **iCE64L08: Global Buffer (GBUF) Connections to Programmable I/O (PIO) Pair**

Global Buffer	Output Connections	Input Clock	Output Clock	Clock Enable
GBUF0	No (connect through PLB LUT)	Yes	Yes	Yes
GBUF1		Yes	Yes	No
GBUF2		Yes	Yes	Yes
GBUF3		Yes	Yes	No
GBUF4		Yes	Yes	Yes
GBUF5		Yes	Yes	No
GBUF6		Yes	Yes	Yes
GBUF7		Yes	Yes	No

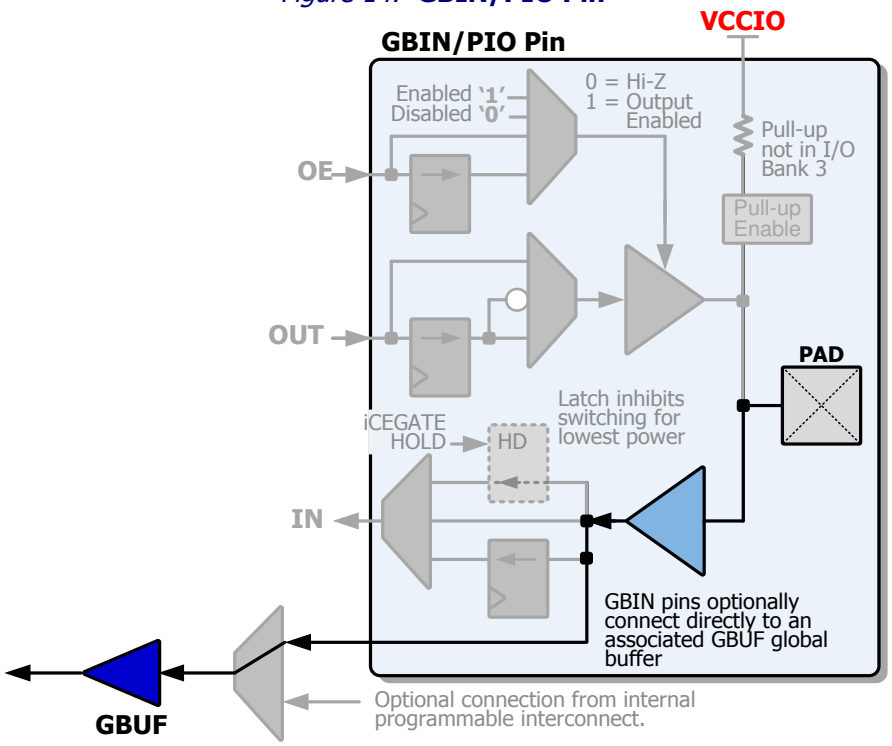
Global Buffer Inputs

The iCE65P component has eight specialized GBIN/PIO pins that are optionally direct inputs to the global buffers, offering the best overall clock characteristics. As shown in Figure 14, each GBIN/PIO pin is a full-featured I/O pin but also provides a direct connection to its associated global buffer. The direct connection to the global buffer bypasses the iCEgate input-blocking latch and other PIO input logic. These special PIO pins are allocated two to an I/O Bank, a total of eight. These pins are labeled GBIN0 through GBIN7, as shown in Figure 13 and the pin locations for each GBIN input appear in Table 14.

Table 14: **Global Buffer Input Ball Number by Package**

Global Buffer Input (GBIN)	I/O Bank	Package Code		
		`P04 CB121	**`P04 CB196**	**`P04 CB284**
GBIN0	0	D6	A7	E10
GBIN1		C6	E7	E11
GBIN2	1	F9	F10	L18
GBIN3		F8	G12	K18
GBIN4	2	L9	L7	V12
GBIN5		L8	P5	V11
GBIN6	3	F4	H1	M5
GBIN7		D3	G1	L5

Figure 14: **GBIN/PIO Pin**



Differential Global Buffer Input

All eight global buffer inputs support single-ended I/O standards such as LVCMOS. Global buffer GBUF7 in I/O Bank 3 also provides an optional direct SubLVDS, LVDS, or LVPECL differential clock input, as shown in Figure 15. The GBIN7 and its associated differential I/O pad accept a differential clock signal. A 100 Ω termination resistor is required across the two pads. Optionally, swap the outputs from the LVDS or LVPECL clock driver to invert the clock as it enters the iCE65P device.

Figure 15: **LVDS or LVPECL Clock Input**

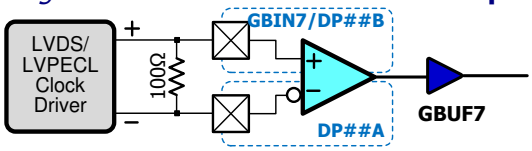


Table 15 lists the pin or ball numbers for the differential global buffer input by package style. Although this differential input is the only one that connects directly to a global buffer, other differential inputs can connect to a global buffer using general-purpose interconnect, with slightly more signal delay.

Table 15: **Differential Global Buffer Input Ball Number by Package**

Differential Global Buffer Input (GBIN)	I/O Bank	Package Code		
		`P04 CB121	`P04 CB196	`P04 CB284
GBIN7/DPxxB	3	D3	G1	L5
DPxxA		E3	G2	L3

Automatic Global Buffer Insertion, Manual Insertion

The iCEcube development software automatically assigns high-fanout signals to a global buffer. However, to manual insert a global buffer input/global buffer (GBIN/GBUF) combination, use the `SB_IO_GB` primitive. To insert just a global buffer (GBUF), use the `SB_GB` primitive.

Global Hi-Z Control

The global high-impedance control signal, GHIZ, connects to all I/O pins on the iCE65P device. This GHIZ signal is automatically asserted throughout the configuration process, forcing all user-I/O pins into their high-impedance state. Similarly, the PIO pins can be forced into their high-impedance state via the JTAG controller.

Global Reset Control

The global reset control signal connects to all PLB and PIO flip-flops on the iCE65P device. The global reset signal is automatically asserted throughout the configuration process, forcing all flip-flops to their defined wake-up state. For PLB flip-flops, the wake-up state is always reset, regardless of the PLB flip-flop primitive used in the application. See Table 3 for more information.

The PIO flip-flops are always reset during configuration, although the output flip-flop can be inverted before leaving the iCE65P device, as shown in Figure 10.

Phase-Locked Loop (PLL)

To support a variety of display, imager, and memory interface applications, the iCE65P FPGA family includes an ultra-low power Phase Locked Loop (PLL), as shown in Figure 16. The iCEcube development software provides three PLL macro variants, depending on whether the clock originates inside the FPGA or from an external source, and whether only the PLL output connects to a global buffer, or whether both the PLL output and the clock input pad, as described in Table 16.

Figure 16: **Phase-Locked Loop (PLL)**

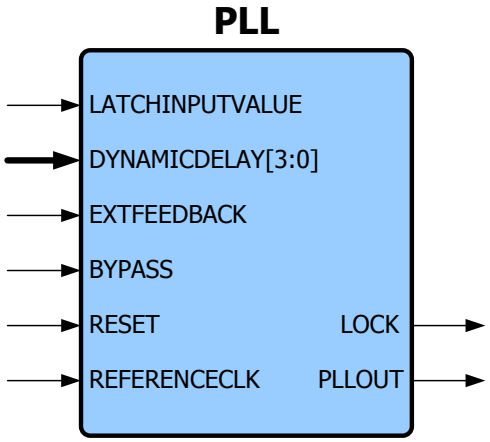


Table 16: **PLL Macro Types**

PLL Macro Name	Clock Input	GBUF	GBUF
SB_PLL_CORE	FPGA routing	PLL output	N/A
SB_PLL_PAD	PAD	PLL output	N/A
SB_PLL_2_PAD	PAD	PLL output	Clock input from pad

The PLL provides the following functions for the iCE65P application.

- Generates a new output clock frequency
  - Clock multiplication
  - Clock division
  - Clock scaling to maximize performance or to minimize power consumption
- De-skews or phase-aligns an output clock to the input reference clock.
  - Faster input setup time
  - Faster clock-to-output time
- Corrects output clock to have nearly a 50% duty cycle, which is important for Double Data Rate (DDR) applications.
- Optionally phase shifts the output clock relative to the input reference clock.
  - Optimal data sampling within the available bit period
  - Fixed quadrant phase shifting at 0°, 90°, 180°, and 270°.
  - Optional fine delay adjustments of up to 2.5 ns (nominal) in 165 ps increments (nominal).

Signals

Table 17 lists the signal names, direction, and function of each connection to the PLL. Some of the signals have an associated attribute or property, listed in Table 18.

Table 17: **PLL Signals**

Signal Name	Direction	Description
REFERENCECLK	Input	Input reference clock
RESET	Input	Reset
BYPASS	Input	When FEEDBACK_PATH is set to SIMPLE, the BYPASS control selects which clock signal connects to the PLLOUT output. 0 = PLL generated signal 1 = REFERENCECLK
EXTFEEDBACK	Input	External feedback input to PLL. Enabled when FEEDBACK_PATH attribute set to EXTERNAL.
DYNAMIC_DELAY[3:0]	Input	Fine delay adjustment control inputs. Enabled when DELAY_ADJUSTMENT_MODE set to DYNAMIC
LATCHINPUTVALUE	Input	When enabled, forces the PLL into low-power mode; PLL output held static at last input clock value. Set ENABLE ICEGATE_PORTA and PORTB to '1' to enable.
PLLOUT	Output	Output from the Phase-Locked Loop (PLL). Connects to programmable interconnect and has optimal connections to global clock buffers GBUF4 and GBUF5.
LOCK	Output	When High, indicates that the PLL output is phase aligned or locked to the input reference clock.

Attributes/Properties

Table 18 lists the attributes or properties associated with the PLL and the allowable settings for each attribute..

Table 18: **PLL Attributes and Settings**

Attribute/Property	Description	Setting	Description
FEEDBACK_PATH	Selects the feedback path to the PLL	SIMPLE	Feedback directly from VCO
		DELAY	Feedback from VCO through fine delay adjustment
		PHASE_AND_DELAY	Feedback from VCO through the fine delay adjustment and phase shifter; feedback is further divided by four
		EXTERNAL	Feedback from EXTFEEDBACK input
DELAY_ADJUSTMENT_MODE	Selects the control input for the fine delay adjustment. Delays the PLLOUT output nominally by (***n***+1) • 150 ps	FIXED	Delay controlled by FIXED_DELAY_ADJUSTMENT setting
		DYNAMIC	Delay controlled by current value of DYNAMIC_DELAY[3:0]
FIXED_DELAY_ADJUSTMENT	Sets the constant value for the fine delay adjustment when DELAY_ADJUSTMENT mode set to FIXED	0, 1, ..., 15	Delays the PLLOUT output by specified setting
PLL_OUT_PHASE	Controls the phase alignment of the PLLOUT output relative to the input reference clock; see Figure 18	NONE	Phase alignment disabled, no duty-cycle correction
		0deg	0° phase shift (no phase shift)
		90deg	90° phase shift (quarter cycle shift)
		180deg	180° phase shift (half-cycle shift)
		270deg	270° phase shift (three-quarter cycle shift)
DIVR	Divider value for the input clock	0, 1, ..., 15	These attributes control the PLL output frequency. See Equation 2 and Equation 3 and the Frequency Synthesis spreadsheet.
DIVF	Divider value for feedback	0, 1, ..., 63	
DIVQ	Divider value for the VCO output, generates PLLOUT	0, 1, ..., 5	
RANGE	Controls the PLL operating range	0, 1, ..., 7	
ENABLE_ICEGATE	Enables iCEgate to disable GBUF transitions	0	GBUF disabled
		1	GBUF enabled

Clock Input Requirements

For proper operation, the PLL requires ...

- A stable monotonic (single frequency) reference clock input.
- The reference clock input must be within the input clock frequency range, F_{REF}, specified in Table 60.
- The reference clock must have a duty cycle that meets the requirement specified in Table 60.
- The jitter on the reference input clock must not exceed the limits specified in Table 60.

PLL Output Requirements

The PLL output clock, PLLOUT requires the following restrictions.

- The PLLOUT output frequency must be within the limits specified in Table 60.
- The PLLOUT output is not valid or stable until the PLL's LOCK output remains High.

Voltage Controlled Oscillator Supply Inputs

The phase-locked loop (PLL) uses separate analog supply inputs for the voltage-controlled oscillator (VCO).

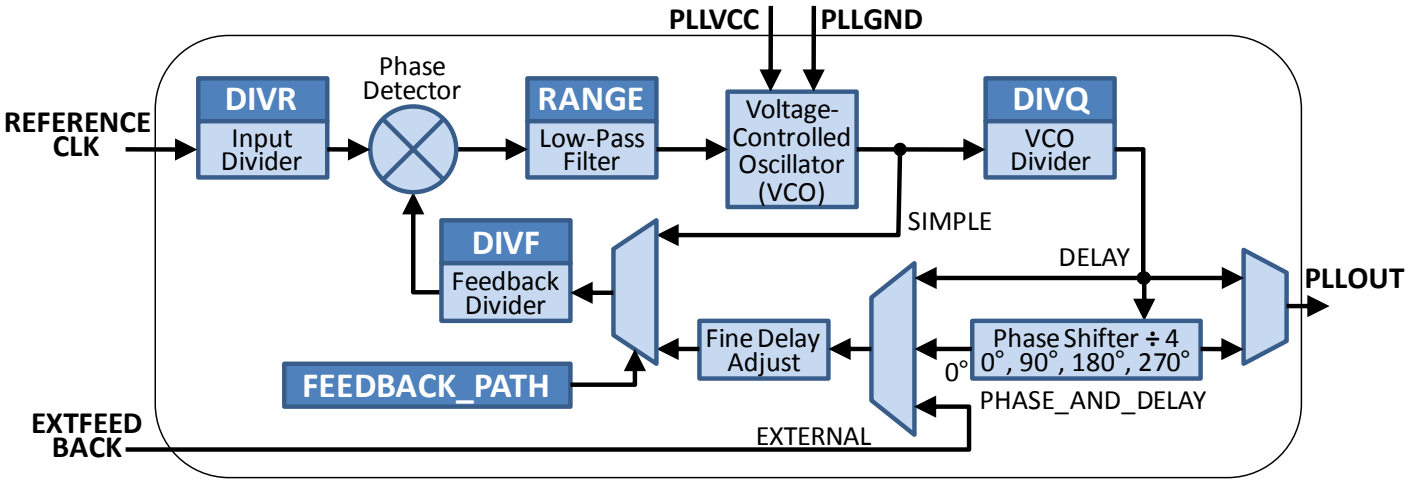
Table 19: **PLL Supply Ball Numbers by Package**

ColdBoot Select	Package Code		
	CB121	**CB196**	**CB284**
PLLGND	L6	M6	Y9
PLLVCC	L7	N6	Y10

Clock Multiplication and Division

The PLL optionally multiplies and/or divides the input reference clock to generate a PLLOUT output clock of another frequency. The output frequency depends on the frequency of the REFERENCLK input clock and the settings for the DIVR, DIVF, DIVQ, RANGE, and FEEDBACK_PATH attribute settings, as indicated in Figure 17.

Figure 17: **PLL Frequency Synthesis**



The PLL's phase detector and Voltage Controlled Oscillator (VCO) synthesize a new output clock frequency based on the attribute settings. The VCO is an analog circuit and has independent voltage supply and ground connections labeled PLLVCC and PLLGND.

The simplest method to determine the optimal settings for a specific application is to use the Frequency Synthesis Spreadsheet

PLLOUT Frequency for All Modes Except FEEDBACK_PATH = SIMPLE

For all the FEEDBACK_PATH modes, except SIMPLE, the PLLOUT frequency is the result of Equation 2.

$$F_{PLLOUT} = \frac{F_{REFERNCECLK} \bullet (DIVF + 1)}{DIVR + 1} \qquad \text{[Equation 2]}$$

PLLOUT Frequency for FEEDBACK_PATH = SIMPLE

If the SIMPLE feedback mode, the PLL feedback signal taps directly from the output of the VCO, before the final divider stage. Consequently, the PLL output frequency has an additions divider step, DIVQ, contributed by the final divider step as shown in Equation 3. (DIVF, DIVQ and DIVR are binary)

$$F_{PLLOUT} = \frac{F_{REFERNCECLK} \bullet (DIVF + 1)}{2^{(DIVQ)} \bullet (DIVR + 1)} \qquad \text{[Equation 3]}$$

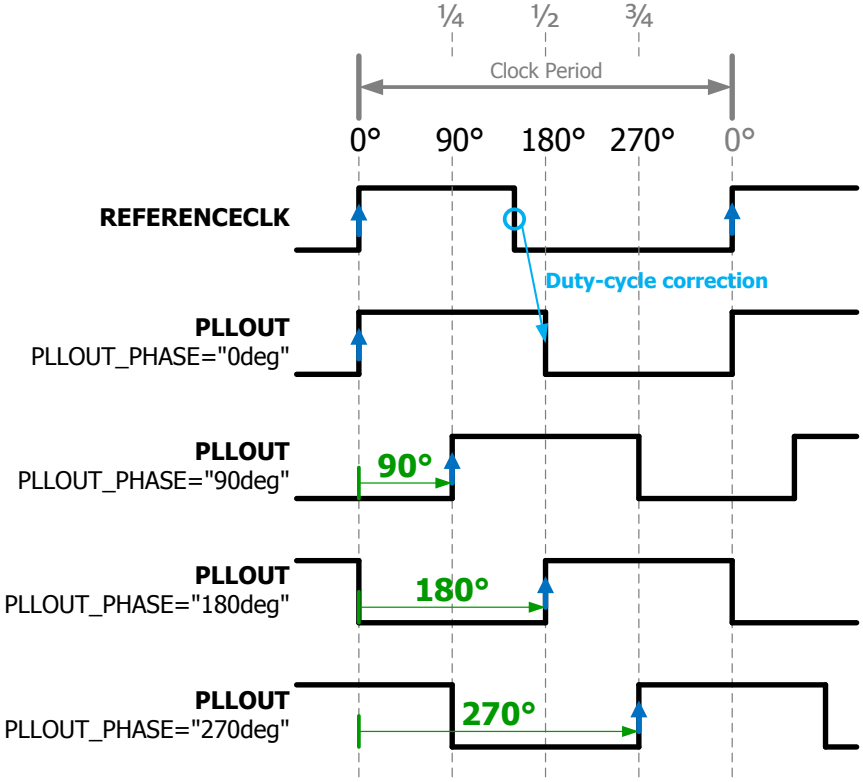
Fixed Quadrant Phase Shift

The PLL optional phase feature shifts the PLLOUT output by a specified quadrant or quarter clock cycle as shown in Figure 18 and Table 20. The quadrant phase shift option is only available when the FEEDBACK_PATH attribute is set to PHASE_AND_DELAY.

Table 20: **PLL Phase Shift Options**

PLLOUT_PHASE	Duty Cycle Correction	Phase Shift (Degrees)	Fraction Clock Cycle
NONE	No	0°	None
0deg	Yes	0°	None
90deg	Yes	90°	Quarter Cycle
180deg	Yes	180°	Half Cycle
270deg	Yes	270°	Three-quarter Cycle

Figure 18: **Fixed Quadrant Phase Shift Control (PLLOUT_PHASE)**



Unlike the Fine Delay Adjustment, the quadrant phase shifter always shifts by a fixed phase angle. The resulting phase shift, measured in delay, depends on the clock period and the PLLOUT_PHASE phase shift setting, as shown in Equation 4.

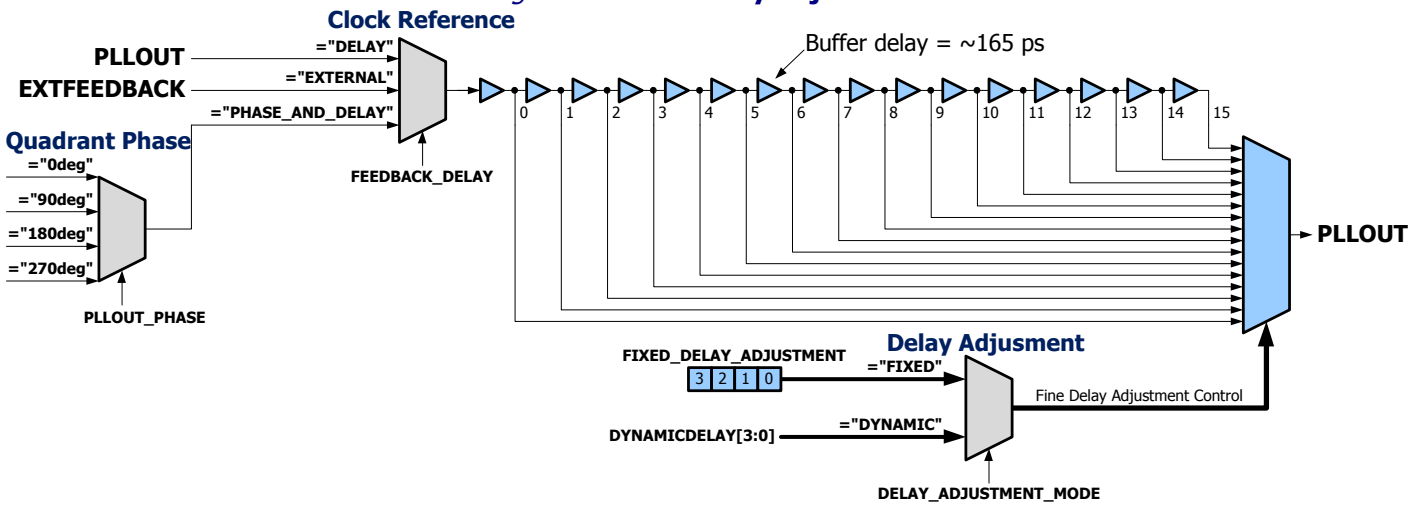
$$Delay = \frac{Phase\_Shift}{360^{\circ}} \bullet Clock\_Period \qquad \text{[Equation 4]}$$

Fine Delay Adjustment

As shown in Figure 19, the PLL provides an optional fine delay adjustment that controls the delay of the PLLOUT output relative to the input reference clock, to an external feedback signal, or relative to the selected quadrant phase shifted clock. The delay is adjusted by selecting one or more of the 16 delay taps. Each tap is approximately 165 ps.

The fine delay adjustment option is available when the FEEDBACK_PATH attribute is set to DELAY, PHASE_AND_DELAY, or EXTERNAL, as shown in Figure 19 and Figure 17.

Figure 19: **Fine Delay Adjust Controls**



Fine Adjustment Control

The number of delay taps is controlled either statically using the FIXED_DELAY_ADJUSTMENT option or dynamically by the application using the PLL's DYNAMIC_DELAY[3:0] inputs, as described in Table 21.

Table 21: **Fine Delay Adjustment Control**

DELAY_ADJUSTMENT_MODE Setting	Adjustment Control
FIXED	FIXED_DELAY_ADJUSTMENT attribute setting
DYNAMIC	DYNAMIC_DELAY[3:0] control inputs

Fine Adjustment Delay

The resulting nominal fine adjustment delay value is shown in Equation 5, where ***n*** is either the value of the FIXED_DELAY_ADJUSTMENT attribute setting or the dynamic binary value presented on the DYNAMIC_DELAY[3:0] inputs. The actual delay varies slightly due to the slight differences in the delay tap buffer delay.

$$\text{Fine Delay Adjustment } \textit{(nominal)} = (n + 1) \bullet 165 \text{ ps} \qquad \text{[Equation 5]}$$

Phase Angle Equivalent

The fine delay adjustment feature always injects an actual delay value, not a fixed phase angle like the Fixed Quadrant Phase Shift feature. Use Equation 6 to convert the fine adjustment delay to a resulting phase angle.

$$\text{Phase\_Shift} = \frac{\text{Fine\_Delay\_Adjustment}}{\text{Clock\_Period}} \bullet 360^{\circ} \qquad \text{[Equation 6]}$$

Low Power Mode

The phase-lock loop (PLL) has low operating power by default. The PLL can be dynamically disabled to further reduce power. The low-power mode must first be enabled by setting the ENABLE_ICEGATE attribute to '1'. Once enabled, use the LATCHINPUTVALUE to control the PLL's operation, as shown in Table 22. The PLL must reacquire the input clock and LOCK when LATCHINPUTVALUE returns from '1' to '0', external feedback is used and path goes out into the fabric.

Table 22: **PLL LATCHINPUTVALUE Control**

ENABLE_ICEGATE Attribute	LATCHINPUTVALUE Input	Function
0	Don't care	PLL is always enabled
1	0	PLL is enabled and operating
	1	PLL is in low-power mode; PLLOUT output holds last clock state

RAM

Each iCE65P device includes multiple high-speed synchronous RAM blocks (RAM4K), each 4Kbit in size. As shown in Table 23 a single iCE65P integrates between 16 to 96 such blocks. Each RAM4K block is generically a 256-word deep by 16-bit wide, two-port register file, as illustrated in Figure 20. The input and output connections, to and from a RAM4K block, feed into the programmable interconnect resources.

Figure 20: **RAM4K Memory Block**

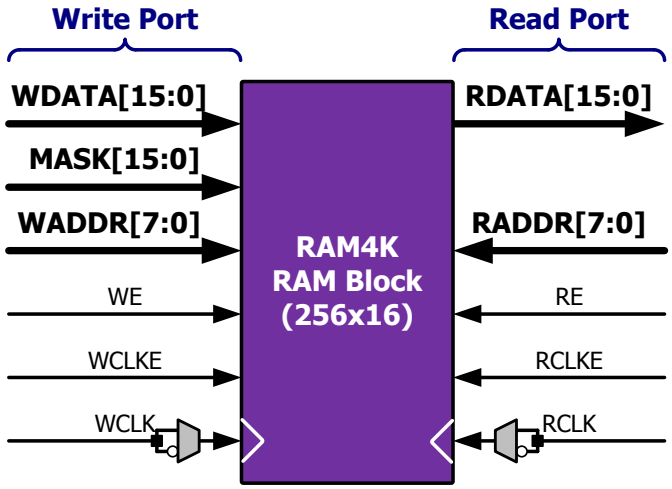


Table 23: **RAM4K Blocks per Device**

Device	RAM4K Blocks	Default Configuration	RAM Bits per Block	Block RAM Bits
iCE65P04	20	256 x 16	4K (4,096)	80K

Using programmable logic resources, a RAM4K block implements a variety of logic functions, each with configurable input and output data width.

- Random-access memory (RAM)
  - Single-port RAM with a common address, enable, and clock control lines
  - Two-port RAM with separate read and write control lines, address inputs, and enable
- Register file and scratchpad RAM
- First-In, First-Out (FIFO) memory for data buffering applications
- Circuit buffer
- A 256-deep by 16-wide ROM with registered outputs, contents loaded during configuration
  - Sixteen different 8-input look-up tables
  - Function or waveform tables such as sine, cosine, etc.
  - Correlators or pattern matching operations
- Counters, sequencers

As pictured in Figure 20, a RAM4K block has separate write and read ports, each with independent control signals. Table 24 lists the signals for both ports. Additionally, the write port has an active-Low bit-line write-enable control; optionally mask write operations on individual bits. By default, input and output data is 16 bits wide, although the data width is configurable using programmable logic and, if needed, multiple RAM4K blocks.

The WCLK and RCLK inputs optionally connect to one of the following clock sources.

- The output from any one of the eight Global Buffers, or
- A connection from the general-purpose interconnect fabric

The data contents of the RAM4K block are optionally pre-loaded during iCE65P device configuration. If the RAM4K blocks are not pre-loaded during configuration, then the resulting configuration bitstream image is smaller. However, if an uninitialized RAM4K block is used in the application, then the application must initialize the RAM contents to guarantee the data value.

See Table 59 for detailed timing information.

Signals

Table 24 lists the signal names, direction, and function of each connection to the RAM4K block. See also Figure 20.

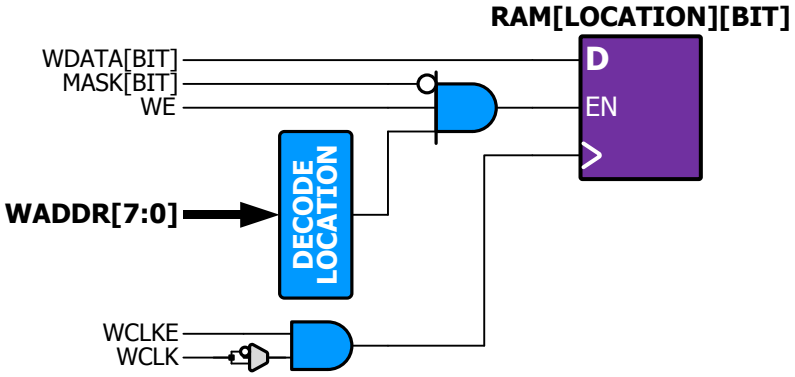
Table 24: **RAM4K Block RAM Signals**

Signal Name	Direction	Description
WDATA[15:0]	Input	Write Data input.
MASK[15:0]	Input	Masks write operations for individual data bit-lines. 0 = Write bit; 1 = Don't write bit
WADDR[7:0]	Input	Write Address input. Selects one of 256 possible RAM locations.
WE	Input	Write Enable input.
WCLKE	Input	Write Clock Enable input.
WCLK	Input	Write Clock input. Default rising-edge, but with falling-edge option.
RDATA[15:0]	Output	Read Data output.
RADDR[7:0]	Input	Read Address input. Selects one of 256 possible RAM locations.
RE	Input	Read Enable input.
RCLKE	Input	Read Clock Enable input.
RCLK	Input	Read Clock input. Default rising-edge, but with falling-edge option.

Write Operations

Figure 21 shows the logic involved in writing a data bit to a RAM location. Table 25 describes various write operations for a RAM4K block. By default, all RAM4K write operations are synchronized to the rising edge of WCLK although the clock is invertible as shown in Figure 21.

Figure 21: **RAM4K Bit Write Logic**



When the WCLKE signal is Low, the clock to the RAM4K block is disabled, keeping the RAM in its lowest power mode.

Table 25: **RAM4K Write Operations**

Operation	WDATA[15:0] Data	MASK[15:0] Mask Bit	WADDR[7:0] Address	WE Write Enable	WCLKE Clock Enable	WCLK Clock	RAM Location
Disabled	X	X	X	X	X	0	No change
Disabled					0	X	No change
Disabled	X	X	X	0	X	X	No change
Write Data	WDATA[i]	MASK[i] = 0	WADDR	1	1	↑	RAM[WADDR][i] = WDATA[i]
Masked Write	X	MASK[i] = 1	WADDR	1	1	↑	RAM[WADDR][i] = No change

To write data into the RAM4K block, perform the following operations.

- Supply a valid address on the WADDR[7:0] address input port
- Supply valid data on the WDATA[15:0] data input port
- To write or mask selected data bits, set the associated MASK input port accordingly. For example, write operations on data bit D[i] are controlled by the associated MASK[i] input.
  - MASK[i] = 0: Write operations are enabled for data line WDATA[i]
  - MASK[i] = 1: Mask write operations are disabled for data line WDATA[i]
- Enable the RAM4K write port (WE = 1)
- Enable the RAM4K write clock (WCLKE = 1)
- Apply a rising clock edge on WCLK (assuming that the clock is not inverted)

Read Operations

Figure 22 shows the logic involved in reading a location from RAM. Table 26 describes various read operations for a RAM4K block. By default, all RAM4K read operations are synchronized to the rising edge of RCLK although the clock is invertible as shown in Figure 22.

Figure 22: **RAM4K Read Logic**

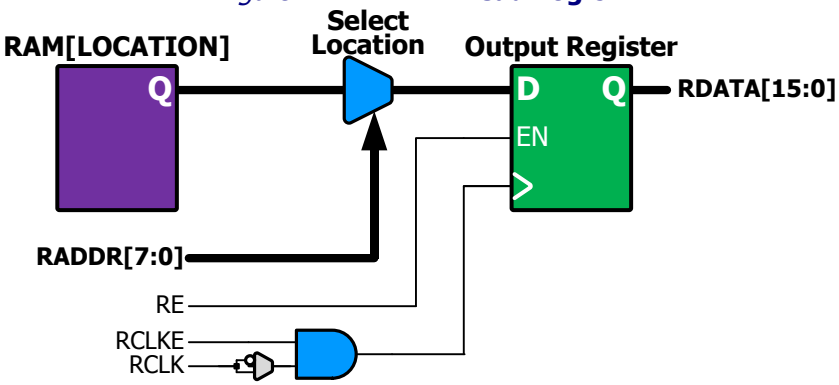


Table 26: **RAM4K Read Operations**

Operation	RADDR[7:0] Address	RE Read Enable	RCLKE Clock Enabe	RCLK Clock	RDATA[15:0]
After configuration, before first valid Read Data operation	X	X	X	X	Undefined
Disabled	X	X	X	0	No Change
Disabled		X	0	X	No Change
Disabled	X	0	X	X	No change
Read Data	RADDR	1	1	↑	RAM[RADDR]

To read data from the RAM4K block, perform the following operations.

- Supply a valid address on the RADDR[7:0] address input port
- Enable the RAM4K read port (RE = 1)
- Enable the RAM4K read clock (RCLKE = 1)
- Apply a rising clock edge on RCLK
- After the clock edge, the RAM contents located at the specified address (RADDR) appear on the RDATA output port

Read Data Register Undefined Immediately after Configuration

Unlike the flip-flops in the Programmable Logic Blocks and Programmable I/O pins, the RDATA[15:0] read data output register is not automatically reset after configuration. Consequently, immediately following configuration and before the first valid Read Data operation, the initial RDATA[15:0] read value is undefined.

Pre-loading RAM Data

The data contents for a RAM4K block can be optionally pre-loaded during iCE65P configuration. If not pre-loaded during configuration, then the RAM contents must be initialized by the iCE65P application before the RAM contents are valid.

Pre-loading the RAM data in the configuration bitstream increases the size of the configuration image accordingly.

RAM Contents Preserved during Configuration

RAM contents are preserved (write protected) during configuration, assuming that voltage supplies are maintained throughout. Consequently, data can be passed between multiple iCE65P configurations by leaving it in a RAM4K block and then skipping pre-loading during the subsequent reconfiguration. See "Cold Boot Configuration Option" and "Warm Boot Configuration Option" for more information.

Low-Power Setting

To place a RAM4K block in its lowest power mode, keep WCLKE = 0 and RCLKE = 0. In other words, when not actively using a RAM4K block, disable the clock inputs.

Device Configuration

As described in Table 27, iCE65P components are configured for a specific application by loading a binary configuration bitstream image, generated by the SiliconBlue development system. For high-volume applications, the bitstream image is usually permanently programmed in the on-chip Nonvolatile Configuration Memory (NVCM). However, the bitstream image can also be stored external in a standard, low-cost commodity SPI serial Flash PROM. The iCE65P component can automatically load the image using the SPI Master Configuration Interface. Similarly, the iCE65P configuration data can be downloaded from an external processor, microcontroller, or DSP processor using an SPI-like serial interface or an IEEE 1149 JTAG interface.

Table 27: **iCE65P Device Configuration Modes**

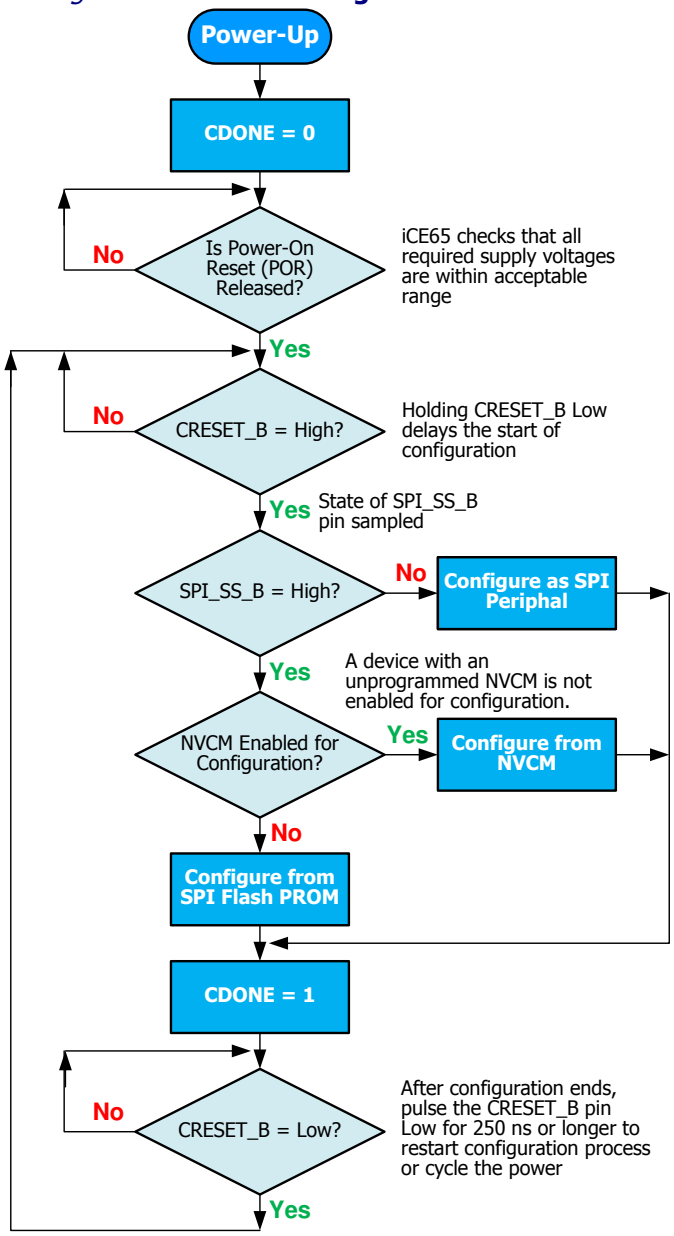
Mode	Analogy	Configuration Data Source
NVCM	ASIC	Internal, lowest-cost, secure, one-time programmable Nonvolatile Configuration Memory (NVCM)
SPI Flash	Microprocessor	External, low-cost, commodity, SPI serial Flash PROM
SPI Peripheral	Processor Peripheral	Configured by external device, such as a processor, microcontroller, or DSP using practically any data source, such as system Flash, a disk image, or over a network connection.
JTAG	JTAG	JTAG configuration requires sending a special command sequence on the SPI interface to enable JTAG configuration. Configuration is controlled by and external device.

Configuration Mode Selection

The iCE65P configuration mode is selected according to the following priority described below and illustrated in Figure 23.

- After exiting the Power-On Reset (POR) state or when CRESET_B returns High after being held Low for 250 ns or more, the iCE65P FPGA samples the logical value on its SPI_SS_B pin. Like other programmable I/O pins, the SPI_SS_B pin has an internal pull-up resistor (see Input Pull-Up Resistors on I/O Banks 0, 1, and 2).
- If the SPI_SS_B pin is sampled as a logic '1' (High), then …
  - Check if the iCE65P is enabled to configure from the Nonvolatile Configuration Memory (NVCM). If the iCE65P device has NVCM memory ('**F**' ordering code) but the NVCM is yet unprogrammed, then the iCE65P device is not enabled to configure from NVCM. Conversely, if the NVCM is programmed, the iCE65P device will configure from NVCM.
    - If enabled to configure from NVCM, the iCE65P device configures itself using the Nonvolatile Configuration Memory (NVCM).
    - If not enabled to configure from NVCM, then the iCE65P FPGA configures using the SPI Master Configuration Interface.
- If the SPI_SS_B pin is sampled as a logic '0' (Low), then the iCE65P device waits to be configured from an external controller or from another iCE65P device in SPI Master Configuration Mode using an SPI-like interface.

Figure 23: **Device Configuration Control Flow**



Configuration Image Size

Table 28 shows the number of memory bits required to configure an iCE65P device. Two values are provided for each device. The "Logic Only" value indicates the minimum configuration size, the number of bits required to configure only the logic fabric, leaving the RAM4K blocks uninitialized. The "Logic + RAM4K" column indicates the maximum configuration size, the number of bits to configure the logic fabric and to pre-initialize all the RAM4K blocks.

Table 28: **iCE65P Configuration Image Size (Kbits)**

Device	MINIMUM Logic Only (RAM4K not initialized)	MAXIUM Logic + RAM4K (RAM4K pre-initialized)
iCE65P04	453 Kbits	533 Kbits

Nonvolatile Configuration Memory (NVCM)

All standard iCE65P devices have an internal, nonvolatile configuration memory (NVCM). The NVCM is large enough to program a complete iCE65P device, including initializing all RAM4K block locations (MAXIMUM column in Table 28). The NVCM memory also has very high programming yield due to extensive error checking and correction (ECC) circuitry.

The NVCM is ideal for cost-sensitive, high-volume production applications, saving the cost and board space associated with an external configuration PROM. Furthermore, the NVCM provides exceptional design security, protecting critical intellectual property (IP). The NVCM contents are entirely contained within the iCE65P device and are not readable once protected by the one-time programmable Security bits. Furthermore, there is no observable difference between a programmed or un-programmed memory cell using optical or electron microscopy.

The NVCM memory has a programming interface similar to a 25-series SPI serial Flash PROM. Consequently, it can be programmed using standard device programmers before or after circuit board assembly or programmed in-system from a microprocessor or other intelligent controller.

Configuration Control Signals

The iCE65P configuration process is self-timed and controlled by a few internal signals and device I/O pins, as described in Table 29.

Table 29: **iCE65P Configuration Control Signals**

Signal Name	Direction	Description
POR	Internal control	Internal Power-On Reset (POR) circuit.
OSC	Internal control	Internal configuration oscillator.
CRESET_B	Input	Configuration Reset input. Active-Low. No internal pull-up resistor.
CDONE	Open-drain Output	Configuration Done output. Permanent, weak pull-up resistor to VCCIO_2.

The Power-On Reset circuit, POR, automatically resets the iCE65P component to a known state during power-up (cold boot). The POR circuit monitors the relevant voltage supply inputs, as shown in Figure 25. Once all supplies exceed their minimum thresholds, the configuration controller can start the configuration process.

The configuration controller begins configuring the iCE65P device, clocked by the Internal Oscillator, OSC. The OSC oscillator continues controlling configuration unless the iCE65P device is configured using the SPI Peripheral Configuration Interface.

Figure 24: **iCE65P Configuration Control Pins**

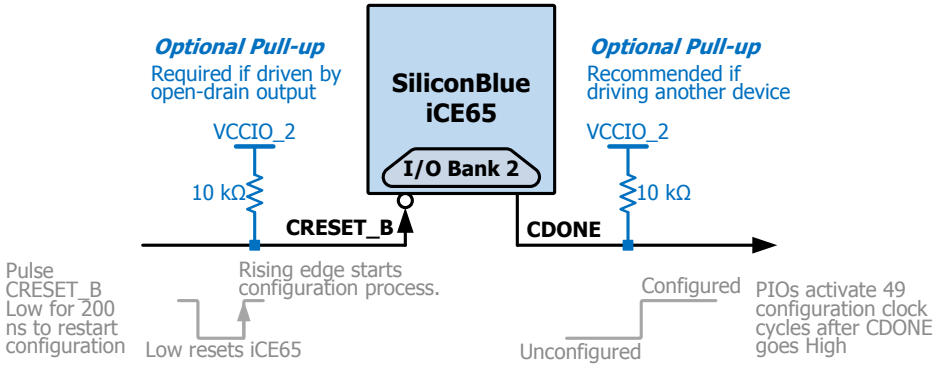


Figure 24 shows the two iCE65P configuration control pins, CRESET_B and CDONE. Table 30 lists the Ball numbers for the configuration control pins by package. When driven Low for at least 200 ns, the dedicated Configuration Reset input, CRESET_B, resets the iCE65P device. When CRESET_B returns High, the iCE65P FPGA restarts the configuration process from its power-on conditions (Cold Boot). The CRESET_B pin is a pure input with no internal pull-up resistor. If driven by open-drain driver or un-driven, then connect the CRESET_B pin to a 10 kΩ pull-up resistor connected to the VCCIO_2 supply.

Table 30: **Configuration Control Ball Numbers by Package**

Configuration Control Pins	Package Code		
	CB121	**CB196**	**CB284**
CRESET_B	K7	L10	R14
CDONE	J7	M10	T14

The iCE65P device signals the end of the configuration process by actively turning off the internal pull-down transistor on the Configuration Done output pin, CDONE. The pin has a permanent, weak internal pull-up resistor to the VCCIO_2 rail. If the iCE65P device drives other devices, then optionally connect the CDONE pin to a 10 kΩ pull-up resistor connected to the VCCIO_2 supply.

The PIO pins activate according to their configured function after 49 configuration clock cycles. The internal oscillator is the configuration clock source for the SPI Master Configuration Interface and when configuring from Nonvolatile Configuration Memory (NVCM). When using the SPI Peripheral Configuration Interface, the configuration clock source is the SPI_SCK clock input pin.

Internal Oscillator

During SPI Master or NVCM configuration mode, the controlling clock signal is generated from an internal oscillator. The oscillator starts operating at the Default frequency. During the configuration process, however, bit settings within the configuration bitstream can specify a higher-frequency mode in order to maximize SPI bandwidth and reduce overall configuration time. See Table 61: Internal Oscillator Frequency on page 81 for the specified oscillator frequency range.

Using the SPI Master Configuration Interface, internal oscillator controls all the interface timing and clocks the SPI serial Flash PROM via the SPI_SCK clock output pin.

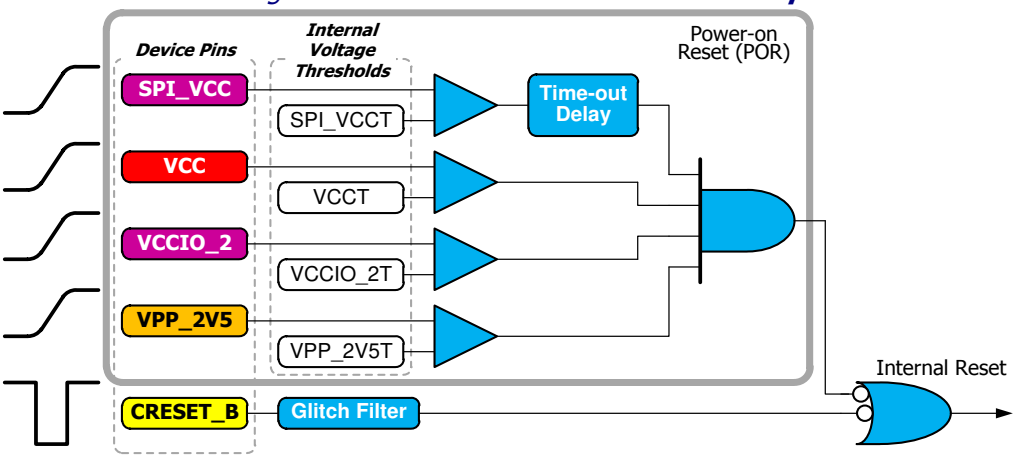
The oscillator output, which also supplies the SPI SCK clock output during the SPI Flash configuration process, has a 50% duty cycle.

Internal Device Reset

Figure 25 presents the various signals that internally reset the iCE65P internal logic.

- Power-On Reset (POR)
- CRESET_B Pin
- JTAG Interface

Figure 25: **iCE65P Internal Reset Circuitry**



Power-On Reset (POR)

The Power-on Reset (POR) circuit monitors specific voltage supply inputs and holds the device in reset until all the relevant supplies exceed the internal voltage thresholds. The SPI_VCC supply also has an additional time-out delay to allow an attached SPI serial PROM to power up properly. Table 31 shows the POR supply inputs. The Nonvolatile Configuration Memory (NVCM) requires that the VPP_2V5 supply be connected, even if the application does not use the NVCM.

Table 31: **Power-on Reset (POR) Voltage Resources**

Supply Rail	iCE65P Production Devices
VCC	Yes
SPI_VCC	Yes
VCCIO_1	No
VCCIO_2	Yes
VPP_2V5	Yes

CRESET_B Pin

The CRESET_B pin resets the iCE65P internal logic when Low.

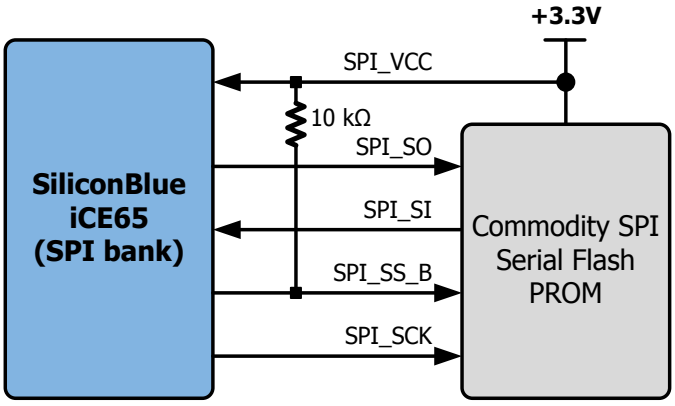
JTAG Interface

Specific command sequences also reset the iCE65P internal logic.

SPI Master Configuration Interface

All iCE65P devices, including those with NVCM, can be configured from an external, commodity SPI serial Flash PROM, as shown in Figure 26. The SPI configuration interface is essentially its own independent I/O bank, powered by the VCC_SPI supply input. Presently, most commercially-available SPI serial Flash PROMs require a 3.3V supply.

Figure 26: **iCE65P SPI Master Configuration Interface**



The SPI configuration interface is used primarily during development before mass production, where the configuration is then permanently programmed in the NVCM configuration memory. However, the SPI interface can also be the primary configuration interface allowing easy in-system upgrades and support for multiple configuration images.

The SPI control signals are defined in Table 32. Table 33 lists the SPI interface ball or pins numbers by package.

Table 32: **SPI Master Configuration Interface Pins (SPI_SS_B High before Configuration)**

Signal Name	Direction	Description
SPI_VCC	Supply	SPI Flash PROM voltage supply input.
SPI_SO	Output	SPI Serial Output from the iCE65P device.
SPI_SI	Input	SPI Serial Input to the iCE65P device, driven by the select SPI serial Flash PROM.
SPI_SS_B	Output	SPI Slave Select output from the iCE65P device. Active Low.
SPI_SCK	Output	SPI Slave Clock output from the iCE65P device.

After configuration, the SPI port pins are available to the user-application as additional PIO pins, supplied by the SPI_VCC input voltage, essentially providing a fifth "mini" I/O bank.

Table 33: **SPI Interface Ball Numbers by Package**

SPI Interface	Package Code		
	CB121	**CB196**	**CB284**
SPI_VCC	J10	L11	R15
PIOS/SPI_SO	J8	M11	T15
PIOS/SPI_SI	K8	P11	V15
PIOS/SPI_SS_B	J9	P13	V17
PIOS/SPI_SCK	K9	P12	V16

SPI PROM Requirements

The iCE65P mobileFPGA SPI Flash configuration interface supports a variety of SPI Flash memory vendors and product families. However, SiliconBlue Technologies does not specifically test, qualify, or otherwise endorse any specific SPI Flash vendor or product family. The iCE65P SPI interface supports SPI PROMs that they meet the following requirements.

- The PROM must operate at 3.3V or 2.5V in order to trigger the iCE65P FPGA's power-on reset circuit.
- The PROM must support the 0x0B Fast Read command, using a 24-bit start address and has 8 dummy bits before the PROM provides first data (see Figure 28: SPI Fast Read Command).
- The PROM must have enough bits to program the iCE65P device (see Table 34: Smallest SPI PROM Size (bits), by Device, by Number of Images).
- The PROM must support data operations at the upper frequency range for the selected iCE65P internal oscillator frequency (see Table 61). The oscillator frequency is selectable when creating the FPGA bitstream image.
- For lowest possible power consumption after configuration, the PROM should also support the 0xB9 Deep Power Down command and the 0xAB Release from Deep Power-down Command (see Figure 27 and Figure 29). The low-power mode is optional.
- The PROM must be ready to accept commands 10 µs after meeting its power-on conditions. In the PROM data sheet, this may be specified as t_{VSL} or t_{VCSL}. It is possible to use slower PROMs by holding the CRESET_B input Low until the PROM is ready, then releasing CRESET_B, either under program control or using an external power-on reset circuit.

The SiliconBlue iCEman65 development board and associated programming software uses an ST Micro/Numonyx M25Pxx SPI serial Flash PROM.

SPI PROM Size Requirements

Table 34 lists the minimum SPI PROM size required to configure an iCE65P device. Larger PROM sizes are allowed, but not required unless the end application uses the additional space. SPI serial PROM sizes are specified in bits. For each device size, the table shows the required minimum PROM size for "Logic Only" (no BRAM initialization) and "Logic + RAM4K" (RAM4K blocks pre-initialized). Furthermore, the table shows the PROM size for varying numbers of configuration images. Most applications will use a single image. Applications that use the Cold Boot or Warm Boot features may use more than one image.

Table 34: **Smallest SPI PROM Size (bits), by Device, by Number of Images**

Device	1 Image		2 Images		3 Images		4 Images	
	Logic Only	**Logic + RAM4K**	**Logic Only**	**Logic + RAM4K**	**Logic Only**	**Logic + RAM4K**	**Logic Only**	**Logic + RAM4K**
iCE65P04	512K	1M	1M	2M	2M	2M	2M	4M

Enabling SPI Configuration Interface

To enable the SPI configuration mode, the SPI_SS_B pin must be allowed to float High. The SPI_SS_B pin has an internal pull-up resistor. If SPI_SS_B is Low, then the iCE65P component defaults to the SPI Slave configuration mode.

SPI Master Configuration Process

The iCE65P SPI Master Configuration Interface supports a variety of modern, high-density, low-cost SPI serial Flash PROMs. Most modern SPI PROMs include a power-saving Deep Power-down mode. The iCE65P component exploits this mode for additional system power savings.

The iCE65P SPI interface starts by driving SPI_SS_B Low, and then sends a Release from Power-down command to the SPI PROM, hexadecimal command code 0xAB. Figure 27 provides an example waveform. This initial command wakes up the SPI PROM if it is already in Deep Power-down mode. If the PROM is not in Deep Power-down mode, the extra command has no adverse affect other than that it requires a few additional microseconds during the configuration process. The iCE65P device transmits data on the SPI_SO output, on the falling edge of the SPI_SCK output. The SPI PROM does not provide any data to the iCE65P device's SPI_SI input. After sending the last command bit, the iCE65P device de-asserts SPI_SS_B High, completing the command. The iCE65P device then waits a minimum of 10 µS before sending the next SPI PROM command.

Figure 27: **SPI Release from Deep Power-down Command**

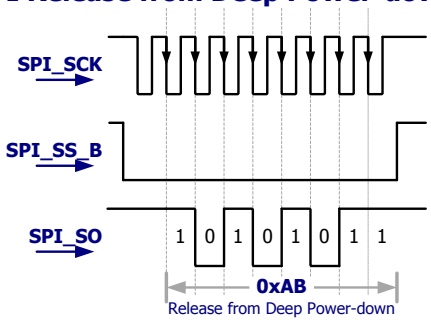
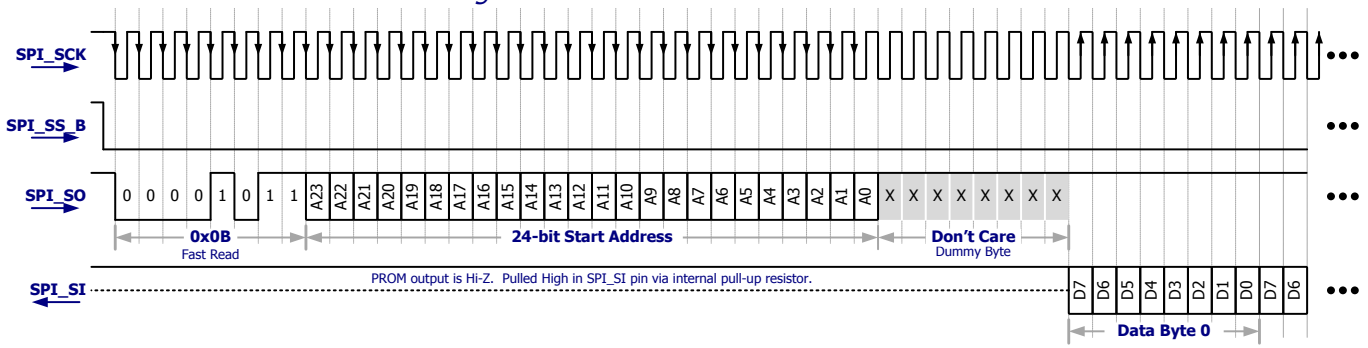


Figure 28 illustrates the next command issued by the iCE65P device. The iCE65P SPI interface again drives SPI_SS_B Low, followed by a Fast Read command, hexadecimal command code 0x0B, followed by a 24-bit start address, transmitted on the SPI_SO output. The iCE65P device provides data on the falling edge of SPI_SS_B. Upon initial power-up, the start address is always 0x00_0000. After waiting eight additional clock cycles, the iCE65P device begins reading serial data from the SPI PROM. Before presenting data, the SPI PROM's serial data output is high-impedance. The SPI_SI input pin has an internal pull-up resistor and sees high-impedance as logic '1'.

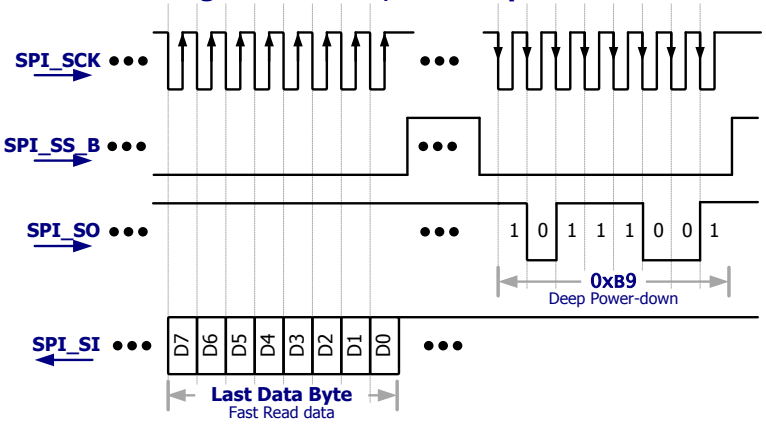
Figure 28: **SPI Fast Read Command**



The external SPI PROM supplies data on the falling edge of the iCE65P device's SPI_SCK clock output. The iCE65P device captures each PROM data value on the SPI_SI input, using the rising edge of the SPI_SCK clock signal. The SPI PROM data starts at the 24-bit address presented by the iCE65P device. PROM data is serially output, byte by byte, with most-significant bit, D7, presented first. The PROM automatically increments an internal byte counter as long as the PROM is selected and clocked.

After transferring the required number configuration data bits, the iCE65P device ends the Fast Read command by de-asserting its SPI_SS_B PROM select output, as shown in Figure 29. To conserve power, the iCE65P device then optionally issues a final Deep Power-down command, hexadecimal command code 0xB9. After de-asserting the SPI_SS_B output, the SPI PROM enters its Deep Power-down mode. The final power-down step is optional; the application may wish to use the SPI PROM and can skip this step, controlled by a configuration option.

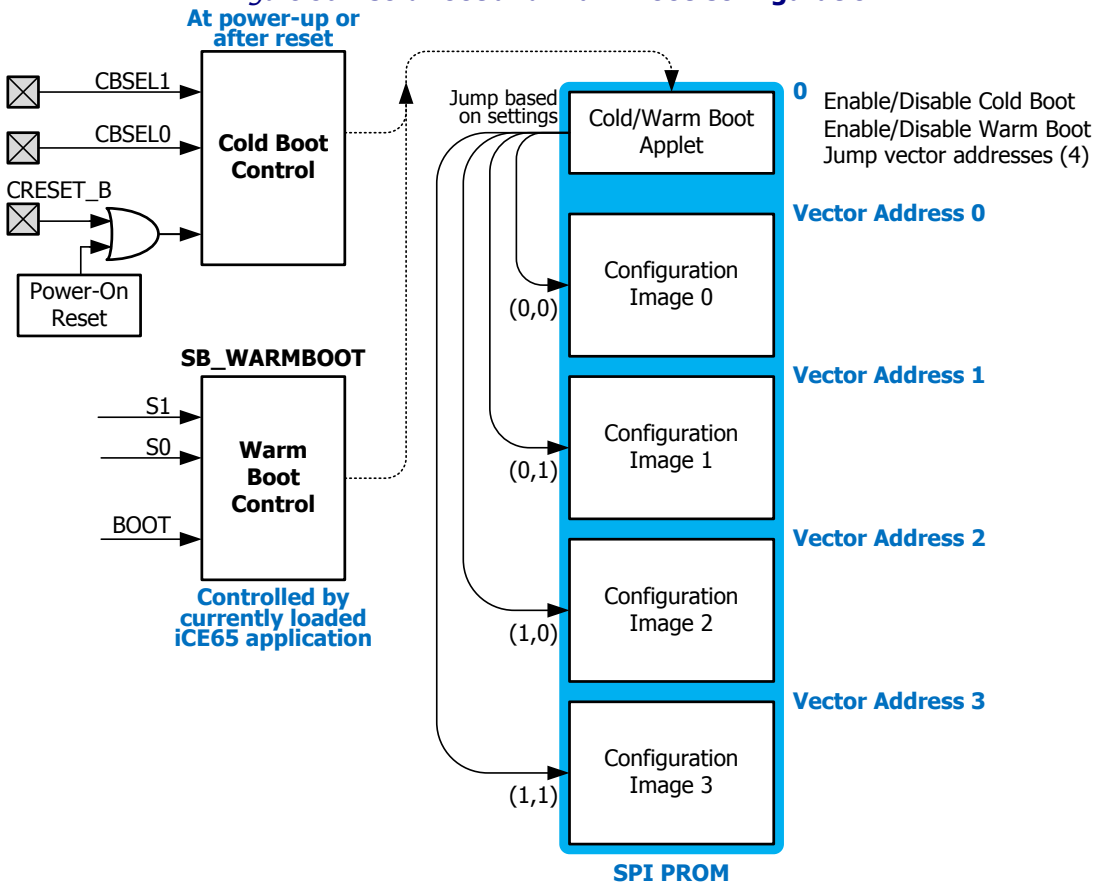
Figure 29: **Final Configuration Data, SPI Deep Power-down Command**



Cold Boot Configuration Option

By default, the iCE65P FPGA is programmed with a single configuration image, either from internal NVCM memory, from an external SPI Flash PROM, or externally from a processor or microcontroller.

Figure 30: **ColdBoot and WarmBoot Configuration**



When self-loading from NVCM or from an SPI Flash PROM, the FPGA supports an additional configuration option called Cold Boot mode. When this option is enabled in the configuration bitstream, the iCE65P FPGA boots normally from power-on or a master reset (CRESET_B = Low pulse), but monitors the value on two PIO pins that are borrowed during configuration, as shown in Figure 30. These pins, labeled PIO2/CBSEL0 and PIO2/CBSEL1, tell the FPGA which of the four possible SPI configurations to load into the device. Table 35 provides the pin or ball locations for these pins.

- Load from initial location, either from NVCM or from address 0 in SPI Flash PROM. For Cold Boot or Warm Boot applications, the initial configuration image contains the cold boot/warm boot applet.
- Check if Cold Boot configuration feature is enabled in the bitstream.
  - If not enabled, FPGA configures normally.
  - If Cold Boot is enabled, then the FPGA reads the logic values on pins CBSEL[1:0]. The FPGA uses the value as a vector and then reads from the indicated vector address.
  - At the selected CBSEL[1:0] vector address, there is a starting address for the selected configuration image.
    - For SPI Flash PROMs, the new address is a 24-bit start address in Flash.
    - If the selected bitstream is in NVCM, then the address points to the internal NVCM.
- Using the new start address, the FPGA restarts reading configuration memory from the new location.

Table 35: **ColdBoot Select Ball Numbers by Package**

ColdBoot Select	Package Code		
	CB121	**CB196**	**CB284**
PIO2/CBSEL0	H6	L9	R13
PIO2/CBSEL1	J6	P10	V14

When creating the initial configuration image, the SiliconBlue development software loads the start address for up to four configuration images in the bitstream. The value on the CBSEL[1:0] pins tell the configuration controller to read a specific start address, then to load the configuration image stored at the selected address. The multiple bitstreams are stored either in the SPI Flash or in the internal NVCM.

After configuration, the CBSEL[1:0] pins become normal PIO pins available to the application.

The Cold Boot feature allows the iCE65P to be reprogrammed for special application requirements such as the following.

- A normal operating mode and a self-test or diagnostics mode.
- Different applications based on switch settings.
- Different applications based on a card-slot ID number.

Warm Boot Configuration Option

The Warm Boot configuration is similar to the Cold Boot feature, but is completely under the control of the FPGA application.

A special design primitive, SB_WARMBOOT, allows an FPGA application to choose between four configuration images using two internal signal ports, S1 and S0, as shown in Figure 30. These internal signal ports connect to programmable interconnect, which in turn can connect to PLB logic and/or PIO pins.

After selecting the desired configuration image, the application then asserts the internal signal BOOT port High to force the FPGA to restart the configuration process from the specified vector address stored in PROM.

Time-Out and Retry

When configuring from external SPI Flash, the iCE65P device looks for a synchronization word. If the device does not find a synchronization word within its timeout period, the device automatically attempts to restart the configuration process from the very beginning. This feature is designed to address any potential power-sequencing issues that may occur between the iCE65P device and the external PROM.

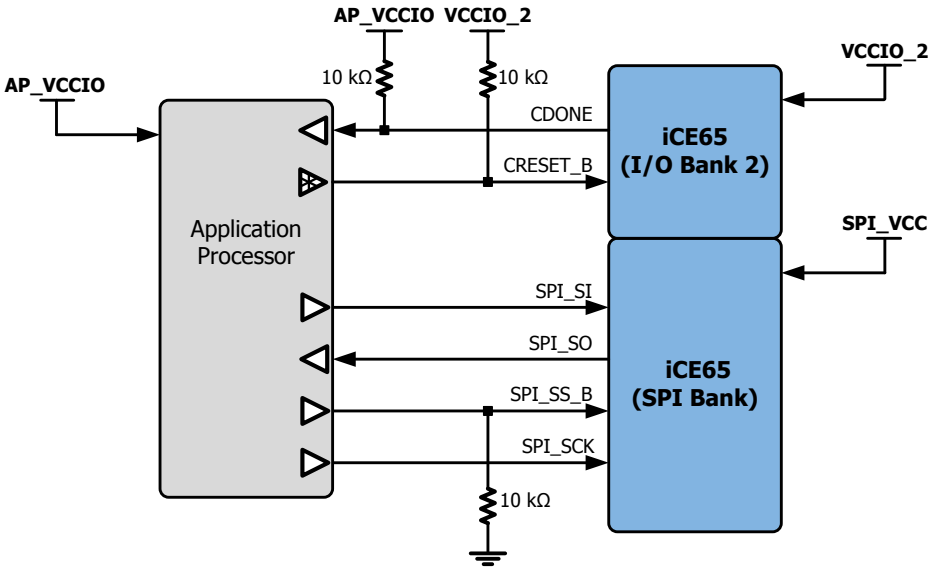
The iCE65P device attempts to reconfigure six times. If not successful after six attempts, the iCE65P FPGA automatically goes into low-power mode.

SPI Peripheral Configuration Interface

Using the SPI peripheral configuration interface, an application processor (AP) serially writes a configuration image to an iCE65P FPGA using the iCE65's SPI interface, as shown in Figure 26. The iCE65's SPI configuration interface is a separate, independent I/O bank, powered by the VCC_SPI supply input. Typically, VCC_SPI is the same voltage as the application processor's I/O. The configuration control signals, CDONE and CRESET_B, are supplied by the separate I/O Bank 2 voltage input, VCCIO_2.

This same SPI peripheral interface supports programming for the iCE65's Nonvolatile Configuration Memory (NVCM).

Figure 31: **iCE65P SPI Peripheral Configuration Interface**



The SPI control signals are defined in Table 32.

Table 36: **SPI Peripheral Configuration Interface Pins (SPI_SS_B Low when CRESET_B Released)**

Signal Name	Direction	iCE65P I/O Supply	Description
CDONE	AP ← iCE65	VCCIO_2	Configuration Done output from iCE65. Connect to a 10kΩ pull-up resistor to the application processor I/O voltage, AP_VCC.
CRESET_B	AP → iCE65		Configuration Reset input on iCE65. Typically driven by AP using an open-drain driver, which also requires a 10kΩ pull-up resistor to VCCIO_2.
SPI_VCC	Supply	SPI_VCC	SPI Flash PROM voltage supply input.
SPI_SI	AP → iCE65		SPI Serial Input to the iCE65P FPGA, driven by the application processor.
SPI_SO	AP ← iCE65		SPI Serial Output from CE65 device to the application processor. Not actually used during SPI peripheral mode configuration but required if the SPI interface is also used to program the NVCM.
SPI_SS_B	AP → iCE65		SPI Slave Select output from the application processor. Active Low. Optionally hold Low prior to configuration using a 10kΩ pull-down resistor to ground.
SPI_SCK	AP → iCE65		SPI Slave Clock output from the application processor.

After configuration, the SPI port pins are available to the user-application as additional PIO pins, supplied by the SPI_VCC input voltage, essentially providing a fifth "mini" I/O bank.

Enabling SPI Configuration Interface

The optional 10 kΩ pull-down resistor on the SPI_SS_B signal ensures that the iCE65P FPGA powers up in the SPI peripheral mode. Optionally, the application processor drives the SPI_SS_B pin Low when CRESET_B is released, forcing the iCE65P FPGA into SPI peripheral mode.

SPI Peripheral Configuration Process

Figure 32 illustrates the interface timing for the SPI peripheral mode and Figure 33 outlines the resulting configuration process. The actual timing specifications appear in Table 64. The application processor (AP) begins by driving the iCE65P CRESET_B pin Low, resetting the iCE65P FPGA. Similarly, the AP holds the iCE65's SPI_SS_B pin Low. The AP must hold the CRESET_B pin Low for at least 200 ns. Ultimately, the AP either releases the CRESET_B pin and allows it to float High via the 10 kΩ pull-up resistor to VCCIO_2 or drives CRESET_B High. The iCE65P FPGA enters SPI peripheral mode when the CRESET_B pin returns High while the SPI_SS_B pin is Low,

After driving CRESET_B High or allowing it to float High, the AP must wait a minimum of 300 µs, allowing the iCE65P FPGA to clear its internal configuration memory.

After waiting for the configuration memory to clear, the AP sends the configuration image generated by the iCEcube development system. An SPI peripheral mode configuration image must not use the ColdBoot or WarmBoot options. Send the entire configuration image, without interruption, serially to the iCE65's SPI_SI input on the falling edge of the SPI_SCK clock input. Once the AP sends the `0x7EAA997E` synchronization pattern, the generated SPI_SCK clock frequency must be within the specified 1 MHz to 25 MHz range (40 ns to 1 µs clock period) while sending the configuration image. Send each byte of the configuration image with most-significant bit (msb) first. The AP sends data to the iCE65P FPGA on the falling edge of the SPI_SCK clock. The iCE65P FPGA internally captures each incoming SPI_SI data bit on the rising edge of the SPI_SCK clock. The iCE65's SPI_SO output pin is not used during SPI peripheral mode but must connect to the AP if the AP also programs the iCE65's Nonvolatile Configuration Memory (NVCM).

The iCE65P configuration image must be sent as one contiguous stream without interruption.

The SPI_SCK clock period must be between 40 ns to 1 µs (1 MHz to 25 MHz).

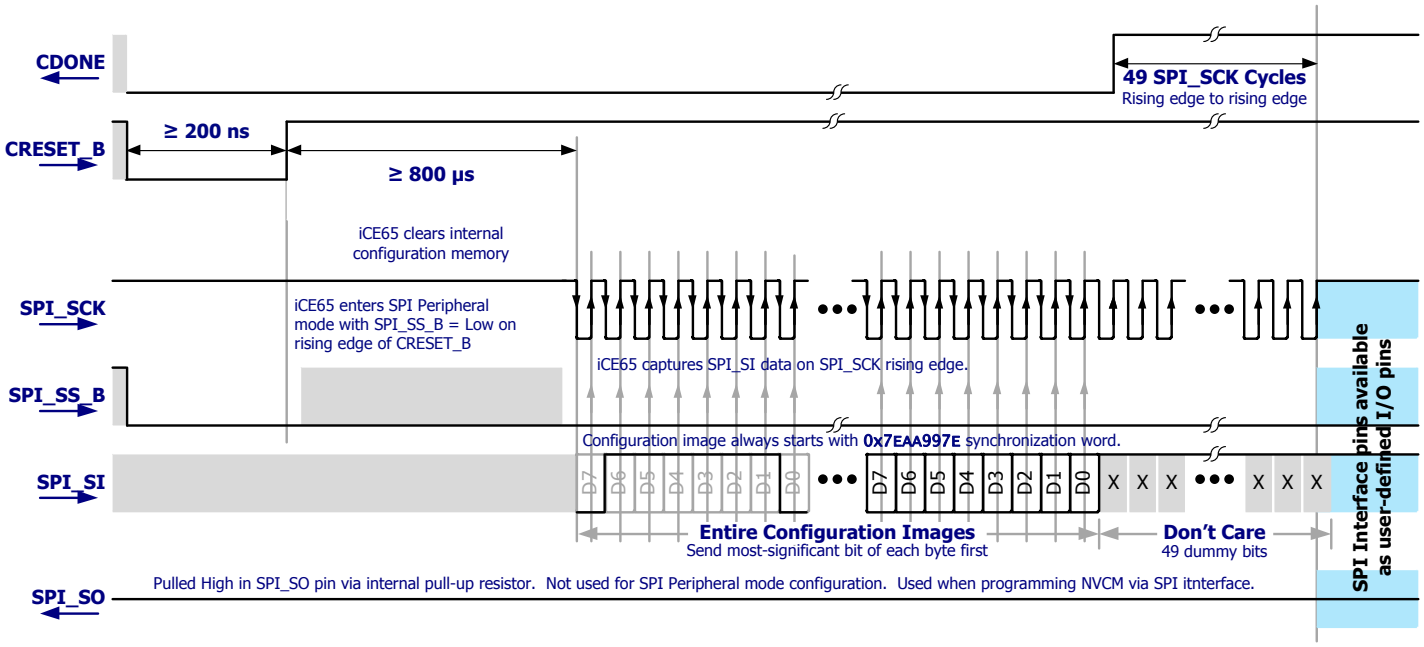
After sending the entire image, the iCE65P FPGA releases the CDONE output allowing it to float High via the 10 kΩ pull-up resistor to AP_VCC. If the CDONE pin remains Low, then an error occurred during configuration and the AP should handle the error accordingly for the application.

After the CDONE output pin goes High, send at least 49 additional dummy bits, effectively 49 additional SPI_SCK clock cycles measured from rising-edge to rising-edge.

After the additional SPI_CLK cycles, the SPI interface pins then become available to the user application loaded in FPGA.

To reconfigure the iCE65P FPGA or to load a different configuration image, merely restart the configuration process by pulsing CRESET_B Low or power-cycling the FPGA.

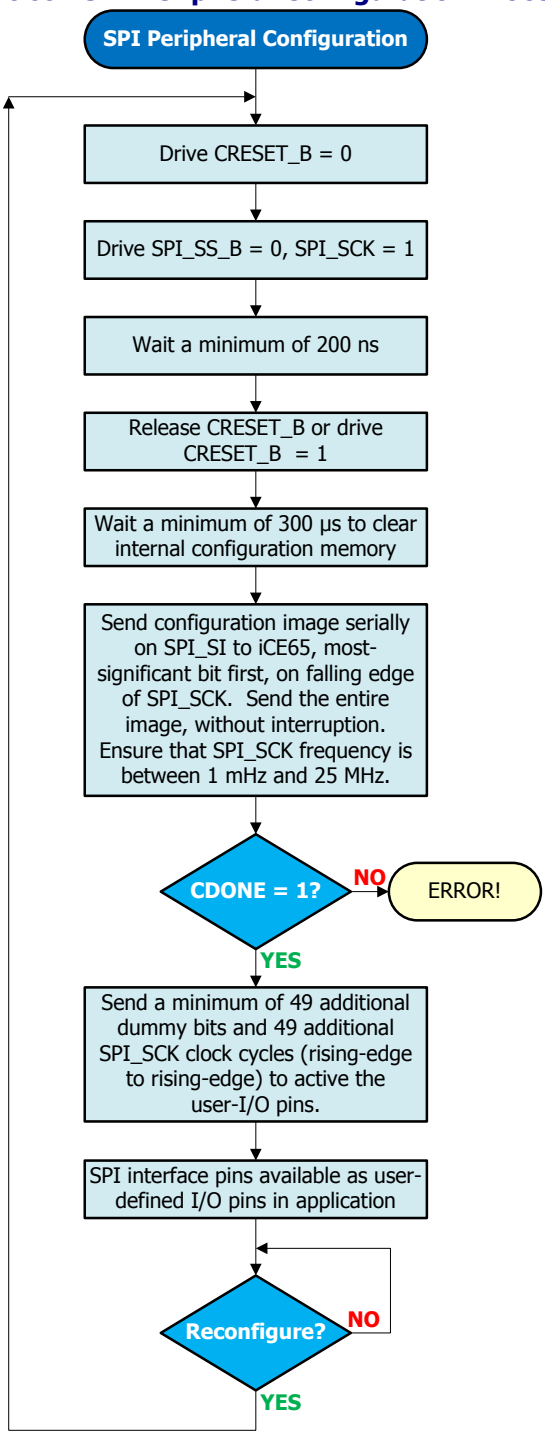
Figure 32: **Application Processor Waveforms for SPI Peripheral Mode Configuration Process**



The iCE65 configuration image must be sent as one contiguous stream without interruption.

The SPI_SCK clock period must be between 40 ns to 1 µs (1 MHz to 25 MHz).

Figure 33: **SPI Peripheral Configuration Process**



Voltage Compatibility

As shown in Figure 26, there are potentially three different supply voltages involved in the SPI Peripheral interface, described in Table 37.

Table 37: **SPI Peripheral Mode Supply Voltages**

Supply Voltage	Description
AP_VCCIO	I/O supply to the Application Processor (AP)
VCC_SPI	Voltage supply for the iCE65P SPI interface.
VCCIO_2	Supply voltage for the iCE65P I/O Bank 2.

Table 38 describes how to maintain voltage compatibility for two interface scenarios. The easiest interface is when the Application Processor's (AP) I/O supply rail and the iCE65's SPI and VCCIO_2 bank supply rails all connect to the same voltage. The second scenario is when the AP's I/O supply voltage is greater than the iCE65's VCCIO_2 supply voltage.

Table 38: **CRESET_B and CDONE Voltage Compatibility**

Condition	CRESET_B			CDONE Pull-up	Requirement
	Direct	**Open-Drain**	**Pull-up**		
VCCIO_AP = VCC_SPI **VCCIO_AP = VCCIO_2**	OK	OK with pull-up	Required if using open-drain output	Recommended	AP can directly drive CRESET_B High and Low although an open-drain output recommended is if multiple devices control CRESET_B. If using an open-drain driver, the CRESET_B input must include a 10 kΩ pull-up resistor to VCCIO_2. The 10 kΩ pull-up resistor to AP_VCCIO is also recommended.
AP_VCCIO > VCCIO_2	N/A	Required, requires pull-up	Required	Required	The AP must control CRESET_B with an open-drain output, which requires a 10 kΩ pull-up resistor to VCCIO_2. The 10 kΩ pull-up resistor to AP_VCCIO is required.

JTAG Boundary Scan Port

Overview

Each iCE65P device includes an IEEE 1149.1-compatible JTAG boundary-scan port. The port supports printed-circuit board (PCB) testing and debugging. It also provides an alternate means to configure the iCE65P device.

Signal Connections

The JTAG port connections are listed in Table 39.

Table 39: **iCE65P JTAG Boundary Scan Signals**

Signal Name	Direction	Description
TDI	Input	Test Data Input.
TMS	Input	Test Mode Select.
TCK	Input	Test Clock.
TDO	Output	Test Data Output.
TRST_B	Input	Test Reset, active Low. Must be Low during normal device operation. Must be High to enable JTAG operations.

Table 40 lists the Ball numbers for the JTAG interface by package code. The JTAG interface is available in select package types. The JTAG port is located in I/O Bank 1 along the right edge of the iCE65P device and powered by the VCCIO_1 supply inputs. Consequently, the JTAG interface uses the associated I/O standards for I/O Bank 1.

Table 40: **JTAG Interface Ball Numbers by Package**

JTAG Interface	Package Code	
	CB196	**CB284**
TDI	M12	T16
TMS	P14	V18
TCK	L12	R16
TDO	N14	U18
TRST_B	M14	T18

Supported JTAG Commands

The JTAG interface supports the IEEE 1149.1 mandatory instructions, including EXTEST, SAMPLE/PRELOAD, and BYPASS.

Package and Pinout Information

Maximum User I/O Pins by Package and by I/O Bank

Table 41 lists the maximum number of user-programmable I/O pins by package, with additional detail showing user I/O pins by I/O bank. In some cases, a smaller iCE65P device is packaged in a larger package with unconnected (N.C.) pins or balls, resulting in fewer overall I/O pins. See Table 2 and Table 42 for device-specific I/O counts by package.

Table 41: **User I/O by Package, by I/O Bank**

	Package Code		
	CB121	**CB196**	**CB284**
Package Leads	121	196	284
Package Area (mm)	6 x 6	8 x 8	12 x 12
Ball Array (balls)	11 x 11	14 x 14	22 x 22
Ball/Lead Pitch (mm)	0.5	0.5	0.5
Maximum user I/O, all I/O banks	**95**	**148**	**220**
PIO Pins in Bank 0	25	37	60
PIO Pins in Bank 1	21	38	55
PIO Pins in Bank 2	23	33	51
PIO Pins in Bank 3	26	36	50
PIO Pins in SPI Interface	4	4	4

Maximum User I/O by Device and Package

Table 42 lists the maximum available user I/O by device and by and package type. Not all devices are available in all packages. Similarly, smaller iCE65P devices may have unconnected balls in some packages. Devices sharing a common package have similar footprints.

Table 42: **Maximum User I/O by Device and Package**

Package	Device
	iCE65P04
CB121	95
CB196	148
CB284	174

iCE65P Pin Descriptions

Table 43 lists the various iCE65P pins, alphabetically by name. The table indicates the directionality of the signal and the associated I/O bank. The table also indicates if the signal has an internal pull-up resistor enabled during configuration. Finally, the table describes the function of the pin.

Table 43: **iCE65P Pin Description**

Signal Name	Direction	I/O Bank	Pull-up during Config	Description
CDONE	Output	2	Yes	Configuration Done. Dedicated output. Includes a permanent weak pull-up resistor to VCCIO_2.. If driving external devices with CDONE output, connect a 10 kΩ pull-up resistor to VCCIO_2.
CRESET_B	Input	2	No	Configuration Reset, active Low. Dedicated input. No internal pull-up resistor. Either actively drive externally or connect a 10 kΩ pull-up resistor to VCCIO_2.
GBIN0/PIO0 GBIN1/PIO0	Input/IO	0	Yes	Global buffer input from I/O Bank 0. Optionally, a full-featured PIO pin.
GBIN2/PIO1 GBIN3/PIO1	Input/IO	1	Yes	Global buffer input from I/O Bank 1. Optionally, a full-featured PIO pin.
GBIN4/PIO2 GBIN5/PIO2	Input/IO	2	Yes	Global buffer input from I/O Bank 2. Optionally, a full-featured PIO pin.
GBIN6/PIO3	Input/IO	3	No	Global buffer input from I/O Bank 3. Optionally, a full-featured PIO pin.
GBIN7/PIO3	Input/IO	3	No	Global buffer input from I/O Bank 3. Optionally, a full-featured PIO pin. Optionally, a differential clock input using the associated differential input pin.
GND	Supply	All	N/A	Ground. All must be connected.
PIOx_yy	I/O	0,1,2	Yes	Programmable I/O pin defined by the iCE65P configuration bitstream. The 'x' number specifies the I/O bank number in which the I/O pin resides. The "yy' number specifies the I/O number in that bank.
PIO2/CBSEL0	Input/IO	2	Yes	Optional ColdBoot configuration SELect input, if ColdBoot mode is enabled. A full-featured PIO pin after configuration.
PIO2/CBSEL1	Input/IO	2	Yes	Optional ColdBoot configuration SELect input, if ColdBoot mode is enabled. A full-featured PIO pin after configuration.
PIO3_yy/ DPwwz	I/O	3	No	Programmable I/O pin that is also half of a differential I/O pair. Only available in I/O Bank 3. The "yy" number specifies the I/O number in that bank. The "ww" number indicates the differential I/O pair. The 'z' indicates the polarity of the pin in the differential pair. 'A'=negative input. 'B'=positive input.
PIOS/SPI_SO	I/O	SPI	Yes	SPI Serial Output. A full-featured PIO pin after configuration.
PIOS /SPI_SI	I/O	SPI	Yes	SPI Serial Input. A full-featured PIO pin after configuration.
PIOS / SPI_SS_B	I/O	SPI	Yes	SPI Slave Select. Active Low. Includes an internal weak pull-up resistor to SPI_VCC during configuration. During configuration, the logic level sampled on this pin determines the configuration mode used by the iCE65P device, as shown in Figure 23. An input when sampled at the start of configuration. An input when in SPI Peripheral configuration mode (SPI_SS_B = Low). An output when in SPI Flash configuration mode. A full-featured PIO pin after configuration.
PIOS/ SPI_SCK	I/O	SPI	Yes	SPI Slave Clock. An input when in SPI Peripheral configuration mode (SPI_SS_B = Low). An output when in SPI Flash configuration mode. A full-featured PIO pin after configuration.
PLLGND	Supply	PLL	N/A	Analog ground for Phase Lock Loop (PLL). If unused, tie to ground.

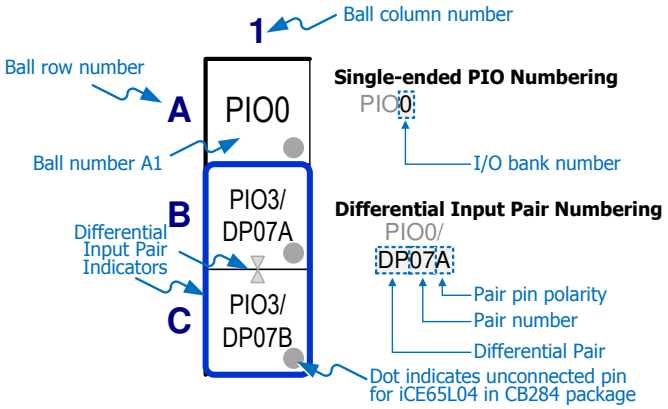
Signal Name	Direction	I/O Bank	Pull-up during Config	Description
PLLVCC	Supply	PLL	N/A	Analog voltage supply for Phase Lock Loop (PLL). If unused, tie to ground.
TDI	Input	1	No	JTAG Test Data Input. If using the JTAG interface, use a 10kΩ pull-up resistor to VCCIO_1.
TMS	Input	1	No	JTAG Test Mode Select. If using the JTAG interface, use a 10kΩ pull-up resistor to VCCIO_1.
TCK	Input	1	No	JTAG Test Clock. If using the JTAG interface, use a 10kΩ pull-up resistor to VCCIO_1.
TDO	Output	1	No	JTAG Test Data Output.
TRST_B	Input	1	No	JTAG Test Reset, active Low. Keep Low during normal operation; High for JTAG operation.
VCC	Supply	All	N/A	Internal core voltage supply. All must be connected.
VCCIO_0	Supply	0	N/A	Voltage supply to I/O Bank 0. All such pins or balls on the package must be connected. Can be disconnected or turned off without affecting the Power-On Reset (POR) circuit.
VCCIO_1	Supply	1	N/A	Voltage supply to I/O Bank 1. All such pins or balls on the package must be connected. Required to guarantee a valid input voltage on TRST_B JTAG pin.
VCCIO_2	Supply	2	N/A	Voltage supply to I/O Bank 2. All such pins or balls on the package must be connected. Required input to the Power-On Reset (POR) circuit.
VCCIO_3	Supply	3	N/A	Voltage supply to I/O Bank 3. All such pins or balls on the package must be connected. Can be disconnected or turned off without affecting the Power-On Reset (POR) circuit.
SPI_VCC	Supply	SPI	N/A	SPI interface voltage supply input. Must have a valid voltage even if configuring from NVCM. Required input to the Power-On Reset (POR) circuit.
VPP_FAST	Supply	All	N/A	Direct programming voltage supply. If unused, leave floating or unconnected during normal operation.
VPP_2V5	Supply	All	N/A	Programming supply voltage. When the iCE65P device is active, VPP_2V5 must be in the valid range between 2.3 V to 3.47 V to release the Power-On Reset circuit, even if the application is not using the NVCM.
VREF	Voltage Reference	3	N/A	Input reference voltage in I/O Bank 3 for the SSTL I/O standard. This pin only appears on the CB284 package and for die-based products.

N/A = Not Applicable

iCE65P Package Footprint Diagram Conventions

Figure 34 illustrates the naming conventions used in the following footprint diagrams. Each PIO pin is associated with an I/O Bank. PIO pins in I/O Bank 3 that support differential inputs are also numbered by differential input pair.

Figure 34: **CS and CB Package Footprint Diagram Conventions**



Pinout Differences between iCE65P04 and iCE65L04

The iCE65P04 FPGA is designed to be nearly pin-compatible with the iCE65L04 FPGA. The primary difference is that the iCE65P04 requires power and ground inputs for the PLL as shown in Table 44 and Table 45. The tables list the package balls that are different between the iCE65P04 and the iCE65L04 pinouts for the CB196 and CB284 packages.

Table 44: **Pinout Differences between iCE65P04 and iCE65L04 in CB196 Package**

Ball Number	iCE65P04	iCE65L04
M6	PLLGND	PIO2
N6	PLLVCC	PIO2

Table 45: **Pinout Differences between iCE65P04 and iCE65L04 in CB284 Package**

Ball Number	iCE65P04	iCE65L04
Y9	PLLGND	PIO2
Y10	PLLVCC	PIO2

CB121 Chip-Scale Ball-Grid Array

The CB121 package is a chip-scale, fully-populated, ball-grid array with 0.5 mm ball pitch.

Footprint Diagram

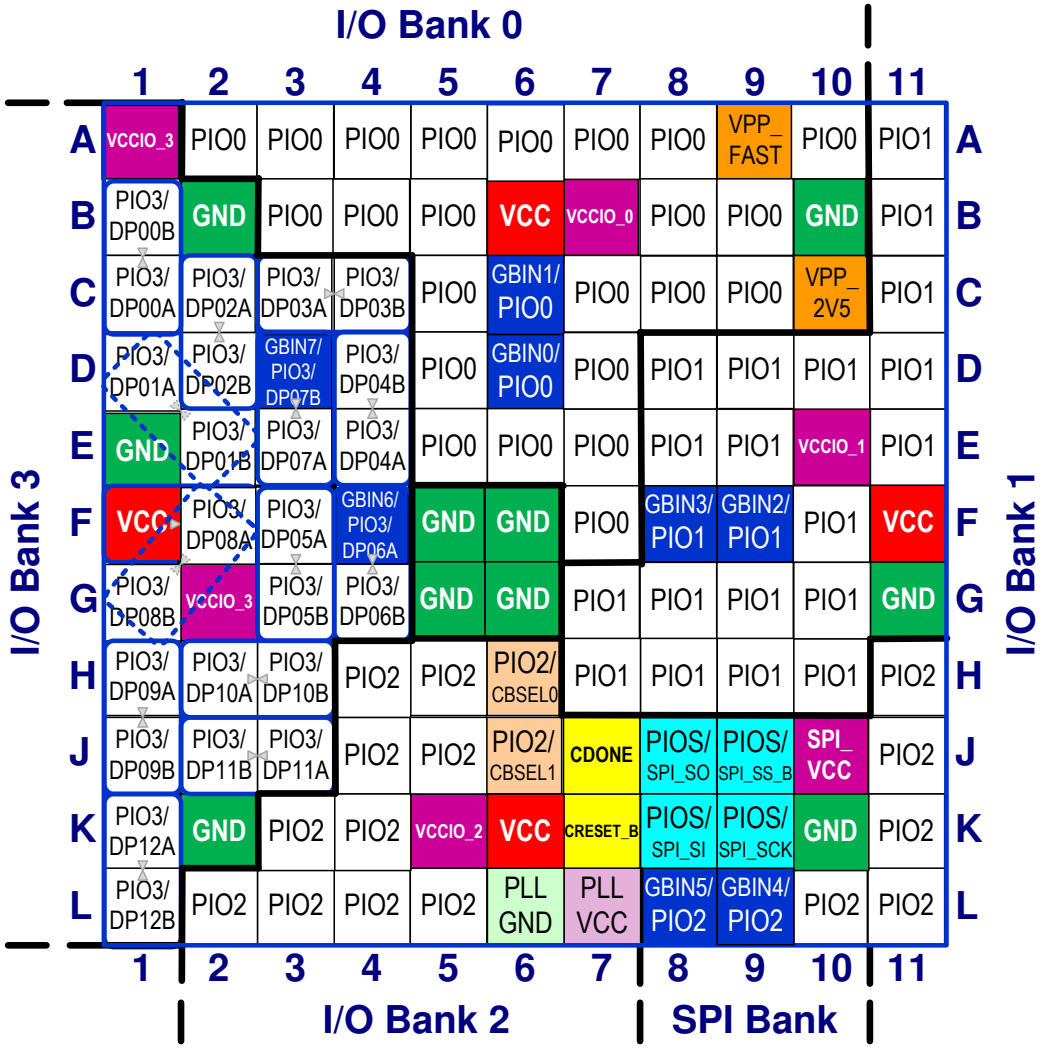
Figure 35 shows the iCE65P04 chip-scale BGA footprint for the 6 x 6 mm CB121 package.

Figure 34 shows the conventions used in the diagram.

Also see Table 46 for a complete, detailed pinout for the 121-ball chip-scale BGA packages.

The signal pins are also grouped into the four I/O Banks and the SPI interface.

Figure 35: **iCE65P04 CB121 Chip-Scale BGA Footprint (Top View)**



Pinout Table

Table 46 provides a detailed pinout table for the iCE65P04 in the CB121 chip-scale BGA package. Pins are generally arranged by I/O bank, then by ball function.

Table 46: **iCE65P04 CB121 Chip-scale BGA Pinout Table**

Ball Function	Ball Number	Pin Type	Bank
GBIN0/PIO0	D6	GBIN	0
GBIN1/PIO0	C6	GBIN	0
PIO0	A2	PIO	0
PIO0	A3	PIO	0

Ball Function	Ball Number	Pin Type	Bank
PIO0	A4	PIO	0
PIO0	A5	PIO	0
PIO0	A6	PIO	0
PIO0	A7	PIO	0
PIO0	A8	PIO	0
PIO0	A10	PIO	0
PIO0	B3	PIO	0
PIO0	B4	PIO	0
PIO0	B5	PIO	0
PIO0	B8	PIO	0
PIO0	B9	PIO	0
PIO0	C5	PIO	0
PIO0	C7	PIO	0
PIO0	C8	PIO	0
PIO0	C9	PIO	0
PIO0	D5	PIO	0
PIO0	D7	PIO	0
PIO0	E5	PIO	0
PIO0	E6	PIO	0
PIO0	E7	PIO	0
PIO0	F7	PIO	0
VCCIO_0	B7	VCCIO	0
GBIN2/PIO1	F9	GBIN	1
GBIN3/PIO1	F8	GBIN	1
PIO1	A11	PIO	1
PIO1	B11	PIO	1
PIO1	C11	PIO	1
PIO1	D8	PIO	1
PIO1	D9	PIO	1
PIO1	D10	PIO	1
PIO1	D11	PIO	1
PIO1	E8	PIO	1
PIO1	E9	PIO	1
PIO1	E11	PIO	1
PIO1	F10	PIO	1
PIO1	G7	PIO	1
PIO1	G8	PIO	1
PIO1	G9	PIO	1
PIO1	G10	PIO	1
PIO1	H7	PIO	1
PIO1	H8	PIO	1
PIO1	H9	PIO	1
PIO1	H10	PIO	1
VCCIO_1	E10	VCCIO	1
CDONE	J7	CONFIG	2
CRESET_B	K7	CONFIG	2
GBIN4/PIO2	L9	GBIN	2
GBIN5/PIO2	L8	GBIN	2
PIO2	H4	PIO	2
PIO2	H5	PIO	2
PIO2	H11	PIO	2

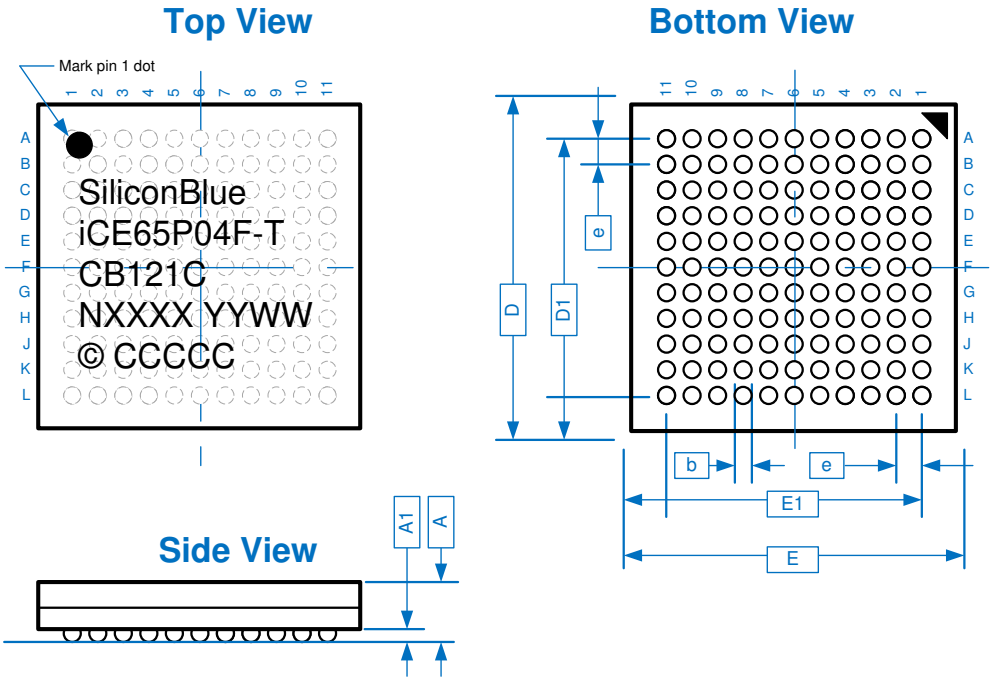
Ball Function	Ball Number	Pin Type	Bank
PIO2	J4	PIO	2
PIO2	J5	PIO	2
PIO2	J11	PIO	2
PIO2	K3	PIO	2
PIO2	K4	PIO	2
PIO2	K11	PIO	2
PIO2	L2	PIO	2
PIO2	L3	PIO	2
PIO2	L4	PIO	2
PIO2	L5	PIO	2
PIO2	L10	PIO	2
PIO2	L11	PIO	2
PIO2/CBSEL0	H6	PIO	2
PIO2/CBSEL1	J6	PIO	2
VCCIO_2	K5	VCCIO	2
PIO3/DP00A	C1	DPIO	3
PIO3/DP00B	B1	DPIO	3
PIO3/DP01A	D1	DPIO	3
PIO3/DP01B	E2	DPIO	3
PIO3/DP02A	C2	DPIO	3
PIO3/DP02B	D2	DPIO	3
PIO3/DP03A	C3	DPIO	3
PIO3/DP03B	C4	DPIO	3
PIO3/DP04A	E4	DPIO	3
PIO3/DP04B	D4	DPIO	3
PIO3/DP05A	F3	DPIO	3
PIO3/DP05B	G3	DPIO	3
PIO3/DP06B	G4	DPIO	3
GBIN6/PIO3/DP06A	F4	GBIN	3
GBIN7/PIO3/DP07B	D3	GBIN	3
PIO3/DP07A	E3	DPIO	3
PIO3/DP08A	F2	DPIO	3
PIO3/DP08B	G1	DPIO	3
PIO3/DP09A	H1	DPIO	3
PIO3/DP09B	J1	DPIO	3
PIO3/DP10A	H2	DPIO	3
PIO3/DP10B	H3	DPIO	3
PIO3/DP11A	J3	DPIO	3
PIO3/DP11B	J2	DPIO	3
PIO3/DP12A	K1	DPIO	3
PIO3/DP12B	L1	DPIO	3
VCCIO_3	A1	VCCIO	3
VCCIO_3	G2	VCCIO	3
PIOS/SPI_SO	J8	SPI	SPI
PIOS/SPI_SI	K8	SPI	SPI
PIOS/SPI_SCK	K9	SPI	SPI
PIOS/SPI_SS_B	J9	SPI	SPI
SPI_VCC	J10	SPI	SPI
PLLGND	L6	PLLGND	PLL
PLLVCC	L7	PLLVCC	PLL

Ball Function	Ball Number	Pin Type	Bank
GND	B2	GND	GND
GND	B10	GND	GND
GND	E1	GND	GND
GND	F5	GND	GND
GND	F6	GND	GND
GND	G5	GND	GND
GND	G6	GND	GND
GND	G11	GND	GND
GND	K2	GND	GND
GND	K10	GND	GND
VCC	B6	VCC	VCC
VCC	F1	VCC	VCC
VCC	F11	VCC	VCC
VCC	K6	VCC	VCC
VPP_2V5	C10	VPP	VPP
VPP_FAST	A9	VPP	VPP

Package Mechanical Drawing

Figure 36: **CB121 Package Mechanical Drawing**

CB121: 6 x 6 mm, 121-ball, 0.5 mm ball-pitch, fully-populated, chip-scale ball grid array



Description		Symbol	Min.	Nominal	Max.	Units
Number of Ball Columns	X			11		Columns
Number of Ball Rows	Y			11		Rows
Number of Signal Balls		n		121		Balls
Body Size	X	E	5.90	6.00	6.10	mm
	Y	D	5.90	6.00	6.10	
Ball Pitch		e	—	0.50	—	
Ball Diameter		b	0.2	—	0.3	
Edge Ball Center to Center	X	E1	—	5.00	—	
	Y	D1	—	5.00	—	
Package Height		A	—	—	1.00	
Stand Off		A1	0.12	—	0.20	

Top Marking Format

Line	Content	Description
1	Logo	Logo
2	iCE65P04F	Part number
	-T	Power/Speed
3	CB121C	Package type
	ENG	Engineering
4	NXXXX	Lot Number
5	YYWW	Date Code
6	© CCCCCC	Country

Thermal Resistance

Junction-to-Ambient θ_{JA} (°C/W)	
0 LFM	200 LFM
54	45

CB196 Chip-Scale Ball-Grid Array

The CB196 package is a chip-scale, fully-populated, ball-grid array with 0.5 mm ball pitch.

Footprint Diagram

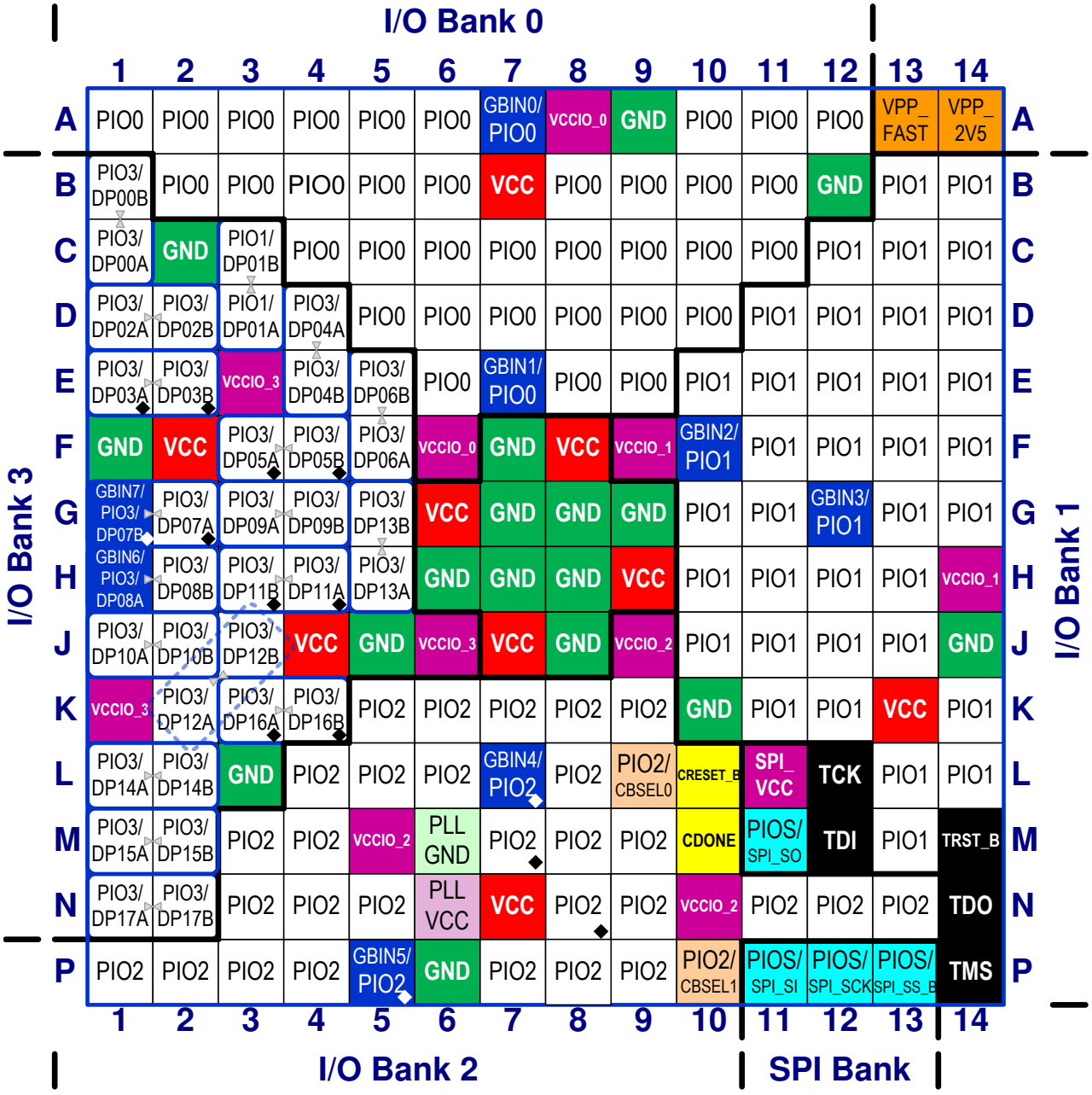
Figure 37 shows the iCE65P04 chip-scale BGA footprint for the 8 x 8 mm CB196 package.

Figure 34 shows the conventions used in the diagram.

Also see Table 47 for a complete, detailed pinout for the 196-ball chip-scale BGA packages.

The signal pins are also grouped into the four I/O Banks and the SPI interface.

Figure 37: **iCE65P04 CB196 Chip-Scale BGA Footprint (Top View)**



Pinout Table

Table 47 provides a detailed pinout table for the iCE65P04 in the CB196 chip-scale BGA package. Pins are generally arranged by I/O bank, then by ball function.

Table 47: **iCE65P04 CB196 Chip-scale BGA Pinout Table**

Ball Function	Ball Number	Pin Type	Bank
GBIN0/PIO0	A7	GBIN	0
GBIN1/PIO0	E7	GBIN	0
PIO0	A1	PIO	0
PIO0	A2	PIO	0
PIO0	A3	PIO	0
PIO0	A4	PIO	0
PIO0	A5	PIO	0
PIO0	A6	PIO	0
PIO0	A10	PIO	0
PIO0	A11	PIO	0
PIO0	A12	PIO	0
PIO0	B2	PIO	0
PIO0	B3	PIO	0
PIO0	B4	PIO	0
PIO0	B5	PIO	0
PIO0	B6	PIO	0
PIO0	B8	PIO	0
PIO0	B9	PIO	0
PIO0	B10	PIO	0
PIO0	B11	PIO	0
PIO0	C4	PIO	0
PIO0	C5	PIO	0
PIO0	C6	PIO	0
PIO0	C7	PIO	0
PIO0	C8	PIO	0
PIO0	C9	PIO	0
PIO0	C10	PIO	0
PIO0	C11	PIO	0
PIO0	D5	PIO	0
PIO0	D6	PIO	0
PIO0	D7	PIO	0
PIO0	D8	PIO	0
PIO0	D9	PIO	0
PIO0	D10	PIO	0
PIO0	E6	PIO	0
PIO0	E8	PIO	0
PIO0	E9	PIO	0
VCCIO_0	A8	VCCIO	0
VCCIO_0	F6	VCCIO	0
GBIN2/PIO1	F10	GBIN	1
GBIN3/PIO1	G12	GBIN	1
PIO1	B13	PIO	1
PIO1	B14	PIO	1
PIO1	C12	PIO	1
PIO1	C13	PIO	1
PIO1	C14	PIO	1
PIO1	D11	PIO	1
PIO1	D12	PIO	1
PIO1	D13	PIO	1
PIO1	D14	PIO	1
PIO1	E10	PIO	1

Ball Function	Ball Number	Pin Type	Bank
PIO1	E11	PIO	1
PIO1	E12	PIO	1
PIO1	E13	PIO	1
PIO1	E14	PIO	1
PIO1	F11	PIO	1
PIO1	F12	PIO	1
PIO1	F13	PIO	1
PIO1	F14	PIO	1
PIO1	G10	PIO	1
PIO1	G11	PIO	1
PIO1	G13	PIO	1
PIO1	G14	PIO	1
PIO1	H10	PIO	1
PIO1	H11	PIO	1
PIO1	H12	PIO	1
PIO1	H13	PIO	1
PIO1	J10	PIO	1
PIO1	J11	PIO	1
PIO1	J12	PIO	1
PIO1	J13	PIO	1
PIO1	K11	PIO	1
PIO1	K12	PIO	1
PIO1	K14	PIO	1
PIO1	L13	PIO	1
PIO1	L14	PIO	1
PIO1	M13	PIO	1
TCK	L12	JTAG	1
TDI	M12	JTAG	1
TDO	N14	JTAG	1
TMS	P14	JTAG	1
TRST_B	M14	JTAG	1
VCCIO_1	F9	VCCIO	1
VCCIO_1	H14	VCCIO	1
CDONE	M10	CONFIG	2
CRESET_B	L10	CONFIG	2
GBIN4/PIO2 (◆)	***iCE65P04:*** L7	GBIN	2
GBIN5/PIO2 (◆)	***iCE65P04:*** P5	GBIN	2
PIO2	K5	PIO	2
PIO2	K6	PIO	2
PIO2	K7	PIO	2
PIO2	K8	PIO	2
PIO2	K9	PIO	2
PIO2	L4	PIO	2
PIO2	L5	PIO	2
PIO2	L6	PIO	2
PIO2	L8	PIO	2
PIO2	M3	PIO	2
PIO2	M4	PIO	2
PIO2 (◆)	***iCE65P04:*** M7	PIO	2
PIO2	M8	PIO	2
PIO2	M9	PIO	2
PIO2	N3	PIO	2

Ball Function	Ball Number	Pin Type	Bank
PIO2	N4	PIO	2
PIO2	N5	PIO	2
PIO2 (◆)	***iCE65P04:*** N8	PIO	2
PIO2	N9	PIO	2
PIO2	N11	PIO	2
PIO2	N12	PIO	2
PIO2	N13	PIO	2
PIO2	P1	PIO	2
PIO2	P2	PIO	2
PIO2	P3	PIO	2
PIO2	P4	PIO	2
PIO2	P7	PIO	2
PIO2	P8	PIO	2
PIO2	P9	PIO	2
PIO2/CBSEL0	L9	PIO	2
PIO2/CBSEL1	P10	PIO	2
VCCIO_2	J9	VCCIO	2
VCCIO_2	M5	VCCIO	2
VCCIO_2	N10	VCCIO	2
PIO3/DP00A	C1	DPIO	3
PIO3/DP00B	B1	DPIO	3
PIO3/DP01A	D3	DPIO	3
PIO3/DP01B	C3	DPIO	3
PIO3/DP02A	D1	DPIO	3
PIO3/DP02B	D2	DPIO	3
PIO3/DP03A (◆)	***iCE65P04:*** E1	DPIO	3
PIO3/DP03B (◆)	***iCE65P04:*** E2	DPIO	3
PIO3/DP04A	D4	DPIO	3
PIO3/DP04B	E4	DPIO	3
PIO3/DP05A (◆)	***iCE65P04:*** F3	DPIO	3
PIO3/DP05B (◆)	***iCE65P04:*** F4	DPIO	3
PIO3/DP06A	F5	DPIO	3
PIO3/DP06B	E5	DPIO	3
PIO3/DP07A (◆)	***iCE65P04:*** G2	DPIO	3
GBIN7/PIO3/DP07B (◆)	***iCE65P04:*** G1	GBIN	3
GBIN6/PIO3/DP08A	H1	GBIN	3
PIO3/DP08B	H2	DPIO	3
PIO3/DP09A	G3	DPIO	3
PIO3/DP09B	G4	DPIO	3
PIO3/DP10A	J1	DPIO	3
PIO3/DP10B	J2	DPIO	3
PIO3/DP11A (◆)	***iCE65P04:*** H4	DPIO	3
PIO3/DP11B (◆)	***iCE65P04:*** H3	DPIO	3
PIO3/DP12A	K2	DPIO	3
PIO3/DP12B	J3	DPIO	3
PIO3/DP13A	H5	DPIO	3
PIO3/DP13B	G5	DPIO	3
PIO3/DP14A	L1	DPIO	3
PIO3/DP14B	L2	DPIO	3
PIO3/DP15A	M1	DPIO	3
PIO3/DP15B	M2	DPIO	3

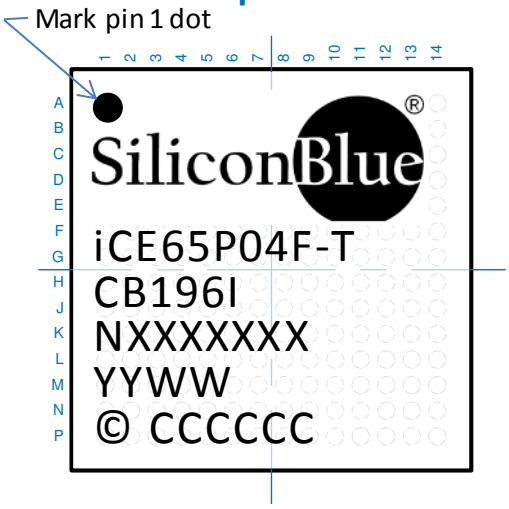
Ball Function	Ball Number	Pin Type	Bank
PIO3/DP16A (◆)	***iCE65P04:*** K3	DPIO	3
PIO3/DP16B (◆)	***iCE65P08:*** K4	DPIO	3
PIO3/DP17A	N1	DPIO	3
PIO3/DP17B	N2	DPIO	3
VCCIO_3	E3	VCCIO	3
VCCIO_3	J6	VCCIO	3
VCCIO_3	K1	VCCIO	3
PIOS/SPI_SO	M11	SPI	SPI
PIOS/SPI_SI	P11	SPI	SPI
PIOS/SPI_SCK	P12	SPI	SPI
PIOS/SPI_SS_B	P13	SPI	SPI
SPI_VCC	L11	SPI	SPI
PLLGND	M6	PLLGND	PLL
PLLVCC	N6	PLLVCC	PLL
GND	A9	GND	GND
GND	B12	GND	GND
GND	C2	GND	GND
GND	F1	GND	GND
GND	F7	GND	GND
GND	G7	GND	GND
GND	G8	GND	GND
GND	G9	GND	GND
GND	H6	GND	GND
GND	H7	GND	GND
GND	H8	GND	GND
GND	J5	GND	GND
GND	J8	GND	GND
GND	J14	GND	GND
GND	K10	GND	GND
GND	L3	GND	GND
GND	P6	GND	GND
VCC	B7	VCC	VCC
VCC	F2	VCC	VCC
VCC	F8	VCC	VCC
VCC	G6	VCC	VCC
VCC	H9	VCC	VCC
VCC	J4	VCC	VCC
VCC	J7	VCC	VCC
VCC	K13	VCC	VCC
VCC	N7	VCC	VCC
VPP_2V5	A14	VPP	VPP
VPP_FAST	A13	VPP	VPP

Package Mechanical Drawing

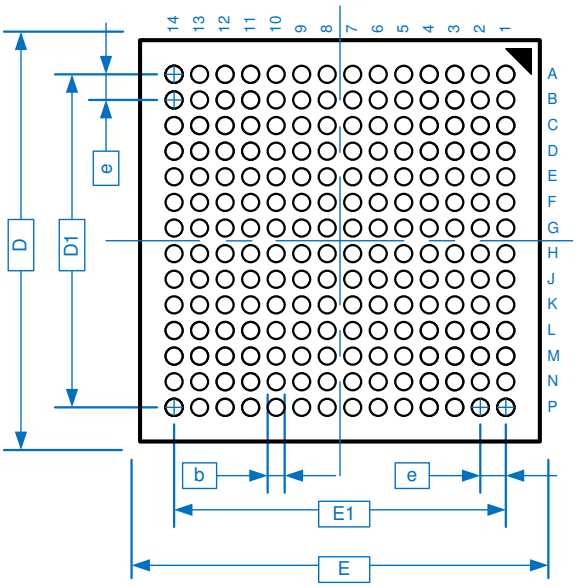
Figure 38: **CB196 Package Mechanical Drawing**

CB196: 8 x8 mm, 196-ball, 0.5 mm ball-pitch, fully-populated, chip-scale ball grid array

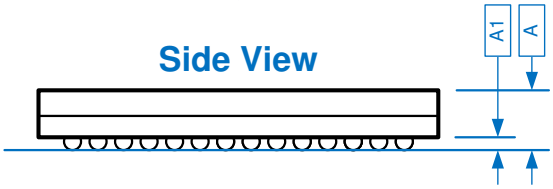
Top View



Bottom View



Side View



Description		Symbol	Min.	Nominal	Max.	Units
Number of Ball Columns	X			14		Columns
Number of Ball Rows	Y			14		Rows
Number of Signal Balls		n		196		Balls
Body Size	X	E	7.90	8.00	8.10	mm
	Y	D	7.90	8.00	8.10	
Ball Pitch		e	—	0.50	—	
Ball Diameter		b	0.27	—	0.37	
Edge Ball Center to Center	X	E1	—	6.50	—	
	Y	D1	—	6.50	—	
Package Height		A	—	—	1.00	
Stand Off		A1	0.16	—	0.26	

Top Marking Format

Line	Content	Description
1	Logo	Logo
2	iCE65P04F	Part number
	-T	Power/Speed
3	CB196I	Package type
	ENG	Engineering
4	NXXXXXXX	Lot Number
5	YYWW	Date Code
6	© CCCCCC	Country

Thermal Resistance

Junction-to-Ambient θ_{JA} (°C/W)	
0 LFM	200 LFM
42	34

CB284 Chip-Scale Ball-Grid Array

The CB284 package, partially-populated 0.5 mm pitch, ball grid array simplifies PCB layout with empty ball rings.

Footprint Diagram

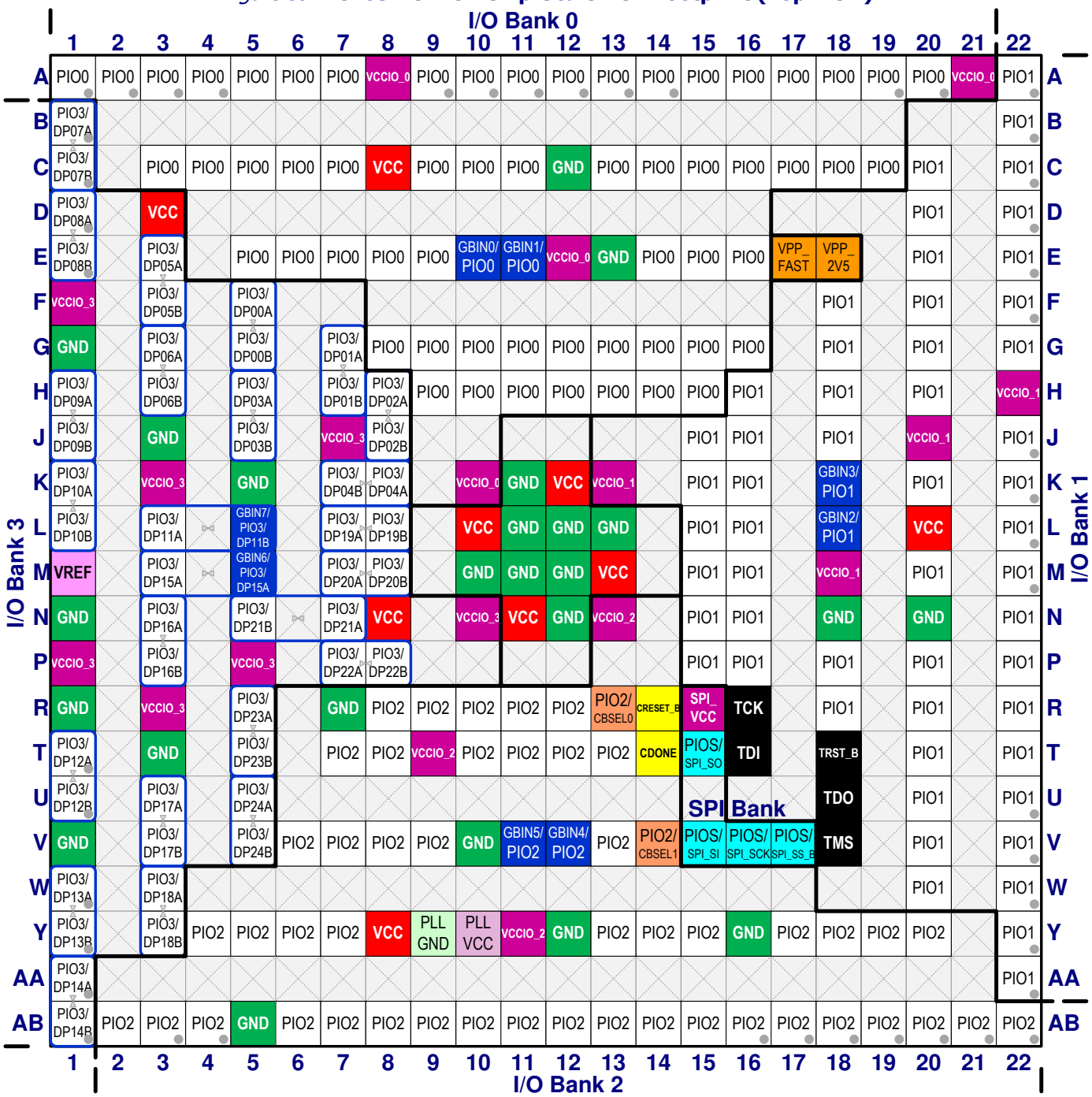
Figure 39 shows the CB284 chip-scale BGA footprint.

Figure 34 shows the conventions used in the diagram.

Also see Table 48 for a complete, detailed pinout for the 284-ball chip-scale BGA packages.

The signal pins are also grouped into the four I/O Banks and the SPI interface.

Figure 39: **iCE65P CB284 Chip-Scale BGA Footprint (Top View)**



Pinout Table

Table 48 provides a detailed pinout table for the two chip-scale BGA packages. Pins are generally arranged by I/O bank, then by ball function. The balls with a black circle (●) are unconnected balls (N.C.) for the iCE65P04 in the CB284 package.

The table also highlights the differential I/O pairs in I/O Bank 3.

Table 48: **iCE65P CB284 Chip-scale BGA Pinout Table (with CB132 cross reference)**

Ball Function	Ball Number	Pin Type by Device		Bank
		iCE65P04	iCE65P08	
GBIN0/PIO0	E10	GBIN	GBIN	0
GBIN1/PIO0	E11	GBIN	GBIN	0
PIO0 (●)	A1	N.C.	PIO	0
PIO0 (●)	A2	N.C.	PIO	0
PIO0 (●)	A3	N.C.	PIO	0
PIO0 (●)	A4	N.C.	PIO	0
PIO0	A5	PIO	PIO	0
PIO0	A6	PIO	PIO	0
PIO0	A7	PIO	PIO	0
PIO0 (●)	A9	N.C.	PIO	0
PIO0 (●)	A10	N.C.	PIO	0
PIO0 (●)	A11	N.C.	PIO	0
PIO0 (●)	A12	N.C.	PIO	0
PIO0 (●)	A13	N.C.	PIO	0
PIO0	A15	PIO	PIO	0
PIO0	A16	PIO	PIO	0
PIO0	A17	PIO	PIO	0
PIO0	A18	PIO	PIO	0
PIO0 (●)	A14	N.C.	PIO	0
PIO0 (●)	A19	N.C.	PIO	0
PIO0 (●)	A20	N.C.	PIO	0
PIO0	C3	PIO	PIO	0
PIO0	C4	PIO	PIO	0
PIO0	C5	PIO	PIO	0
PIO0	C6	PIO	PIO	0
PIO0	C7	PIO	PIO	0
PIO0	C9	PIO	PIO	0
PIO0	C10	PIO	PIO	0
PIO0	C11	PIO	PIO	0
PIO0	C13	PIO	PIO	0
PIO0	C14	PIO	PIO	0
PIO0	C15	PIO	PIO	0
PIO0	C16	PIO	PIO	0
PIO0	C17	PIO	PIO	0
PIO0	C18	PIO	PIO	0
PIO0	C19	PIO	PIO	0
PIO0	E5	PIO	PIO	0
PIO0	E6	PIO	PIO	0
PIO0	E7	PIO	PIO	0
PIO0	E8	PIO	PIO	0
PIO0	E9	PIO	PIO	0
PIO0	E14	PIO	PIO	0
PIO0	E15	PIO	PIO	0
PIO0	E16	PIO	PIO	0

Ball Function	Ball Number	Pin Type by Device		Bank
		iCE65P04	iCE65P08	
PIO0	G8	PIO	PIO	0
PIO0	G9	PIO	PIO	0
PIO0	G10	PIO	PIO	0
PIO0	G11	PIO	PIO	0
PIO0	G12	PIO	PIO	0
PIO0	G13	PIO	PIO	0
PIO0	G14	PIO	PIO	0
PIO0	G15	PIO	PIO	0
PIO0	G16	PIO	PIO	0
PIO0	H9	PIO	PIO	0
PIO0	H10	PIO	PIO	0
PIO0	H11	PIO	PIO	0
PIO0	H12	PIO	PIO	0
PIO0	H13	PIO	PIO	0
PIO0	H14	PIO	PIO	0
PIO0	H15	PIO	PIO	0
VCCIO_0	A8	VCCIO	VCCIO	0
VCCIO_0	A21	VCCIO	VCCIO	0
VCCIO_0	E12	VCCIO	VCCIO	0
VCCIO_0	K10	VCCIO	VCCIO	0
GBIN2/PIO1	L18	GBIN	GBIN	1
GBIN3/PIO1	K18	GBIN	GBIN	1
PIO1 (●)	A22	N.C.	PIO	1
PIO1 (●)	AA22	N.C.	PIO	1
PIO1 (●)	B22	N.C.	PIO	1
PIO1	C20	PIO	PIO	1
PIO1 (●)	C22	N.C.	PIO	1
PIO1	D20	PIO	PIO	1
PIO1 (●)	D22	N.C.	PIO	1
PIO1	E20	PIO	PIO	1
PIO1 (●)	E22	N.C.	PIO	1
PIO1	F18	PIO	PIO	1
PIO1	F20	PIO	PIO	1
PIO1 (●)	F22	N.C.	PIO	1
PIO1	G18	PIO	PIO	1
PIO1	G20	PIO	PIO	1
PIO1	G22	PIO	PIO	1
PIO1	H16	PIO	PIO	1
PIO1	H18	PIO	PIO	1
PIO1	H20	PIO	PIO	1
PIO1	J15	PIO	PIO	1
PIO1	J16	PIO	PIO	1
PIO1	J18	PIO	PIO	1
PIO1 (●)	J22	N.C.	PIO	1
PIO1	K15	PIO	PIO	1
PIO1	K16	PIO	PIO	1
PIO1	K20	PIO	PIO	1
PIO1 (●)	K22	N.C.	PIO	1
PIO1	L15	PIO	PIO	1
PIO1	L16	PIO	PIO	1

Ball Function	Ball Number	Pin Type by Device		Bank
		iCE65P04	iCE65P08	
PIO1 (●)	L22	N.C.	PIO	1
PIO1	M15	PIO	PIO	1
PIO1	M16	PIO	PIO	1
PIO1	M20	PIO	PIO	1
PIO1 (●)	M22	N.C.	PIO	1
PIO1	N15	PIO	PIO	1
PIO1	N16	PIO	PIO	1
PIO1	N22	PIO	PIO	1
PIO1	P15	PIO	PIO	1
PIO1	P16	PIO	PIO	1
PIO1	P18	PIO	PIO	1
PIO1	P20	PIO	PIO	1
PIO1	P22	PIO	PIO	1
PIO1	R18	PIO	PIO	1
PIO1	R20	PIO	PIO	1
PIO1	R22	PIO	PIO	1
PIO1	T20	PIO	PIO	1
PIO1	T22	PIO	PIO	1
PIO1	U20	PIO	PIO	1
PIO1 (●)	U22	N.C.	PIO	1
PIO1	V20	PIO	PIO	1
PIO1 (●)	V22	N.C.	PIO	1
PIO1	W20	PIO	PIO	1
PIO1 (●)	W22	N.C.	PIO	1
PIO1 (●)	Y22	N.C.	PIO	1
TCK	R16	JTAG	JTAG	1
TDI	T16	JTAG	JTAG	1
TDO	U18	JTAG	JTAG	1
TMS	V18	JTAG	JTAG	1
TRST_B	T18	JTAG	JTAG	1
VCCIO_1	H22	VCCIO	VCCIO	1
VCCIO_1	J20	VCCIO	VCCIO	1
VCCIO_1	K13	VCCIO	VCCIO	1
VCCIO_1	M18	VCCIO	VCCIO	1
CDONE	T14	CONFIG	CONFIG	2
CRESET_B	R14	CONFIG	CONFIG	2
GBIN4/PIO2	V12	GBIN	GBIN	2
GBIN5/PIO2	V11	GBIN	GBIN	2
PIO2	R8	PIO	PIO	2
PIO2	R9	PIO	PIO	2
PIO2	R10	PIO	PIO	2
PIO2	R11	PIO	PIO	2
PIO2	R12	PIO	PIO	2
PIO2	T7	PIO	PIO	2
PIO2	T8	PIO	PIO	2
PIO2	T10	PIO	PIO	2
PIO2	T11	PIO	PIO	2
PIO2	T12	PIO	PIO	2
PIO2	T13	PIO	PIO	2
PIO2	V6	PIO	PIO	2
PIO2	V7	PIO	PIO	2

Ball Function	Ball Number	Pin Type by Device		Bank
		iCE65P04	iCE65P08	
PIO2	V8	PIO	PIO	2
PIO2	V9	PIO	PIO	2
PIO2	V13	PIO	PIO	2
PIO2	Y4	PIO	PIO	2
PIO2	Y5	PIO	PIO	2
PIO2	Y6	PIO	PIO	2
PIO2	Y7	PIO	PIO	2
PIO2	Y13	PIO	PIO	2
PIO2	Y14	PIO	PIO	2
PIO2	Y15	PIO	PIO	2
PIO2	Y17	PIO	PIO	2
PIO2	Y18	PIO	PIO	2
PIO2	Y19	PIO	PIO	2
PIO2	Y20	PIO	PIO	2
PIO2	AB2	PIO	PIO	2
PIO2 (●)	AB3	N.C.	PIO	2
PIO2 (●)	AB4	N.C.	PIO	2
PIO2	AB6	PIO	PIO	2
PIO2	AB7	PIO	PIO	2
PIO2	AB8	PIO	PIO	2
PIO2	AB9	PIO	PIO	2
PIO2	AB10	PIO	PIO	2
PIO2	AB11	PIO	PIO	2
PIO2	AB12	PIO	PIO	2
PIO2	AB13	PIO	PIO	2
PIO2	AB14	PIO	PIO	2
PIO2	AB15	PIO	PIO	2
PIO2 (●)	AB16	N.C.	PIO	2
PIO2 (●)	AB17	N.C.	PIO	2
PIO2 (●)	AB18	N.C.	PIO	2
PIO2 (●)	AB19	N.C.	PIO	2
PIO2 (●)	AB20	N.C.	PIO	2
PIO2 (●)	AB21	N.C.	PIO	2
PIO2 (●)	AB22	N.C.	PIO	2
PIO2/CBSEL0	R13	PIO	PIO	2
PIO2/CBSEL1	V14	PIO	PIO	2
VCCIO_2	N13	VCCIO	VCCIO	2
VCCIO_2	T9	VCCIO	VCCIO	2
VCCIO_2	Y11	VCCIO	VCCIO	2
PIO3/DP00A	F5	DPIO	DPIO	3
PIO3/DP00B	G5	DPIO	DPIO	3
PIO3/DP01A	G7	DPIO	DPIO	3
PIO3/DP01B	H7	DPIO	DPIO	3
PIO3/DP02A	H8	DPIO	DPIO	3
PIO3/DP02B	J8	DPIO	DPIO	3
PIO3/DP03A	H5	DPIO	DPIO	3
PIO3/DP03B	J5	DPIO	DPIO	3
PIO3/DP04A	K8	DPIO	DPIO	3
PIO3/DP04B	K7	DPIO	DPIO	3
PIO3/DP05A	E3	DPIO	DPIO	3

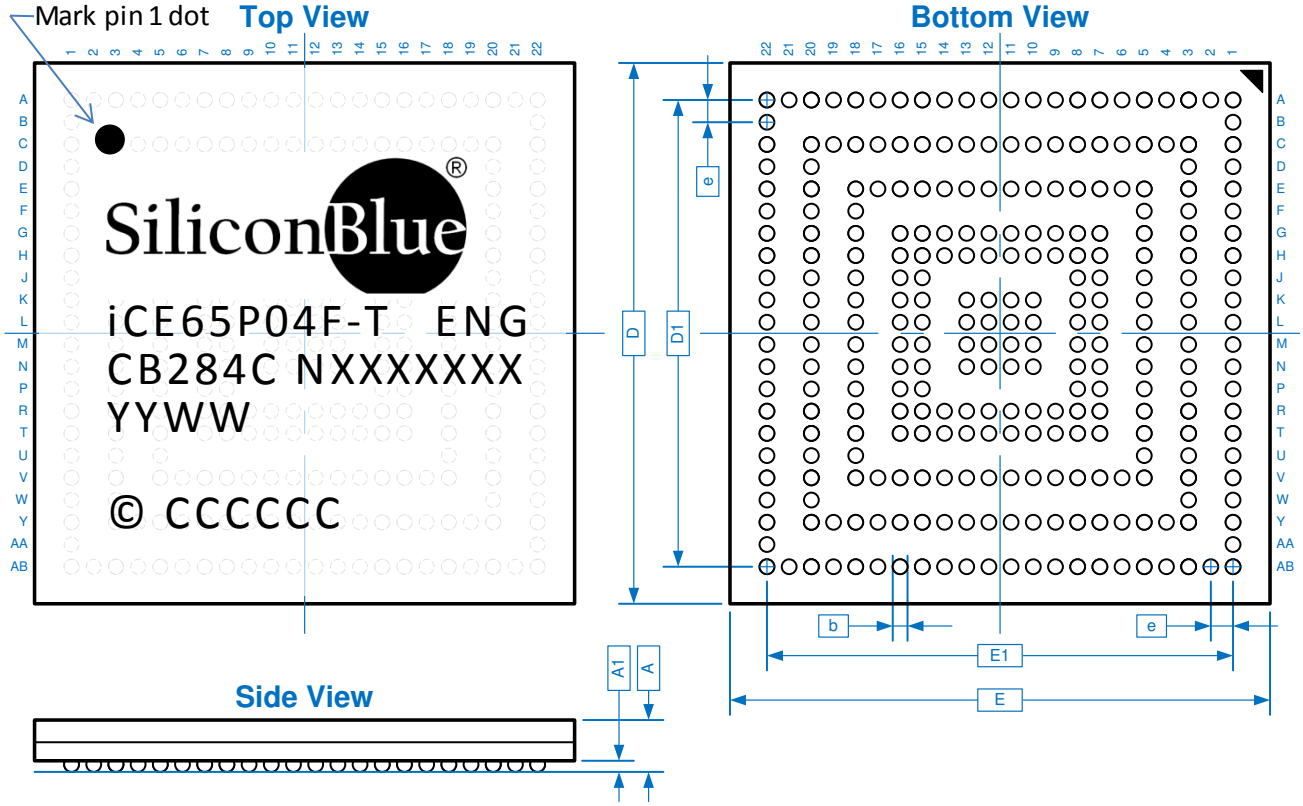
Ball Function	Ball Number	Pin Type by Device		Bank
		iCE65P04	iCE65P08	
PIO3/DP05B	F3	DPIO	DPIO	3
PIO3/DP06A	G3	DPIO	DPIO	3
PIO3/DP06B	H3	DPIO	DPIO	3
PIO3/DP07A (●)	B1	N.C.	DPIO	3
PIO3/DP07B (●)	C1	N.C.	DPIO	3
PIO3/DP08A (●)	D1	N.C.	DPIO	3
PIO3/DP08B (●)	E1	N.C.	DPIO	3
PIO3/DP09A	H1	DPIO	DPIO	3
PIO3/DP09B	J1	DPIO	DPIO	3
PIO3/DP10A	K1	DPIO	DPIO	3
PIO3/DP10B	L1	DPIO	DPIO	3
PIO3/DP11A	L3	DPIO	DPIO	3
GBIN7/PIO3/DP11B	L5	GBIN	GBIN	3
PIO3/DP12A (●)	T1	N.C.	DPIO	3
PIO3/DP12B (●)	U1	N.C.	DPIO	3
PIO3/DP13A (●)	W1	N.C.	DPIO	3
PIO3/DP13B (●)	Y1	N.C.	DPIO	3
PIO3/DP14A (●)	AA1	N.C.	DPIO	3
PIO3/DP14B (●)	AB1	N.C.	DPIO	3
GBIN6/PIO3/DP15A	M5	GBIN	GBIN	3
PIO3/DP15B	M3	DPIO	DPIO	3
PIO3/DP16A	N3	DPIO	DPIO	3
PIO3/DP16B	P3	DPIO	DPIO	3
PIO3/DP17A	U3	DPIO	DPIO	3
PIO3/DP17B	V3	DPIO	DPIO	3
PIO3/DP18A	W3	DPIO	DPIO	3
PIO3/DP18B	Y3	DPIO	DPIO	3
PIO3/DP19A	L7	DPIO	DPIO	3
PIO3/DP19B	L8	DPIO	DPIO	3
PIO3/DP20A	M7	DPIO	DPIO	3
PIO3/DP20B	M8	DPIO	DPIO	3
PIO3/DP21A	N7	DPIO	DPIO	3
PIO3/DP21B	N5	DPIO	DPIO	3
PIO3/DP22A	P7	DPIO	DPIO	3
PIO3/DP22B	P8	DPIO	DPIO	3
PIO3/DP23A	R5	DPIO	DPIO	3
PIO3/DP23B	T5	DPIO	DPIO	3
PIO3/DP24A	U5	DPIO	DPIO	3
PIO3/DP24B	V5	DPIO	DPIO	3
VCCIO_3	F1	VCCIO	VCCIO	3
VCCIO_3	P1	VCCIO	VCCIO	3
VCCIO_3	J7	VCCIO	VCCIO	3
VCCIO_3	K3	VCCIO	VCCIO	3
VCCIO_3	N10	VCCIO	VCCIO	3
VCCIO_3	P5	VCCIO	VCCIO	3
VCCIO_3	R3	VCCIO	VCCIO	3
VREF	M1	VREF	VREF	3

Ball Function	Ball Number	Pin Type by Device		Bank
		iCE65P04	iCE65P08	
PIOS/SPI_SO	T15	SPI	SPI	SPI
PIOS/SPI_SI	V15	SPI	SPI	SPI
PIOS/SPI_SCK	V16	SPI	SPI	SPI
PIOS/SPI_SS_B	V17	SPI	SPI	SPI
SPI_VCC	R15	SPI	SPI	SPI
PLLGND	Y9	PLLGND	PLLGND	PLL
PLLVCC	Y10	PLLVCC	PLLVCC	PLL
GND	C12	GND	GND	GND
GND	E13	GND	GND	GND
GND	J3	GND	GND	GND
GND	K5	GND	GND	GND
GND	K11	GND	GND	GND
GND	L11	GND	GND	GND
GND	L12	GND	GND	GND
GND	L13	GND	GND	GND
GND	M10	GND	GND	GND
GND	M11	GND	GND	GND
GND	M12	GND	GND	GND
GND	N1	GND	GND	GND
GND	N12	GND	GND	GND
GND	N18	GND	GND	GND
GND	N20	GND	GND	GND
GND	R7	GND	GND	GND
GND	T3	GND	GND	GND
GND	V1	GND	GND	GND
GND	V10	GND	GND	GND
GND	Y12	GND	GND	GND
GND	Y16	GND	GND	GND
GND	AB5	GND	GND	GND
GND	G1	GND	GND	GND
GND	R1	GND	GND	GND
VCC	C8	VCC	VCC	VCC
VCC	D3	VCC	VCC	VCC
VCC	K12	VCC	VCC	VCC
VCC	L10	VCC	VCC	VCC
VCC	L20	VCC	VCC	VCC
VCC	M13	VCC	VCC	VCC
VCC	N8	VCC	VCC	VCC
VCC	N11	VCC	VCC	VCC
VCC	Y8	VCC	VCC	VCC
VPP_2V5	E18	VPP	VPP	VPP
VPP_FAST	E17	VPP	VPP	VPP

Package Mechanical Drawing

Figure 40: **CB284 Package Mechanical Drawing**

CB284: 12 x 12 mm, 284-ball, 0.5 mm ball-pitch, chip-scale ball grid array



Description		Symbol	Min.	Nominal	Max.	Units
Number of Ball Columns	X			22		Columns
Number of Ball Rows	Y			22		Rows
Number of Signal Balls		n		284		Balls
Body Size	X	E	11.90	12.00	12.10	mm
	Y	D	11.90	12.00	12.10	
Ball Pitch		e	—	0.50	—	
Ball Diameter		b	0.27	—	0.37	
Edge Ball Center to Center	X	E1	—	10.50	—	
	Y	D1	—	10.50	—	
Package Height		A	—	—	1.00	
Stand Off		A1	0.16	—	0.26	

Top Marking Format

Line	Content	Description
1	Logo	Logo
2	iCE65P04F	Part number
	-T	Power/Speed
	ENG	Engineering
3	CB284C NXXXXXXX	Package type and Lot number
4	YYWW	Date Code
5	N/A	Blank
6	© CCCCCC	Country

Thermal Resistance

Junction-to-Ambient θ_{JA} (°C/W)	
0 LFM	200 LFM
35	28

Die Cross Reference

The tables in this section list all the pads on a specific die type and provide a cross reference on how a specific pad connects to a ball or pin in each of the available package offerings. Similarly, the tables provide the pad coordinates for the die-based version of the product (iCE DiCE). These tables also provide a way to prototype with one package option and then later move to a different package or die.

As described in "Input and Output Register Control per PIO Pair" on page 14, PIO pairs share register control inputs. Similarly, as described in "Differential Inputs and Outputs" on page 11, a PIO pair can form a differential input or output. PIO pairs in I/O Bank 3 are optionally differential inputs or differential outputs. PIO pairs in all other I/O Banks are optionally differential outputs. In the tables, differential pairs are surrounded by a heavy blue box.

iCE65P04

Table 49 lists all the pads on the iCE65P04 die and how these pads connect to the balls or pins in the supported package styles. Most VCC, VCCIO, and GND pads are double-bonded inside the package although the table shows only a single connection.

For additional information on the iCE65P04 DiePlus product, please contact your SiliconBlue sales representative..

Table 49: **iCE65P04 Die Cross Reference**

iCE65P04 Pad Name	Available Packages		DiePlus		
	CB196	CB284	Pad	X (µm)	Y (µm)
PIO3_00/DP00A	C1	F5	1	129.40	2,687.75
PIO3_01/DP00B	B1	G5	2	231.40	2,642.74
PIO3_02/DP01A	D3	G7	3	129.40	2,597.75
PIO3_03/DP01B	C3	H7	4	231.40	2,552.74
GND	F1	K5	5	129.40	2,507.75
GND	—	—	6	231.40	2,462.74
VCCIO_3	E3	J7	7	129.40	2,417.75
VCCIO_3	—	—	8	231.40	2,372.74
PIO3_04/DP02A	D1	H8	9	129.40	2,327.75
PIO3_05/DP02B	D2	J8	10	231.40	2,292.74
PIO3_06/DP03A	E1	H5	11	129.40	2,257.75
PIO3_07/DP03B	E2	J5	12	231.40	2,222.74
VCC	H9	D3	13	129.40	2,187.75
PIO3_08/DP04A	D4	K8	14	231.40	2,152.74
PIO3_09/DP04B	E4	K7	15	129.40	2,117.75
PIO3_10/DP05A	F3	E3	16	231.40	2,082.74
PIO3_11/DP05B	F4	F3	17	129.40	2,047.75
GND	A9	M10	18	231.40	2,012.74
PIO3_12/DP06A	F5	G3	19	129.40	1,977.75
PIO3_13/DP06B	E5	H3	20	231.40	1,942.74
GND	A9	J3	21	129.40	1,907.75
GND	—	—	22	231.40	1,872.74
PIO3_14/DP07A	—	H1	23	129.40	1,837.75
PIO3_15/DP07B	—	J1	24	231.40	1,802.74
VCCIO_3	K1	K3	25	129.40	1,767.75
VCC	G6	L10	26	231.40	1,732.74
PIO3_16/DP08A	—	K1	27	129.40	1,697.75
PIO3_17/DP08B	—	L1	28	231.40	1,662.74
PIO3_18/DP09A	G2	L3	29	129.40	1,627.75
GBIN7/PIO3_19/DP09B	G1	L5	30	231.40	1,592.74
VCCIO_3	J6	N10	31	129.40	1,557.75

iCE65P04 Pad Name	Available Packages		DiePlus		
	CB196	CB284	Pad	X (µm)	Y (µm)
VREF	N/A	M1	32	231.40	1,522.74
GND	A9	N1	33	129.40	1,487.75
GBIN6/PIO3_20/DP10A	H1	M5	34	231.40	1,452.74
PIO3_21/DP10B	H2	M3	35	129.40	1,417.75
GND	A9	M11	36	231.40	1,382.74
PIO3_22/DP11A	G3	N3	37	129.40	1,347.75
PIO3_23/DP11B	G4	P3	38	231.40	1,312.74
VCCIO_3	K1	R3	39	129.40	1,277.75
VCCIO_3	—	—	40	231.40	1,242.74
GND	A9	T3	41	129.40	1,207.75
GND	—	—	42	231.40	1,172.74
PIO3_24/DP12A	J1	U3	43	129.40	1,137.75
PIO3_25/DP12B	J2	V3	44	231.40	1,102.74
GND	A9	V1	45	129.40	1,067.75
PIO3_26/DP13A	H4	W3	46	231.40	1,032.74
PIO3_27/DP13B	H3	Y3	47	129.40	997.75
PIO3_28/DP14A	K2	L7	48	231.40	962.74
PIO3_29/DP14B	J3	L8	49	129.40	927.75
PIO3_30/DP15A	H5	M7	50	231.40	892.74
PIO3_31/DP15B	G5	M8	51	129.40	857.75
VCC	F2	N8	52	231.40	822.74
PIO3_32/DP16A	L1	N7	53	129.40	787.75
PIO3_33/DP16B	L2	N5	54	231.40	752.74
VCCIO_3	K1	P5	55	129.40	717.75
VCCIO_3	—	—	56	231.40	682.74
GND	L3	R7	57	129.40	637.75
GND	—	—	58	231.40	592.74
PIO3_34/DP17A	M1	P7	59	129.40	547.75
PIO3_35/DP17B	M2	P8	60	231.40	502.74
PIO3_36/DP18A	K3	R5	61	129.40	457.75
PIO3_37/DP18B	K4	T5	62	231.40	412.74
PIO3_38/DP19A	N1	U5	63	129.40	367.75
PIO3_39/DP19B	N2	V5	64	231.40	322.74
PIO2_00	—	AB2	65	440.00	139.20
PIO2_01	L4	V6	66	490.00	37.20
PIO2_02	M3	T7	67	540.00	139.20
GND	C2	AB5	68	590.00	37.20
PIO2_03	P1	R8	69	640.00	139.20
PIO2_04	N3	V7	70	690.00	37.20
PIO2_05	P2	T8	71	740.00	139.20
PIO2_06	L5	R9	72	790.00	37.20
PIO2_07	M4	V8	73	825.00	139.20
PIO2_08	P3	R10	74	860.00	37.20
VCCIO_2	M5	T9	75	895.00	139.20
PIO2_09	K5	V9	76	930.00	37.20

iCE65P04 Pad Name	Available Packages		DiePlus		
	CB196	CB284	Pad	X (µm)	Y (µm)
PIO2_10	N4	T10	77	965.00	139.20
GND	H7	V10	78	1,000.00	37.20
PIO2_11	P4	Y4	79	1,035.00	139.20
PIO2_12	L6	Y5	80	1,070.00	37.20
PIO2_13	—	AB6	81	1,105.00	139.20
PIO2_14	—	AB7	82	1,140.00	37.20
PIO2_15	—	AB8	83	1,175.00	139.20
PIO2_16	—	AB9	84	1,210.00	37.20
PIO2_17	—	AB10	85	1,245.00	139.20
PIO2_18	—	AB11	86	1,280.00	37.20
GND	H8	N12	87	1,315.00	139.20
PIO2_19	K6	Y6	88	1,350.00	37.20
PIO2_20	N5	Y7	89	1,385.00	139.20
VCC	J4	Y8	90	1,420.00	37.20
PIO2_21	—	—	91	1,455.00	139.20
PIO2_22	—	—	92	1,490.00	37.20
PLLGND	M6	Y9	93	1,525.00	139.20
PLLVCC	N6	Y10	94	1,595.00	37.20
GBIN5/PIO2_23	P5	V11	95	1,630.00	139.20
GBIN4/PIO2_24	L7	V12	96	1,665.00	37.20
PIO2_25	—	AB12	97	1,700.00	139.20
VCCIO_2	J9	Y11	98	1,735.00	37.20
PIO2_26	—	AB13	99	1,770.00	139.20
PIO2_27	K7	AB14	100	1,805.00	37.20
GND	J5	Y12	101	1,840.00	139.20
PIO2_28	K9	AB15	102	1,875.00	37.20
PIO2_29	M7	Y13	103	1,910.00	139.20
PIO2_30	K8	Y14	104	1,945.00	37.20
PIO2_31	P7	Y15	105	1,980.00	139.20
PIO2_32	L8	Y17	106	2,015.00	37.20
PIO2_33	P8	Y18	107	2,050.00	139.20
PIO2_34	N8	Y19	108	2,085.00	37.20
PIO2_35	M8	Y20	109	2,120.00	139.20
VCC	J7	N11	110	2,155.00	37.20
VCC	—	—	111	2,190.00	139.20
PIO2_36	P9	V13	112	2,225.00	37.20
PIO2_37	N9	T11	113	2,260.00	139.20
VCCIO_2	N10	N13	114	2,295.00	37.20
PIO2_38	M9	R11	115	2,330.00	139.20
GND	J8	M12	116	2,365.00	37.20
PIO2_39	N12	T12	117	2,400.00	139.20
PIO2_40	N11	R12	118	2,435.00	37.20
PIO2_41	N13	T13	119	2,470.00	139.20
PIO2_42/CBSEL0	L9	R13	120	2,505.00	37.20
PIO2_43/CBSEL1	P10	V14	121	2,540.00	139.20
CDONE	M10	T14	122	2,575.00	37.20
CRESET_B	L10	R14	123	2,625.00	139.20

iCE65P04 Pad Name	Available Packages		DiePlus		
	CB196	CB284	Pad	X (µm)	Y (µm)
PIOS_00/SPI_SO	M11	T15	124	2,690.00	37.20
PIOS_01/SPI_SI	P11	V15	125	2,740.00	139.20
GND	P6	Y16	126	2,790.00	37.20
PIOS_02/SPI_SCK	P12	V16	127	2,840.00	139.20
PIOS_03/SPI_SS_B	P13	V17	128	2,890.00	37.20
SPI_VCC	L11	R15	129	2,990.00	37.20
TDI	M12	T16	130	3,610.80	342.00
TMS	P14	V18	131	3,712.80	392.00
TCK	L12	R16	132	3,610.80	442.00
TDO	N14	U18	133	3,712.80	492.00
TRST_B	M14	T18	134	3,610.80	542.00
PIO1_00	K11	R18	135	3,712.80	592.00
PIO1_01	L13	P16	136	3,610.80	642.00
PIO1_02	K12	P15	137	3,712.80	692.00
PIO1_03	M13	P18	138	3,610.80	727.00
GND	J14	N18	139	3,712.80	762.00
GND	J14	N18	140	3,610.80	797.00
PIO1_04	J10	N16	141	3,712.80	832.00
PIO1_05	L14	N15	142	3,610.80	867.00
VCCIO_1	H14	M18	143	3,712.80	902.00
VCCIO_1	—	—	144	3,610.80	937.00
PIO1_06	J11	M16	145	3,712.80	972.00
PIO1_07	K14	M15	146	3,610.80	1,007.00
PIO1_08	H10	W20	147	3,712.80	1,042.00
PIO1_09	J13	V20	148	3,610.80	1,077.00
PIO1_10	J12	U20	149	3,712.80	1,112.00
VCC	N7	M13	150	3,610.80	1,147.00
VCC	—	—	151	3,712.80	1,182.00
PIO1_11	H13	T22	152	3,610.80	1,217.00
PIO1_12	H12	R22	153	3,712.80	1,252.00
PIO1_13	—	P22	154	3,610.80	1,287.00
PIO1_14	—	N22	155	3,712.80	1,322.00
PIO1_15	G13	T20	156	3,610.80	1,357.00
PIO1_16	H11	R20	157	3,712.80	1,392.00
PIO1_17	G14	P20	158	3,610.80	1,427.00
GND	K10	N20	159	3,712.80	1,462.00
GND	—	—	160	3,610.80	1,497.00
PIO1_18	G10	M20	161	3,712.80	1,532.00
GBIN3/PIO1_19	G12	K18	162	3,610.80	1,567.00
GBIN2/PIO1_20	F10	L18	163	3,712.80	1,602.00
PIO1_21	F14	K20	164	3,610.80	1,637.00
VCCIO_1	H14	J20	165	3,712.80	1,672.00
VCCIO_1	—	—	166	3,610.80	1,707.00
PIO1_22	F13	H20	167	3,712.80	1,742.00
PIO1_23	D13	G20	168	3,610.80	1,777.00
PIO1_24	G11	F20	169	3,712.80	1,812.00

iCE65P04 Pad Name	Available Packages		DiePlus		
	CB196	CB284	Pad	X (µm)	Y (µm)
PIO1_25	F11	E20	170	3,610.80	1,847.00
PIO1_26	E10	D20	171	3,712.80	1,882.00
PIO1_27	E14	C20	172	3,610.80	1,917.00
GND	G8	L12	173	3,712.80	1,952.00
GND	—	—	174	3,610.80	1,987.00
PIO1_28	F12	G22	175	3,712.80	2,022.00
PIO1_29	D14	L16	176	3,610.80	2,057.00
PIO1_30	E13	L15	177	3,712.80	2,092.00
PIO1_31	C14	K16	178	3,610.80	2,127.00
VCC	K13	L20	179	3,712.80	2,162.00
VCC	—	—	180	3,610.80	2,197.00
PIO1_32	E11	J18	181	3,712.80	2,232.00
PIO1_33	C13	K15	182	3,610.80	2,267.00
VCCIO_1	F9	K13	183	3,712.80	2,302.00
VCCIO_1	—	—	184	3,610.80	2,337.00
PIO1_34	E12	J16	185	3,712.80	2,377.00
PIO1_35	B14	H18	186	3,610.80	2,427.00
GND	G9	L13	187	3,712.80	2,477.00
PIO1_36	B13	J15	188	3,610.80	2,527.00
PIO1_37	D12	H16	189	3,712.80	2,577.00
PIO1_38	C12	G18	190	3,610.80	2,627.00
PIO1_39	D11	F18	191	3,712.80	2,677.00
VPP_2V5	A14	E18	192	3,610.80	2,739.68
VPP_FAST	A13	E17	193	3,096.90	2,962.80
VCC	F8	K12	194	2,997.00	2,860.80
VCC	F8	K12	195	2,947.00	2,962.80
PIO0_00	C11	E16	196	2,897.00	2,860.80
PIO0_01	—	G16	197	2,847.00	2,962.80
PIO0_02	A12	E15	198	2,797.00	2,860.80
PIO0_03	B11	G15	199	2,747.00	2,962.80
PIO0_04	—	H15	200	2,697.00	2,860.80
PIO0_05	D10	E14	201	2,647.00	2,962.80
PIO0_06	A11	G14	202	2,612.00	2,860.80
PIO0_07	D9	H14	203	2,577.00	2,962.80
GND	H6	E13	204	2,542.00	2,860.80
GND	—	—	205	2,507.00	2,962.80
PIO0_08	C10	G13	206	2,472.00	2,860.80
PIO0_09	A10	H13	207	2,437.00	2,962.80
PIO0_10	B10	G12	208	2,402.00	2,860.80
PIO0_11	E9	H12	209	2,367.00	2,962.80
PIO0_12	—	A18	210	2,332.00	2,860.80
PIO0_13	—	A17	211	2,297.00	2,962.80
PIO0_14	—	A16	212	2,262.00	2,860.80
PIO0_15	—	A15	213	2,227.00	2,962.80
VCCIO_0	A8	E12	214	2,192.00	2,860.80
VCCIO_0	—	—	215	2,157.00	2,962.80
PIO0_16	—	C19	216	2,122.00	2,860.80

iCE65P04 Pad Name	Available Packages		DiePlus		
	CB196	CB284	Pad	X (µm)	Y (µm)
PIO0_17	C9	C18	217	2,087.00	2,962.80
PIO0_18	B9	C17	218	2,052.00	2,860.80
PIO0_19	D8	C16	219	2,017.00	2,962.80
PIO0_20	C8	C15	220	1,982.00	2,860.80
PIO0_21	E8	C14	221	1,947.00	2,962.80
PIO0_22	B8	C13	222	1,912.00	2,860.80
GBIN1/PIO0_23	E7	E11	223	1,877.00	2,962.80
GND	B12	C12	224	1,842.00	2,860.80
GND	—	—	225	1,807.00	2,962.80
GBIN0/PIO0_24	A7	E10	226	1,772.00	2,860.80
PIO0_25	D7	C11	227	1,737.00	2,962.80
PIO0_26	C7	C10	228	1,702.00	2,860.80
PIO0_27	E6	C9	229	1,667.00	2,962.80
VCC	B7	C8	230	1,632.00	2,860.80
VCC	—	—	231	1,597.00	2,962.80
PIO0_28	A6	C7	232	1,562.00	2,860.80
PIO0_29	B6	C6	233	1,527.00	2,962.80
PIO0_30	A5	C5	234	1,492.00	2,860.80
PIO0_31	D6	C4	235	1,457.00	2,962.80
GND	F7	K11	236	1,422.00	2,860.80
GND	—	—	237	1,387.00	2,962.80
PIO0_32	—	C3	238	1,352.00	2,860.80
PIO0_33	—	A7	239	1,317.00	2,962.80
PIO0_34	—	A6	240	1,282.00	2,860.80
PIO0_35	—	A5	241	1,247.00	2,962.80
PIO0_36	C6	G11	242	1,212.00	2,860.80
VCCIO_0	F6	K10	243	1,177.00	2,962.80
VCCIO_0	F6	K10	244	1,142.00	2,860.80
PIO0_37	C5	H11	245	1,107.00	2,962.80
PIO0_38	B5	G10	246	1,072.00	2,860.80
PIO0_39	A4	E9	247	1,037.00	2,962.80
PIO0_40	B4	H10	248	1,002.00	2,860.80
PIO0_41	D5	G9	249	967.00	2,962.80
PIO0_42	A3	E8	250	917.00	2,860.80
GND	G7	L11	251	867.00	2,962.80
PIO0_43	B3	H9	252	817.00	2,860.80
PIO0_44	C4	G8	253	767.00	2,962.80
PIO0_45	A2	E7	254	717.00	2,860.80
PIO0_46	A1	E6	255	667.00	2,962.80
PIO0_47	B2	E5	256	617.00	2,860.80

Electrical Characteristics

All parameter limits are specified under worst-case supply voltage, junction temperature, and processing conditions.

Absolute Maximum Ratings

Stresses beyond those listed under Table 50 may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions is not implied. Exposure to absolute maximum conditions for extended periods of time adversely affects device reliability.

Table 50: **Absolute Maximum Ratings**

Symbol	Description	Minimum	Maximum	Units
VCC	Core supply Voltage	–0.5	1.42	V
VPP_2V5	VPP_2V5 NVCM programming and operating supply			V
VPP_FAST	Optional fast NVCM programming supply			V
VCCIO_0 **VCCIO_1** **VCCIO_2** **SPI_VCC**	I/O bank supply voltage (I/O Banks 0, 1, and 2 plus SPI interface)	–0.5	4.00	V
VCCIO_3	I/O Bank 3 supply voltage	–0.5	3.60	V
VIN_0 **VIN_1** **VIN_2** **VIN_SPI**	Voltage applied to PIO pin within a specific I/O bank (I/O Banks 0, 1, and 2 plus SPI interface)	–1.0	5.5	V
VIN_3 **VIN_VREF**	Voltage applied to PIO pin within I/O Bank 3	–0.5	3.60	V
VCCPLL	Analog voltage supply to the Phase Locked Loop (PLL)	–0.5	3.60	V
$\mathbf{I_{OUT}}$	DC output current per pin	—	20	mA
$\mathbf{T_J}$	Junction temperature	–55	125	°C
$\mathbf{T_{STG}}$	Storage temperature, no bias	–65	150	°C

Recommended Operating Conditions

Table 51: **Recommended Operating Conditions**

Symbol	Description		Minimum	Nominal	Maximum	Units
VCC	Core supply voltage	High Performance, low-power	1.14	1.20	1.26	V
VPP_2V5	VPP_2V5 NVCM programming and operating supply	Release from Power-on Reset	1.30	—	3.47	V
		Configure from NVCM	2.30	—	3.47	V
		NVCM programming	2.30	—	3.00	V
VPP_FAST	Optional fast NVCM programming supply		Leave unconnected in application			
SPI_VCC	SPI interface supply voltage		1.71	—	3.47	V
VCCIO_0 VCCIO_1 VCCIO_2 VCCIO_3 SPI_VCC	I/O standards, all banks	**LVCMOS33**	2.70	3.30	3.47	V
		LVCMOS25, LVDS	2.38	2.50	2.63	V
		LVCMOS18, SubLVDS	1.71	1.80	1.89	V
		LVCMOS15	1.43	1.50	1.58	V
VCCIO_3	I/O standards only available in I/O Bank 3	**SSTL2**	2.38	2.50	2.63	V
		SSTL18	1.71	1.80	1.89	V
		MDDR	1.71	1.80	1.89	V
VCCPLL	Analog voltage supply to the Phase Locked Loop (PLL)		1.71	2.50	2.63	V
T_A	Ambient temperature	Commercial (C)	0	—	70	°C
		Industrial (I)	–40	—	85	°C
$\mathbf{T_{PROG}}$	NVCM programming temperature		10	25	30	°C

NOTE:

VPP_FAST is only used for fast production programming. Leave floating or unconnected in application. When the iCE65P device is active, VPP_2V5 must be connected to a valid voltage.

I/O Characteristics

Table 52: **PIO Pin Electrical Characteristics**

Symbol	Description	Conditions	Minimum	Nominal	Maximum	Units
I_I	Input pin leakage current	V_{IN} = $VCCIO_{max}$ to 0 V			±10	µA
I_{OZ}	Three-state I/O pin (Hi-Z) leakage current	V_O = $VCCIO_{max}$ to 0 V			±10	µA
C_{PIO}	PIO pin input capacitance			6		pF
C_{GBIN}	GBIN global buffer pin input capacitance			6		pF
R_{PULLUP}	Internal PIO pull-up resistance during configuration	VCCIO = 3.3V		40		kΩ
		VCCIO = 2.5V		50		kΩ
		VCCIO = 1.8V		90		kΩ
		VCCIO = 1.5V				kΩ
		VCCIO = 1.2V				kΩ
V_{HYST}	Input hysteresis	VCCIO = 1.5V to 3.3V		50		mV

NOTE: All characteristics are characterized and may or may not be tested on each pin on each device.

Single-ended I/O Characteristics

Table 53: **I/O Characteristics (I/O Banks 0, 1, 2 and SPI only)**

I/O Standard	Nominal I/O Bank Supply Voltage	Input Voltage (V)		Output Voltage (V)		Output Current at Voltage (mA)	
		V_{IL}	V_{IH}	V_{OL}	V_{OH}	I_{OL}	I_{OH}
LVCMOS33	3.3V	0.80	2.00	0.4	2.40	8	8
LVCMOS25	2.5V	0.70	1.70	0.4	2.00	6	6
LVCMOS18	1.8V	35% VCCIO	65% VCCIO	0.4	1.40	4	4
LVCMOS15	1.5V	Not supported: Use I/O Bank 3 and SPI Bank		0.4	1.20	2	2

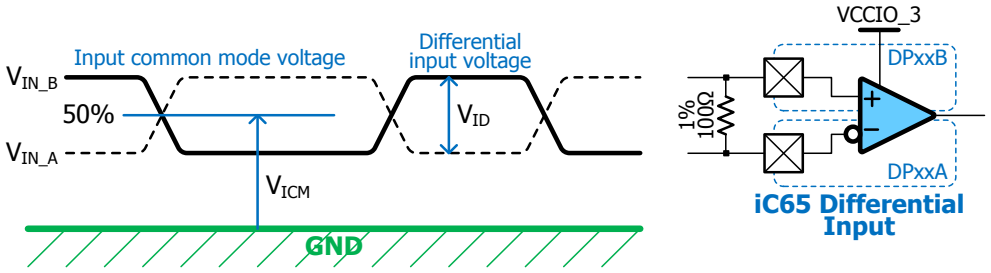
Table 54: **I/O Characteristics (I/O Bank 3 only)**

I/O Standard	Supply Voltage	Input Voltage (V)		Output Voltage (V)		I/O Attribute Name	mA at Voltage
		Max. V_{IL}	Min. V_{IH}	Max. V_{OL}	Min. V_{OH}		I_{OL}, I_{OH}
LVCMOS33	3.3V	0.80	2.20	0.4	2.40	SL_LVCMOS33_8	±8
LVCMOS25	2.5V	0.70	1.70	0.4	2.00	SB_LVCMOS25_16	±16
						SB_LVCMOS25_12	±12
						SB_LVCMOS25_8 *	±8
						SB_LVCMOS25_4	±4
LVCMOS18	1.8V	35% VCCIO	65% VCCIO	0.4	VCCIO–0.45	SB_LVCMOS18_10	±10
						SB_LVCMOS18_8	±8
						SB_LVCMOS18_4 *	±4
						SB_LVCMOS18_2	±2
LVCMOS15	1.5V	35% VCCIO	65% VCCIO	25% VCCIO	75% VCCIO	SB_LVCMOS15_4	±4
						SB_LVCMOS15_2 *	±2
MDDR	1.8V	35% VCCIO	65% VCCIO	0.4	VCCIO–0.45	SB_MDDR10	±10
						SB_MDDR8	±8
						SB_MDDR4 *	±4
						SB_MDDR2	±2
SSTL2 (Class 2)	2.5V	VREF–0.180	VREF+0.180	0.35	VTT+0.430	SB_SSTL2_CLASS_2	±16.2
SSTL2 (Class 1)				0.54		SB_SSTL2_CLASS_1	±8.1
SSTL18 (Full)	1.8V	VREF–0.125	VREF+0.125	0.28	VTT+0.280	SB_SSTL18_FULL	±13.4
SSTL18 (Half)				VTT–0.475	VTT+0.475	SB_SSTL18_HALF	±6.7

NOTES:
SSTL2 and SSTL18 I/O standards require the VREF input pin, which is only available on the CB284 package and for die-based products.

Differential Inputs

Figure 41: **Differential Input Specifications**



Input common mode voltage: $$V_{ICM} = \frac{VCCIO\_3}{2} \pm \Delta V_{ICM}$$

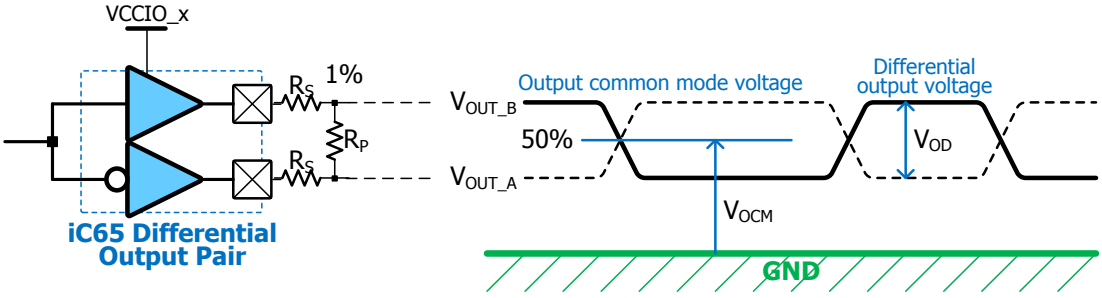
Differential input voltage: $$V_{ID} = |V_{IN\_B} - V_{IN\_A}|$$

Table 55: **Recommended Operating Conditions for Differential Inputs**

I/O Standard	VCCIO_3 (V)			V_{ID} (mV)			V_{ICM} (V)		
	Min	**Nom**	**Max**	**Min**	**Nom**	**Max**	**Min**	**Nom**	**Max**
LVDS	2.38	2.50	2.63	250	350	450	$\frac{VCCIO\_3}{2} - 0.30$	$\frac{VCCIO\_3}{2}$	$\frac{VCCIO\_3}{2} + 0.30$
SubLVDS	1.71	1.80	1.89	100	150	200	$\frac{VCCIO\_3}{2} - 0.25$	$\frac{VCCIO\_3}{2}$	$\frac{VCCIO\_3}{2} + 0.25$

Differential Outputs

Figure 42: **Differential Output Specifications**



Output common mode voltage: $$V_{OCM} = \frac{VCCIO\_x}{2} \pm \Delta V_{OCM}$$

Differential output voltage: $$V_{OD} = |V_{OUT\_B} - V_{OUT\_A}|$$

Table 56: **Recommended Operating Conditions for Differential Outputs**

I/O Standard	VCCIO_x (V)			Ω		V_{OD} (mV)			V_{OCM} (V)		
	Min	**Nom**	**Max**	**R_S**	**R_P**	**Min**	**Nom**	**Max**	**Min**	**Nom**	**Max**
LVDS	2.38	2.50	2.63	150	140	300	350	400	$\frac{VCCIO}{2} - 0.15$	$\frac{VCCIO}{2}$	$\frac{VCCIO}{2} + 0.15$
SubLVDS	1.71	1.80	1.89	270	120	100	150	200	$\frac{VCCIO}{2} - 0.10$	$\frac{VCCIO}{2}$	$\frac{VCCIO}{2} + 0.10$

I/O Banks 0, 1, 2 and SPI Bank Characteristic Curves

Figure 43: **Typical LVCMOS Output Low Characteristics (I/O Banks 0, 1, 2, and SPI)**

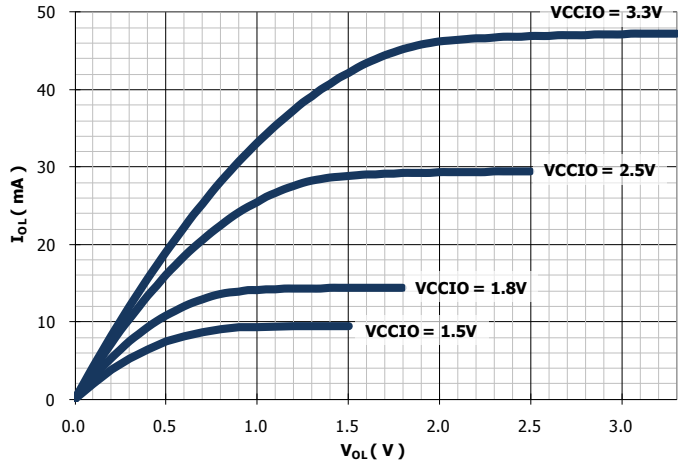


Figure 44: **Typical LVCMOS Output High Characteristics (I/O Banks 0, 1, 2, and SPI)**

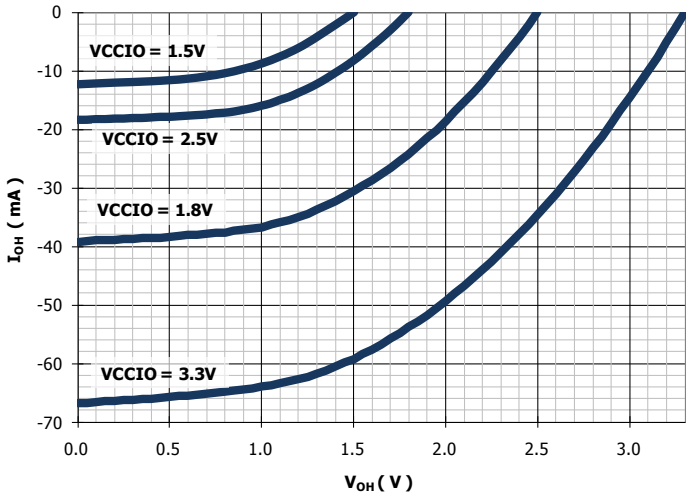
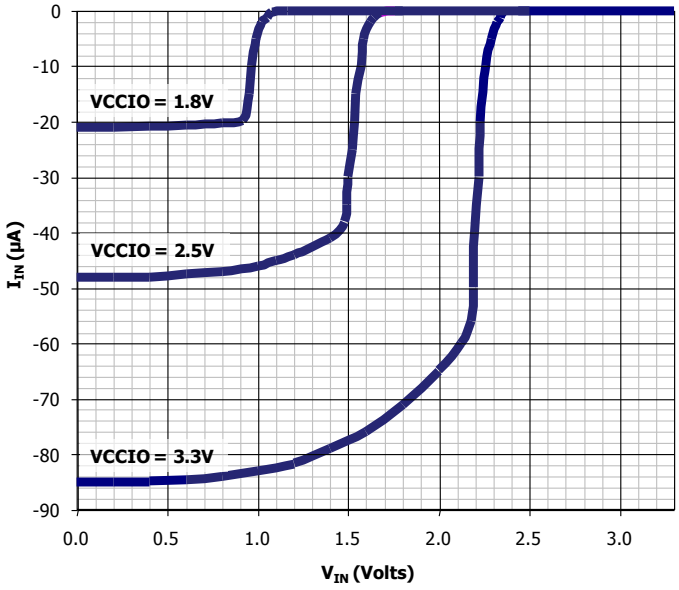


Figure 45: **Input with Internal Pull-Up Resistor Enabled (I/O Banks 0, 1, 2, and SPI)**



AC Timing Guidelines

The following examples provide some guidelines of device performance. The actual performance depends on the specific application and how it is physically implemented in the iCE65P FPGA using the SiliconBlue iCEcube software. The following guidelines assume typical conditions (VCC = 1.0 V or 1.2 V as specified, temperature = 25 °C). Apply derating factors using the iCEcube timing analyzer to adjust to other operating regimes.

Programmable Logic Block (PLB) Timing

Table 57 provides timing information for the logic in a Programmable Logic Block (PLB), which includes the paths shown in Figure 46 and Figure 47.

Figure 46 **PLB Sequential Timing Circuit**

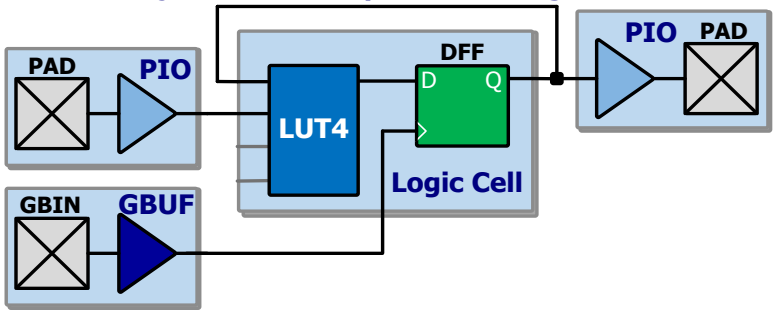


Figure 47 **PLB Combinational Timing Circuit**

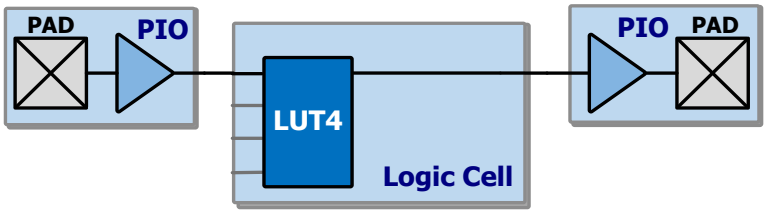


Table 57: **Typical Programmable Logic Block (PLB) Timing**

Symbol	From	To	Description	Power/Speed Grade: –T Nominal VCC: 1.2 V Typ.	Units
Sequential Logic Paths					
F_{TOGGLE}	GBIN input	GBIN input	Flip-flop toggle frequency. DFF flip-flop output fed back to LUT4 input with 4-input XOR, clocked on same clock edge	256	MHz
t_{CKO}	DFF clock input	PIO output	Logic cell flip-flop (DFF) clock-to-output time, measured from the DFF CLK input to PIO output, including interconnect delay.	7.1	ns
t_{GBCKLC}	GBIN input	DFF clock input	Global Buffer Input (GBIN) delay, though Global Buffer (GBUF) clock network to clock input on the logic cell DFF flip-flop.	2.7	ns
t_{SULI}	PIO input	GBIN input	Minimum setup time on PIO input, through LUT4, to DFF flip-flop D-input before active clock edge on the GBIN input, including interconnect delay.	1.2	ns
t_{HDLI}	GBIN input	PIO input	Minimum hold time on PIO input, through LUT4, to DFF flip-flop D-input after active clock edge on the GBIN input, including interconnect delay.	0	ns
Combinational Logic Paths					
t_{LUT4IN}	PIO input	LUT4 input	Asynchronous delay from PIO input pad to adjacent PLB interconnect.	3.3	ns
t_{ILO}	LUT4 input	LUT4 output	Logic cell LUT4 combinational logic propagation delay, regardless of logic complexity from input to output.	0.62	ns
t_{LUT4IN}	LUT4 output	PIO output	Asynchronous delay from adjacent PLB interconnect to PIO output pad.	6.6	ns

Programmable Input/Output (PIO) Block

Table 58 provides timing information for the logic in a Programmable Logic Block (PLB), which includes the paths shown in Figure 48 and Figure 49. The timing shown is for the LVCMOS25 I/O standard in all I/O banks. The iCEcube development software reports timing adjustments for other I/O standards.

Figure 48: **Programmable I/O (PIO) Pad-to-Pad Timing Circuit**

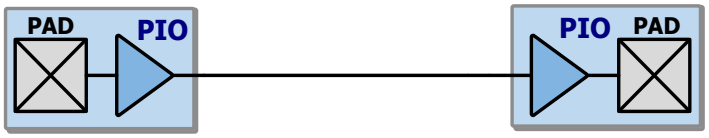


Figure 49: **Programmable I/O (PIO) Sequential Timing Circuit**

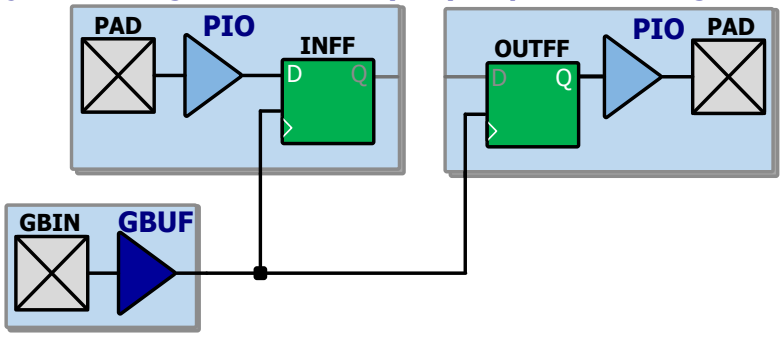


Table 58: **Typical Programmable Input/Output (PIO) Timing (LVCMOS25)**

Symbol	From	To	*Power/Speed Grad* / *Nominal VCC* / Description	–T / 1.2 V / Typ.	Units
Synchronous Output Paths					
t_{OCKO}	OUTFF clock input	PIO output	Delay from clock input on OUTFF output flip-flop to PIO output pad.	5.6	ns
t_{GBCKIO}	GBIN input	OUTFF clock input	Global Buffer Input (GBIN) delay, though Global Buffer (GBUF) clock network to clock input on the PIO OUTFF output flip-flop.	2.6	ns
Synchronous Input Paths					
t_{SUPDIN}	PIO input	GBIN input	Setup time on PIO input pin to INFF input flip-flop before active clock edge on GBIN input, including interconnect delay.	0	ns
t_{HDPDIN}	GBIN input	PIO input	Hold time on PIO input to INFF input flip-flop after active clock edge on the GBIN input, including interconnect delay.	2.8	ns
Pad to Pad					
t_{PADIN}	PIO input	Inter-connect	Asynchronous delay from PIO input pad to adjacent interconnect.	3.2	ns
t_{PADO}	Inter-connect	PIO output	Asynchronous delay from adjacent interconnect to PIO output pad including interconnect delay.	6.2	ns

RAM4K Block

Table 59 provides timing information for the logic in a RAM4K block, which includes the paths shown in Figure 50.

Figure 50: **RAM4K Timing Circuit**

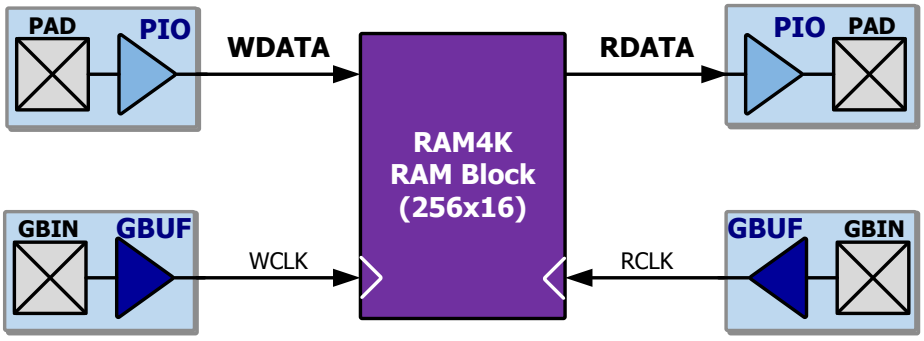


Table 59: **Typical RAM4K Block Timing**

Symbol	From	To	Description	Power/Speed Grade: –T Nominal VCC: 1.2 V Typ.	Units
Write Setup/Hold Time					
t_{SUWD}	PIO input	GBIN input	Minimum write data setup time on PIO inputs before active clock edge on GBIN input, include interconnect delay.	0.8	ns
t_{HDWD}	GBIN input	PIO input	Minimum write data hold time on PIO inputs after active clock edge on GBIN input, including interconnect delay.	0	ns
Read Clock-Output-Time					
t_{CKORD}	RCLK clock input	PIO output	Clock-to-output delay from RCLK input pin, through RAM4K RDATA output flip-flop to PIO output pad, including interconnect delay.	7.3	ns
t_{GBCKRM}	GBIN input	RCLK clock input	Global Buffer Input (GBIN) delay, though Global Buffer (GBUF) clock network to the RCLK clock input.	2.6	ns
Write and Read Clock Characteristics					
t_{RMWCKH}	WCLK RCLK	WCLK RCLK	Write clock High time	0.54	ns
t_{RMWCKL}			Write clock Low time	0.63	ns
t_{RMWCYC}			Write clock cycle time	1.27	ns
F_{WMAX}			Sustained write clock frequency	256	MHz

Phase-Locked Loop (PLL) Block

Table 59 provides timing information for the Phase-Locked Loop (PLL) block shown in Figure 50.

Figure 51: **Phase-Locked Loop (PLL)**

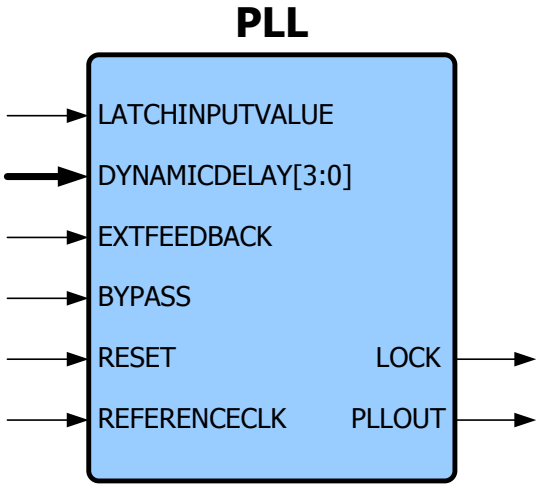


Table 60: **Phase-Locked Loop (PLL) Block Timing**

Symbol	From	To	Description	Power/Speed Grade: –T Nominal VCC: 1.2 V Min.	Typical	Max.	Units
Frequency Range							
F_{REF}			Input clock frequency range	10	—	133	MHz
F_{OUT}			Output clock frequency range (cannot exceed maximum frequency supported by global buffers)	10	—	533	MHz
Duty Cycle							
PLL_{IJ}			Input duty cycle	35	—	65	%
Tw_{HI}			Input clock high time	2.5	—	—	ns
Tw_{LOW}			Input clock low time	2.5	—	—	ns
PLL_{OJD}			Output duty cycle (divided frequency)	45	—	55	%
PLL_{OJM}			Output duty cycle (undivided frequency)	40	—	60	%
Fine Delay							
t_{FDTAP}			Fine delay adjustment, per tap		165		ps
PLL_{TAPS}			Fine delay adjustment settings	0	—	15	taps
PLL_{FDAM}			Maximum delay adjustment		2.5		ns
Jitter							
PLL_{IPJ}			Input clock period jitter	—	—	+/- 300	ps
PLL_{OPJ}			PLLOUT output period jitter	—	1% or ≤ 100	+/- 1.1% output period or ≥ 110	ps
Lock/Reset Time							
t_{LOCK}			PLL lock time after receive stable, monotonic REFERENCECLK input	—	—	50	µs
tw_{RST}			Minimum reset pulse width	20	—	—	ns

Notes:

1. Output jitter performance is affected by input jitter. A clean reference clock < 100ps jitter must be used to ensure best jitter performance.
2. The output jitter specification refers to the intrinsic jitter of the PLL.

Internal Configuration Oscillator Frequency

Table 61 shows the operating frequency for the iCE65's internal configuration oscillator.

Table 61: **Internal Oscillator Frequency**

Symbol	Oscillator Mode	Frequency (MHz)		Description
		Min.	**Max.**	
f_{OSCD}	**Default**	4.0	6.8	Default oscillator frequency. Slow enough to safely operate with any SPI serial PROM.
f_{OSCL}	**Low Frequency**	14	21	Supported by most SPI serial Flash PROMs
f_{OSCH}	**High Frequency**	21	31	Supported by some high-speed SPI serial Flash PROMs
	Off	0	0	Oscillator turned off by default after configuration to save power.

Configuration Timing

Table 62 shows the maximum time to configure an iCE65P device, by oscillator mode. The calculations use the slowest frequency for a given oscillator mode from Table 61 and the maximum configuration bitstream size from Table 1, which includes full RAM4K block initialization. The configuration bitstream selects the desired oscillator mode based on the performance of the configuration data source.

Table 62: **Maximum SPI Master or NVCM Configuration Timing by Oscillator Mode**

Symbol	Description	Device	Default	Low Freq.	High Freq.	Units
$t_{CONFIGL}$	Time from when minimum Power-on Reset (POR) threshold is reached until user application starts.	**iCE65P04**	115	55	25	ms

Table 63 provides timing for the CRESET_B and CDONE pins.

Table 63: **General Configuration Timing**

Symbol	From	To	Description		All Grades Min.	All Grades Max.	Units
t_{CRESET_B}	CREST_B	CREST_B	Minimum CRESET_B Low pulse width required to restart configuration, from falling edge to rising edge		200	—	ns
t_{DONE_IO}	CDONE High	PIO pins active	Number of configuration clock cycles after CDONE goes High before the PIO pins are activated.		—	49	Clock cycles
			SPI Peripheral Mode (Clock = SPI_SCK, cycles measured rising-edge to rising-edge)		Depends on SPI_SCK frequency		
			NVCM or SPI Master Mode by internal oscillator frequency setting (Clock = internal oscillator)s	Default	7.20	12.25	µs
				Low	2.34	3.50	µs
				High	1.59	2.33	µs

Table 64 provides various timing specifications for the SPI peripheral mode interface.

Table 64: **SPI Peripheral Mode Timing**

Symbol	From	To	Description	All Grades		Units
				Min.	Max.	
t_{CR_SCK}	CRESET_B	SPI_SCK	Minimum time from a rising edge on CRESET_B until the first SPI write operation, first SPI_SCK. During this time, the iCE65P FPGA is clearing its internal configuration memory	300	—	µs
$t_{SUSPISI}$	SPI_SI	SPI_SCK	Setup time on SPI_SI before the rising SPI_SCK clock edge	12	—	ns
$t_{HDSPISI}$	SPI_SCK	SPI_SI	Hold time on SPI_SI after the rising SPI_SCK clock edge	12	—	ns
$t_{SPISCKH}$	SPI_SCK	SPI_SCK	SPI_SCK clock High time	20	—	ns
$t_{SPISCKL}$	SPI_SCK	SPI_SCK	SPI_SCK clock Low time	20	—	ns
$t_{SPISCKCYC}$	SPI_SCK	SPI_SCK	SPI_SCK clock period*	40	1,000	ns
F_{SPI_SCK}	SPI_SCK	SPI_SCK	Sustained SPI_SCK clock frequency*	1	25	MHz

* = Applies after sending the synchronization pattern.

Power Consumption Characteristics

Core Power

Table 65 shows the power consumed on the internal VCC supply rail when the device is filled with 16-bit binary counters, measured with a 32.768 kHz and at 32.0 MHz

Table 65: **VCC Power Consumption for Device Filled with 16-Bit Binary Counters**

Symbol	Description	Grade	VCC	iCE65P04		Units
				Typical	Max.	
I_{CC0K}	f =0	–T	1.2V	45		µA
I_{CC32K}	f ≤ 32.768 kHz	–T	1.2V	52		µA
I_{CC32M}	f = 32.0 MHz	–T	1.2V	8		mA

I/O Power

Table 66 provides the static current by I/O bank. The typical current for I/O Banks 0, 1, 2 and the SPI bank is not measurable within the accuracy of the test environment. The PIOs in I/O Bank 3 use different circuitry and dissipate a small amount of static current.

Table 66: I/O Bank Static Current (f = 0 MHz)

Symbol	Description		Typical	Maximum	Units
I_{CCO_0}	I/O Bank 0	Static current consumption per I/O bank. f = 0 MHz. No PIO pull-up resistors enabled. All inputs grounded. All outputs driving Low.	« 1		uA
I_{CCO_1}	I/O Bank 1		« 1		uA
I_{CCO_2}	I/O Bank 2		« 1		uA
I_{CCO_3}	I/O Bank 3		1.2		uA
I_{CCO_SPI}	SPI Bank		« 1		uA

NOTE: The typical static current for I/O Banks 0, 1, 2, and the SPI bank is less than the accuracy of the device tester.

Power Estimator

To estimate the power consumption for a specific application, please download and use the iCE65P Power Estimator Spreadsheet our use the power estimator built into the iCEcube software.

Notes:

Revision History

Version	Date	Description
1.31	22-APR-2011	Updated Figure 35: iCE65P04 CB121 Chip-Scale BGA Footprint (Top View) A10 to PIO0 and G1 to PIO3/DP08B. Updated Table 46: iCE65P04 CB121 Chip-scale BGA Pinout Table F4 to GBIN6/PIO3/DP06A and G4 to PIO3/DP06B.
1.3	17-DEC-2010	Updated Table 60: Phase-Locked Loop (PLL) Block Timing duty cycle, jitter and lock/reset time parameters
1.2	08-OCT-2010	Changed FSPI_SCK from 0.125 MHz to 1 MHz in SPI Peripheral Configuration Process and Table 64. Updated equation: PLLOUT Frequency for FEEDBACK_PATH = SIMPLE
1.1	06-AUG-2010	Added CB121 package. Removed Programmable Interconnect description
1.0	15-FEB-2010	Initial Release

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