

QUICK START GUIDE FOR DEMONSTRATION CIRCUIT 653A DUAL 15A HIGH FREQUENCY STEP-DOWN DC/DC CONVERTER

LTC3802EGN

DESCRIPTION

Demonstration circuit 653A is a dual 15A high frequency step-down DC/DC converter featuring the LTC3802EGN. The LTC3802EGN itself is a synchronous voltage mode controller. The nominal switching frequency of the LTC3802 is 550kHz and its phase lockable synchronization range is 330kHz to 750kHz, typical. Output #1 of demonstration circuit 653A is a 3.3V / 15A rail and output #2 is a 2.5V / 15A rail. The input voltage range is 7V to 24V.

Features of the LTC3802EGN highlighted by demonstration circuit 653A include programmable up/down rail tracking, high efficiency, and a fast load step response. Typical applications include notebook computers, portable instruments, and battery operated devices.

Design files for this circuit board are available. Call the LTC factory.

Table 1. Performance Summary ($T_A = 25^\circ\text{C}$)

PARAMETER	CONDITION	VALUE
Minimum Input Voltage		7V
Maximum Input Voltage		24V
Output Voltage V_{OUT1}	$V_{IN} = 7V \text{ to } 24V, I_{OUT1} = 0A \text{ to } 15A$	3.3V $\pm 3\%$
Output Voltage V_{OUT2}	$V_{IN} = 7V \text{ to } 24V, I_{OUT2} = 0A \text{ to } 15A$	2.5V $\pm 3\%$
Maximum Output Current V_{OUT1}	I_{OUT1}	15A
Maximum Output Current V_{OUT2}	I_{OUT2}	15A
Typical Efficiency V_{OUT1} (5V bias supplied externally, V_{OUT2} disabled)	$V_{IN} = 24V, I_{OUT1} = 15A$	92.3%
	$V_{IN} = 12V, I_{OUT1} = 15A$	94.3%
	$V_{IN} = 7V, I_{OUT1} = 15A$	94.5%
Typical Efficiency V_{OUT2} (5V bias supplied externally, V_{OUT1} disabled)	$V_{IN} = 24V, I_{OUT2} = 15A$	90.2%
	$V_{IN} = 12V, I_{OUT2} = 15A$	93.0%
	$V_{IN} = 7V, I_{OUT2} = 15A$	93.0%
Airflow	$T_{AMB} \leq 30^\circ\text{C}$	No airflow required

QUICK START PROCEDURE

Demonstration circuit 653A is easy to set up to evaluate the performance of the LTC3802EGN. Refer to Figure 1 for the proper measurement equipment setup and follow the procedure below.

1. Make sure JP1 is in the INT5V position, JP4 is in either the RATIOMETRIC or COINCIDENT position and JP2 is in either the 90 DEG. or 0 DEG. position.
2. Connect load to Vout1 and Vout2. Set to 15A.
3. With power off, connect the input power supply from Vin to GND.
4. Turn on the input power supply and set the input voltage to 12.0V.
5. Check for the proper output voltages.
Vout1 = 3.201V to 3.399V
Vout2 = 2.425V to 2.575V
6. Apply 15A load to each of the outputs and re-check regulation.
7. Once the proper output voltages are established, adjust the loads and input voltage within their respective operating range and observe the output voltage regulation, ripple voltage, efficiency and other parameters. Refer to Figures 4 through 13 for efficiency curves and plots showing the output voltage ripple, load step response and rail tracking performance.

EXTERNAL 5V BIAS

Demonstration circuit 653A contains an on-board 5V buck regulator to provide a nominal 5V bias to the LTC3802EGN. This 5V bias is used to power the gate drivers and internal logic of the LTC3802EGN. To use the internal supply, put jumper JP1 in the INT5V position. To use an external lab supply, put jumper in the EXT5V position and connect output of lab supply from EXT5V to GND.

NOTE: The external bias voltage needs to be between 4.5V and 6.0V.

LOAD STEP TESTING

The load step response can be tested with on-board MOSFETs located at the output of each rail and pulse generator. Refer to Figure 3 and follow the steps below to measure the load step response.

1. Set the output of the pulse generator for a duty cycle of less than 5% and an amplitude of 1V or below.
2. Connect the output of pulse generator from PULSE GEN1 to GND or from PULSE GEN2 to GND.
3. Connect PULSED LOAD1 CURRENT or PULSED LOAD2 current coaxial output to oscilloscope to monitor load step current waveform. 10mV = 1A.
4. Connect oscilloscope probe to output voltage.
5. Apply input voltage to demonstration circuit 653A and the desired amount of static load to the output.
6. Increase the amplitude of the pulse generator output to obtain the desired load step height.

RAIL TRACKING

Either ratiometric or coincident rail tracking can be implemented with the LTC3802. Use jumper JP4 to select the rail tracking mode. A controlled ramp-down and ramp-up can be implemented by shorting the PHASE pin to ground and then releasing the short. Refer to Figures 9 – 13 for examples.

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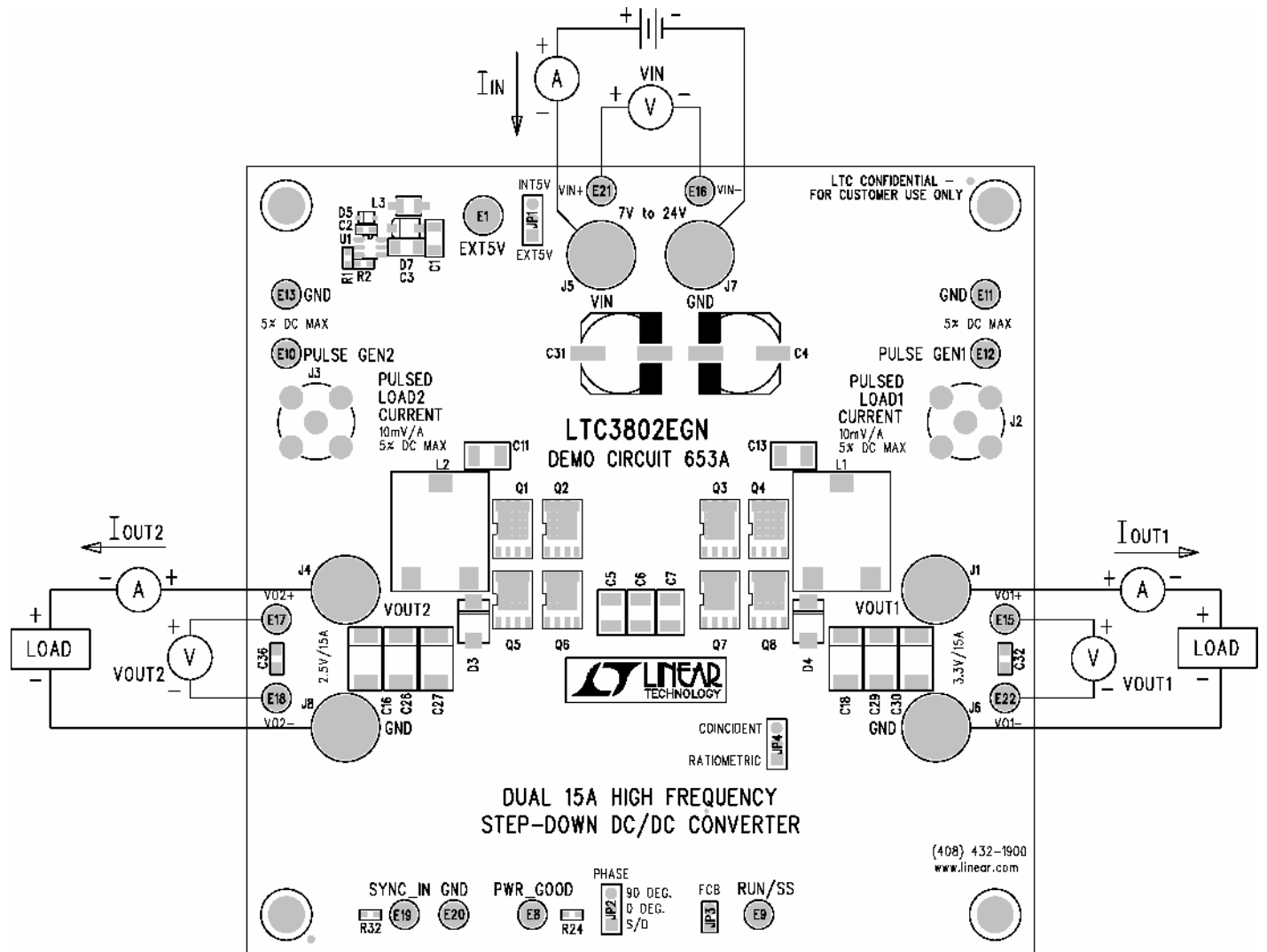


Figure 1. Proper setup of measurement equipment.

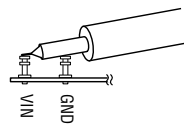


Figure 2. Measuring input or output voltage ripple.

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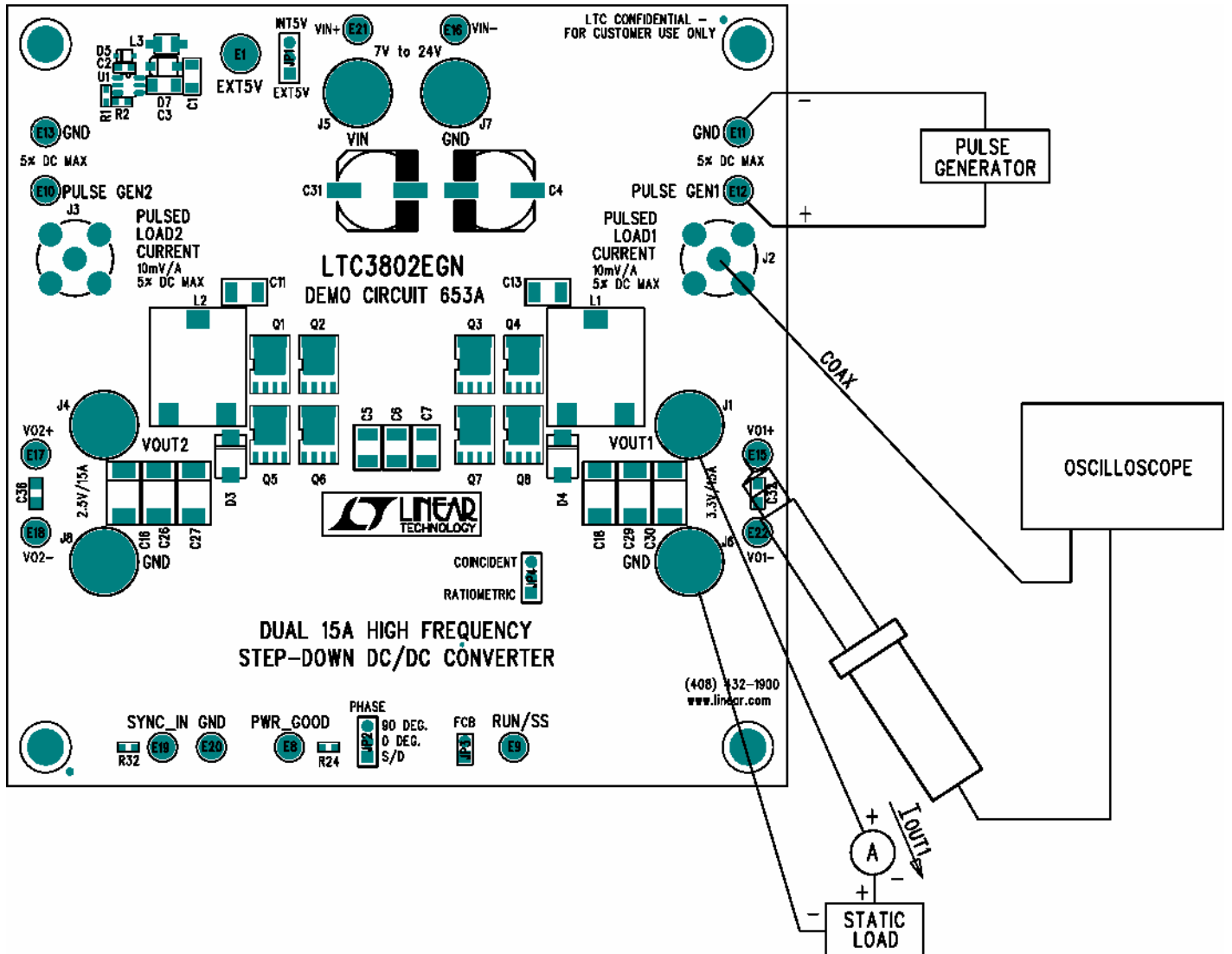


Figure 3. Equipment setup for load step testing.

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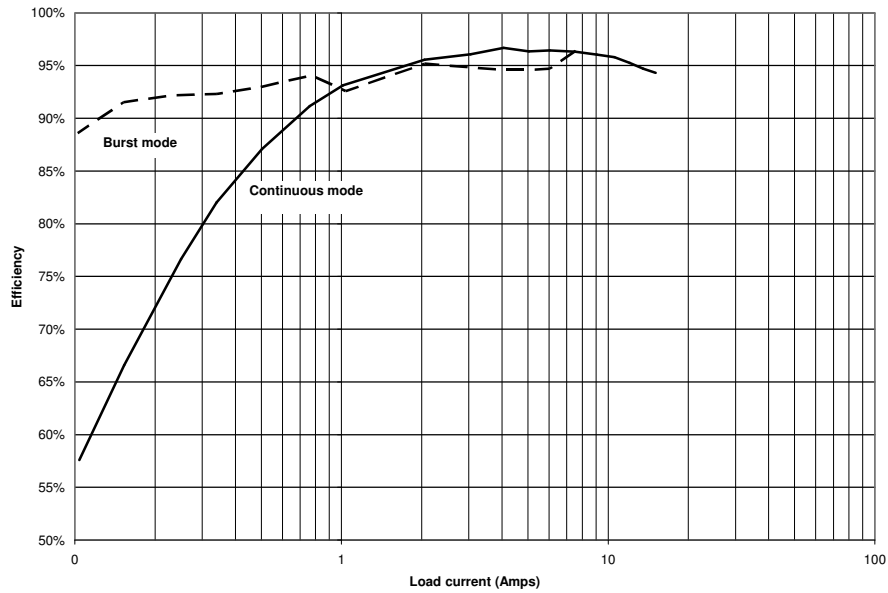


Figure 4. Typical efficiency curve of 3.3V rail at an input voltage of 12V. +5V bias supplied separately and 2.5V rail disabled. $F_{\text{SWITCH}} = 525\text{kHz}$.

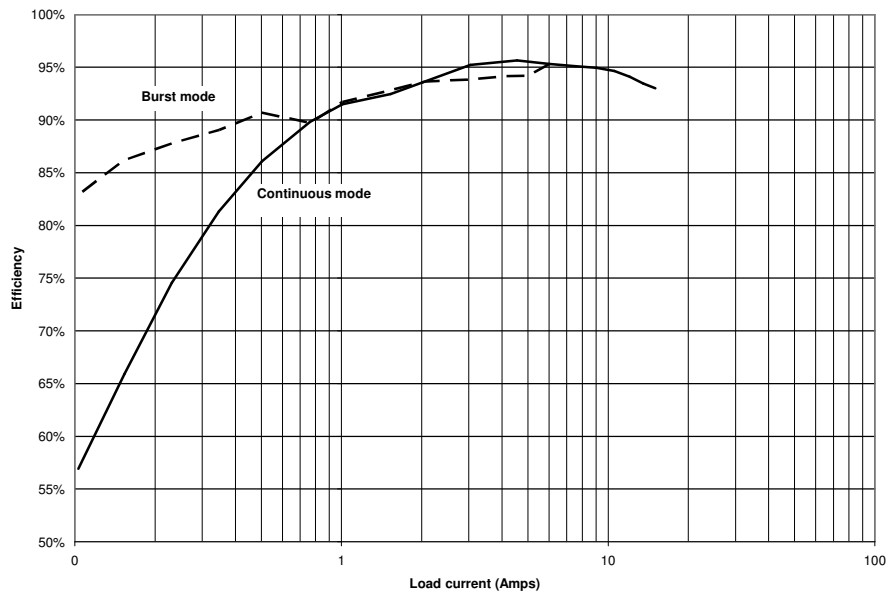


Figure 5. Typical efficiency curve of 2.5V rail at an input voltage of 12V. +5V bias supplied separately and 3.3V rail disabled. $F_{\text{SW}} = 525\text{kHz}$.

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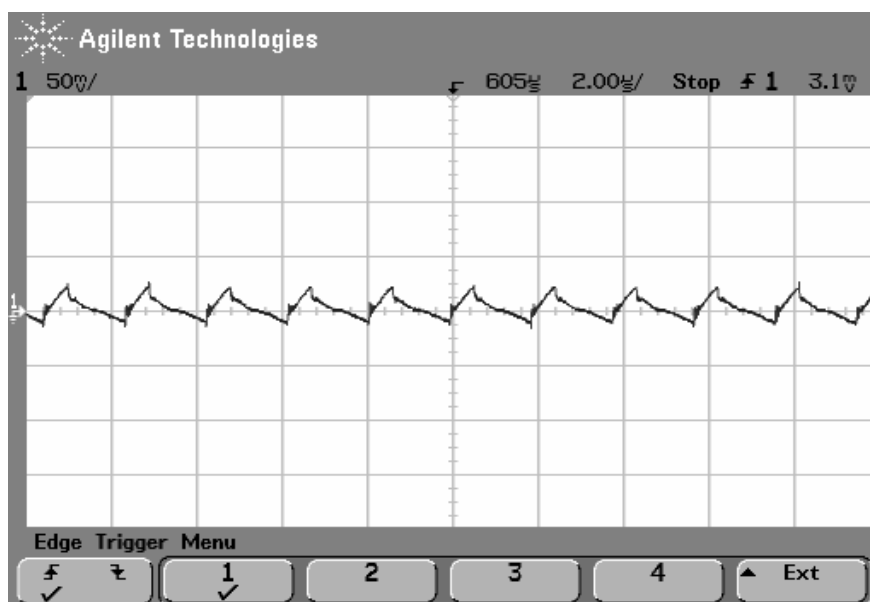


Figure 6. 3.3V output ripple. $V_{IN} = 12.0V$, $I_{OUT} = 15A$, $F_{SW} = 525KhZ$. Measured directly across C_{OUT} .

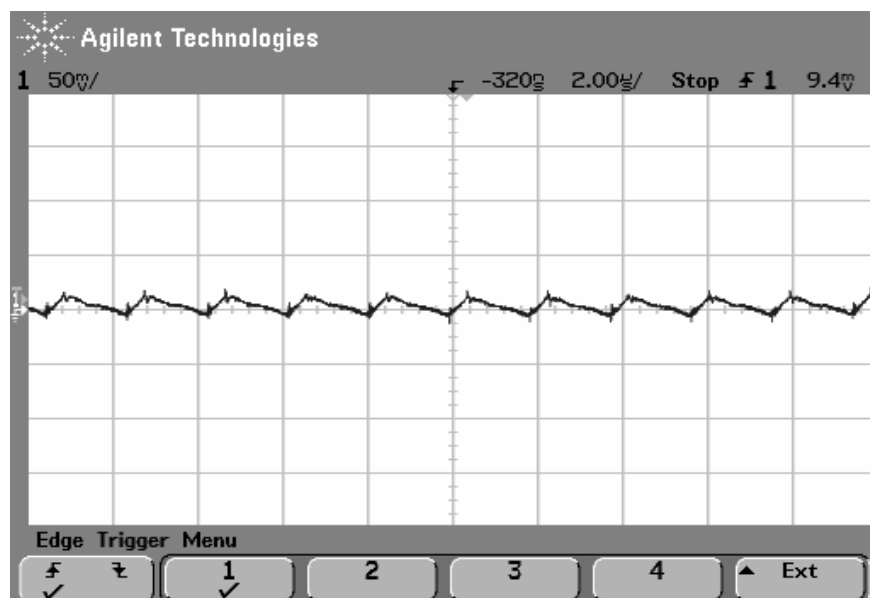


Figure 7. 2.5V output ripple. $V_{IN} = 12.0V$, $I_{OUT} = 15A$, $F_{SW} = 525KhZ$. Measured directly across C_{OUT} .

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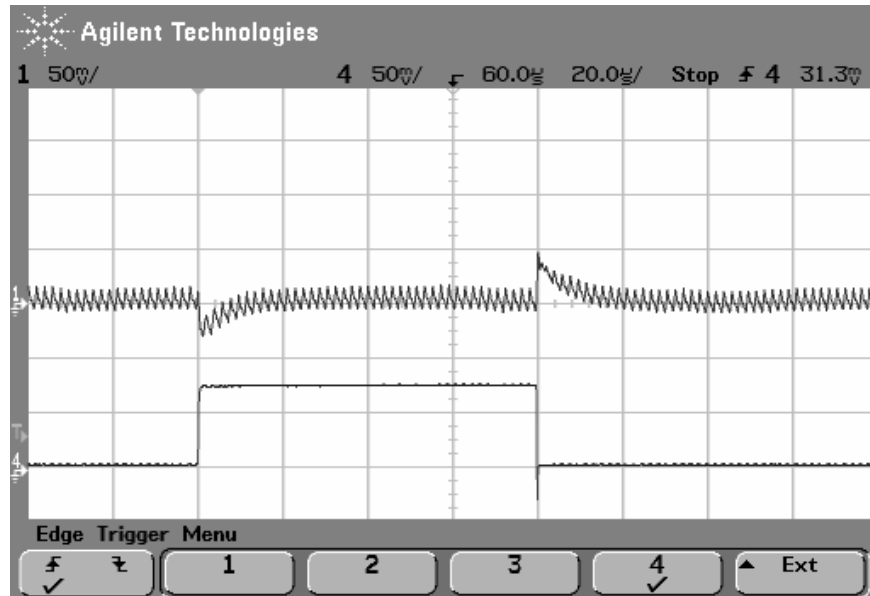


Figure 8. 3.3V load step response, 7.5A to 15A. $V_{IN} = 12.0V$, $F_{SW} = 525KHz$. Measured directly across C_{OUT} .

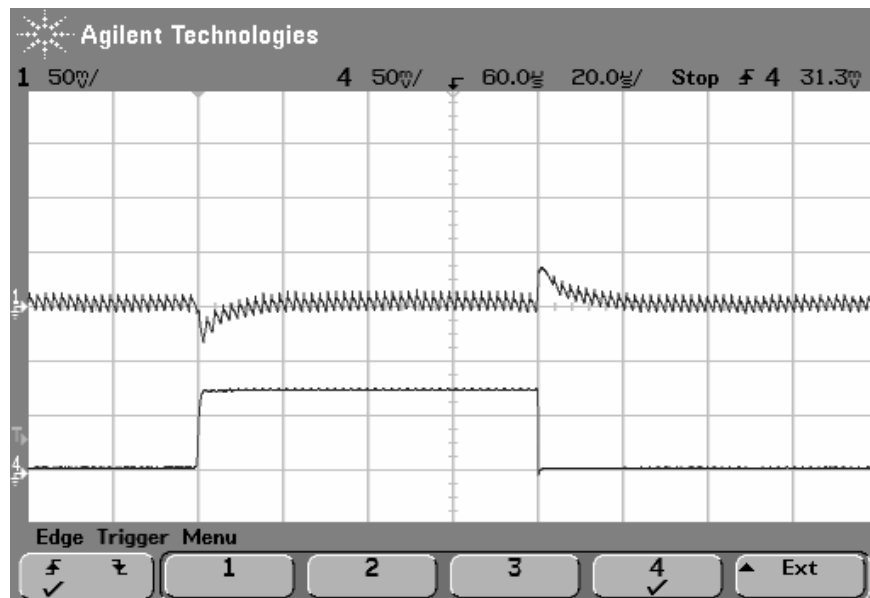


Figure 9. 2.5V load step response, 7.5A to 15A. $V_{IN} = 12.0V$, $F_{SW} = 525KHz$. Measured directly across C_{OUT} .

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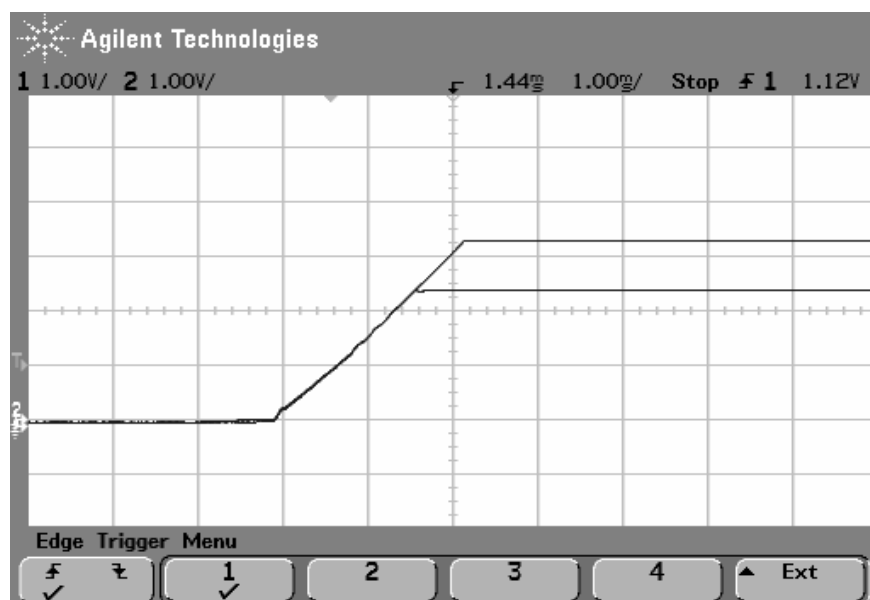


Figure 10. Coincident ramp-up tracking. $I_{OUT1,2} = 15A$. $V_{IN} = 12.0V$. PHASE pin released from ground.

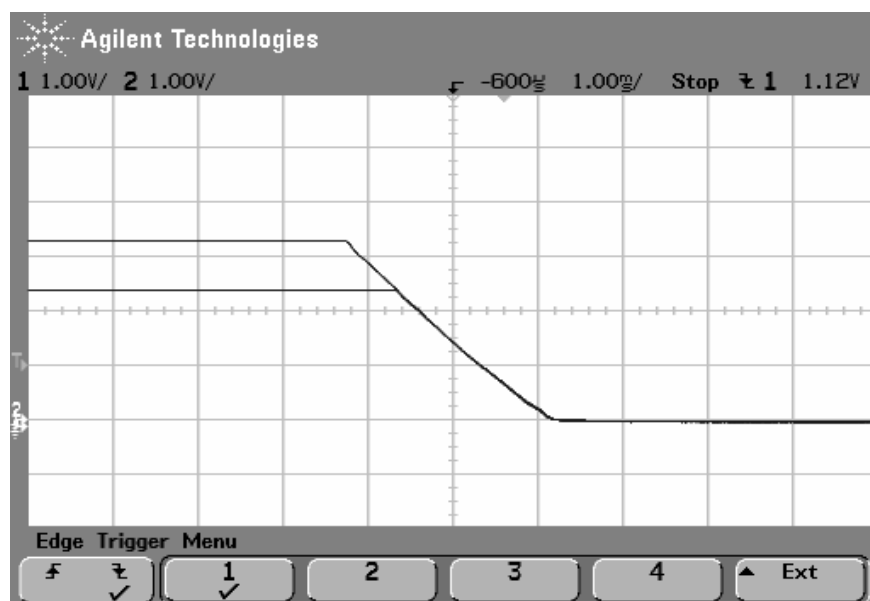


Figure 11. Coincident ramp-down tracking. $I_{OUT1,2} = 15A$. $V_{IN} = 12.0V$. PHASE pin shorted to ground.

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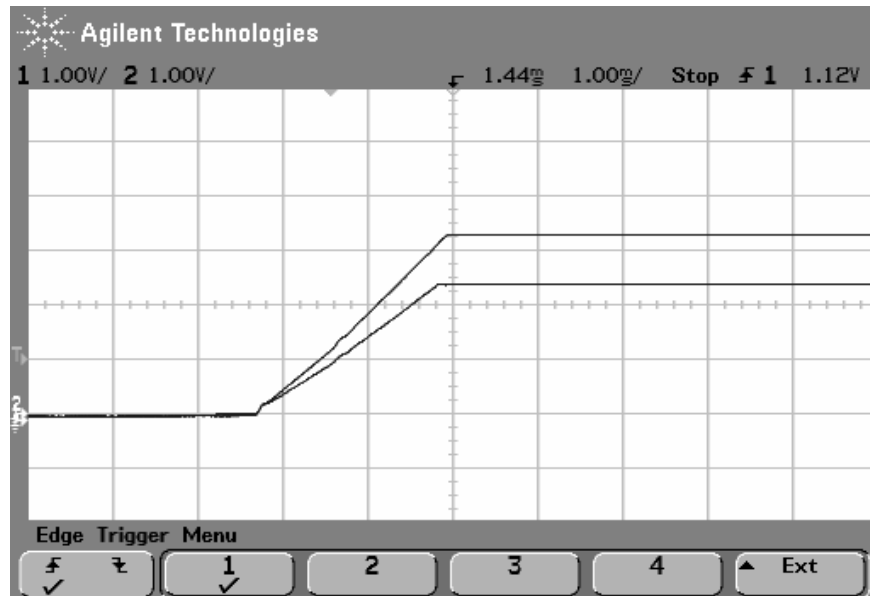


Figure 12. Ratiometric ramp-up tracking. $I_{OUT1,2} = 15A$. $V_{IN} = 12.0V$. PHASE pin released from ground.

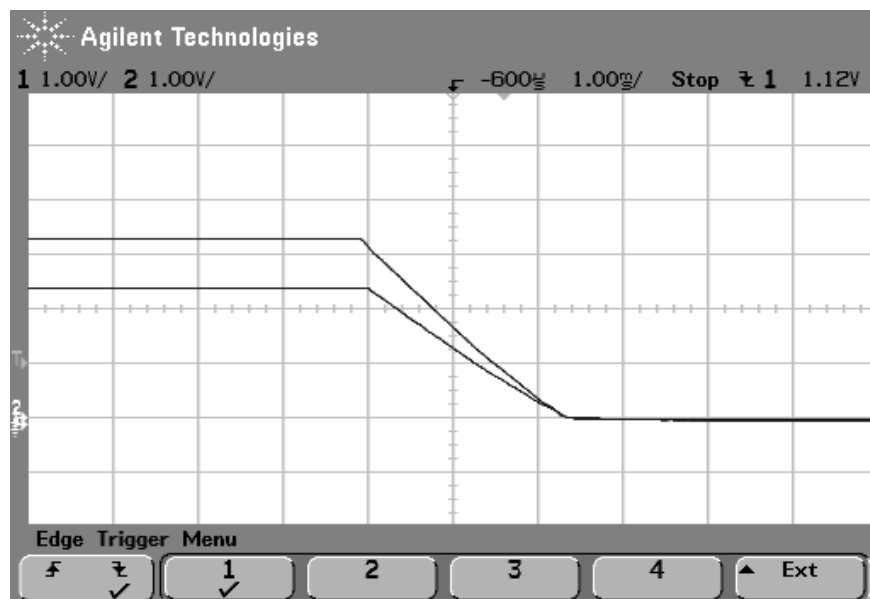
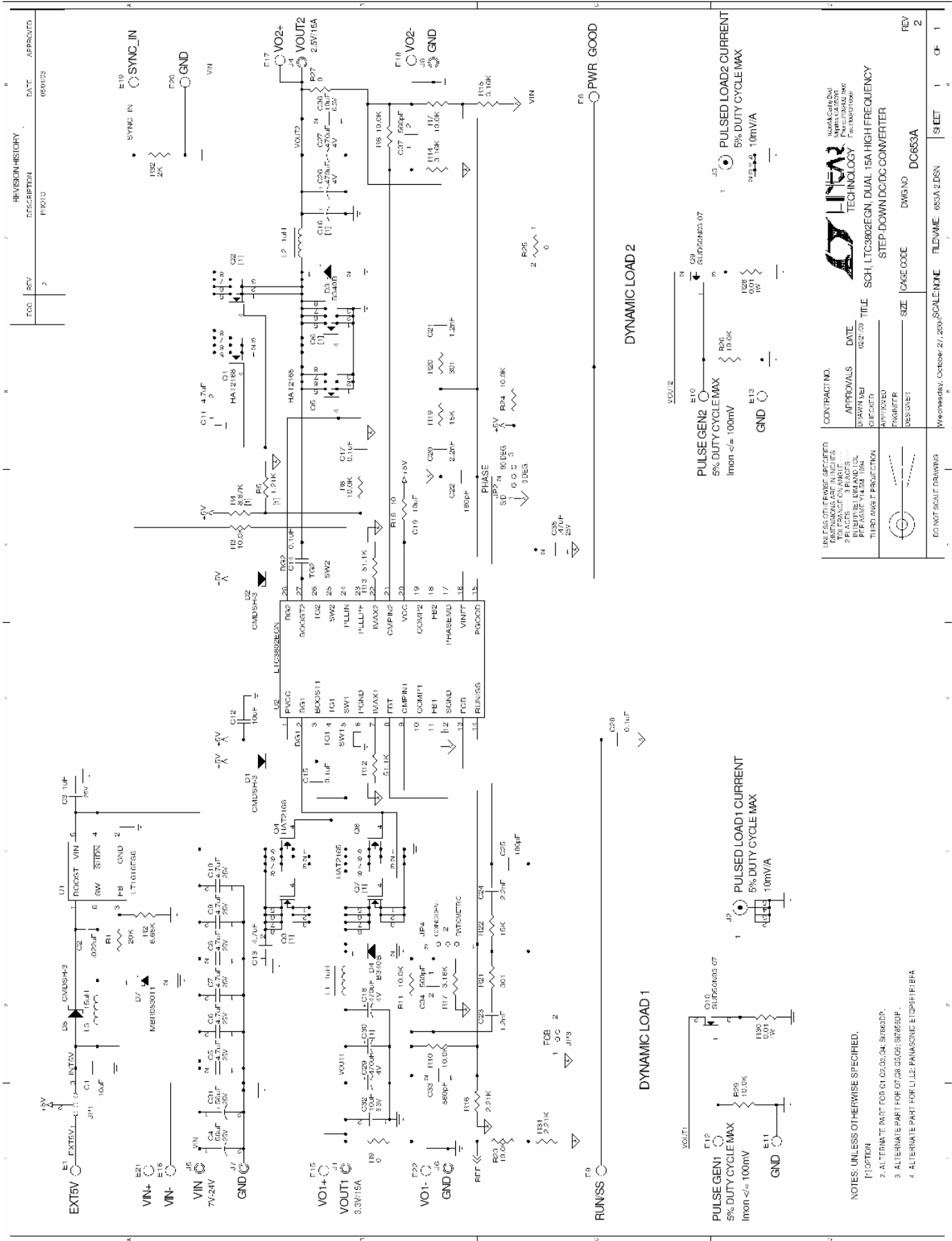


Figure 13. Ratiometric ramp-down tracking. $I_{OUT1,2} = 15A$. $V_{IN} = 12.0V$. PHASE pin shorted to ground.

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CONTRACT NO.	DATE	REV	OF
APPROVALS	08/27/02	2	1
DESIGNED BY	SIZE	DWG NO	SHEET
CHECKED		DC653A	1
DESIGNED			2

FILENAME: 653A2.DSN

UNLESS OTHERWISE SPECIFIED, 1) OPTION 2. ALTERNATE PART FOR C1, C2, C3, C4, S1, S6, S7, S8, S9, S10, S11, S12, S13, S14, S15, S16, S17, S18, S19, S20, S21, S22, S23, S24, S25, S26, S27, S28, S29, S30, S31, S32, S33, S34, S35, S36, S37, S38, S39, S40, S41, S42, S43, S44, S45, S46, S47, S48, S49, S50, S51, S52, S53, S54, S55, S56, S57, S58, S59, S60, S61, S62, S63, S64, S65, S66, S67, S68, S69, S70, S71, S72, S73, S74, S75, S76, S77, S78, S79, S80, S81, S82, S83, S84, S85, S86, S87, S88, S89, S90, S91, S92, S93, S94, S95, S96, S97, S98, S99, S100.

3. ALTERNATE PART FOR 07, 08, 05, 06, 07, 08, 09, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100.

4. ALTERNATE PART FOR L1, L2: PANASONIC E12PH1R1EFA