# LP2953QML Adjustable Micropower Low-Dropout Voltage Regulators

Check for Samples: LP2953QML, LP2953QML-SP

## FEATURES

- Output Voltage Adjusts from 1.23V to 29V
- Ensured 250 mA Output Current
- Extremely Low Quiescent Current
- Low Dropout Voltage
- Extremely Tight Line and Load Regulation
- Very Low Temperature Coefficient
- Current and Thermal Limiting
- Reverse Battery Protection
- 50 mA (Typical) Output Pulldown Crowbar
- Auxiliary Comparator Included with CMOS/TTL Compatible Output Levels. Can be used for Fault Detection, Low Input Line Detection, etc.

## APPLICATIONS

- High-Efficiency Linear Regulator
- Regulator with Under-Voltage Shutdown
- Low Dropout Battery-Powered Regulator
- Snap-ON/Snap-OFF Regulator

## DESCRIPTION

The LP2953A is a micropower voltage regulator with very low quiescent current (130 µA typical at 1 mA load) and very low dropout voltage (typ. 60 mV at light load and 470 mV at 250 mA load current). It is ideally suited for battery-powered systems. Furthermore, the quiescent current increases only slightly at dropout, which prolongs battery life.

The LP2953A retains all the desirable characteristics of the LP2951, but offers increased output current, additional features, and an improved shutdown function.

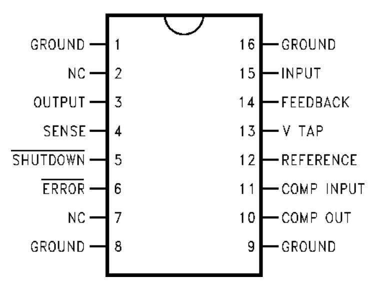
The internal crowbar pulls the output down quickly when the shutdown is activated.

The error flag goes low if the output voltage drops out of regulation.

Reverse battery protection is provided.

The internal voltage reference is made available for external use, providing a low-T.C. reference with very good line and load regulation.

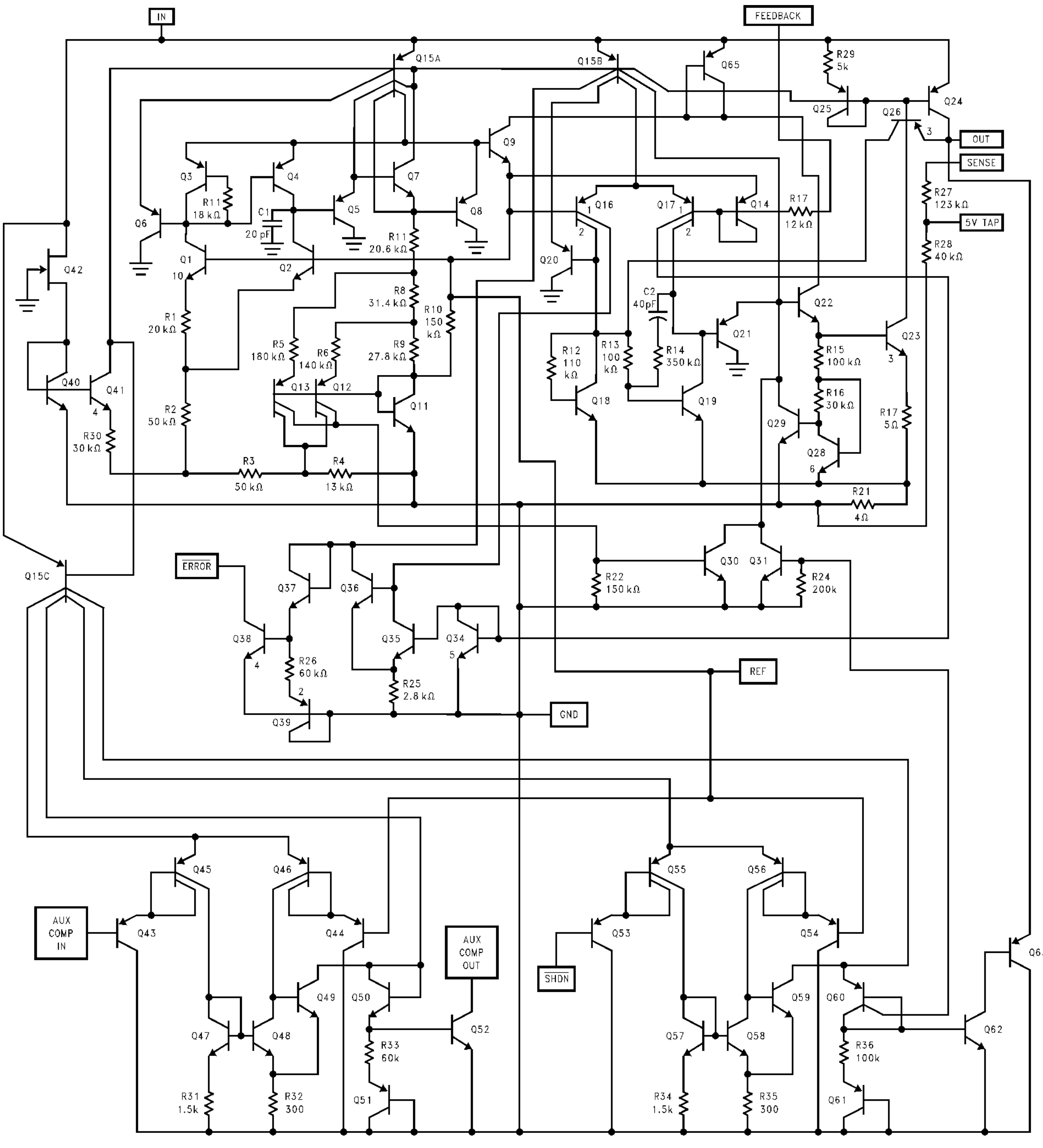
## Connection Diagram




Note: Pins 1, 8, 9, 16 must be shorted together on customer PC board application

**Figure 1. 16-Pin CFP Package**

## Schematic Diagram



## Block Diagram

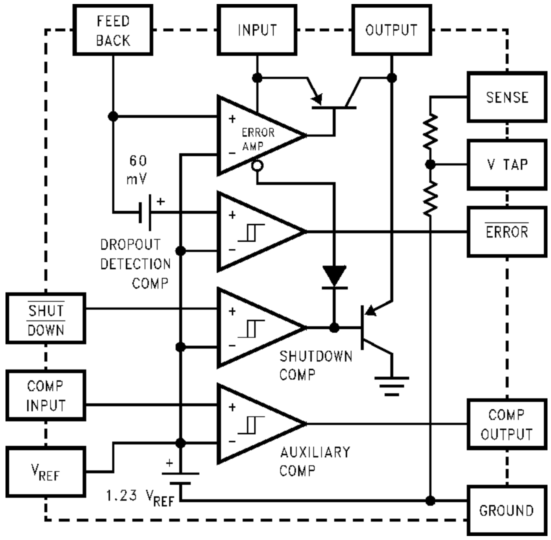



**Figure 2. LP2953**

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## Absolute Maximum Ratings[1]

| | | | |
|---|---|---|---|
| Storage Temperature Range | | | $-65°C \le T_A \le +150°C$ |
| Operating Temperature Range | | | $-55°C \le T_A \le +125°C$ |
| Maximum Junction Temperature | | | +150°C |
| Lead Temp. (Soldering, 5 seconds) | | | 260°C |
| Power Dissipation[2] | | | Internally Limited |
| Input Supply Voltage | | | −20V to +30V |
| Feedback Input Voltage[3] | | | −0.3V to +5V |
| Comparator Input Voltage[4] | | | −0.3V to +30V |
| Shutdown Input Voltage[4] | | | −0.3V to +30V |
| Comparator Output Voltage[4] | | | −0.3V to +30V |
| Thermal Resistance | $\theta_{JA}$ | 16LD CFP "WG" (device 01) (Still Air) | 134°C/W |
| | | 16LD CFP "WG" (device 01) (500LF/Min Air flow) | 81°C/W |
| | | 16LD CFP "GW" (device 02) (Still Air) | 140°C/W |
| | | 16LD CFP "GW" (device 02) (500LF/Min Air flow) | 90°C/W |
| | $\theta_{JC}$ | 16LD CFP "WG" (device 01)[5] | 7°C/W |
| | | 16LD CFP "GW" (device 02) | 15°C/W |
| Package Weight (Typical) | 16LD CFP "WG" (device 01) | | 360mg |
| | 16LD CFP "GW" (device 02) | | 410mg |
| ESD Rating[6] | | | 2 KV |

(1) Abs. Max Ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see Electrical Characteristics. The specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) The maximum power dissipation must be derated at elevated temperatures and is dictated by $T_{Jmax}$ (maximum junction temperature), $\theta_{JA}$ (package junction to ambient thermal resistance), and $T_A$ (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.
(3) When used in dual-supply systems where the regulator load is returned to a negative supply, the output voltage must be diode-clamped to ground.
(4) May exceed the input supply voltage.
(5) The package material for these devices allows much improved heat transfer over our standard ceramic packages. In order to take full advantage of this improved heat transfer, heat sinking must be provided between the package base (directly beneath the die), and either metal traces on, or thermal vias through, the printed circuit board. Without this additional heat sinking, device power dissipation must be calculated using $\theta_{JA}$, rather than $\theta_{JC}$, thermal resistance. It must not be assumed that the device leads will provide substantial heat transfer out the package, since the thermal resistance of the leadframe material is very poor, relative to the material of the package base. The stated $\theta_{JC}$ thermal resistance is for the package material only, and does not account for the additional thermal resistance between the package base and the printed circuit board. The user must determine the value of the additional thermal resistance and must combine this with the stated value for the package, to calculate the total allowed power dissipation for the device.
(6) Human body model, 1.5 KΩ in series with 100 pF.

## Quality Conformance Inspection

**Table 1. Mil-Std-883, Method 5005 - Group A**

| Subgroup | Description | Temp (°C) |
|---|---|---|
| 1 | Static tests at | +25 |
| 2 | Static tests at | +125 |
| 3 | Static tests at | -55 |
| 4 | Dynamic tests at | +25 |
| 5 | Dynamic tests at | +125 |
| 6 | Dynamic tests at | -55 |
| 7 | Functional tests at | +25 |
| 8A | Functional tests at | +125 |
| 8B | Functional tests at | -55 |
| 9 | Switching tests at | +25 |
| 10 | Switching tests at | +125 |
| 11 | Switching tests at | -55 |
| 12 | Settling time at | +25 |
| 13 | Settling time at | +125 |
| 14 | Settling time at | -55 |

## LP2953A Electrical Characteristics DC Parameters

The following conditions apply, unless otherwise specified. $V_I$ = 6V, $I_L$ = 1mA, $C_L$ = 2.2µF, $V_O$ = 5V
Feedback pin is tied to 5V Tap pin. Output pin is tied to Output Sense Pin.

| Parameter | | Test Conditions | Notes | Min | Max | Units | Sub-groups |
|---|---|---|---|---|---|---|---|
| $V_O$ | Output Voltage | | | 4.975 | 5.025 | V | 1 |
| | | | | 4.94 | 5.06 | V | 2, 3 |
| | | 1mA ≤ $I_L$ ≤ 250mA | | 4.93 | 5.07 | V | 1, 2, 3 |
| $\Delta V_O / V_O$ | Output Voltage Line Regulation | $V_I$ = 6V to 30V | | | 0.1 | % | 1 |
| | | | | | 0.2 | % | 2, 3 |
| $\Delta V_O / V_O$ | Output Voltage Load Regulation | $I_L$ = 1mA to 250mA | | | 0.16 | % | 1 |
| | | | | | 0.2 | % | 2, 3 |
| | | $I_L$ = 0.1mA to 1mA | | | 0.16 | % | 1 |
| | | | | | 0.2 | % | 2, 3 |
| $V_I - V_O$ | Dropout Voltage | $I_L$ = 1mA | See (1) | | 100 | mV | 1 |
| | | | | | 150 | mV | 2, 3 |
| | | $I_L$ = 50mA | See (1) | | 300 | mV | 1 |
| | | | | | 420 | mV | 2, 3 |
| | | $I_L$ = 100mA | See (1) | | 400 | mV | 1 |
| | | | | | 520 | mV | 2, 3 |
| | | $I_L$ = 250mA | See (1) | | 600 | mV | 1 |
| | | | | | 800 | mV | 2, 3 |

(1) Dropout voltage is defined as the input to output differential at which the output voltage drops 100 mV below the value measured with a 1V differential. At very low values of programmed output voltage, the input voltage minimum of 2V (2.3V over temperature) must be observed.

## LP2953A Electrical Characteristics DC Parameters (continued)

The following conditions apply, unless otherwise specified. $V_I$ = 6V, $I_L$ = 1mA, $C_L$ = 2.2µF, $V_O$ = 5V
Feedback pin is tied to 5V Tap pin. Output pin is tied to Output Sense Pin.

| Parameter | | Test Conditions | Notes | Min | Max | Units | Sub-groups |
|---|---|---|---|---|---|---|---|
| $I_{Gnd}$ | Ground Pin Current | $I_L$ = 1mA | See (2) | | 170 | µA | 1 |
| | | | | | 200 | µA | 2, 3 |
| | | $I_L$ = 50mA | See (2) | | 2.0 | mA | 1 |
| | | | | | 2.5 | mA | 2, 3 |
| | | $I_L$ = 100mA | See (2) | | 6.0 | mA | 1 |
| | | | | | 8.0 | mA | 2, 3 |
| | | $I_L$ = 250mA | See (2) | | 28 | mA | 1 |
| | | | | | 33 | mA | 2, 3 |
| $I_{Gnd}$ | Ground Pin Current at Dropout | $V_I$ = 4.5V, $I_L$ = 100µA | See (2) | | 210 | µA | 1 |
| | | | | | 240 | µA | 2, 3 |
| $I_{Gnd}$ | Ground Pin Current at Shutdown | | See (2) (3) | | 140 | µA | 1 |
| $I_{Limit}$ | Current Limit | $V_O$ = 0V | | | 500 | mA | 1 |
| | | | | | 530 | mA | 2, 3 |
| $\Delta V_O / \Delta P_D$ | Thermal Regulation | | See (4) | | 0.2 | %/W | 1 |
| $V_{Ref}$ | Reference Voltage | | See (5) | 1.215 | 1.245 | V | 1 |
| | | | | 1.205 | 1.255 | V | 2, 3 |
| $\Delta V_{Ref} / V_{Ref}$ | Reference Voltage Line Regulation | $V_I$ = 2.5V to 6V | | | 0.1 | % | 1 |
| | | | | | 0.2 | % | 2, 3 |
| | | $V_I$ = 6V to 30V | | | 0.1 | % | 1 |
| | | | | | 0.2 | % | 2, 3 |
| $\Delta V_{Ref} / V_{Ref}$ | Reference Voltage Load Regulation | $I_{Ref}$ = 0 to 200µA | | | 0.4 | % | 1 |
| | | | | | 0.6 | % | 2, 3 |
| $I_{B\ FB}$ | Feedback Pin Bias Current | | | | 40 | nA | 1 |
| | | | | | 60 | nA | 2, 3 |
| $I_{O\ Sink}$ | Output "Off" Pulldown Current | | See (6) | 30 | | mA | 1 |
| | | | | 20 | | mA | 2, 3 |

(2) Ground pin current is the regulator quiescent current. The total current drawn from the source is the sum of the ground pin current, output load current, and current through the external resistive divider (if used).
(3) $V_{Shutdown} \leq 1.1V$, $V_O = V_O(Nom)$.
(4) Thermal regulation is the change in output voltage at a time T after a change in power dissipation, excluding load or line regulation effects. Specifications are for a 200 mA load pulse at $V_I = V_O(Nom)+15V$ (3W pulse) for T = 10 mS.
(5) $V_{Ref} \leq V_O \leq (V_I - 1V)$, $2.3V \leq V_I \leq 30V$, $100\ \mu A \leq I_L \leq 250$ mA.
(6) $V_{Shutdown} \leq 1.1V$, $V_O = V_O(Nom)$.

## LP2953A Electrical Characteristics Dropout Detection Comparator Parameters

The following conditions apply, unless otherwise specified. $V_I$ = 6V, $I_L$ = 1mA, $C_L$ = 2.2µF, $V_O$ = 5V
Feedback pin is tied to 5V Tap pin. Output pin is tied to Output Sense Pin.

| Parameter | | Test Conditions | Notes | Min | Max | Units | Sub-groups |
|---|---|---|---|---|---|---|---|
| $I_{OH}$ | Output "High" Leakage | $V_{OH}$ = 30V | | | 1.0 | µA | 1 |
| | | | | | 2.0 | µA | 2, 3 |
| $V_{OL}$ | Output "Low" Voltage | $V_I$ = 4V, $I_O$ Comp = 400µA | | | 250 | mV | 1 |
| | | | | | 400 | mV | 2, 3 |
| $V_{Th\ Max}$ | Upper Threshold Voltage | | See (1) | -320 | -150 | mV | 1 |
| | | | | -380 | -130 | mV | 2 |
| | | | | -380 | -120 | mV | 3 |
| $V_{Th\ Min}$ | Lower Threshold Voltage | | See (1) | -450 | -280 | mV | 1 |
| | | | | -640 | -180 | mV | 2 |
| | | | | -640 | -155 | mV | 3 |

(1) Comparator thresholds are expressed in terms of a voltage differential at the Feedback terminal below the nominal $V_{Ref}$ measured at $V_I$ = $V_O$(Nom) + 1V. To express these thresholds in terms of output voltage change, multiply by the Error amplifier gain, which is $V_O$/ $V_{Ref}$ = (R1 + R2)/R2 (refer to Figure 31).

## LP2953A Electrical Characteristics $\overline{\text{SHUTDOWN}}$ Input Parameters

The following conditions apply, unless otherwise specified. $V_I$ = 6V, $I_L$ = 1mA, $C_L$ = 2.2µF, $V_O$ = 5V
Feedback pin is tied to 5V Tap pin. Output pin is tied to Output Sense Pin.

| Parameter | | Test Conditions | Notes | Min | Max | Units | Sub-groups |
|---|---|---|---|---|---|---|---|
| $V_{IO}$ | Input Offset Voltage | Referred to $V_{Ref}$ | | -7.5 | 7.5 | mV | 1 |
| | | | | -10 | 10 | mV | 2 |
| | | | | -12 | 12 | mV | 3 |
| $I_{IB}$ | Input Bias Current | $V_I$ Comp = 0 to 5V | | -30 | 30 | nA | 1 |
| | | | | -50 | 50 | nA | 2 |
| | | | | -75 | 75 | nA | 3 |

## LP2953A Electrical Characteristics Auxillary Comparator Parameters

The following conditions apply, unless otherwise specified. $V_I$ = 6V, $I_L$ = 1mA, $C_L$ = 2.2µF, $V_O$ = 5V
Feedback pin is tied to 5V Tap pin. Output pin is tied to Output Sense Pin.

| Parameter | | Test Conditions | Notes | Min | Max | Units | Sub-groups |
|---|---|---|---|---|---|---|---|
| $V_{IO}$ | Input Offset Voltage | Referred to $V_{Ref}$ | | -7.5 | 7.5 | mV | 1 |
| | | | | -10 | 10 | mV | 2 |
| | | | | -12 | 12 | mV | 3 |
| $I_{IB}$ | Input Bias Current | $V_I$ Comp = 0 to 5V | | -30 | 30 | nA | 1 |
| | | | | -50 | 50 | nA | 2 |
| | | | | -75 | 75 | nA | 3 |
| $I_{OH}$ | Output "High" Leakage | $V_{OH}$ = 30V, $V_I$ Comp = 1.3V | | | 1.0 | µA | 1 |
| | | | | | 2.0 | µA | 2 |
| | | | | | 2.2 | µA | 3 |
| $V_{OL}$ | Output "Low" Voltage | $V_I$ Comp = 1.1V, $I_O$ Comp = 400µA | | | 250 | mV | 1 |
| | | | | | 400 | mV | 2 |
| | | | | | 420 | mV | 3 |

## LP2953A Electrical Characteristics DC Drift Parameters

The following conditions apply, unless otherwise specified. $V_I$ = 6V, $I_L$ = 1mA, $C_L$ = 2.2µF, $V_O$ = 5V
Feedback pin is tied to 5V Tap pin. Output pin is tied to Output Sense Pin.
Δcalculations performed on QMLV devices at group B , subgroup 5.

| Parameter | | Test Conditions | Notes | Min | Max | Units | Sub-groups |
|---|---|---|---|---|---|---|---|
| $V_I$ - $V_O$ | Dropout Voltage | $I_L$ = 1mA | | -12 | 12 | % | 1 |
| | | $I_L$ = 50mA | | -12 | 12 | % | 1 |
| | | $I_L$ = 100mA | | -12 | 12 | % | 1 |
| | | $I_L$ = 250mA | | -12 | 12 | % | 1 |
| $I_{Gnd}$ | Ground Pin Current | $I_L$ = 1mA, ±5µA or ±10% whichever is greater | | -5.0 | 5.0 | µA | 1 |
| | | $I_L$ = 50mA, ±5µA or ±10% whichever is greater | | -5.0 | 5.0 | µA | 1 |
| | | $I_L$ = 100mA, ±5µA or ±10% whichever is greater | | -5.0 | 5.0 | µA | 1 |
| | | $I_L$ = 250mA, ±5µA or ±10% whichever is greater | | -5.0 | 5.0 | µA | 1 |
| $I_{Gnd}$ | Ground Pin Current at Dropout | $V_I$ = 4.5V, $I_L$ = 100µA, ±5µA or ±10% whichever is greater | | -5.0 | 5.0 | µA | 1 |
| $I_{Gnd}$ | Ground Pin Current at Shutdown | ±5µA or ±10% whichever is greater | | -5.0 | 5.0 | µA | 1 |
| $V_{IO}$ | Input Offset Voltage | Referred to $V_{Ref}$ $\overline{\text{SHUTDOWN}}$ Input | | -1.0 | 1.0 | mV | 1 |
| | | Referred to $V_{Ref}$ Auxillary Comparator | | -1.0 | 1.0 | mV | 1 |
| $I_{IB}$ | Input Bias Current | $V_I$ Comp = 0 to 5V $\overline{\text{SHUTDOWN}}$ Input | | -5.0 | 5.0 | nA | 1 |
| | | $V_I$ Comp = 0 to 5V Auxillary Comparator | | -5.0 | 5.0 | nA | 1 |

## Typical Performance Characteristics

Unless otherwise specified: $V_I$ = 6V, $I_L$ = 1 mA, $C_L$ = 2.2 μF, $V_{SD}$ = 3V, $T_A$ = 25°C, $V_O$ = 5V.

**Quiescent Current**

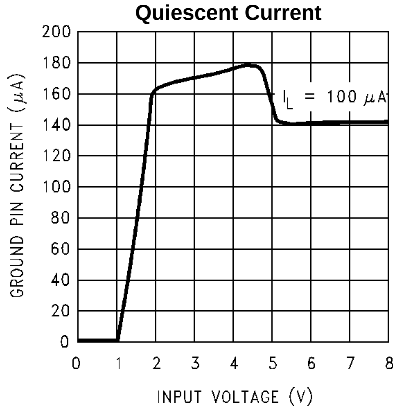



**Figure 3.**

**Quiescent Current**

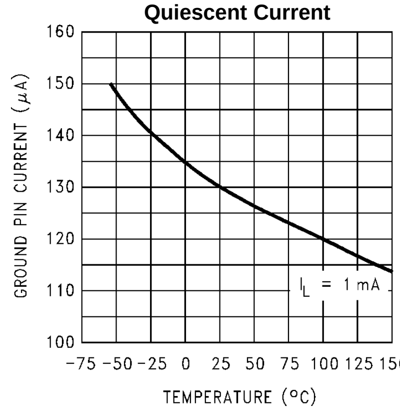



**Figure 4.**

**Ground Pin Current vs Load**

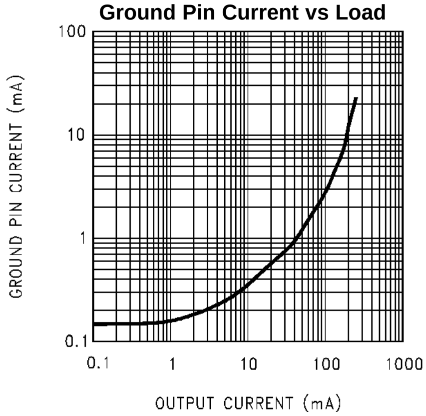



**Figure 5.**

**Ground Pin Current**

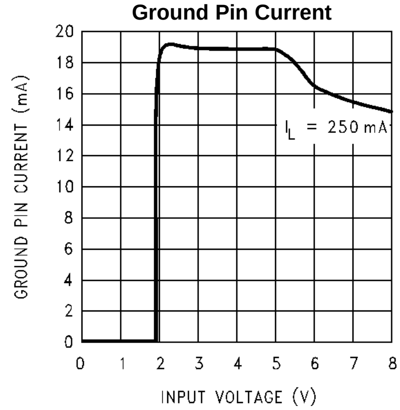



**Figure 6.**

**Ground Pin Current**

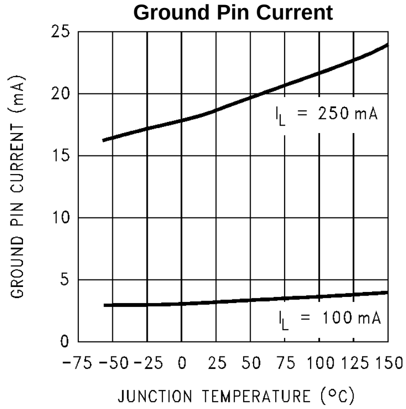



**Figure 7.**

**Output Noise Voltage**

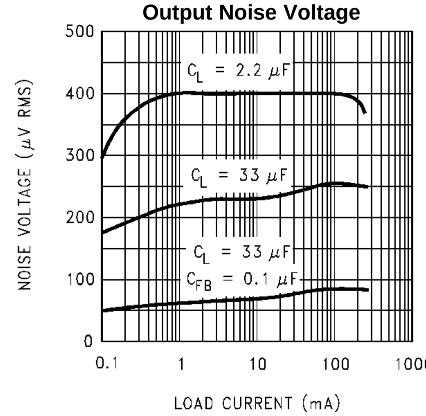



**Figure 8.**

## Typical Performance Characteristics (continued)

Unless otherwise specified: $V_I$ = 6V, $I_L$ = 1 mA, $C_L$ = 2.2 µF, $V_{SD}$ = 3V, $T_A$ = 25°C, $V_O$ = 5V.

**Ripple Rejection**

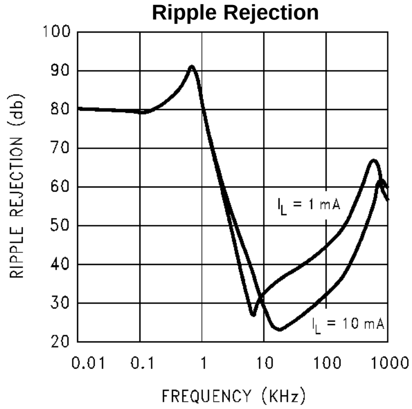



**Figure 9.**

**Ripple Rejection**

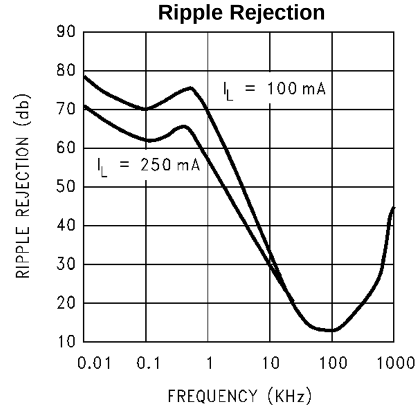



**Figure 10.**

**Ripple Rejection**

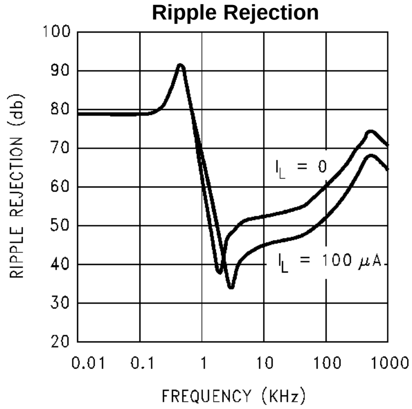



**Figure 11.**

**Line Transient Response**

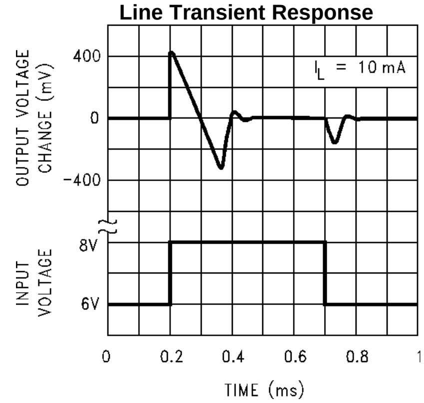



**Figure 12.**

**Line Transient Response**

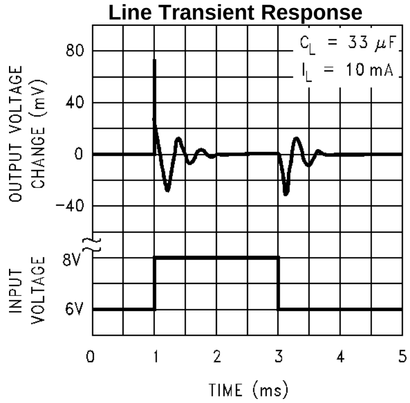



**Figure 13.**

**Output Impedance**

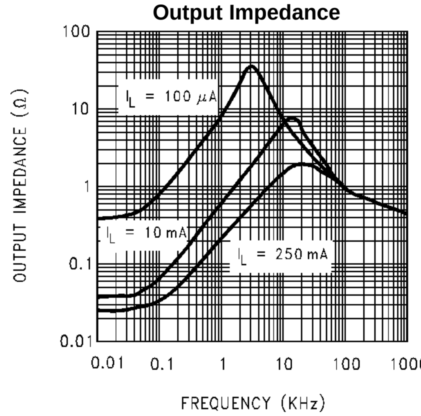



**Figure 14.**

## Typical Performance Characteristics (continued)

Unless otherwise specified: $V_I$ = 6V, $I_L$ = 1 mA, $C_L$ = 2.2 µF, $V_{SD}$ = 3V, $T_A$ = 25°C, $V_O$ = 5V.

**Load Transient Response**

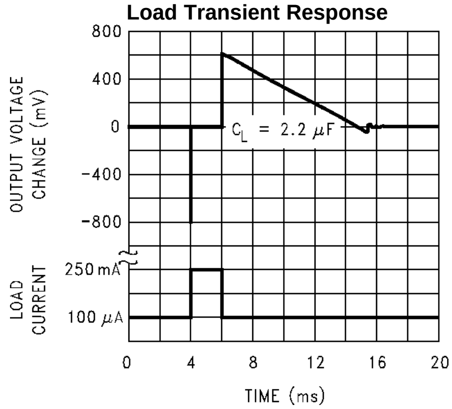



**Figure 15.**

**Load Transient Response**

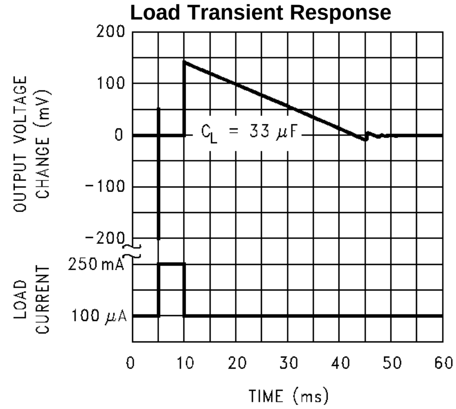



**Figure 16.**

**Dropout Characteristics**

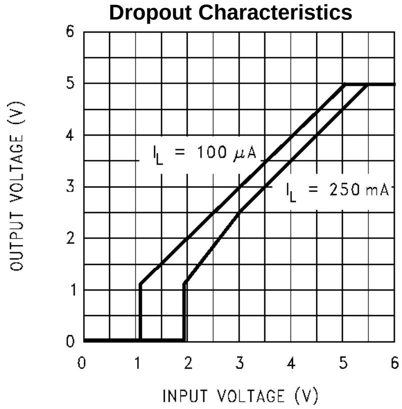



**Figure 17.**

**Enable Transient**

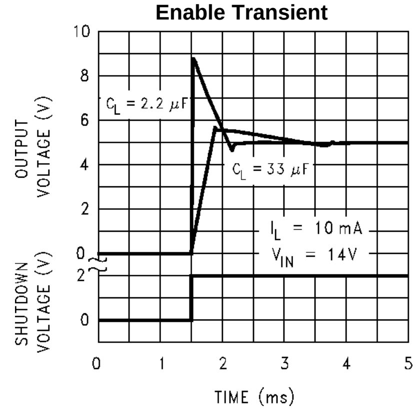



**Figure 18.**

**Enable Transient**

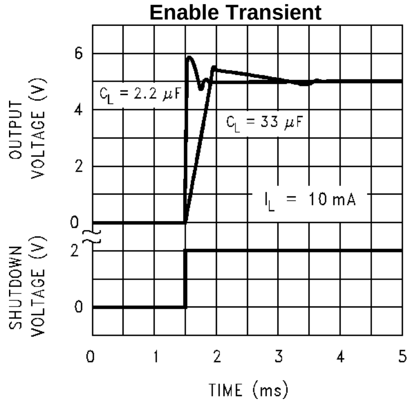



**Figure 19.**

**Short-Circuit Output Current and Maximum Output Current**

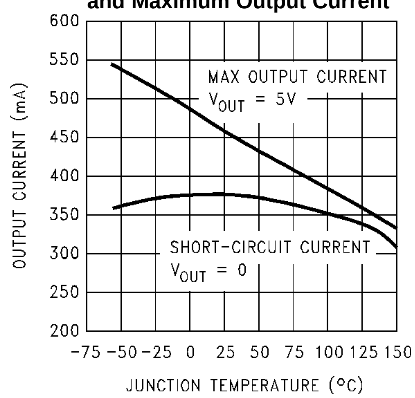



**Figure 20.**

## Typical Performance Characteristics (continued)

Unless otherwise specified: $V_I$ = 6V, $I_L$ = 1 mA, $C_L$ = 2.2 µF, $V_{SD}$ = 3V, $T_A$ = 25°C, $V_O$ = 5V.

**Feedback Bias Current**

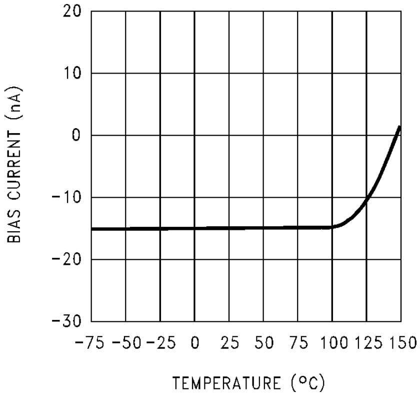



**Figure 21.**

**Feedback Pin Current**

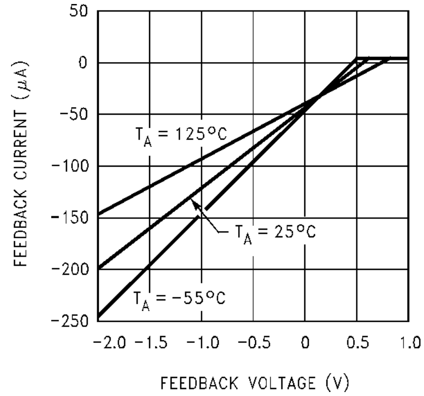



**Figure 22.**

**Error Output**

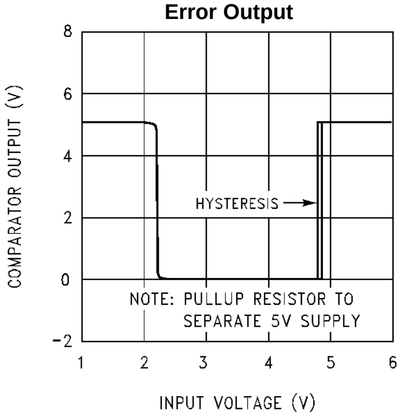



**Figure 23.**

**Comparator Sink Current**

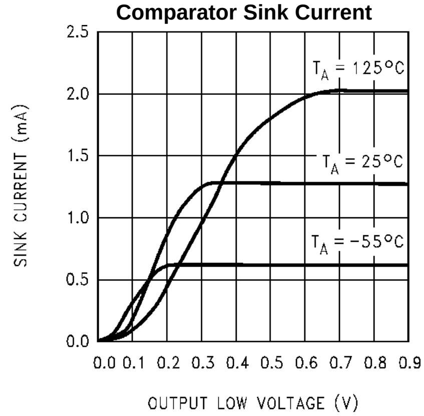



**Figure 24.**

**Divider Resistance**

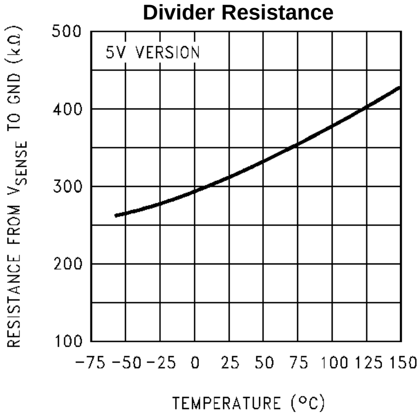



**Figure 25.**

**Dropout Detection Comparator Threshold Voltages**

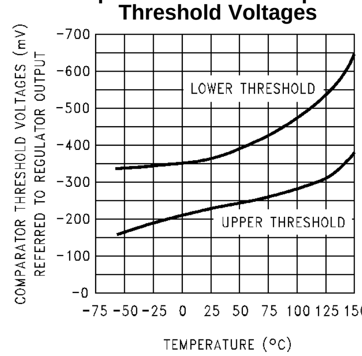



**Figure 26.**

## Typical Performance Characteristics (continued)

Unless otherwise specified: $V_I$ = 6V, $I_L$ = 1 mA, $C_L$ = 2.2 µF, $V_{SD}$ = 3V, $T_A$ = 25°C, $V_O$ = 5V.

**Thermal Regulation**

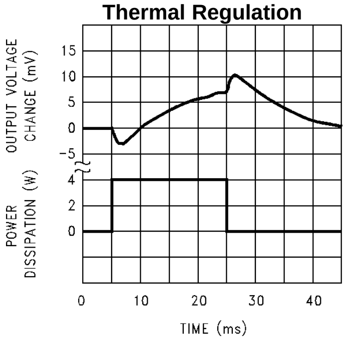



**Figure 27.**

**Minimum Operating Voltage**

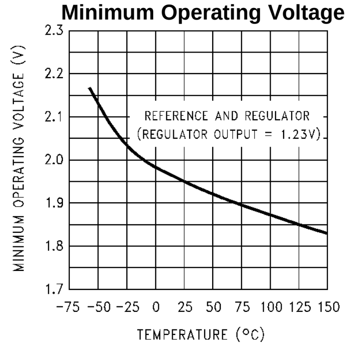



**Figure 28.**

**Dropout Voltage**

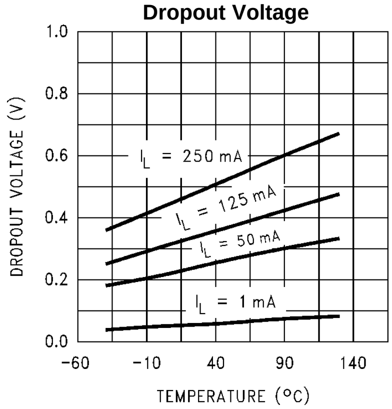



**Figure 29.**

# APPLICATION HINTS

## Ground Pins

For the LP2953 16–Pin Ceramic SOIC, Pins 1, 8, 9, 16 MUST BE SHORTED TOGETHER ON CUSTOMER'S P.C. BOARD APPLICATION.

## Heatsink Requirements

The maximum allowable power dissipation for the LP2953 is limited by the maximum junction temperature (+150°C) and the two parameters that determine how quickly heat flows away from the die: *the ambient temperature and the junction-to-ambient thermal resistance of the part*.

The military parts which are manufactured in ceramic DIP packages contain a KOVAR lead frame (unlike the industrial parts, which have a copper lead frame). The KOVAR material is necessary to attain the hermetic seal required in military applications.

The KOVAR lead frame does not conduct heat as well as copper, which means that the PC board copper can not be used to significantly reduce the overall junction-to-ambient thermal resistance.

The power dissipation calculations are done using a fixed value for $\theta_{(J-A)}$, the junction-to-ambient thermal resistance, of 134°C/W and can not be changed by adding copper foil patterns to the PC board. This leads to an important fact: The *maximum allowable power dissipation in any application using the LP2953 is dependent only on the ambient temperature:*

$$P(max) = T_{R(max)} / \theta_{(J-A)}$$

$$P(max) = \frac{T_{J(max)} - T_{A(max)}}{\theta_{(J-A)}}$$

$$P(max) = \frac{150 - T_{A(max)}}{95} \quad (1)$$

## External Capacitors

A 2.2 µF (or greater) capacitor is required between the output pin and ground to assure stability when the output is set to 5V. Without this capacitor, the part will oscillate. Most type of tantalum or aluminum electrolytics will work here. Film types will work, but are more expensive. Many aluminum electrolytics contain electrolytes which freeze at −30°C, which requires the use of solid tantalums below −25°C. The important parameters of the capacitor are an ESR of about 5Ω or less and a resonant frequency above 500 kHz (the ESR may increase by a factor of **20** or **30** as the temperature is reduced from 25°C to −30°C). The value of this capacitor may be increased without limit.

At lower values of output current, less output capacitance is required for stability. The capacitor can be reduced to 0.68 µF for currents below 10 mA or 0.22 µF for currents below 1 mA.

Programming the output for voltages below 5V runs the error amplifier at lower gains requiring *more* output capacitance for stability. At 3.3V output, a minimum of 4.7 µF is required. For the worst-case condition of 1.23V output and 250 mA of load current, a 6.8 µF (or larger) capacitor should be used.

A 1 µF capacitor should be placed from the input pin to ground if there is more than 10 inches of wire between the input and the AC filter capacitor or if a battery input is used.

Stray capacitance to the Feedback terminal can cause instability. This problem is most likely to appear when using high value external resistors to set the output voltage. Adding a 100 pF capacitor between the Output and Feedback pins and increasing the output capacitance to 6.8 µF (or greater) will cure the problem.

## Minimum Load

When setting the output voltage using an external resistive divider, a minimum current of 1 µA is recommended through the resistors to provide a minimum load.

It should be noted that a minimum load current is specified in several of the electrical characteristic test conditions, so this value must be used to obtain correlation on these tested limits.

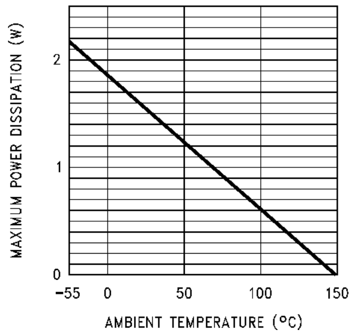



**Figure 30. Power Derating Curve for LP2953**

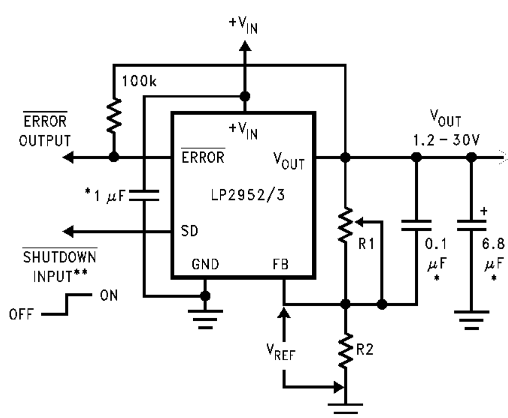
## Programming the Output Voltage

The regulator may be pin-strapped for 5V operation using its internal resistive divider by tying the Output and Sense pins together and also tying the Feedback and 5V Tap pins together.

Alternatively, it may be programmed for any voltage between the 1.23V reference and the 30V maximum rating using an external pair of resistors (see Figure 31). The complete equation for the output voltage is:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right) + (I_{FB} \times R1) \tag{2}$$

where $V_{REF}$ is the 1.23V reference and $I_{FB}$ is the Feedback pin bias current (−20 nA typical). The minimum recommended load current of 1 μA sets an upper limit of 1.2 MΩ on the value of R2 in cases where the regulator must work with no load (see Minimum Load). $I_{FB}$ will produce a typical 2% error in $V_O$ which can be eliminated at room temperature by trimming R1. For better accuracy, choosing R2 = 100 kΩ will reduce this error to 0.17% while increasing the resistor program current to 12 μA. Since the typical quiescent current is 120 μA, this added current is negligible.




* See Application Hints
** Drive with TTL-low to shut down

**Figure 31. Adjustable Regulator**

## Dropout Voltage

The dropout voltage of the regulator is defined as the minimum input-to-output voltage differential required for the output voltage to stay within 100 mV of the output voltage measured with a 1V differential. The dropout voltage is independent of the programmed output voltage.

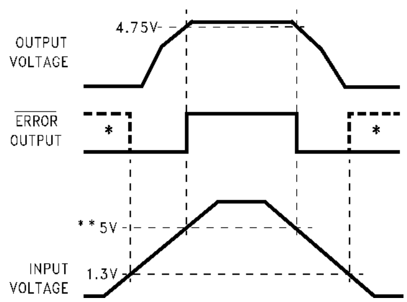
## Dropout Detection Comparator

This comparator produces a logic "LOW" whenever the output falls out of regulation by more than about 5%. This figure results from the comparator's built-in offset of 60 mV divided by the 1.23V reference (refer to Block Diagram). The 5% low trip level remains constant regardless of the programmed output voltage. An out-of-regulation condition can result from low input voltage, current limiting, or thermal limiting.

Figure 32 gives a timing diagram showing the relationship between the output voltage, the $\overline{\text{ERROR}}$ output, and input voltage as the input voltage is ramped up and down to a regulator programmed for 5V output. The $\overline{\text{ERROR}}$ signal becomes low at about 1.3V input. It goes high at about 5V input, where the output equals 4.75V. Since the dropout voltage is load dependent, the **input** voltage trip points will vary with load current. The **output** voltage trip point does not vary.

The comparator has an open-collector output which requires an external pull-up resistor. This resistor may be connected to the regulator output or some other supply voltage. Using the regulator output prevents an invalid "HIGH" on the comparator output which occurs if it is pulled up to an external voltage while the regulator input voltage is reduced below 1.3V. In selecting a value for the pull-up resistor, note that while the output can sink 400 µA, this current adds to battery drain. Suggested values range from 100 kΩ to 1 MΩ. This resistor is not required if the output is unused.

When $V_{IN} \leq 1.3V$, the error flag pin becomes a high impedance, allowing the error flag voltage to rise to its pull-up voltage. Using $V_{OUT}$ as the pull-up voltage (rather than an external 5V source) will keep the error flag voltage below 1.2V (typical) in this condition. The user may wish to divide down the error flag voltage using equal-value resistors (10 kΩ suggested) to ensure a low-level logic signal during any fault condition, while still allowing a valid high logic level during normal operation.




* In shutdown mode, $\overline{\text{ERROR}}$ will go high if it has been pulled up to an external supply. To avoid this invalid response, pull up to regulator output.
** Exact value depends on dropout voltage. (See Application Hints)

**Figure 32. $\overline{\text{ERROR}}$ Output Timing**

## Output Isolation

The regulator output can be left connected to an active voltage source (such as a battery) with the regulator input power shut off, **as long as the regulator ground pin is connected to ground.** If the ground pin is left floating, **damage to the regulator can occur** if the output is pulled up by an external voltage source.

## Reducing Output Noise

In reference applications it may be advantageous to reduce the AC noise present on the output. One method is to reduce regulator bandwidth by increasing output capacitance. This is relatively inefficient, since large increases in capacitance are required to get significant improvement.

Noise can be reduced more effectively by a bypass capacitor placed across R1 (refer to Figure 31). The formula for selecting the capacitor to be used is:

$$C_B = \frac{1}{2\pi \, R1 \times 20 \, Hz} \quad (3)$$

This gives a value of about 0.1 µF. When this is used, the output capacitor must be 6.8 µF (or greater) to maintain stability. The 0.1 µF capacitor reduces the high frequency gain of the circuit to unity, lowering the output noise from 260 µV to 80 µV using a 10 Hz to 100 kHz bandwidth. Also, noise is no longer proportional to the output voltage, so improvements are more pronounced at high output voltages.

## Auxiliary Comparator

The LP2953 contains an auxiliary comparator whose inverting input is connected to the 1.23V reference. The auxiliary comparator has an open-collector output whose electrical characteristics are similar to the dropout detection comparator. The non-inverting input and output are brought out for external connections.

## SHUTDOWN Input

A logic-level signal will shut off the regulator output when a "LOW" (<1.2V) is applied to the $\overline{\text{Shutdown}}$ input.

To prevent possible mis-operation, the $\overline{\text{Shutdown}}$ input must be actively terminated. If the input is driven from open-collector logic, a pull-up resistor (20 kΩ to 100 kΩ recommended) should be connected from the $\overline{\text{Shutdown}}$ input to the regulator input.

If the $\overline{\text{Shutdown}}$ input is driven from a source that actively pulls high and low (like an op-amp), the pull-up resistor is not required, but may be used.

If the shutdown function is not to be used, the cost of the pull-up resistor can be saved by simply tying the $\overline{\text{Shutdown}}$ input directly to the regulator input.

**IMPORTANT:** Since the Absolute Maximum Ratings state that the $\overline{\text{Shutdown}}$ input can not go more than 0.3V below ground, the reverse-battery protection feature which protects the regulator input is sacrificed if the $\overline{\text{Shutdown}}$ input is tied directly to the regulator input.

If reverse-battery protection is required in an application, *the pull-up resistor between the $\overline{\text{Shutdown}}$ input and the regulator input must be used.*

## Typical Applications

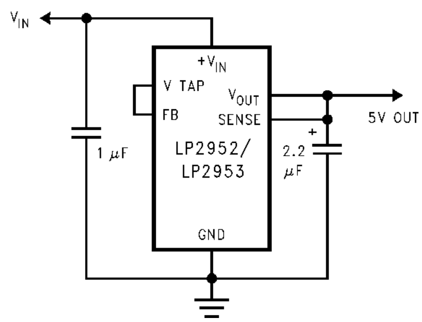
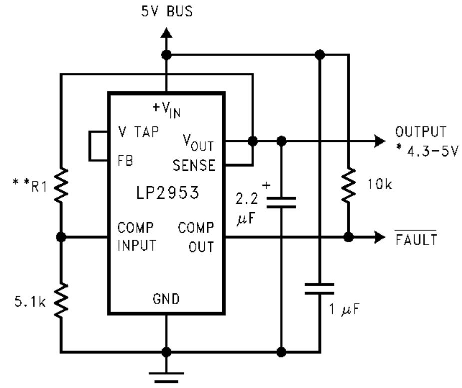



**Figure 33. Basic 5V Regulator**




* Output voltage equals $+V_{IN}$ minum dropout voltage, which varies with output current. Current limits at a maximum of 380 mA (typical).
** Select R1 so that the comparator input voltage is 1.23V at the output voltage which corresponds to the desired fault current value.

**Figure 34. 5V Current Limiter with Load Fault Indicator**

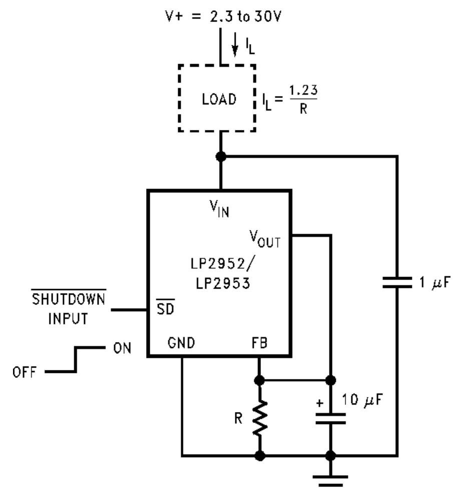
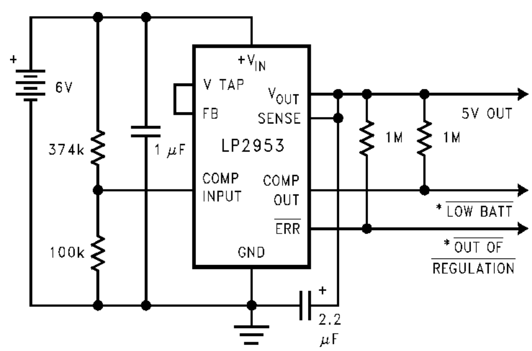
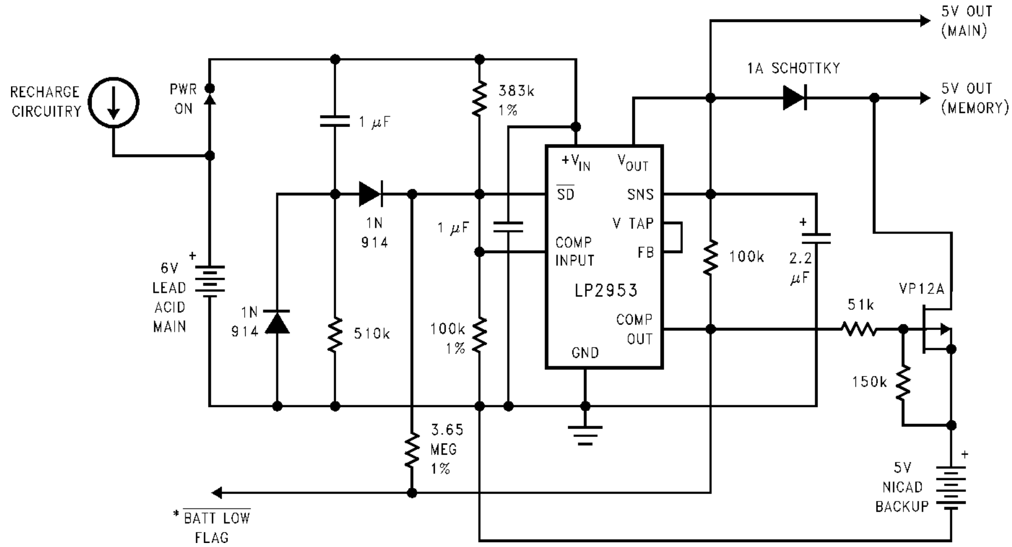



**Figure 35. Low T.C. Current Sink**




* Connect to Logic or µP control inputs.
LOW BATT flag warns the user that the battery has discharged down to about 5.8V, giving the user time to recharge the battery or power down some hardware with high power requirements. The output is still in regulation at this time.
OUT OF REGULATION flag indicates when the battery is almost completely discharged, and can be used to initiate a power-down sequence.

**Figure 36. 5V Regulator with Error Flags for LOW BATTERY and OUT OF REGULATION**




The circuit switches to the NI-CAD backup battery when the main battery voltage drops below about 5.6V, and returns to the main battery when its voltage is recharged to about 6V.

The 5V MAIN output powers circuitry which requires no backup, and the 5V MEMORY output powers critical circuitry which can not be allowed to lose power.

* The BATTERY LOW flag goes low whenever the circuit switches to the NI-CAD backup battery.

**Figure 37. 5V Battery Powered Supply with Backup and Low Battery Flag**

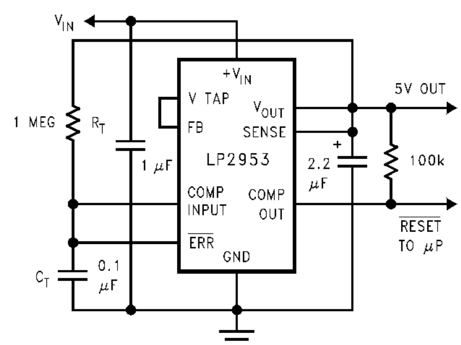
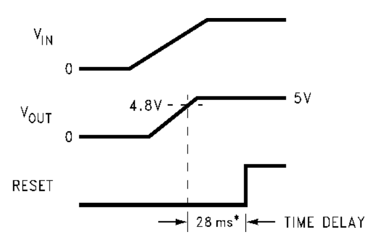
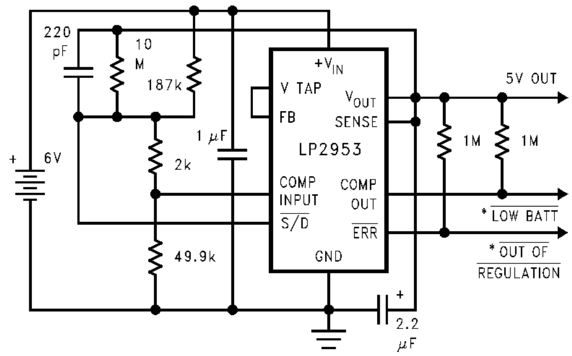



**Figure 38. 5V Regulator with Timed Power-On Reset**




* $R_T$ = 1 MEG, $C_T$ = 0.1 µF

**Figure 39. Timing Diagram for Timed Power-On Reset**




* Connect to Logic or µP control inputs.
OUTPUT has SNAP-ON/SNAP-OFF feature.
LOW BATT flag warns the user that the battery has discharged down to about 5.8V, giving the user time to recharge the battery or shut down hardware with high power requirements. The output is still in regulation at this time.
OUT OF REGULATION flag goes low if the output goes below about 4.7V, which could occur from a load fault.
OUTPUT has SNAP-ON/SNAP-OFF feature. Regulator snaps ON at about 5.7V input, and OFF at about 5.6V.

**Figure 40. 5V Regulator with Error Flags for LOW BATTERY and OUT OF REGULATION with SNAP-ON/SNAP-OFF Output**

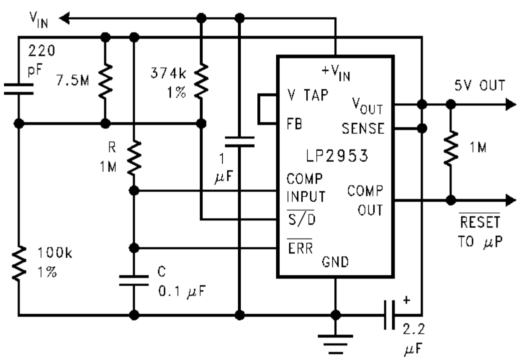
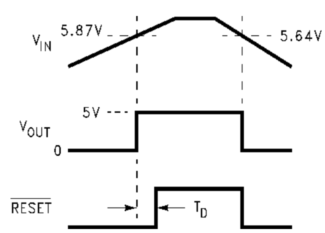



**Figure 41. 5V Regulator with Timed Power-On Reset, Snap-On/Snap-Off Feature and Hysteresis**




Td = (0.28) RC = 28 ms for components shown.

**Figure 42. Timing Diagram**

# REVISION HISTORY SECTION

| Released | Revision | Section | Changes |
|---|---|---|---|
| 11/30/2010 | A | New Release, Corporate format | 1 MDS data sheet converted into one Corp. data sheet format. MNLP2953AM-X Rev 1A1 will be archived. |
| 09/01/2011 | B | Ordering Information, Absolute Maximum Ratings | Ordering Information — entered new 'GW' devices. Absolute Maximum Ratings — added new Theta JA and Theta JC numbers. LP2953QML Rev A will be archived. |
| 09/20/2012 | C | Connection Diagrams, Application Notes | Connection Diagrams and Applications Notes : Added: * Pins 1, 8, 9, 16 MUST BE SHORTED TOGETHER ON CUSTOMER'S P.C. BOARD APPLICATION. Rev B will be archived. |

## REVISION HISTORY

| Changes from Revision B (April 2013) to Revision C | Page |
|---|---|
| • Changed layout of National Data Sheet to TI format | 17 |

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 5962-9233602QXA | ACTIVE | CFP | NAC | 16 | 42 | Non-RoHS & Green | Call TI | Level-1-NA-UNLIM | -55 to 125 | LP2953AMGW /883 Q 5962-92336 02QXA ACO 02QXA >T | Samples |
| 5962-9233602VXA | ACTIVE | CFP | NAC | 16 | 42 | Non-RoHS & Green | Call TI | Level-1-NA-UNLIM | -55 to 125 | LP2953AMGW- QMLV Q 5962-92336 02VXA ACO 02VXA >T | Samples |
| LP2953 MDS | ACTIVE | DIESALE | Y | 0 | 34 | RoHS & Green | Call TI | Level-1-NA-UNLIM | -55 to 125 | | Samples |
| LP2953AMGW-QMLV | ACTIVE | CFP | NAC | 16 | 42 | Non-RoHS & Green | Call TI | Level-1-NA-UNLIM | -55 to 125 | LP2953AMGW- QMLV Q 5962-92336 02VXA ACO 02VXA >T | Samples |
| LP2953AMGW/883 | ACTIVE | CFP | NAC | 16 | 42 | Non-RoHS & Green | Call TI | Level-1-NA-UNLIM | -55 to 125 | LP2953AMGW /883 Q 5962-92336 02QXA ACO 02QXA >T | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.



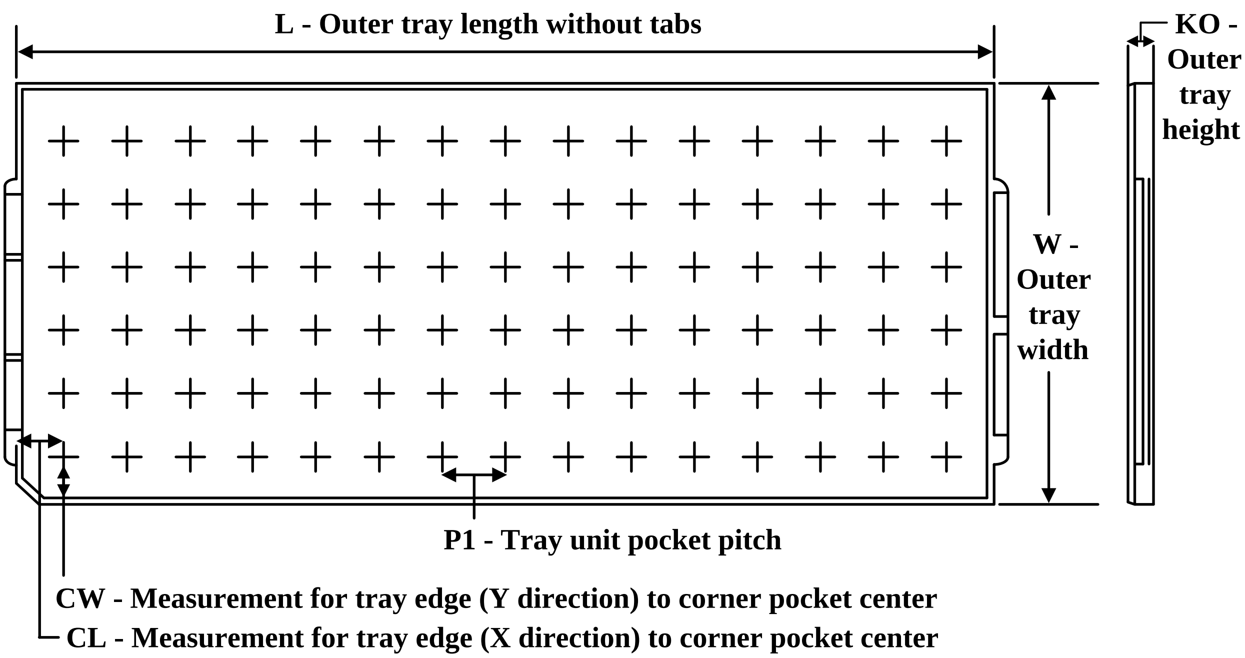
**OTHER QUALIFIED VERSIONS OF LP2953QML, LP2953QML-SP :**

- Military : LP2953QML
- Space : LP2953QML-SP

NOTE: Qualified Version Definitions:

- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

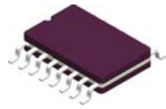
## TRAY




Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | Unit array matrix | Max temperature (°C) | L (mm) | W (mm) | K0 (µm) | P1 (mm) | CL (mm) | CW (mm) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 5962-9233602QXA | NAC | CFP | 16 | 42 | 7 X 6 | NA | 101.6 | 101.6 | 8001 | 2.84 | 15.24 | 15.24 |
| 5962-9233602VXA | NAC | CFP | 16 | 42 | 7 X 6 | NA | 101.6 | 101.6 | 8001 | 2.84 | 15.24 | 15.24 |
| LP2953AMGW-QMLV | NAC | CFP | 16 | 42 | 7 X 6 | NA | 101.6 | 101.6 | 8001 | 2.84 | 15.24 | 15.24 |
| LP2953AMGW/883 | NAC | CFP | 16 | 42 | 7 X 6 | NA | 101.6 | 101.6 | 8001 | 2.84 | 15.24 | 15.24 |

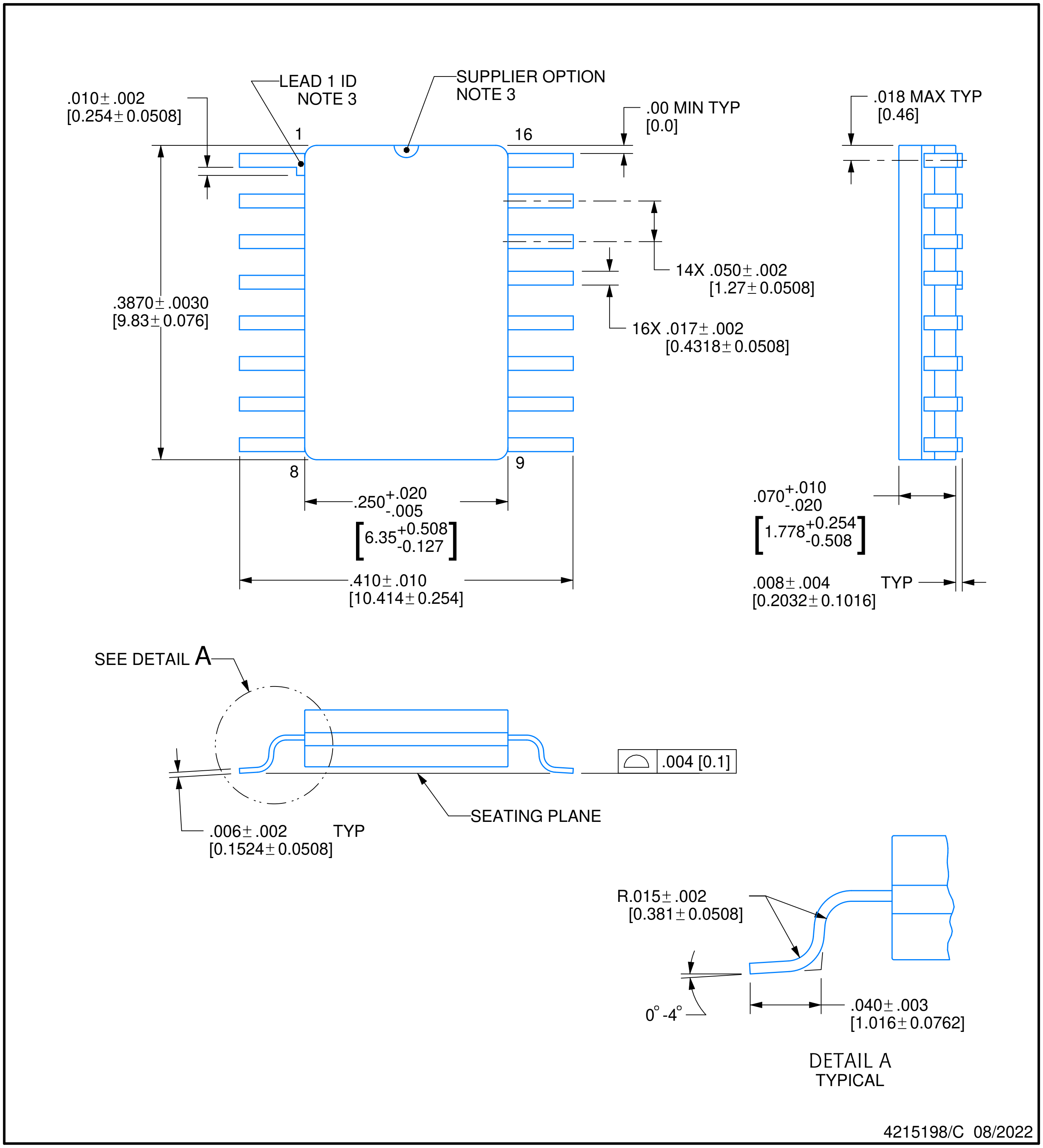


# PACKAGE OUTLINE

## NAC0016A

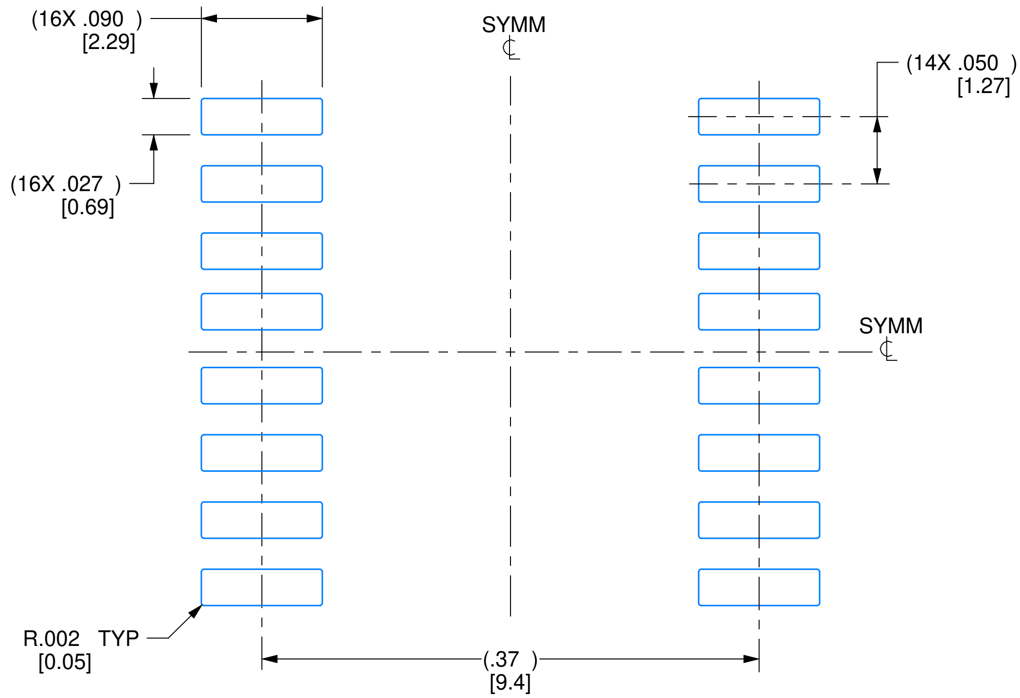
**CFP - 2.33mm max height**

CERAMIC FLATPACK

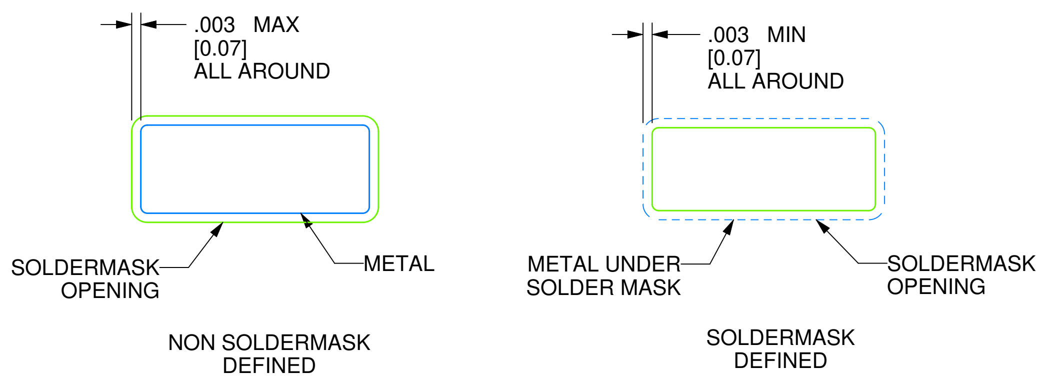



NOTES:

1. Controlling dimension is Inch. Values in [ ] are milimeters. Dimensions in ( ) for reference only.
2. For solder thickness and composition, see the "Lead Finish Composition/Thickness" link in the packaging section of the Texas Instruments website
3. Lead 1 identification shall be:
   a) A notch or other mark within this area
   b) A tab on lead 1, either side
4. No JEDEC registration as of December 2021




RECOMMENDED LAND PATTERN




4215198/C 08/2022

## REVISIONS

| REV | DESCRIPTION | E.C.N. | DATE | BY/APP'D |
|---|---|---|---|---|
| A | RELEASE TO DOCUMENT CONTROL | 2197879 | 12/30/2021 | TINA TRAN / ANIS FAUZI |
| B | NO CHANGE TO DRAWING; REVISION FOR YODA RELEASE; | 2198832 | 02/15/2022 | K. SINCERBOX |
| C | .387± .003 WAS .39000± .00012; | 2200917 | 08/08/2022 | D. CHIN / K. SINCERBOX |

| SCALE | SIZE | | REV | PAGE |
|---|---|---|---|---|
| | A | 4215198 | C | 4 OF 4 |