

September 1997 - Revised February 2004

High-Speed CMOS Logic Octal D-Type Flip-Flop With Data Enable

Features

- Buffered Common Clock
- Buffered Inputs
- Typical Propagation Delay at $C_L = 15\text{pF}$, $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$
 - 14 ns (HC Types)
 - 16 ns (HCT Types)
- Fanout (Over Temperature Range)
 - Standard Outputs 10 LSTTL Loads
 - Bus Driver Outputs 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
 - 2V to 6V Operation
 - High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} at $V_{CC} = 5\text{V}$
- HCT Types
 - 4.5V to 5.5V Operation
 - Direct LSTTL Input Logic Compatibility, $V_{IL} = 0.8\text{V}$ (Max), $V_{IH} = 2\text{V}$ (Min)
 - CMOS Input Compatibility, $I_I \leq 1\mu\text{A}$ at V_{OL} , V_{OH}

Description

The 'HC377 and 'HCT377 are octal D-type flip-flops with a buffered clock (CP) common to all eight flip-flops. All the flip-flops are loaded simultaneously on the positive edge of the clock (CP) when the Data Enable (\bar{E}) is Low.

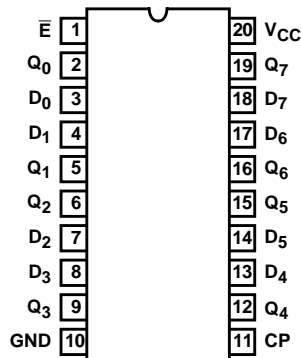
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54HC377F3A	-55 to 125	20 Ld CERDIP
CD54HCT377F3A	-55 to 125	20 Ld CERDIP
CD74HC377E	-55 to 125	20 Ld PDIP
CD74HC377M	-55 to 125	20 Ld SOIC
CD74HC377M96	-55 to 125	20 Ld SOIC
CD74HC377PW	-55 to 125	20 Ld TSSOP
CD74HC377PWR	-55 to 125	20 Ld TSSOP
CD74HCT377E	-55 to 125	20 Ld PDIP
CD74HCT377M	-55 to 125	20 Ld SOIC
CD74HCT377M96	-55 to 125	20 Ld SOIC

NOTE: When ordering, use the entire part number. The suffixes 96 and R denote tape and reel.

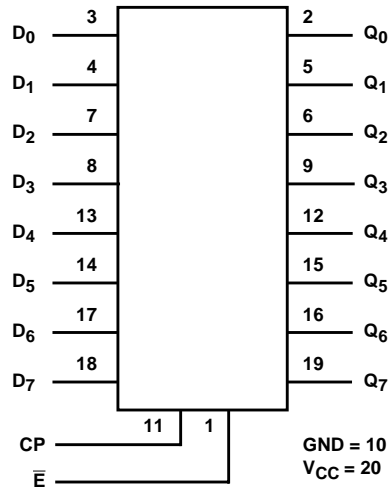
Pinout

CD54HC377, CD54HCT377
(CERDIP)
CD74HC377
(PDIP, SOIC, TSSOP)
CD74HCT377
(PDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

Functional Diagram

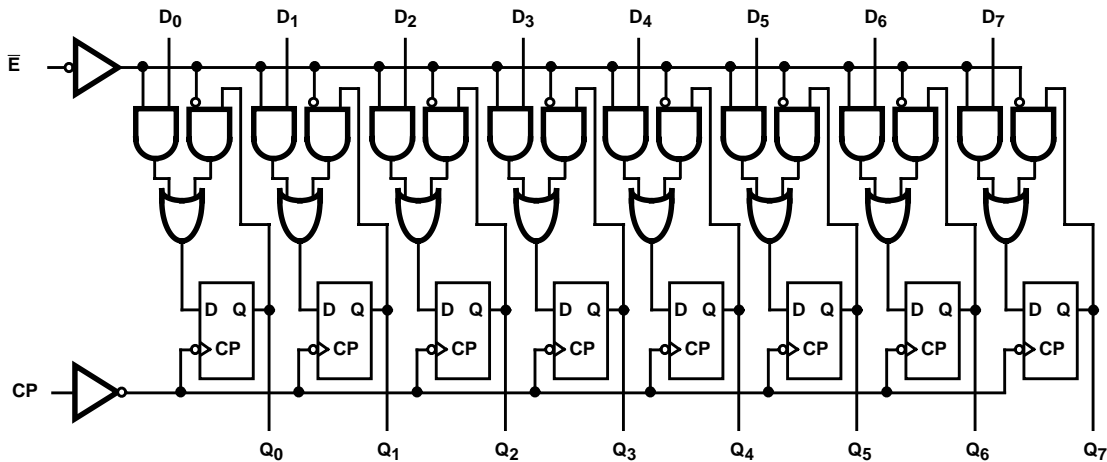


TRUTH TABLE

OPERATING MODE	INPUTS			OUTPUTS
	CP	\bar{E}	D_n	Q_n
Load "1"	↑	L	h	H
Load "0"	↑	L	L	L
Hold (Do Nothing)	↑	h	X	No Change
	X	H	X	No Change

H = High Voltage Level Steady State.
 h = High Voltage Level One Set-up Time Prior to the Low to High Clock Transition.
 L = Low Voltage Level Steady State.
 l = Low Voltage Level One Set-up Time Prior to the Low to High Clock Transition.
 X = Don't Care.
 ↑ = Low to High Clock Transition.

Logic Diagram



CD54HC377, CD74HC377, CD54HCT377, CD74HCT377

Absolute Maximum Ratings

DC Supply Voltage, V_{CC}	-0.5V to 7V
DC Input Diode Current, I_{IK}	
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$	$\pm 20mA$
DC Output Diode Current, I_{OK}	
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$	$\pm 20mA$
DC Output Source or Sink Current per Output Pin, I_O	
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$	$\pm 25mA$
DC V_{CC} or Ground Current, I_{CC} or I_{GND}	$\pm 50mA$

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^{\circ}C/W$)
E (PDIP) Package	69
M (SOIC) Package	58
PW (TSSOP) Package	83
Maximum Junction Temperature	150 $^{\circ}C$
Maximum Storage Temperature Range	-65 $^{\circ}C$ to 150 $^{\circ}C$
Maximum Lead Temperature (Soldering 10s)	300 $^{\circ}C$
(SOIC - Lead Tips Only)	

Operating Conditions

Temperature Range (T_A)	-55 $^{\circ}C$ to 125 $^{\circ}C$
Supply Voltage Range, V_{CC}	
HC Types2V to 6V
HCT Types	4.5V to 5.5V
DC Input or Output Voltage, V_I , V_O	0V to V_{CC}
Input Rise and Fall Time	
2V	1000ns (Max)
4.5V	500ns (Max)
6V	400ns (Max)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	25 $^{\circ}C$			-40 $^{\circ}C$ TO 85 $^{\circ}C$		-55 $^{\circ}C$ TO 125 $^{\circ}C$		UNITS
		V_I (V)	I_O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES												
High Level Input Voltage	V_{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V_{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads	V_{OH}	V_{IH} or V_{IL}	-	-	-	-	-	-	-	-	-	V
			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads	V_{OL}	V_{IH} or V_{IL}	-	-	-	-	-	-	-	-	-	V
			4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} or GND	-	6	-	-	± 0.1	-	± 1	-	± 1	∞A
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	6	-	-	8	-	80	-	160	∞A

CD54HC377, CD74HC377, CD54HCT377, CD74HCT377

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V _I (V)	I _O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HCT TYPES												
High Level Input Voltage	V _{IH}	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V _{IL}	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V _{OH}	V _{IH} or V _{IL}	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V _{OL}	V _{IH} or V _{IL}	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I _I	V _{CC} and GND	0	5.5	-	-	±0.1	-	±1	-	±1	∞A
Quiescent Device Current	I _{CC}	V _{CC} or GND	0	5.5	-	-	8	-	80	-	160	∞A
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI _{CC} (Note 2)	V _{CC} -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	∞A

NOTE:

- For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

INPUT	UNIT LOADS
\bar{E}	1.5
CP	0.5
All D _n Inputs	0.25

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Table, e.g., 360∞A max at 25°C.

Prerequisite for Switching Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
Maximum Clock Frequency	f _{MAX}	-	2	6	-	-	5	-	4	-	MHz
			4.5	30	-	-	25	-	20	-	MHz
			6	35	-	-	29	-	23	-	MHz
Clock Pulse Width	t _w	-	2	80	-	-	100	-	120	-	ns
			4.5	16	-	-	20	-	24	-	ns
			6	14	-	-	17	-	20	-	ns

CD54HC377, CD74HC377, CD54HCT377, CD74HCT377

Prerequisite for Switching Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Set-up Time, \bar{E} , Data to CP	t _{SU}	-	2	60	-	-	75	-	90	-	ns
			4.5	12	-	-	15	-	18	-	ns
			6	10	-	-	13	-	15	-	ns
Hold Time, Data to CP	t _H	-	2	3	-	-	3	-	3	-	ns
			4.5	3	-	-	3	-	3	-	ns
			6	3	-	-	3	-	3	-	ns
Hold Time, \bar{E} to CP	t _H	-	2	5	-	-	5	-	5	-	ns
			4.5	5	-	-	5	-	5	-	ns
			6	5	-	-	5	-	5	-	ns
HCT TYPES											
Maximum Clock Frequency	f _{MAX}	-	4.5	25	-	-	20	-	16	-	MHz
Clock Pulse Width	t _W	-	4.5	20	-	-	25	-	30	-	ns
Set-up, Time \bar{E} , Data to CP	t _{SU}	-	4.5	12	-	-	15	-	18	-	ns
Hold Time, Data to CP	t _H	-	4.5	3	-	-	3	-	3	-	ns
Hold Time, \bar{E} to CP	t _H	-	4.5	5	-	-	5	-	5	-	ns

Switching Specifications Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
Propagation Delay (Figure 1) CP to Q	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	-	175	-	220	-	265	ns
			4.5	-	-	35	-	44	-	53	ns
		C _L = 15pF	5	-	14	-	-	-	-	-	ns
		C _L = 50pF	6	-	-	30	-	37	-	45	ns
Output Transition Time (Figure 1)	t _{TLH} , t _{THL}	C _L = 50pF	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Input Capacitance	C _{IN}	C _L = 50pF	-	-	-	10	-	10	-	10	pF
Maximum Clock Frequency	f _{MAX}	C _L = 15pF	5	-	60	-	-	-	-	-	MHz
Power Dissipation Capacitance (Notes 3, 4)	C _{PD}	C _L = 15pF	5	-	31	-	-	-	-	-	pF
HCT TYPES											
Propagation Delay (Figure 1) CP to Q	t _{PLH} , t _{PHL}	C _L = 50pF	4.5	-	-	38	-	48	-	57	ns
		C _L = 15pF	5	-	16	-	-	-	-	-	ns
Output Transition Time (Figure 1)	t _{TLH} , t _{THL}	C _L = 50pF	4.5	-	-	15	-	19	-	22	ns
Input Capacitance	C _{IN}	C _L = 50pF	-	-	-	10	-	10	-	10	pF

CD54HC377, CD74HC377, CD54HCT377, CD74HCT377

Switching Specifications Input t_r , $t_f = 6\text{ns}$ (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Maximum Clock Frequency	f_{MAX}	$C_L = 15\text{pF}$	5	-	50	-	-	-	-	-	MHz
Power Dissipation Capacitance (Notes 3, 4)	C_{PD}	$C_L = 15\text{pF}$	5	-	35	-	-	-	-	-	pF

NOTES:

3. C_{PD} is used to determine the dynamic power consumption, per flip-flop.
4. $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = Input Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

Test Circuits and Waveforms

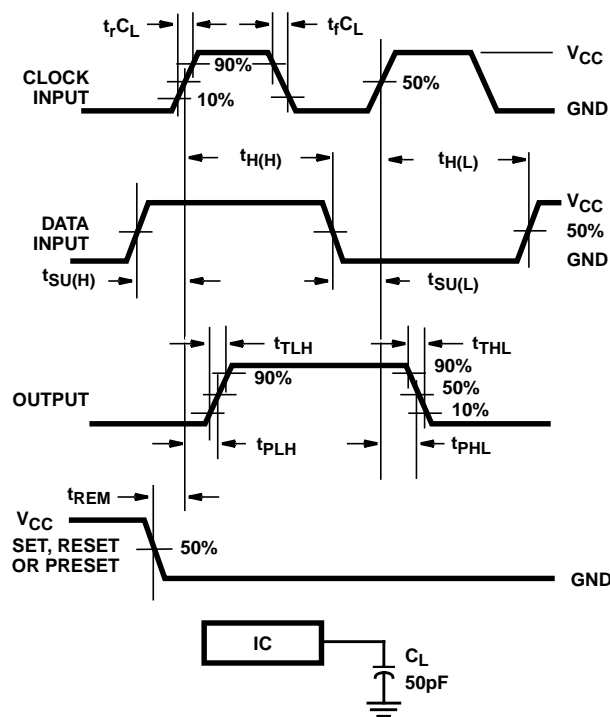


FIGURE 1. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

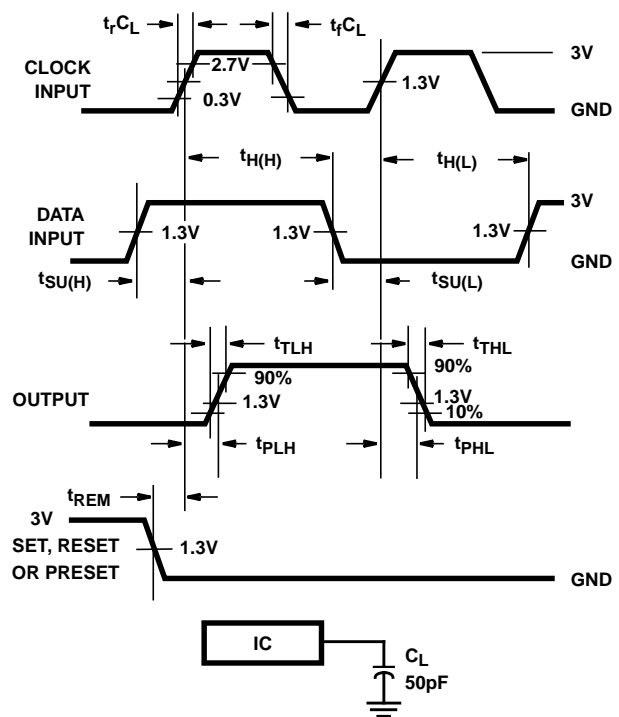


FIGURE 2. HCT SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8976901RA	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-8976901RA CD54HCT377F3A	Samples
CD54HC377F3A	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-8780701RA CD54HC377F3A	Samples
CD54HCT377F3A	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-8976901RA CD54HCT377F3A	Samples
CD74HC377E	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC377E	Samples
CD74HC377M	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC377M	Samples
CD74HC377M96	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC377M	Samples
CD74HC377PW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ377	Samples
CD74HC377PWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ377	Samples
CD74HC377PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ377	Samples
CD74HC377PWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ377	Samples
CD74HCT377E	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT377E	Samples
CD74HCT377EE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT377E	Samples
CD74HCT377M	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT377M	Samples
CD74HCT377M96	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT377M	Samples
CD74HCT377ME4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT377M	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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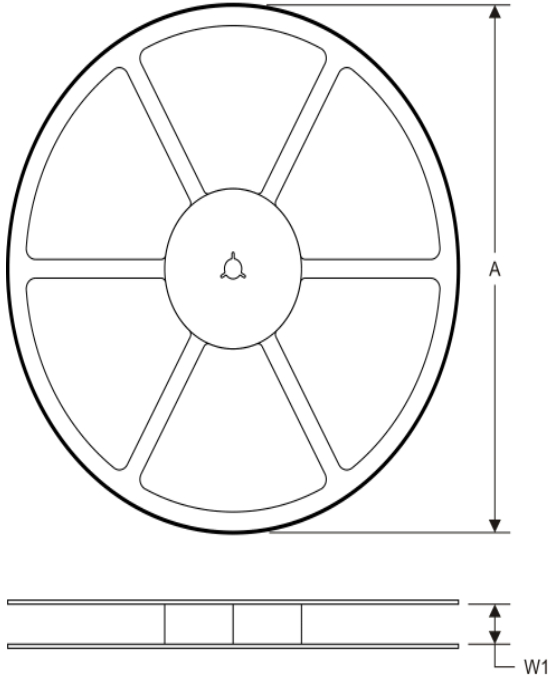
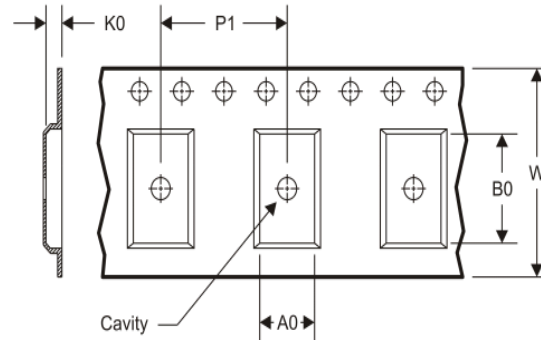
OTHER QUALIFIED VERSIONS OF CD54HC377, CD54HCT377, CD74HC377, CD74HCT377 :

● Catalog: [CD74HC377](#), [CD74HCT377](#)

● Military: [CD54HC377](#), [CD54HCT377](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC377M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
CD74HC377PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
CD74HCT377M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

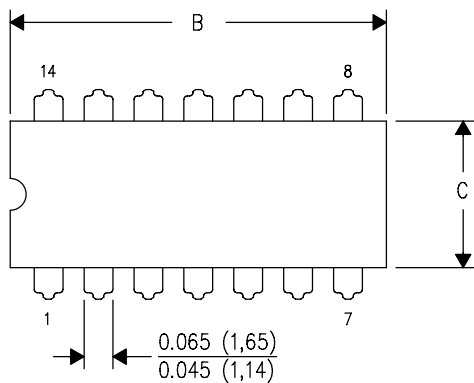

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC377M96	SOIC	DW	20	2000	367.0	367.0	45.0
CD74HC377PWR	TSSOP	PW	20	2000	367.0	367.0	38.0
CD74HCT377M96	SOIC	DW	20	2000	367.0	367.0	45.0

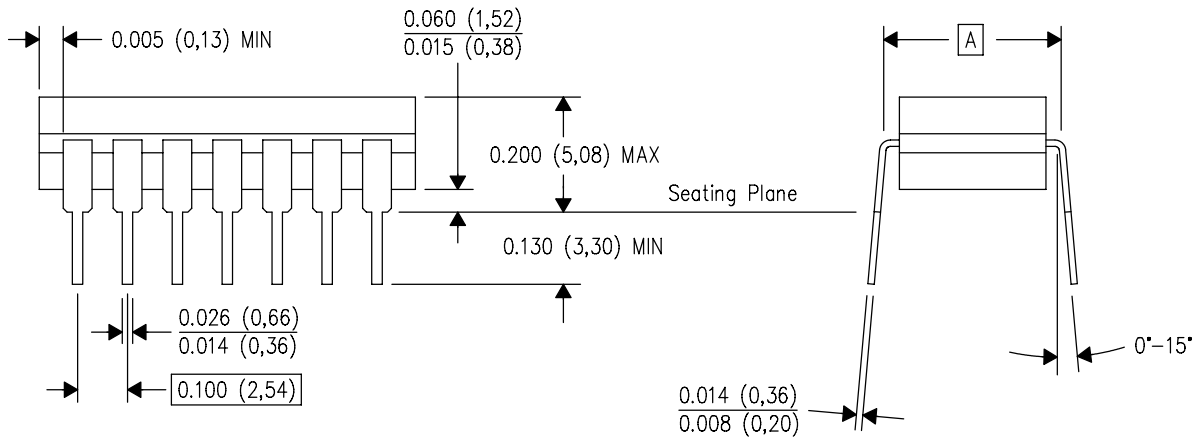
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14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

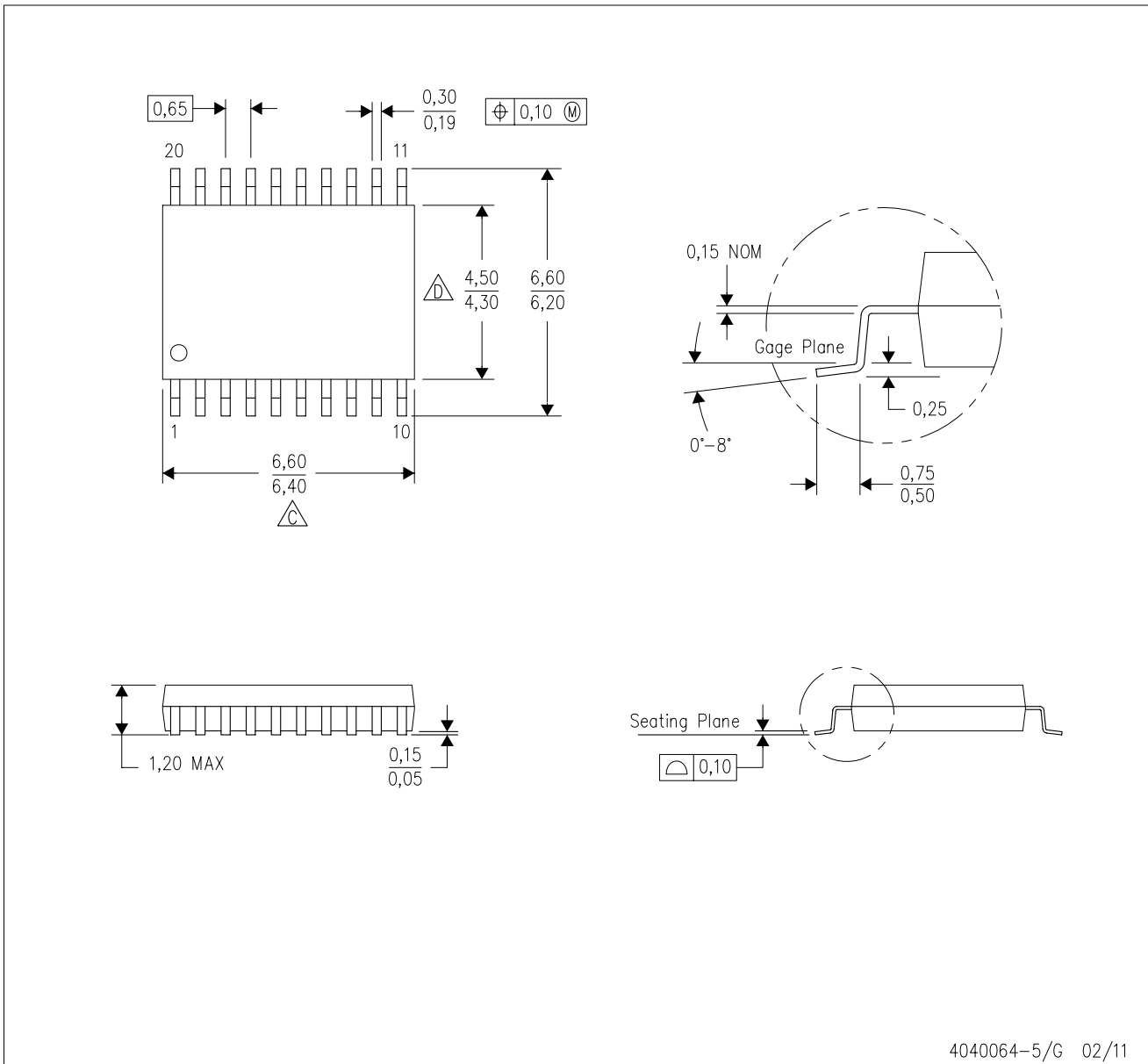


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- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

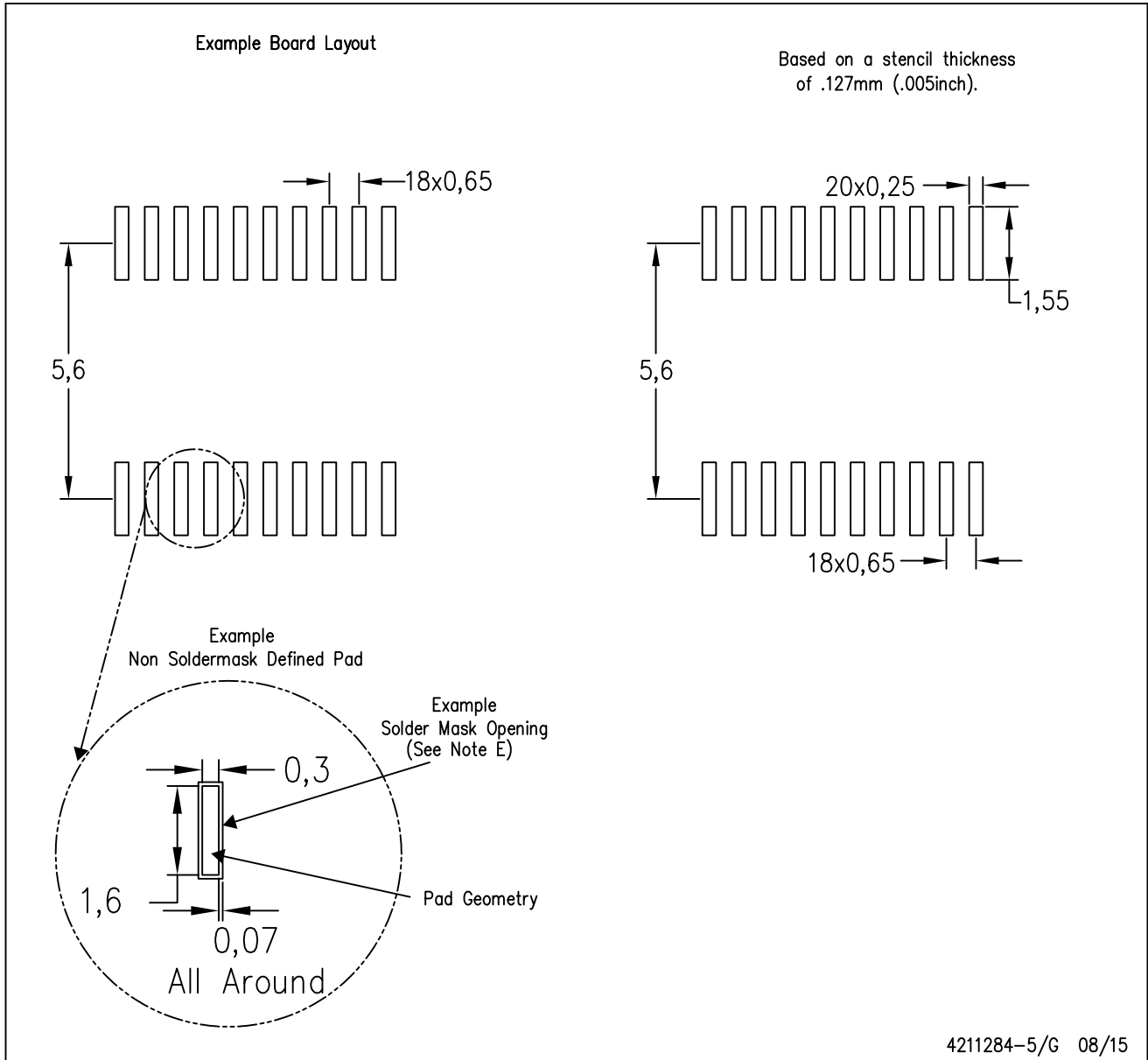


4040064-5/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

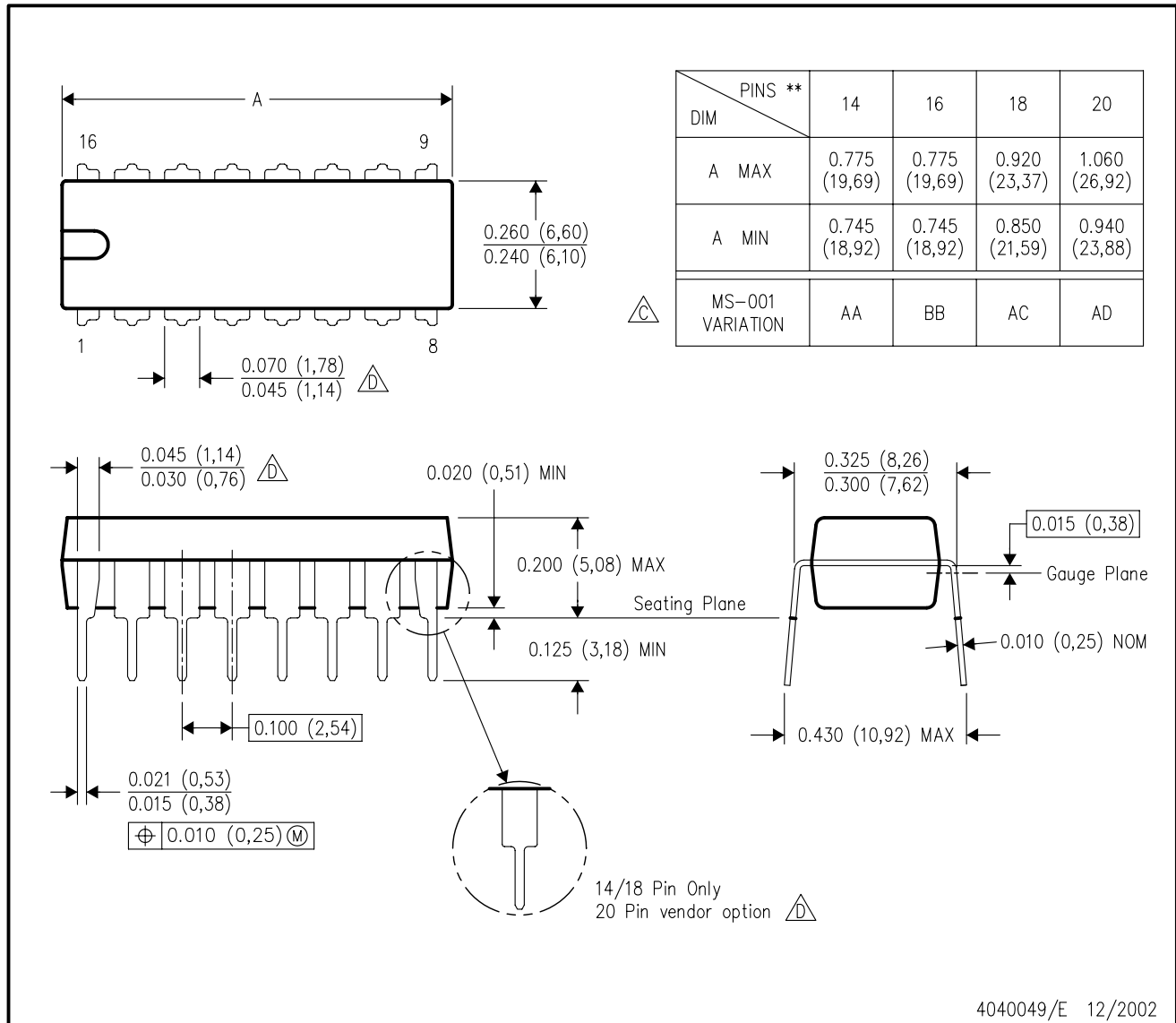


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.

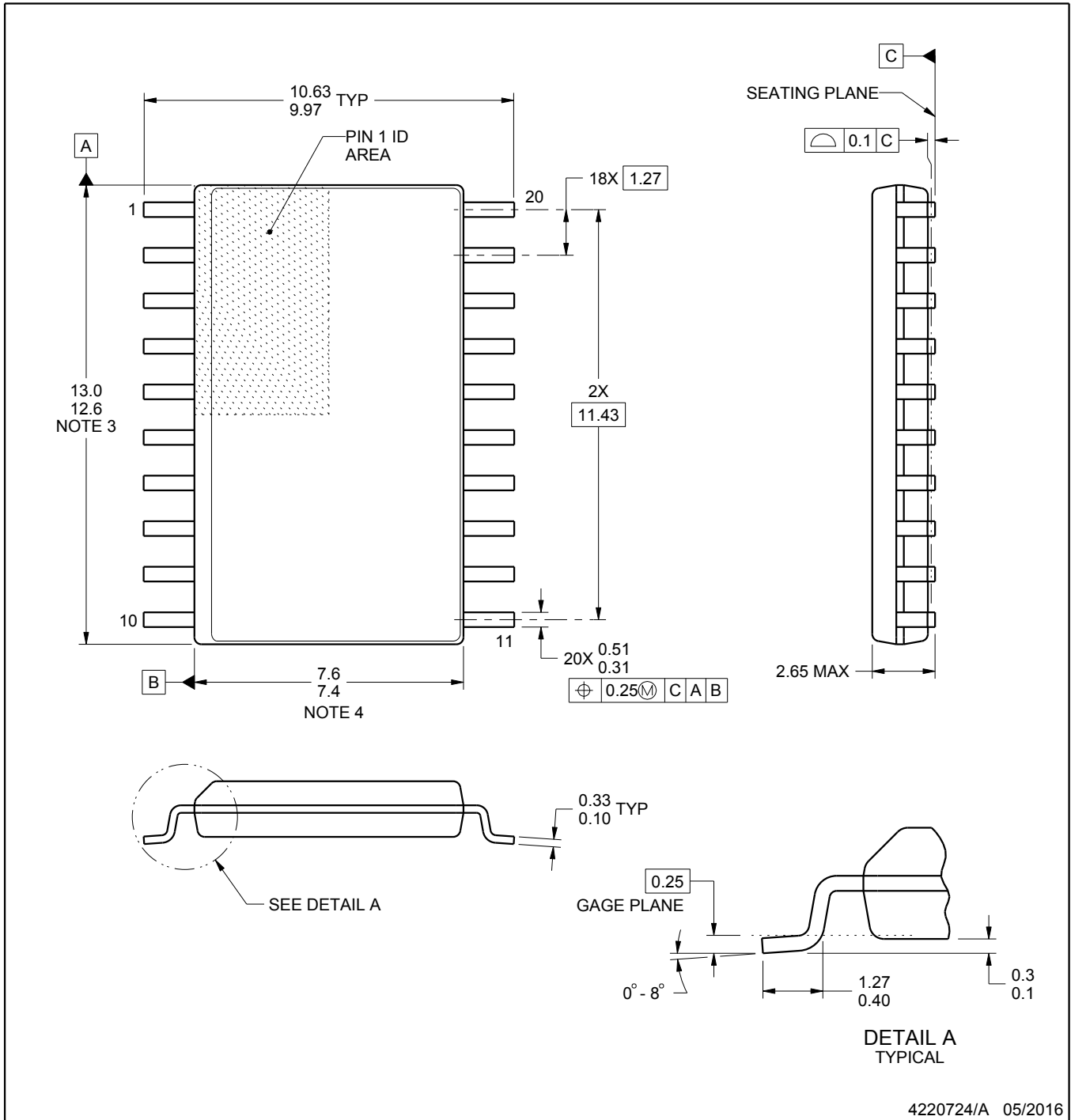
DW0020A



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

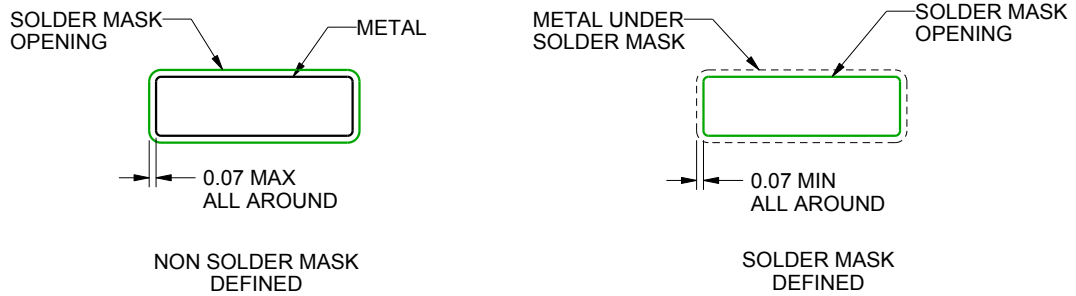
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

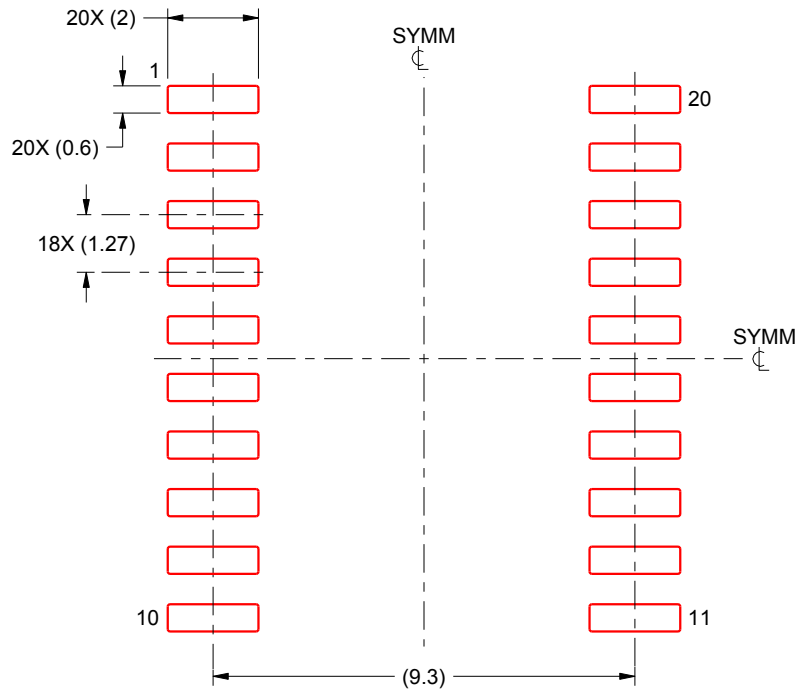
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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