AZKN1040T

±70V Fault Protected High-Speed CAN Transceiver with IEC 61000-4-2 contact ±12kV ESD Protection

Features

- ISO 11898-2:2016 and SAE J2284-1 to SAE J2284-5 compliant for 2Mbps and 5Mbps CAN FD with basic wake-up implementation
- Fault voltage up to ±70V for bus pins, suitable for 12V, 24V and 36V systems
- Integrated ESD and Surge Transient Voltage Suppressor (TVS) for bus pins
- TVS protection Immunities for bus terminals :
  ±12kV IEC 61000-4-2, Contact Discharge
  ±15kV IEC 61000-4-2, Air Discharge
  ±100V IEC 61000-4-5, Surge (8/20μs, 2Ω)
- HBM ±6kV ESD protection for all pins
- MM ±400V ESD protection for all pins
- High CDM protection up to ±800V for all pins
- Latch up immunity up to ±400mA for all pins.
- IEC 61000-4-4 Electrical Fast Transient (EFT) coupling immunity up to ±2kV for bus pins under communication
- Capability for both low ElectroMagnetic Emission (EME) and high ElectroMagnetic Immunity (EMI)
- Low standby current (13uA, typical) for power saving
- Wide range digital inputs allow for direct interfacing with 3.3V to 5.0V microcontrollers, provided the microcontroller I/Os are 5 V tolerant.
- Ideal passive behavior to CAN bus with supply power off
- Transmit Data (TXD) dominant time-out function
- SPLIT voltage output to stabilize the common mode voltage on the bus
- Bus-dominant time-out function in standby mode
- Undervoltage detection on the pin of V_{CC} power
- Current-limitation and thermal shutdown for the driver design

Applications

- Industrial Control and Instrumentation Networks
- Motor Control
- Building Automation
- Security Systems
- Medical Equipments
- Battery Control

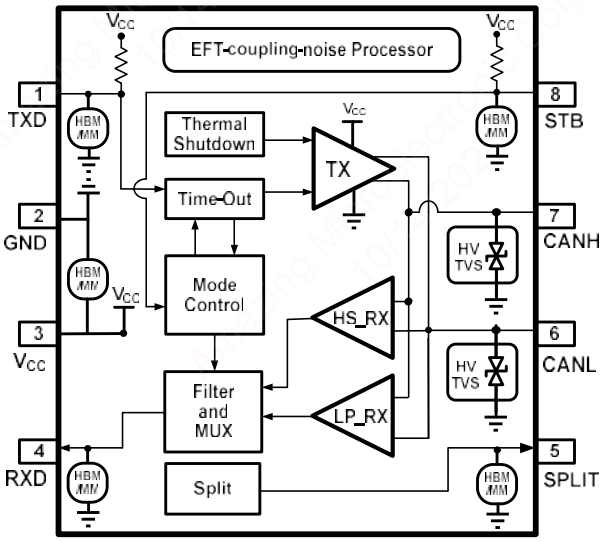
Description

AZKN1040T is a ±12kV IEC 61000-4-2 protected Controller Area Network (CAN) transceiver IC. It serves as an interface between a CAN protocol controller (MCU) and the physical two-wire CAN bus. This device operates at 5V power supply and is fully compliant with ISO 11898-2:2016 standard for CAN FD application. The data rate of both driver and receiver is up to 5Mbps to support the high-speed application of the CAN FD.

AZKN1040T has the capabilities of both the ±40V common mode range of the receiver and the low EME of the transmitter, which has been patented as the Amazing's intellectual property. Moreover, the whole-chip design of the AZKN1040T can sustain ±2kV EFT coupling under communication.

AZKN1040T is a robust CAN transceiver, which features ±70V fault protection to sustain the DC short voltage on the bus pins. Moreover, AZKN1040T has ±100V surge protection immunity to avoid the possible damage from the EOS events. In addition, the whole-chip ESD protection immunity of AZKN1040T can sustain HBM ±6kV, MM ±400V and CDM ±800V, which is satisfied to overcome the ESD zapping under the worst manufacture environment.

Functional Block of AZKN1040T



Thermal Characteristics

Refer to the Integrated Circuits Thermal Test Method Environmental Conditions – Natural Convection (Still Air) (EIA/JESD51-2A)

PARAMETER	SYMBOL	Conditions	Value	UNIT
Thermal resistance from virtual junction to ambient	θ_{JA} [1]	P_H=70mW under the air flow rate = 0 (m/s) in the ambient temperature	120.98	°C/W

[1] The thermal resistance between virtual junction and ambient is $\theta_{JA}= (T_J - T_{AMB})/P_H$, where T_J is the virtual junction temperature and T_{AMB} is the ambient temperature under the power dissipation of P_H.

Absolute Maximum Ratings [1]

PARAMETER	SYMBOL	MIN	MAX	UNIT
DC voltage on CANH, CANL and SPLIT	V_{CANH}, V_{CANL}, V_{SPLIT}	-70	70	V
DC voltage between pin CANH and pin CANL	$V_{(CANH-CANL)}$	-50	50	V
DC voltage on all other pins	V_X	-0.3	7	V
System-level ESD (IEC 61000-4-2, Contact Discharge) -- at pin CANH, CANL	$V_{ESD(contact)}$	-12	12	kV
System-level ESD (IEC 61000-4-2, Air-Gap Discharge) -- at pin CANH, CANL	$V_{ESD(air)}$	-15	15	kV
Surge (IEC 61000-4-5) at pin CANH, CANL [2]	V_{SURGE}	-100	100	V
HBM ESD (Human Body Model; 100pF; 1.5 kΩ) -- at any pins [3]	V_{HBM}	-6	6	kV
MM ESD (Machine Model; 200pF) -- at any pins [4]	V_{MM}	-400	400	V
CDM ESD (Charged Device Model; field induced charge) -- at any pins [5]	V_{CDM}	-800	800	V
Virtual junction temperature	T_J	-40	105	°C
Storage temperature	T_{STO}	-55	150	°C

[1] Stresses listed above may cause permanent damage to the device under “Maximum Ratings”. This is a stress rating only and functional operation of the device at those or other conditions above those indicated in the operational listings of this specification are not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

[2] Applied surge source voltage: tp =8/20μs, 2Ω source impedance.

[3] Verified by thirty-party referred to MIL-STD-883J Method 3015.9

[4] Verified by thirty-party referred to JESEC EIA/JESD22-A115

[5] Verified by thirty-party referred to JESD22-C101-D

DC Electrical Characteristics

(V_{CC}=4.75V to 5.25V; T_{AMB}= -40 °C to +85 °C; R_L=60Ω unless otherwise noted. Typical values are at V_{CC}=5V and T_{AMB}= 25 °C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Internal Supply : V_{CC}						
Supply voltage	V_{CC}		4.75	-	5.25	V
Undervoltage detection voltage on pin V_{CC}	$V_{uvd(VCC)\_1}$		3.5	4.0	4.5	V
	$V_{uvd(VCC)\_2}$			2.0		
Supply current	I_{CC}	Standby mode				
		V_{TXD}=V_{CC}	-	13	25	μA
		Normal mode				
		Recessive; V_{TXD}=V_{CC}	2.5	5	12	mA
		Dominant; V_{TXD}=0V	20	40	70	mA
		Dominant; V_{TXD}=0V; Short circuit on bus lines; -3V < (V_{CANH}=V_{CANL}) < +18V	2.5	70	110	mA
Bus lines : CANH and CANL						
Dominant output voltage	$V_{O(dom)}$	V_{TXD}=0V; t < $t_{to(dom)TXD}$				
		pin CANH; RL = 50 Ω to 65 Ω	2.75	3.5	4.5	V
		pin CANL; RL = 50 Ω to 65 Ω	0.5	1.5	2.25	V
Transmitter dominant voltage symmetry	$V_{dom(TX)sym}$	$V_{dom(TX)sym}$= VCC-(V_{CANH}-V_{CANL})	-400	-	+400	mV
Transmitter voltage symmetry	V_{TXsym}	V_{TXsym}=V_{CANH}+V_{CANL}; [2] f_{TXD}=250KHz, 1MHz and 2.5MHz; [3] C_{SPLIT}=4.7nF	0.9V_{CC}	-	1.1V_{CC}	
Bus differential output voltage	$V_{O(dif)bus}$	V_{TXD}=0V; t < $t_{to(dom)TXD}$				
		R_L = 50 Ω to 65 Ω	1.5	-	3	V
		R_L = 45 Ω to 70 Ω	1.4	-	3.3	V
		R_L = 2240 Ω	1.5	-	5	V
		recessive; no load				
		Normal mode; V_{TXD}=V_{CC}	-50	-	+50	mV
		Standby mode	-0.2	-	+0.2	V
Recessive output voltage	$V_{O(rec)}$	Normal mode; V_{TXD}=V_{CC}; no load	2	0.5V_{CC}	3	V
		Standby mode; no load	-0.1	-	+0.1	V
Receiver recessive voltage	$V_{rec(RX)}$	$V_{CM(CAN)}$= -40V to +40V [1]				
		Normal mode	-4	-	0.5	V
		Standby mode	-4	-	0.4	V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Receiver dominant voltage	$V_{dom(RX)}$	$V_{CM(CAN)}$= -40V to +40V [1]				
		Normal mode	0.9	-	9	V
		Standby mode	1.15	-	9	V
Differential receiver threshold voltage	$V_{th(RX)dif}$	$V_{CM(CAN)}$= -40V to +40V [1]				
		Normal mode	0.5	0.7	0.9	V
		Standby mode	0.4	0.7	1.15	V
Differential receiver hysteresis voltage	$V_{hys(RX)dif}$	$V_{CM(CAN)}$= -40V to +40V [1] Normal mode		100		mV
Dominant short-circuit output current	$I_{O(SC)dom}$	V_{TXD}=0V; t < $t_{to(dom)TXD}$; V_{CC}=5V				
		Pin CANH; V_{CANH}=-15V to 40V	-115	-70		mA
		Pin CANL; V_{CANL}=-15V to 40V		65	115	mA
Recessive short-circuit output current	$I_{O(SC)rec}$	Normal mode; V_{TXD}=V_{CC} V_{CANH}=V_{CANL}=-47V to +52V	-10	-	+10	mA
Leakage current	I_L	V_{CC}=0V or V_{CC}=shorted to ground via 47 kΩ; V_{CANH}=V_{CANL}=5V	-5	-	+5	μA
Input resistance	R_i	-2V≦V_{CANL}≦+7V; -2V≦V_{CANL}≦+7V	9	15	28	kΩ
Input resistance deviation	ΔR_i	0V≦V_{CANL}≦+5V; 0V≦ V_{CANL}≦+5V	-1	-	+1	%
Differential input resistance	$R_{i(dif)}$	-2V≦V_{CANL}≦+7V; -2V≦ V_{CANL}≦+7V	19	30	52	kΩ
Common-mode input capacitance	$C_{i(cm)}$	[2]	-	-	20	pF
Differential input capacitance	$C_{i(dif)}$	[2]	-	-	10	pF
Common mode output : SPLIT						
Output voltage	$V_{O(split)}$	Normal mode I_{SPLIT}=-500μA to +500μA	$0.3V_{CC}$	$0.5V_{CC}$	$0.7V_{CC}$	V
		Normal mode; R_L=1 MΩ	$0.45V_{CC}$	$0.5V_{CC}$	$0.55V_{CC}$	V
Leakage current	I_L	Standby mode V_{SPLIT}= -50V to +50V	-10	-	+10	μA
Temperature Protection						
Shutdown temperature	$T_{J(sd)}$	[2]	-	190	-	°C
Standby mode control input : STB						
High-level input voltage	V_{IH}		2	-	V_{CC}+0.3	V
Low-level input voltage	V_{IL}		-0.3	-	+0.8	V
High-level input current	I_{IH}	V_{STB}=V_{CC}	-1	-	+1	μA
Low-level input current	I_{IL}	V_{STB}=0V	-15	-8	-1	μA

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Transmit data input : TXD						
High-level input voltage	V_{IH}		2	-	V_{CC}+0.3	V
Low-level input voltage	V_{IL}		-0.3	-	+0.8	V
High-level input current	I_{IH}	$V_{TXD}=V_{CC}$	-5	-	+5	μA
Low-level input current	I_{IL}	V_{TXD}=0V	-260	-120	-30	μA
Input capacitance	C_i	[2]	-	5	10	pF
Receive data output : RXD						
High-level output current	I_{OH}	$V_{RXD}=V_{CC}$-0.4V	-8	-3	-1	mA
Low-level output current	I_{OL}	V_{RXD}=0.4V; bus dominant	2	7	12	mA

[1] $V_{CM(CAN)}$ is the common mode voltage of CANH and CANL.

[2] Not tested in production; guaranteed by design.

[3] The test circuit used to measure the bus output voltage symmetry (which includes C_{SPLIT}) is shown in Figure 7.

Switching Characteristics

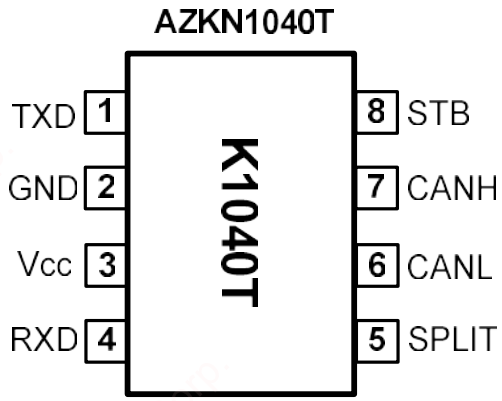
(V_{CC}=4.75V to 5.25V; T_{AMB}= -40 °C to +85 °C; R_L=60Ω unless otherwise noted. Typical values are at V_{CC}=5V and T_{AMB}= 25 °C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Transceiver timing; pins CANH, CANL, TXD and RXD; see Figure 1 and Figure 5						
Delay time from TXD to bus dominant	$t_{d(TXD-busdom)}$	Normal mode	-	75	-	ns
Delay time from TXD to bus recessive	$t_{d(TXD-busrec)}$	Normal mode	-	93	-	ns
Delay time from bus dominant to RXD	$t_{d(busdom-RXD)}$	Normal mode	-	70	-	ns
Delay time from bus recessive to RXD	$t_{d(busrec-RXD)}$	Normal mode	-	85	-	ns
Propagation delay from TXD to RXD	$t_{PD(TXD-RXD)}$	Normal mode	60	-	220	ns
Bit time on Bus	$t_{bit(Bus)}$	$t_{bit(TXD)}$=500ns [1]	435	-	530	ns
		$t_{bit(TXD)}$=200ns [1]	155		210	ns
Bit time on pin RXD	$t_{bit(RXD)}$	$t_{bit(TXD)}$=500ns [1]	400	-	550	ns
		$t_{bit(TXD)}$=200ns [1]	120		220	ns
Receiver timing symmetry	Δt_{Rec}	Δt_{Rec}= $t_{bit(RXD)}$ - $t_{bit(Bus)}$				
		$t_{bit(TXD)}$=500ns	-65	-	+40	ns
		$t_{bit(TXD)}$=200ns	-45	-	+15	ns
TXD dominant time-out time	$t_{to(dom)TXD}$	V_{TXD}=0V; Normal mode	0.8	3	8	ms
Bus dominant time-out time	$t_{to(dom)bus}$	Standby mode	0.8	3	8	ms
Bus wake-up filter time	$t_{filtr(wake)bus}$	Standby mode	0.5	1	3	μs
Standby to normal mode delay time	$t_{d(stb-norm)}$	[2]	20	34	55	μs

[1] See Figure 2.

[2] See Figure 3.

Pin Configuration



AZKN1040T : SOP8

Pin Function Description

Pin Number	Mnemonic	Function
1	TXD	Transmit data input
2	GND	Ground supply
3	V_{CC}	Supply voltage
4	RXD	Receive data output; reads out data from the bus lines
5	SPLIT	Common-mode stabilization output
6	CANL	LOW-level CAN bus line
7	CANH	HIGH-level CAN bus line
8	STB	Standby mode control input

Detail Description of Part

AZKN1040T is a high-speed CAN transceiver compliant with the ISO 11898-2:2016. The function of the SPLIT output is the common mode bias of the bus terminated device.

The SPLIT pin will generate the reference voltage (defined as $0.5V_{CC}$) for common mode stabilization of the bus termination (see Figure 4) in the normal mode. The stability of the common mode voltage of the bus will effectively reduce the EME. The SPLIT pin is active in normal mode but is floating in both standby mode and under-V_{CC} condition ($V_{CC} < V_{uvd(VCC)\_1}$). Therefore, the SPLIT pin suggests to be opened when the devices are not the terminated node.

Operation Modes

The normal and standby are two operating modes for AZKN1040T, which are selected by STB pin. The detail description of the operating modes related to both bus pins and RXD pin is listed in the Table1.

- **Normal mode**

  When STB pin ties to logic LOW, AZKN1040T will switch to the normal mode. In the normal mode, the driver will translate the logic state of TXD to differential output of HS CAN. The data rate of driver is up to the 5Mbps with both the controlled slew rate and common mode voltage, which is Amazing's property. So that the driver performs the low common mode noise and has the low EME performance, which is evaluated by IEC 61967-4.

  The normal receiver with the ±40V common mode range operates in the normal mode, which is also Amazing's property. The normal receiver translates the differential signal of HS CAN to the digital output of RXD with data rate up to 5Mbps. The EM Immunity of normal receiver is evaluated by IEC 62132-4.

  The loop delay symmetry from TXD to RXD is optimized by both driver and normal receiver in AZKN1040T.

- **Standby mode**

  When the STB ties to logic HIGH, AZKN1040T will switch to the standby mode. In the standby mode, both the driver and normal receiver are turned off so that the bus pins are biased to GND to save V_{CC} power. Only the low power receiver operates to monitor the activity of the bus so as to inform the microcontroller if go to the normal mode or not. The wake-up filter on the output of the low-power receiver ensures that only bus dominant and bus recessive states that persist longer than $t_{fltr(wake)bus}$ are reflected on pin RXD. Therefore, the data on RXD is not exact but is a wake-up signal to microcontroller.

  The bus pins of AZKN1040T bias to GND via input resistor so that it is passive behavior in the standby mode.

Fail-safe Protection

- **TXD dominant time-out function**

  The function of "TXD dominant time-out" prevents the failure of the hardware or software from keeping the bus in the dominate state. The failure cause the bus to be blocked all communication. The timer of "TXD dominate time-out" is started when TXD pin is set to LOW. If the time of TXD pin in the LOW state is longer than $t_{to(dom)TXD}$, the driver will be turn off to release the bus. The timer of "TXD dominate time-out" will be reset when TXD pin is set to HIGH. Therefore, the minimum data rate of 25kbps is defined by the function of "TXD dominant time-out".

- **Bus dominant time-out function**

  The function of "bus dominant time-out" prevents the clamped dominate state due to failure of one of the bus nodes or bus short-circuit event, so as to trigger the permanent wake-up request in the standby mode. The timer of "bus dominant time-out" is started when the bus translates from recessive to dominate state. If the time of dominate is longer than $t_{to(dom)bus}$, the RXD will force to HIGH. The timer of "bus dominant time-out" is reset if the bus goes from dominate to recessive state.

- **Pull-up of TXD and STB input pins**

  The pins of both TXD and STB with internal pull-ups to V_{CC} are safe-guarantee design due to one or both of these pins in floating condition. When TXD pin is internally pulled up, the transmitter is forced into the recessive state. When STB pin is internally pulled up, AZKN1040T is forced into the low power standby mode. By the way, the pull-up currents will

be generated if the pins are biased to low state. In standby mode, both pins should be held HIGH to reduce the current.

- **Undervoltage detection on pin V_{CC}**
  When V_{CC} drops below the V_{CC} undervoltage detection level, $V_{uvd(VCC)\_1}$, the transceiver will switch to standby mode. The logic state of STB pin will be ignored until V_{CC} has recovered. When the V_{CC} drops below the undervoltage detection level, $V_{uvd(VCC)\_2}$, the transceiver will switch off and disengage from the bus (zero load) until V_{CC} has recovered. The undervoltage detection is the protection function to avoid the abnormal operation of V_{CC} power.

- **Overtemperature protection**
  When the virtual junction temperature exceeds the shutdown junction temperature, $T_{J(sd)}$, the output of the drivers will be disabled to protect AZKN1040T from burn out issue. In this state, both CANH and CANL are biased to the recessive level no matter what the logic level of TXD pin is and the receiver still remains operational. When the temperature falls below $T_{J(sd)}$, the overtemperature protection will be released. The typical $T_{J(sd)}$ is designed as 190°C under V_{CC} = 5.0V.

High-Immunity Communication

- **High EFT coupling Immunity**
  AZKN1040T has ±2kV EFT coupling immunity on the bus line under the normal operation. The output of transmitter (CANH and CANL) and the output of receiver (RXD) could be recovered after next bit when the high voltage ±2kV pulse of EFT coupled to the bus line through the coupling box (CCC method), as Figure 6. So the AZKN1040T has more ability to communicate with low Bit-Error-Rate (BER) under the high noise environment.

High Protection for All Pins

- **±12kV System-level ESD for CANH and CANL**
  AZKN1040T is embedded high voltage ±70V TVS on the pins of CANH and CANL to achieve IEC 61000-4-2 contact ±12kV of the system-level ESD protection. In the evaluation of system-level ESD, both CANH and CANL of AZKN1040T are zapped by ESD gun referred to GND on the evaluation board.

- **Basic surge protection for CANH and CANL**
  AZKN1040T pass ±100V of the IEC 61000-4-5 (8/20μs) with 2Ω of source impedance for directly injection. With both the surge and fault protection, AZKN1040T can efficiently prevent the EOS event in the harsh environment.

- **HBM 6kV , MM 400V and 800V CDM for all pins**
  To achieve the high reliability and high assembly yield rate, AZKN1040T have high ESD specification of the component-level for both HBM and MM. With the high robust whole-chip ESD protection, AZKN1040T can still sustain no matter the ESD pulse comes from power pin or the I/O pins. For the IC self-discharge issue, the CDM protection level of AZKN1040T is up to ±800V.

Table 1. **Operating modes**

STB Pin		**Low**	**High**
Mode		**Normal**	**Standby**
Bus pins (CANH, CANL)		Dominant / Recessive	Bias to GND[1]
RXD	**High**	Recessive	No Wake-up
	Low	Dominant	Wake-up[1]

[1] In standby mode, the standby RX is active to wake-up MCU.

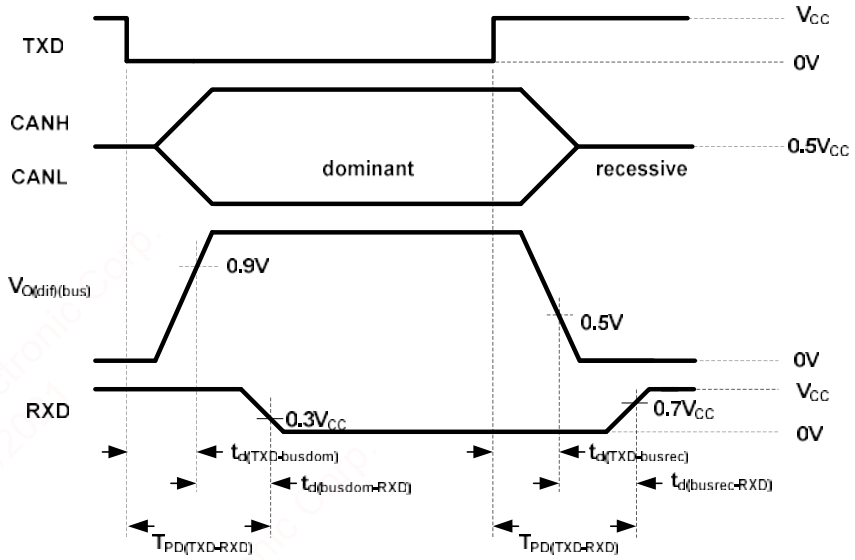


Figure 1. Timing diagram of the CAN transceiver.

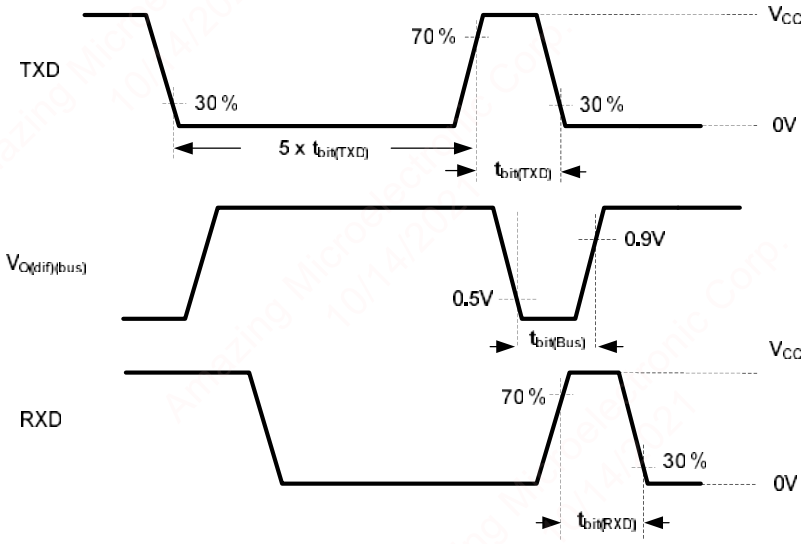


Figure 2. Timing diagram for loop delay symmetry.

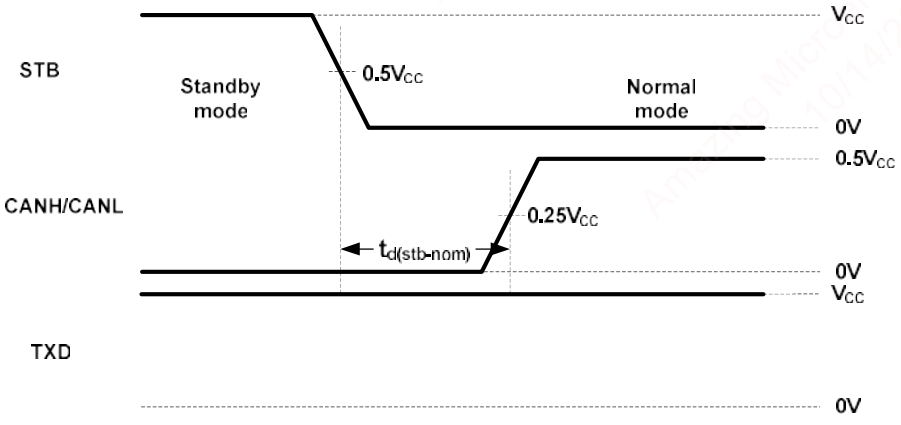


Figure 3. Timing diagram for the delay of the standby to normal mode.

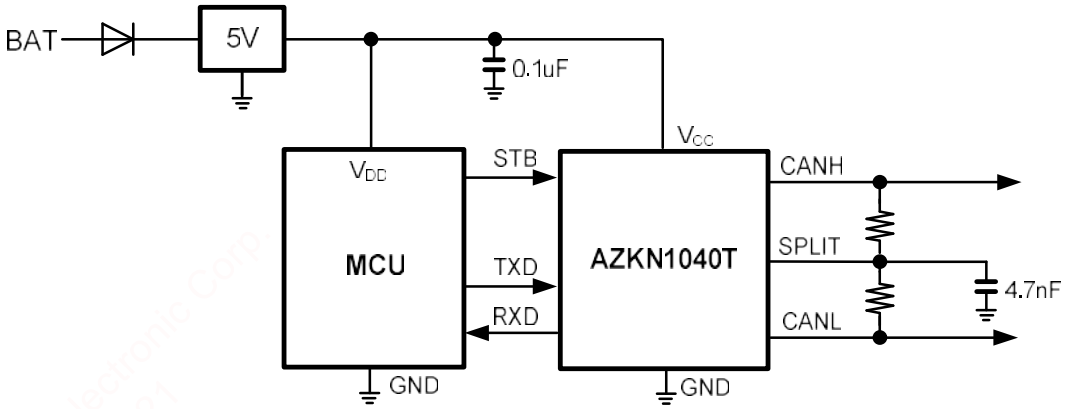


Figure 4. Typical application circuit for AZKN1040T with 5V MCU.

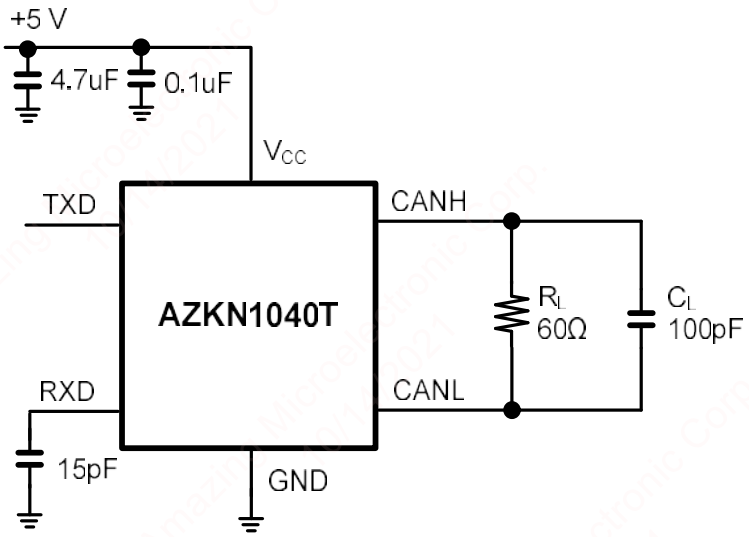


Figure 5. CAN transceiver timing test circuit

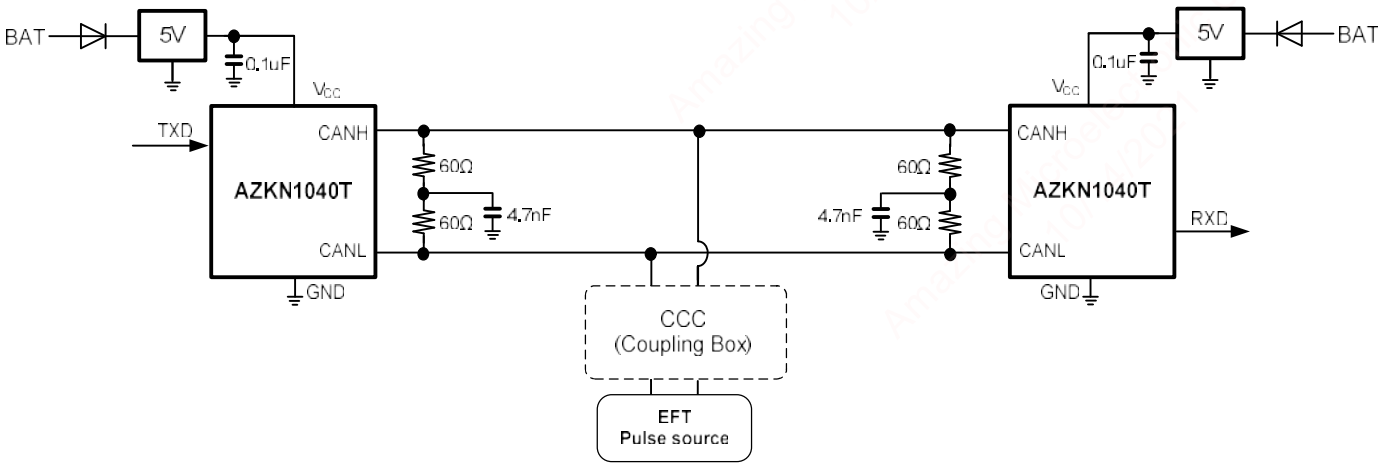


Figure 6. EFT coupling test circuit for AZKN1040T.

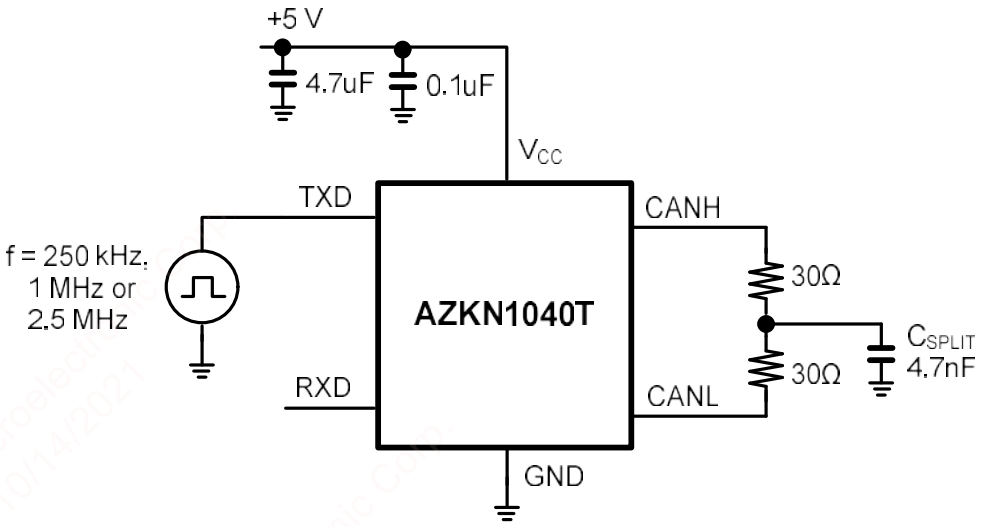
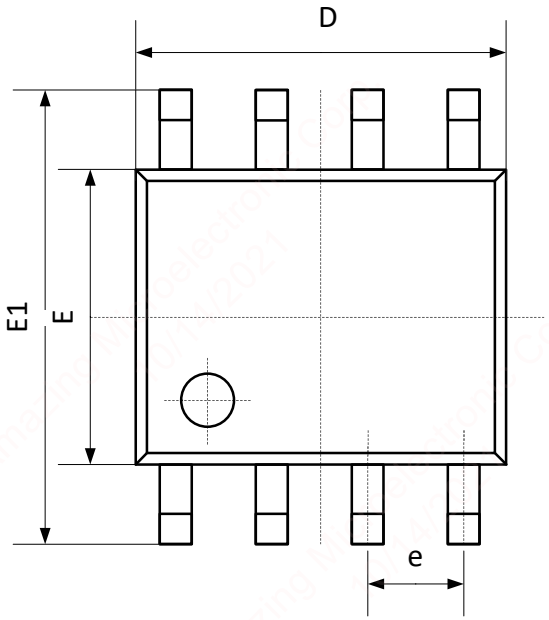


Figure 7. Test circuit for measuring transmitter driver symmetry.

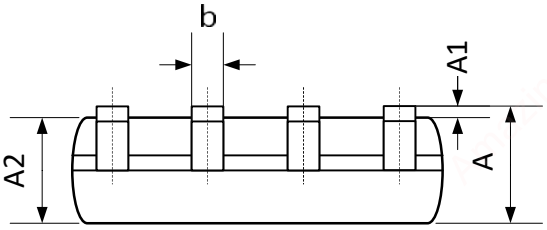
Mechanical Details

PACKAGE DIAGRAMS

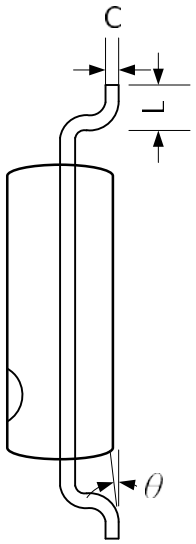
TOP VIEW



SIDE VIEW



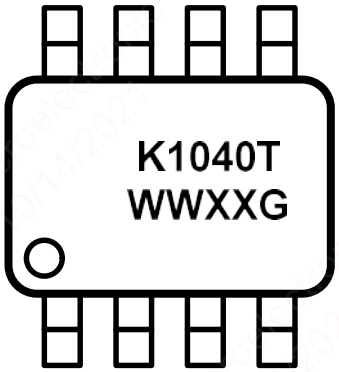
END VIEW



PACKAGE DIMENSIONS

Symbol	Millimeters		Inches	
	min	Max	min	max
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
A2	1.25	1.55	0.049	0.061
b	0.33	0.51	0.013	0.020
C	0.17	0.26	0.007	0.010
D	4.70	5.10	0.185	0.201
E	3.70	4.10	0.146	0.161
E1	5.80	6.20	0.228	0.244
e	1.27 BSC		0.05BSC	
L	0.40	1.27	0.016	0.050
Θ	0	8	0	8

MARKING CODE



K1040T = Device Code

WW = Date Code ; XX = Control Code

G = Green Part Indication

Part Number	Marking Code
AZKN1040T.RDG	K1040T WWXXG

Ordering Information

PN#	Material	Type	Reel size	MOQ	MOQ/internal box	MOQ/carton
AZKN1040T.RDG	Green	T/R	13 inch	2,500/reel	1 reel=2,500/box	5 boxes =12,500/carton

Revision History

Revision Date	Modification Description
2021/10/14	MP Release