ISL95873

Buck PWM Controller with Internal Compensation and External Reference Tracking

FN8390
Rev 0.00
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The ISL95873 is a Single-Phase Synchronous-Buck PWM controller featuring Intersil's proprietary R4™ Technology. The R4™ modulator has integrated compensation, fast transient performance, accurate switching frequency control, and excellent light-load efficiency. These technology advances, together with integrated MOSFET drivers and a Schottky bootstrap diode, allow for a high performance regulator that is highly compact and needs few external components. Differential remote sensing of the output voltage is an additional feature. For maximum efficiency, the converter automatically enters diode-emulation mode (DEM) during light-load conditions, such as system standby.

The ISL95873 accepts a wide 3.3V to 25V input voltage range, making it ideal for systems that run on battery or AC-adapter power sources. It also is a low-cost solution for applications requiring tracking of an external reference voltage during soft-start. When the external reference level meets the internal reference voltage, the ISL95873 switches from the external reference to the internal reference. The external reference is only used during soft-start.

Features

- External reference tracking
- Intersil's R4™ modulator technology
  - Internal compensation
  - Fast, optimal transient response
- Input voltage range: 3.3V to 25V
- Output voltage range: 0.5V to 3.3V
- Precision voltage regulation
  - ±0.5% System accuracy over -10°C to +100°C
- Output voltage remote sense
- Fixed 300kHz PWM frequency in continuous conduction
  - Proprietary frequency control loop
- Automatic diode emulation mode for highest efficiency
- Power-good monitor for soft-start and fault detection

Applications

- Compact buck regulators requiring external tracking

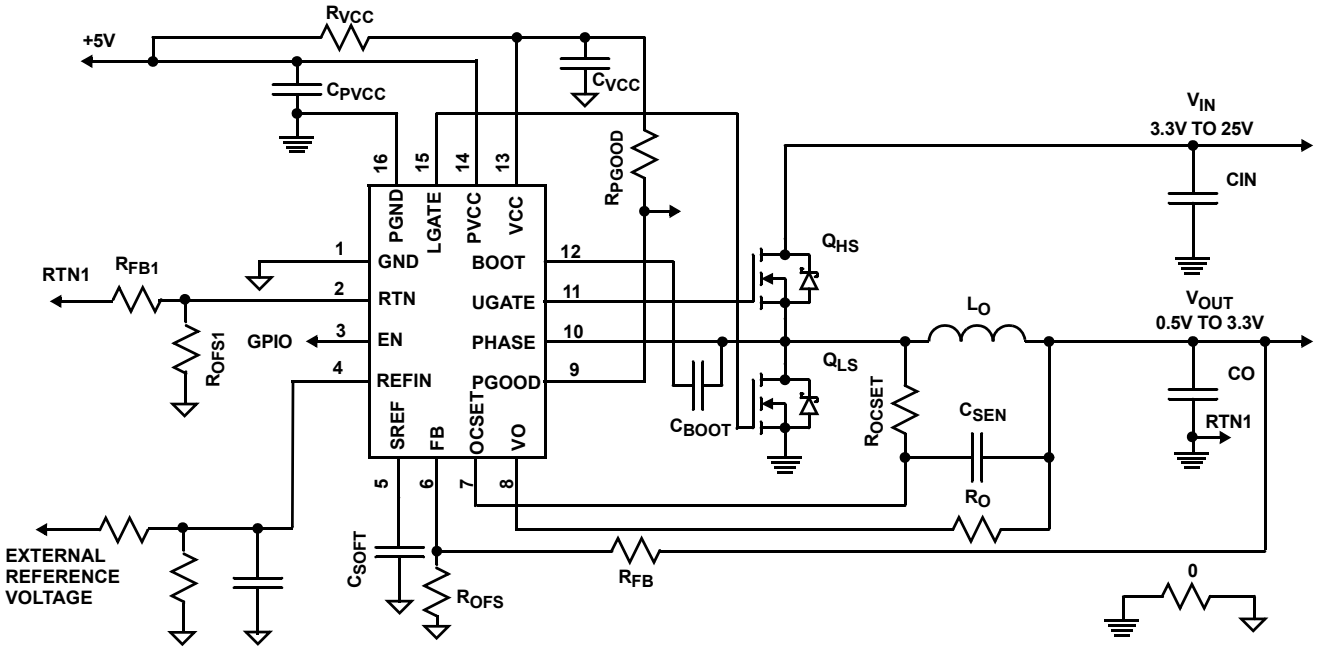


FIGURE 1. ISL95873 APPLICATION SCHEMATIC WITH DCR CURRENT SENSE

Application Schematics

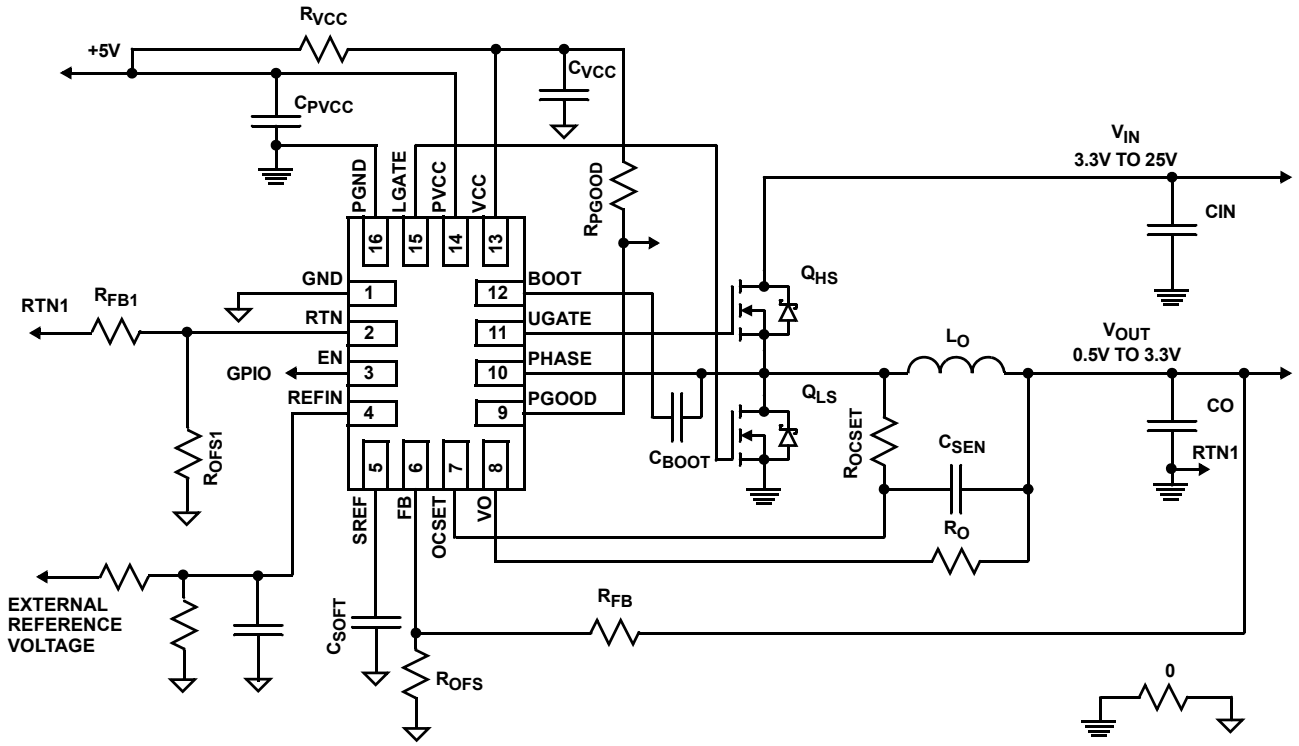


FIGURE 2. ISL95873 APPLICATION SCHEMATIC WITH ONE OUTPUT VOLTAGE SETPOINT AND DCR CURRENT SENSE

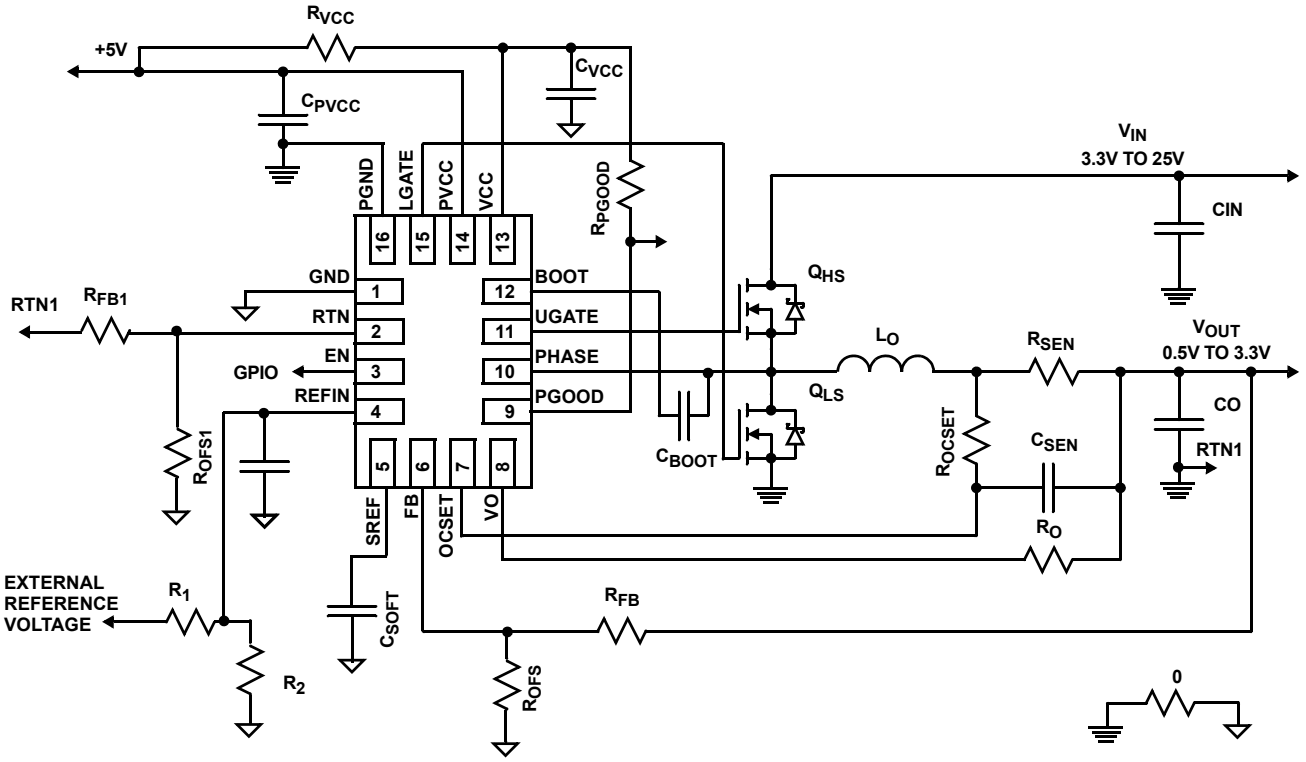


FIGURE 3. ISL95873 APPLICATION SCHEMATIC WITH ONE OUTPUT VOLTAGE SETPOINT AND RESISTOR CURRENT SENSE

Block Diagram

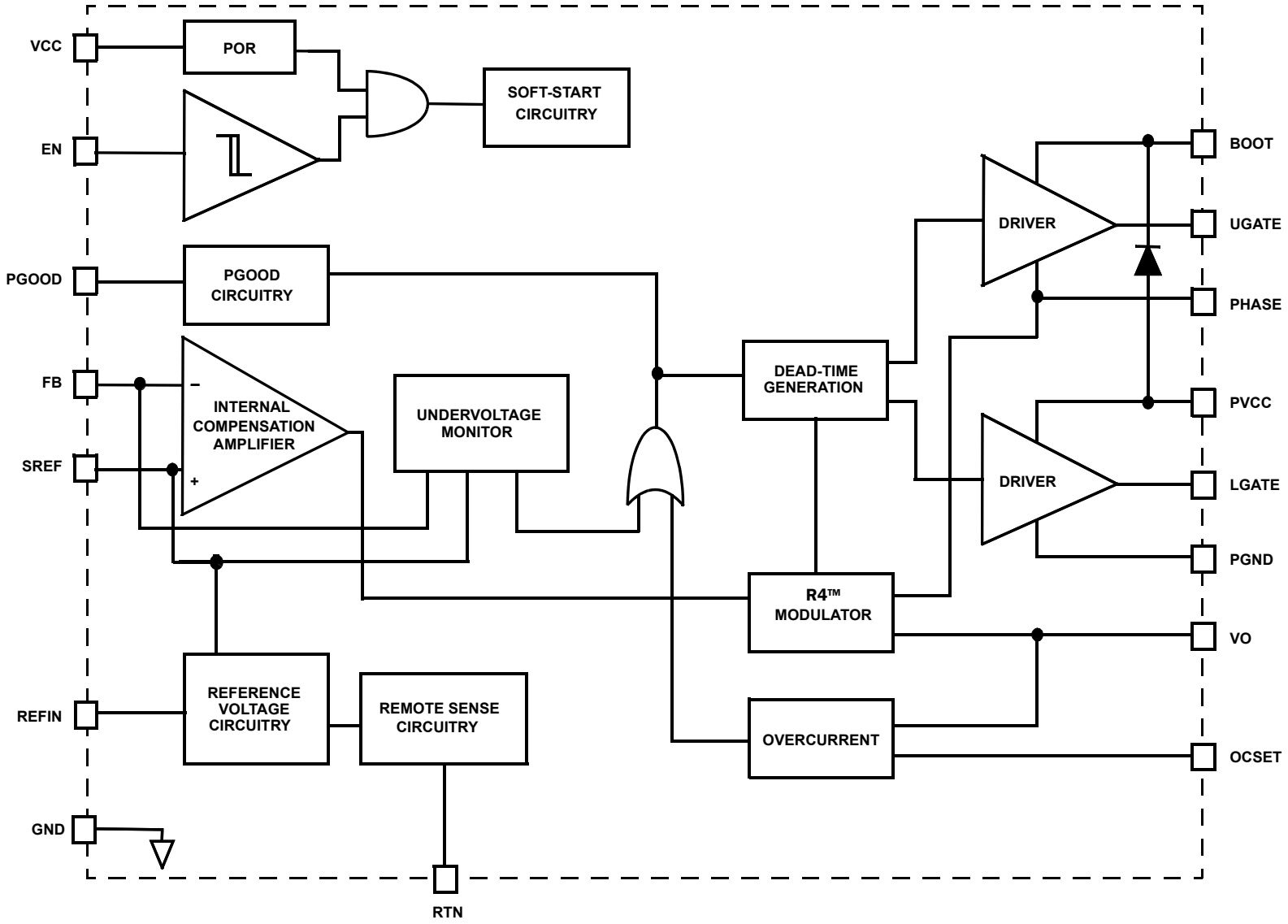


FIGURE 4. SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM OF ISL95873

Ordering Information

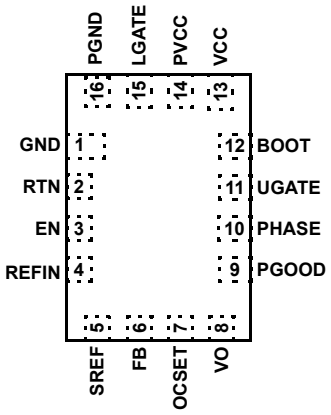
PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL95873HRUZ-T	873	-10 to +100	16 Ld 2.6x1.8 UTQFN	L16.2.6x1.8A

NOTES:

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate-e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL95873. For more information on MSL, please see tech brief TB363

Pin Configuration

ISL95873
(16 LD 2.6X1.8 UTQFN)
TOP VIEW



Functional Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
1	GND	IC ground for bias supply and signal reference.
2	RTN	Negative remote sense input of V_{OUT}. If resistor divider consisting of R_{FB} and R_{OFS} is used at FB pin, the same resistor divider should be used at RTN pin, i.e. keep $R_{FB1} = R_{FB}$, and $R_{OFS1} = R_{OFS}$.
3	EN	Enable input for the IC. Pulling EN above the rising threshold voltage initializes the soft-start sequence.
4	REFIN	Input for supplying the external reference voltage followed by the controller during soft-start.
5	SREF	Soft-start and voltage slew-rate programming capacitor input. Connects internally to the inverting input of the V_{SET} voltage setpoint amplifier.
6	FB	Voltage feedback sense input. Connects internally to the inverting input of the control-loop error amplifier. The converter is in regulation when the voltage at the FB pin equals the voltage on the SREF pin.

Functional Pin Descriptions (Continued)

PIN NUMBER	SYMBOL	DESCRIPTION
7	OCSET	Input for the overcurrent detection circuit. The overcurrent setpoint programming resistor R_{OCSET} connects from this pin to the sense node.
8	VO	Output voltage sense input for the R4™ modulator. The VO pin also serves as the reference input for the overcurrent detection circuit.
9	PGOOD	Power-good open-drain indicator output. This pin changes to high impedance when the converter is able to supply regulated voltage.
10	PHASE	Return current path for the UGATE high-side MOSFET driver, V_{IN} sense input for the R4™ modulator, and inductor current polarity detector input.
11	UGATE	High-side MOSFET gate driver output. Connect to the gate terminal of the high-side MOSFET of the converter.
12	BOOT	Positive input supply for the UGATE high-side MOSFET gate driver. The BOOT pin is internally connected to the cathode of the Schottky boot-strap diode. Connect an MLCC between the BOOT pin and the PHASE pin.
13	VCC	Input for the IC bias voltage. Connect +5V to the VCC pin and decouple with at least a MLCC to the GND pin.
14	PVCC	Input for the LGATE and UGATE MOSFET driver circuits. The PVCC pin is internally connected to the anode of the Schottky boot-strap diode. Connect +5V to the PVCC pin and decouple with a MLCC to the PGND pin.
15	LGATE	Low-side MOSFET gate driver output. Connect to the gate terminal of the low-side MOSFET of the converter.
16	PGND	Return current path for the LGATE MOSFET driver. Connect to the source of the low-side MOSFET.

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Absolute Maximum Ratings

VCC, PVCC, PGOOD, FSEL to GND . . . . . -0.3V to +7.0V
VCC, PVCC to PGND . . . . . -0.3V to +7.0V
GND to PGND . . . . . -0.3V to +0.3V
EN, VO, REFIN, FB, RTN, OCSET, SREF . . . . . -0.3V to GND, VCC + 0.3V
BOOT Voltage ($V_{BOOT-GND}$) . . . . . -0.3V to 33V
BOOT To PHASE Voltage ($V_{BOOT-PHASE}$) . . . . . -0.3V to 7V (DC)
-0.3V to 9V (<10ns)
PHASE Voltage . . . . . GND - 0.3V to 28V
GND -8V (<20ns Pulse Width, 10µJ)
UGATE Voltage . . . . . V_{PHASE} - 0.3V (DC) to V_{BOOT}
V_{PHASE} - 5V (<20ns Pulse Width, 10µJ) to V_{BOOT}
LGATE Voltage . . . . . GND - 0.3V (DC) to VCC + 0.3V
. . . . . GND - 2.5V (<20ns Pulse Width, 5µJ) to VCC + 0.3V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
16 Ld UTQFN (Notes 4, 5)	90	60

Junction Temperature Range . . . . . -55°C to +150°C
Operating Temperature Range . . . . . -10°C to +100°C
Storage Temperature . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Ambient Temperature Range . . . . . -10°C to +100°C
Converter Input Voltage to GND . . . . . 3.3V to 25V
VCC, PVCC to GND . . . . . 5V ±5%

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
5. For θ_{JC}, the "case temp" location is taken at the package top center.

Electrical Specifications

All typical specifications T_A = +25°C, V_{CC} = 5V. **Boldface limits apply over the operating temperature range, -10°C to +100°C, unless otherwise stated.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
VCC and PVCC						
VCC Input Bias Current	I_{VCC}	EN = 5V, VCC = 5V, FB = 0.55V, SREF < FB	-	1.2	**1.9**	mA
VCC Shutdown Current	I_{VCCoff}	EN = GND, VCC = 5V	-	0	**1.0**	µA
PVCC Shutdown Current	$I_{PVCCoff}$	EN = GND, PVCC = 5V	-	0	**1.0**	µA
VCC POR THRESHOLD						
Rising VCC POR Threshold Voltage	V_{VCC_THR}		**4.40**	4.52	**4.60**	V
Falling VCC POR Threshold Voltage	V_{VCC_THF}		**4.10**	4.22	**4.35**	V
REGULATION						
System Accuracy		PWM Mode = CCM	**-0.5**	-	**+0.5**	%
Internal Reference Voltage			-	0.5	-	V
Feedback Voltage Reference Transfer Voltage			**0.461**	0.482	**0.4975**	V
PWM						
Switching Frequency Accuracy	F_{SW}	PWM Mode = CCM	**255**	300	**345**	kHz
VO						
VO Input Impedance	R_{VO}	EN = 5V	-	600	-	kΩ
VO Reference Offset Current	I_{VOSS}	V_{ENTHR} < EN, SREF = Soft-Start Mode	-	8.5	-	µA
VO Input Leakage Current	I_{VOoff}	EN = GND, VO = 3.6V	-	0	-	µA
ERROR AMPLIFIER						
FB Input Bias Current	I_{FB}	EN = 5V, FB = 0.50V	**-30**	-	**+50**	nA
SREF						
Maximum Soft-Start Current	I_{SS}	SREF = Soft-Start Mode	**±51**	85	**±119**	µA
POWER GOOD						
PGOOD Pull-down Impedance	R_{PG}	PGOOD = 5mA Sink	-	50	**150**	Ω

Electrical Specifications All typical specifications T_A = +25°C, V_{CC} = 5V. **Boldface limits apply over the operating temperature range, -10°C to +100°C, unless otherwise stated. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
PGOOD Leakage Current	I_{PG}	PGOOD = 5V	-	0.1	**1.0**	µA
GATE DRIVER						
UGATE Pull-Up Resistance (Note 6)	R_{UGPU}	200mA Source Current	-	1.1	**1.7**	Ω
UGATE Source Current (Note 6)	I_{UGSRC}	UGATE - PHASE = 2.5V	-	1.8	-	A
UGATE Sink Resistance (Note 6)	R_{UGPD}	250mA Sink Current	-	1.1	**1.7**	Ω
UGATE Sink Current (Note 6)	I_{UGSNK}	UGATE - PHASE = 2.5V	-	1.8	-	A
LGATE Pull-Up Resistance (Note 6)	R_{LGPU}	250mA Source Current	-	1.1	**1.7**	Ω
LGATE Source Current (Note 6)	I_{LGSRC}	LGATE - GND = 2.5V	-	1.8	-	A
LGATE Sink Resistance (Note 6)	R_{LGPD}	250mA Sink Current	-	0.55	**1.0**	Ω
LGATE Sink Current (Note 6)	I_{LGSNK}	LGATE - PGND = 2.5V	-	3.6	-	A
UGATE to LGATE Deadtime	t_{UGFLGR}	UGATE falling to LGATE rising, no load	-	21	-	ns
LGATE to UGATE Deadtime	t_{LGFUGR}	LGATE falling to UGATE rising, no load	-	21	-	ns
PHASE						
PHASE Input Impedance	R_{PHASE}		**-**	33	**-**	kΩ
BOOTSTRAP DIODE						
Forward Voltage	V_F	PVCC = 5V, I_F = 2mA	**-**	0.58	**-**	V
Reverse Leakage	I_R	V_R = 25V	**-**	0	**-**	µA
CONTROL INPUTS						
EN High Threshold Voltage	V_{ENTHR}		**2.0**	-	**-**	V
EN Low Threshold Voltage	V_{ENTHF}		**-**	-	**1.0**	V
EN Input Bias Current	I_{EN}	EN = 5V	**0.85**	1.7	**2.55**	µA
EN Leakage Current	I_{ENoff}	EN = GND	**-**	0	**1.0**	µA
PROTECTION						
OCP Threshold Voltage	V_{OCPTH}	V_{OCSET} - V_O	**-1.15**	-	**1.15**	mV
OCP Reference Current	I_{OCP}	EN = 5.0V	**7.905**	8.5	**8.925**	µA
OCSET Input Resistance	R_{OCSET}	EN = 5.0V	**-**	600	**-**	kΩ
OCSET Leakage Current	I_{OCSET}	EN = GND	**-**	0	**-**	µA
UVP Threshold Voltage	V_{UVTH}	V_{FB} = %V_{SREF}	**81**	84	**87**	%
OVP Rising Threshold Voltage	V_{OVRTH}	V_{FB} = %V_{SREF}	**113**	116	**120**	%
OVP Falling Threshold Voltage	V_{OVFTH}	V_{FB} = %V_{SREF}	**100**	102	**106**	%
OTP Rising Threshold Temperature (Note 6)	T_{OTRTH}		**-**	150	**-**	°C
OTP Hysteresis (Note 6)	T_{OTHYS}		**-**	25	**-**	°C

NOTES:

6. Limits established by characterization and are not production tested.
7. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Theory of Operation

The following sections will provide a detailed description of the inner workings of the ISL95873.

Power-On Reset

The IC is disabled until the voltage at the VCC pin has increased above the rising power-on reset (POR) threshold voltage V_{VCC_THR}. The controller will become disabled when the voltage at the VCC pin decreases below the falling POR threshold voltage V_{VCC_THF}. The POR detector has a noise filter of approximately 1µs.

Enabling the Controller

Once VCC has ramped above V_{VCC_THR}, the controller can be enabled by pulling the EN pin voltage above the input-high threshold V_{ENTHR}. Once EN exceeds this threshold, the soft-start sequence is initiated.

External Reference Setup

The REFIN input of the ISL95873 requires an external reference voltage to be connected to this pin. Typically, this will be another system rail, which requires the output of the ISL95873 to follow it up during boot-up of the two regulators. A resistor divider is required between the external reference voltage and the REFIN pin to scale the external voltage down to the internal reference voltage, see Figure 5.

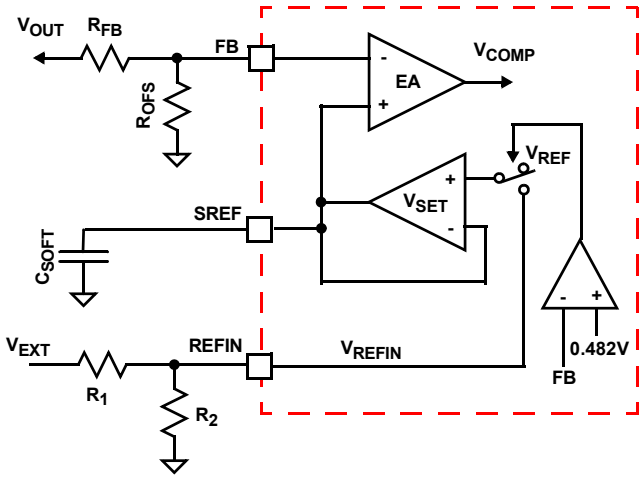

FIGURE 5. REFIN CONNECTION TO SYSTEM RAIL

The relation between the voltage at the REFIN pin, V_{REFIN}, and the external reference voltage, V_{EXT}, is given in Equation 1:

$$V_{REFIN} = V_{REF} = V_{EXT} \cdot \frac{R_2}{R_1 + R_2} \quad \text{(EQ. 1)}$$

From this expression the resistor divider values can be calculated. The voltage on the REFIN pin must equal to the internal reference of the ISL95873.

Soft-Start

Once the POR threshold on VCC has been met and ENABLE is applied, the SREF pin releases its discharge clamp, and enables the reference amplifier V_{SET}. The soft-start current I_{SS} is limited to 85µA and is sourced out of the SREF pin and begins charging the C_{SOFT} capacitor on the SREF pin until it equals V_{REFIN}. The soft-start current will adjust to match the external reference ramp rate as seen through the resistor divider on the REFIN pin. The regulator controls the PWM, such that the voltage on the SREF pin tracks the rising voltage on the REFIN pin. The maximum dv/dt that the external voltage (V_{EXT}) can achieve is outlined in Equation 2.

$$\frac{dV_{EXT}}{dt} = \frac{I_{SS}}{C_{SOFT}} \cdot \frac{R_1 + R_2}{R_2} \quad \text{(EQ. 2)}$$

The elapsed time from when the EN pin is asserted to when V_{SREF} has charged C_{SOFT} to $V_{REF\ IN}$ will depend on the dv/dt of the external reference voltage used to generate the signal at REFIN. C_{SOFT} will not impact the dv/dt unless it is over sized or the dv/dt (outlined in Equation 2), is exceeded by the external reference. The minimum C_{SOFT} capacitance is 10nF.

Once the feedback voltage, FB, exceeds the 0.482V threshold on an internal comparator, the ISL95873 switches from the external reference (V_{EXT}) to the internal reference, V_{REF}, see Figure 6.The end of soft-start is detected by I_{SS} tapering off when capacitor C_{SOFT} charges to V_{REFIN}. The pull-down on PGOOD is released to indicate that the controller is regulating properly.

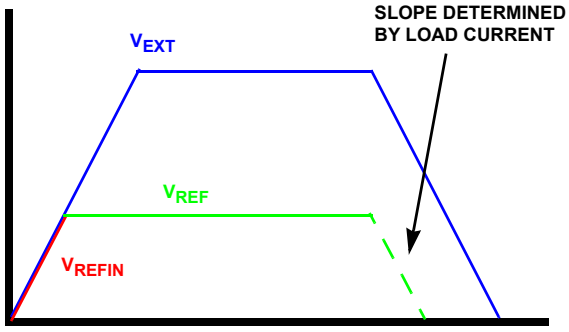

FIGURE 6. SOFT-START TRACKING OF EXTERNAL REFERENCE

During soft-start, the regulator always operates in CCM until the soft-start sequence is complete. Once soft-start is complete, diode emulation mode (DEM) is enabled.

If REFIN is pre-charged, the ISL95873 will begin switching and charging the output voltage of the regulator to the pre-charged REFIN level once enabled. Then the controller waits for REFIN to begin to move and starts charging the SREF capacitor and ramping as described previously.

Output Voltage Programming

The ISL95873 has a fixed 0.5V internal reference voltage (V_{SREF}). Figure 7 shows that the output voltage is the reference voltage if R_{FB} is shorted and R_{OFS} is open. A resistor divider consisting of R_{OFS} and R_{FB} allows the user to scale the output voltage between 0.5V and 3.3V. The relation between the output voltage and the reference voltage is given in Equation 3:

$$V_{OUT} = V_{REF} \cdot \frac{R_{FB} + R_{OFS}}{R_{OFS}} \quad \text{(EQ. 3)}$$

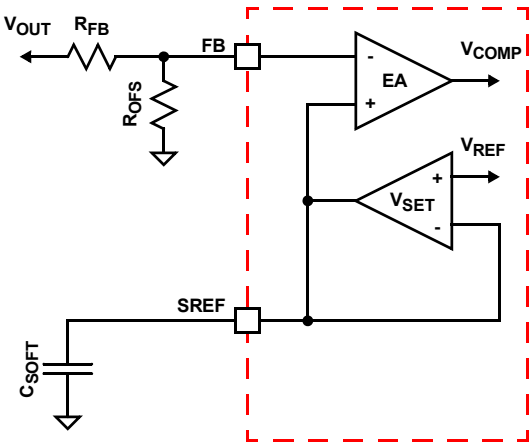

FIGURE 7. ISL95873 VOLTAGE PROGRAMMING CIRCUIT

R4™ Modulator

The R4™ modulator is an evolutionary step in R3™ technology. Like R3™, the R4™ modulator allows variable frequency in response to load transients and maintains the benefits of current-mode hysteretic controllers. However, in addition, the R4™ modulator reduces regulator output impedance and uses accurate referencing to eliminate the need for a high-gain voltage amplifier in the compensation loop. The result is a topology that can be tuned to voltage-mode hysteretic transient speed while maintaining a linear control model and removes the need for any compensation. This greatly simplifies the regulator design for customers and reduces external component cost.

Stability

The removal of compensation derives from the R4™ modulator's lack of need for high DC gain. In traditional architectures, high DC gain is achieved with an integrator in the voltage loop. The integrator introduces a pole in the open-loop transfer function at low frequencies. Thus, combined with the double-pole from the output L/C filter, creates a three pole system that must be compensated to maintain stability.

Classic control theory requires a single-pole transition through unity gain to ensure a stable system. Current-mode architectures (includes peak, peak-valley, current-mode hysteretic, R3™ and R4™) generate a zero at or near the L/C resonant point, effectively canceling one of the system's poles. The system still contains two poles, one of which must be canceled with a zero before unity gain crossover to achieve stability. Compensation components are added to introduce the necessary zero.

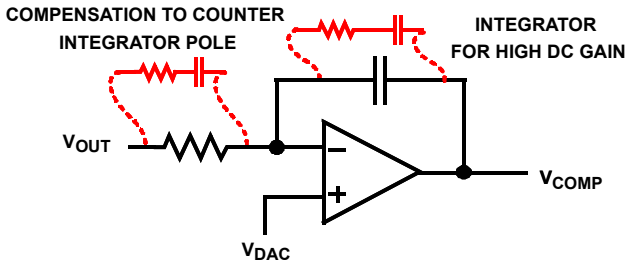

FIGURE 8. INTEGRATOR ERROR-AMPLIFIER CONFIGURATION

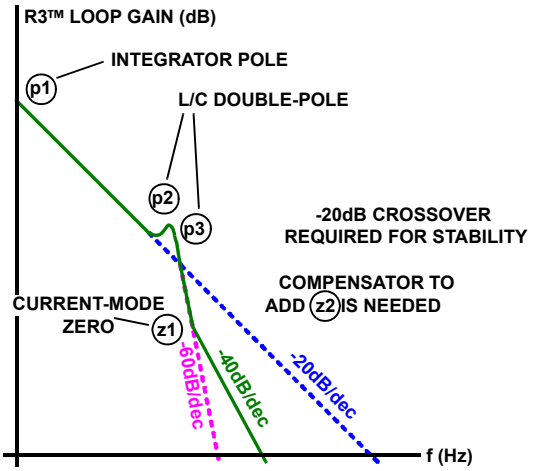

FIGURE 9. UNCOMPENSATED INTEGRATOR OPEN-LOOP RESPONSE

Figure 8 illustrates the classic integrator configuration for a voltage loop error-amplifier. While the integrator provides the high DC gain required for accurate regulation in traditional technologies, it also introduces a low-frequency pole into the control loop. Figure 9 shows the open-loop response that results from the addition of an integrating capacitor in the voltage loop. The compensation components found in Figure 8 are necessary to achieve stability.

Because R4™ does not require a high-gain voltage loop, the integrator can be removed, reducing the number of inherent poles in the loop to two. The current-mode zero continues to cancel one of the poles, ensuring a single-pole crossover for a wide range of output filter choices. The result is a stable system with no need for compensation components or complex equations to properly tune the stability.

Figure 10 shows the R4™ error-amplifier that does not require an integrator for high DC gain to achieve accurate regulation. The result to the open loop response can be seen in Figure 11.

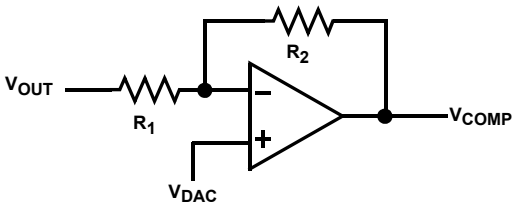

FIGURE 10. NON-INTEGRATED R4™ ERROR-AMPLIFIER CONFIGURATION

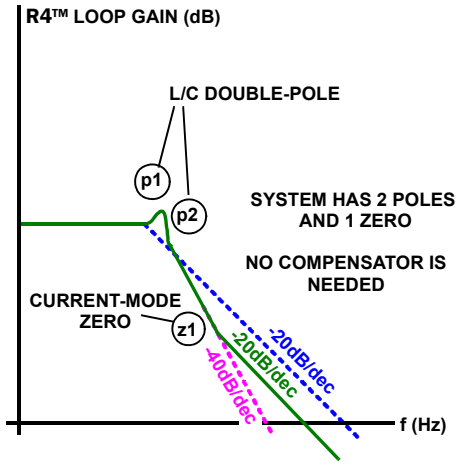

FIGURE 11. UNCOMPENSATED R4™ OPEN-LOOP RESPONSE

Transient Response

In addition to requiring a compensation zero, the integrator in traditional architectures also slows system response to transient conditions. The change in COMP voltage is slow in response to a rapid change in output voltage. If the integrating capacitor is removed, COMP moves as quickly as V_{OUT}, and the modulator immediately increases or decreases switching frequency to recover the output voltage.

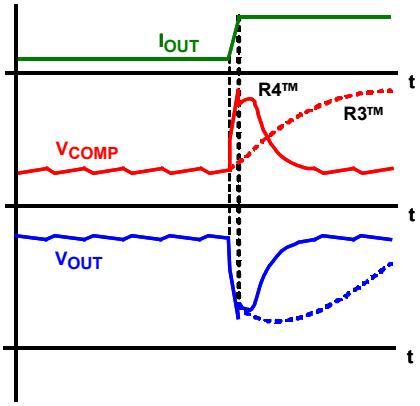

FIGURE 12. R3™ vs R4™ IDEALIZED TRANSIENT RESPONSE

The dotted red and blue lines in Figure 12 represent the time delayed behavior of V_{OUT} and V_{COMP} in response to a load transient when an integrator is used. The solid red and blue lines illustrate the increased response of R4™ in the absence of the integrator capacitor.

Diode Emulation

The polarity of the output inductor current is defined as positive when conducting away from the phase node, and defined as negative when conducting towards the phase node. The DC component of the inductor current is positive, but the AC component known as the ripple current, can be either positive or negative. Should the sum of the AC and DC components of the inductor current remain positive for the entire switching period, the converter is in continuous-conduction-mode (CCM). However, if the inductor current becomes negative or zero, the converter is in discontinuous-conduction-mode (DCM).

Unlike the standard DC/DC buck regulator, the synchronous rectifier can sink current from the output filter inductor during DCM, reducing the light-load efficiency with unnecessary conduction loss as the low-side MOSFET sinks the inductor current. The ISL95873 controller avoids the DCM conduction loss by making the low-side MOSFET emulate the current-blocking behavior of a diode. This smart-diode operation called diode-emulation-mode (DEM) is triggered when the negative inductor current produces a positive voltage drop across the $r_{DS(ON)}$ of the low-side MOSFET for eight consecutive PWM cycles while the LGATE pin is high. The converter will exit DEM on the next PWM pulse after detecting a negative voltage across the $r_{DS(ON)}$ of the low-side MOSFET.

It is characteristic of the R4™ architecture for the PWM switching frequency to decrease while in DCM, increasing efficiency by reducing unnecessary gate-driver switching losses. The extent of the frequency reduction is proportional to the reduction of load current. Upon entering DEM, the PWM frequency is forced to fall approximately 30% by forcing a similar increase of the window voltage V_W. This measure is taken to prevent oscillating between modes at the boundary between CCM and DCM. The 30% increase of V_W is removed upon exit of DEM, forcing the PWM switching frequency to jump back to the nominal CCM value.

Overcurrent

The overcurrent protection (OCP) setpoint is programmed with resistor R_{OCSET}, which is connected across the OCSET and PHASE pins. Resistor R_O is connected between the VO pin and the actual output voltage of the converter. During normal operation, the VO pin is a high impedance path, therefore there is no voltage drop across R_O. The value of resistor R_O should always match the value of resistor R_{OCSET}.

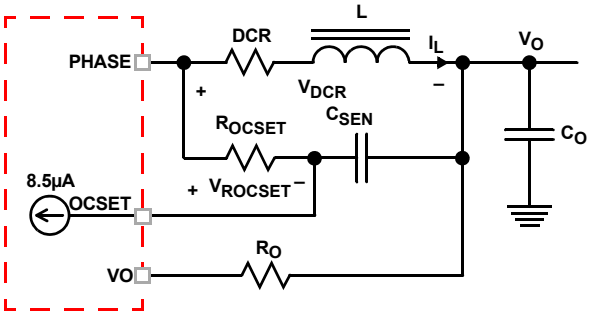

FIGURE 13. OVERCURRENT PROGRAMMING CIRCUIT

Figure 13 shows the overcurrent set circuit. The inductor consists of inductance L and the DC resistance DCR. The inductor DC current I_L creates a voltage drop across DCR, which is given by Equation 4:

$$V_{DCR} = I_L \cdot DCR \quad \text{(EQ. 4)}$$

The I_{OCSET} current source sinks 8.5µA into the OCSET pin, creating a DC voltage drop across the resistor R_{OCSET}, which is given by Equation 5:

$$V_{ROCSET} = 8.5\mu A \cdot R_{OCSET} \quad \text{(EQ. 5)}$$

The DC voltage difference between the OCSET pin and the VO pin, given by Equation 6:

$$V_{OCSET} - V_{VO} = V_{DCR} - V_{ROCSET} = I_L \cdot DCR - I_{OCSET} \cdot R_{OCSET} \quad \text{(EQ. 6)}$$

The IC monitors the voltage of the OCSET pin and the VO pin. When the voltage of the OCSET pin is higher than the voltage of the VO pin for more than 10µs, an OCP fault latches the converter off.

The value of R_{OCSET} is calculated with Equation 7, which is written as:

$$R_{OCSET} = \frac{I_{OC} \cdot DCR}{I_{OCSET}} \quad \text{(EQ. 7)}$$

Where:

- R_{OCSET} (Ω) is the resistor used to program the overcurrent setpoint
- I_{OC} is the output DC load current that will activate the OCP fault detection circuit
- DCR is the inductor DC resistance

For example, if I_{OC} is 20A and DCR is 4.5mΩ, the choice of R_{OCSET} is equal to 20A x 4.5mΩ/8.5µA = 10.5kΩ.

Resistor R_{OCSET} and capacitor C_{SEN} form an R-C network to sense the inductor current. To sense the inductor current correctly not only in DC operation, but also during dynamic operation, the R-C network time constant R_{OCSET} C_{SEN} needs to match the inductor time constant L/DCR. The value of C_{SEN} is then written as Equation 8:

$$C_{SEN} = \frac{L}{R_{OCSET} \cdot DCR} \quad \text{(EQ. 8)}$$

For example, if L is 1.5µH, DCR is 4.5mΩ, and R_{OCSET} is 9kΩ, the choice of C_{SEN} = 1.5µH/(9kΩ x 4.5mΩ) = 0.037µF.

When an OCP fault is declared, the converter will be latched off and the PGOOD pin will be asserted low. The fault will remain latched until the EN pin has been pulled below the falling EN threshold voltage V_{ENTHF} or if VCC has decayed below the falling POR threshold voltage V_{VCC_THF}.

Overvoltage

The overvoltage (OV) detection circuit triggers after the FB pin voltage is above the rising overvoltage threshold V_{OVRTH} for more than 2µs. For example, if the converter is programmed to regulate 1.0V at the FB pin, that voltage would have to rise above the typical V_{OVRTH} threshold of 116% for more than 2µs to trigger an OV. In numerical terms, that would be 116% x 1.0V = 1.16V. When an OV is detected, the converter will take PGOOD low and continue to switching. The converter is not latched off. When the converter output voltage drops below the falling overvoltage threshold, V_{OVFTH}, for more than 2µs then PGOOD is taken high again and the OV detection is considered cleared.

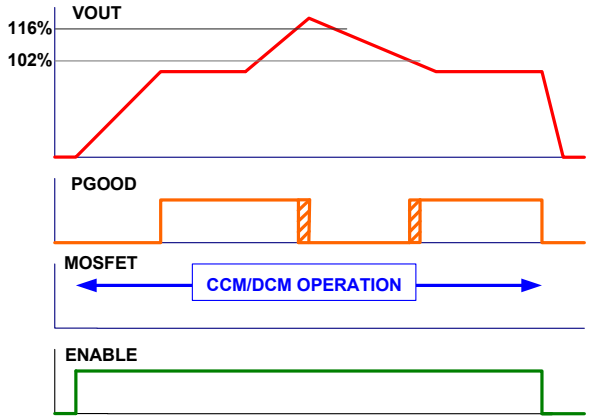

FIGURE 14. OVERVOLTAGE OPERATION

The falling overvoltage threshold V_{OVFTH} is typically 102%. That means if the FB pin voltage falls below 102% x 1.0V = 1.02V for more than 2µs, the controller will return PGOOD high. Figure 14 shows a simple illustration of PGOOD operation during an OV detection event. The cross hatch portion of the PGOOD waveform shown represents the 2µs recognition time prior to the PGOOD transition.

Undervoltage

The UVP fault detection circuit triggers after the FB pin voltage is below the undervoltage threshold V_{UVTH} for more than 2µs. For example, if the converter is programmed to regulate 1.0V at the FB pin, that voltage would have to fall below the typical V_{UVTH} threshold of 84% for more than 2µs in order to trip the UVP fault latch. In numerical terms, that would be 84% x 1.0V = 0.84V. When a UVP fault is declared, the converter will be latched off and the PGOOD pin will be asserted low. The fault will remain latched until the EN pin has been pulled below the falling EN threshold voltage V_{ENTHF} or if VCC has decayed below the falling POR threshold voltage V_{VCC_THF}.

Over-Temperature

When the temperature of the IC increases above the rising threshold temperature T_{OTRTH}, it will enter the OTP state that suspends the PWM, forcing the LGATE and UGATE gate-driver outputs low. The status of the PGOOD pin does not change nor does the converter latch-off. The PWM remains suspended until the IC temperature falls below the hysteresis temperature T_{OTHYS} at which time normal PWM operation resumes. The OTP state can be reset if the EN pin is pulled below the falling EN threshold voltage V_{ENTHF} or if VCC has decayed below the falling POR threshold voltage V_{VCC_THF}. All other protection circuits remain functional while the IC is in the OTP state. It is likely that the IC will detect an UVP fault because in the absence of PWM, the output voltage decays below the undervoltage threshold V_{UVTH}.

PGOOD Monitor

The PGOOD pin indicates when the converter is capable of supplying regulated voltage. The PGOOD pin is an undefined impedance if the VCC pin has not reached the rising POR threshold V_{VCC_THR}, or if the VCC pin is below the falling POR threshold V_{VCC_THF}. If there is a fault condition of output overcurrent or undervoltage, PGOOD is asserted low. The PGOOD pull-down impedance is 50Ω.

The PGOOD pin will transition low when an OV condition is detected, but will return high when the OV condition is removed.

Integrated MOSFET Gate-Drivers

The LGATE pin and UGATE pins are MOSFET driver outputs. The LGATE pin drives the low-side MOSFET of the converter while the UGATE pin drives the high-side MOSFET of the converter.

The LGATE driver is optimized for low duty-cycle applications where the low-side MOSFET experiences long conduction times. In this environment, the low-side MOSFETs require exceptionally low $r_{DS(ON)}$ and tend to have large parasitic charges that conduct transient currents within the devices in response to high dv/dt switching present at the phase node. The drain-gate charge in particular can conduct sufficient current through the driver pull-down resistance that the $V_{GS(th)}$ of the device can be exceeded and turned on. For this reason, the LGATE driver has been designed with low pull-down resistance and high sink current capability to ensure clamping the MOSFETs gate voltage below $V_{GS(th)}$.

Adaptive Shoot-Through Protection

Adaptive shoot-through protection prevents a gate-driver output from turning on until the opposite gate-driver output has fallen below approximately 1V. The dead-time shown in Figure 15 is extended by the additional period that the falling gate voltage remains above the 1V threshold. The high-side gate-driver output voltage is measured across the UGATE and PHASE pins while the low-side gate-driver output voltage is measured across the LGATE and PGND pins. The power for the LGATE gate-driver is sourced directly from the PVCC pin. The power for the UGATE gate-driver is supplied by a boot-strap capacitor connected across the BOOT and PHASE pins. The capacitor is charged each time the phase node voltage falls a diode drop below PVCC such as when the low-side MOSFET is turned on.

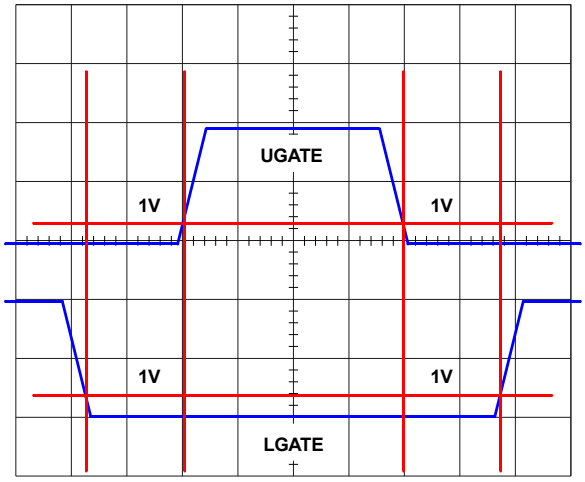

FIGURE 15. GATE DRIVE ADAPTIVE SHOOT-THROUGH PROTECTION

General Application Design Guide

This design guide is intended to provide a high-level explanation of the steps necessary to design a single-phase buck converter. It is assumed that the reader is familiar with many of the basic skills and techniques referenced in the following. In addition to this guide, Intersil provides complete reference designs that include schematics, bill of materials, and example board layouts.

Selecting the LC Output Filter

The duty cycle of an ideal buck converter is a function of the input and the output voltage. This relationship is expressed in Equation 9:

$$D = \frac{V_O}{V_{IN}} \quad \text{(EQ. 9)}$$

The output inductor peak-to-peak ripple current is expressed in Equation 10:

$$I_{P\text{-}P} = \frac{V_O \cdot (1 - D)}{F_{SW} \cdot L} \quad \text{(EQ. 10)}$$

A typical step-down DC/DC converter will have an $I_{P\text{-}P}$ of 20% to 40% of the maximum DC output load current. The value of $I_{P\text{-}P}$ is selected based upon several criteria, such as MOSFET switching loss, inductor core loss, and the resistive loss of the inductor winding. The DC copper loss of the inductor can be estimated using Equation 11:

$$P_{COPPER} = I_{LOAD}^{2} \cdot DCR \quad \text{(EQ. 11)}$$

Where, I_{LOAD} is the converter output DC current.

The copper loss can be significant so close attention needs to be given to the DCR of the inductor. Another factor to consider when choosing the inductor is its saturation characteristics at elevated temperature. A saturated inductor could cause destruction of circuit components, as well as nuisance OCP faults.

A DC/DC buck regulator must have output capacitance C_O into which ripple current I_{P-P} can flow. Current I_{P-P} develops a corresponding ripple voltage V_{P-P} across C_O, which is the sum of the voltage drop across the capacitor ESR and of the voltage change stemming from charge moved in and out of the capacitor. These two voltages are expressed in Equations 12 and 13:

$$\Delta V_{ESR} = I_{P-P} \cdot ESR \quad \text{(EQ. 12)}$$

$$\Delta V_C = \frac{I_{P-P}}{8 \cdot C_O \cdot F_{SW}} \quad \text{(EQ. 13)}$$

If the output of the converter has to support a load with high pulsating current, several capacitors will need to be paralleled to reduce the total ESR until the required V_{P-P} is achieved. The inductance of the capacitor can significantly impact the output voltage ripple and cause a brief voltage spike if the load transient has an extremely high slew rate. Low inductance capacitors should be considered. A capacitor dissipates heat as a function of RMS current and frequency. Be sure that I_{P-P} is shared by a sufficient quantity of paralleled capacitors so that they operate below the maximum rated RMS current at F_{SW}. Take into account that the rated value of a capacitor can fade as much as 50% as the DC voltage across it increases.

Selecting the Input Capacitor

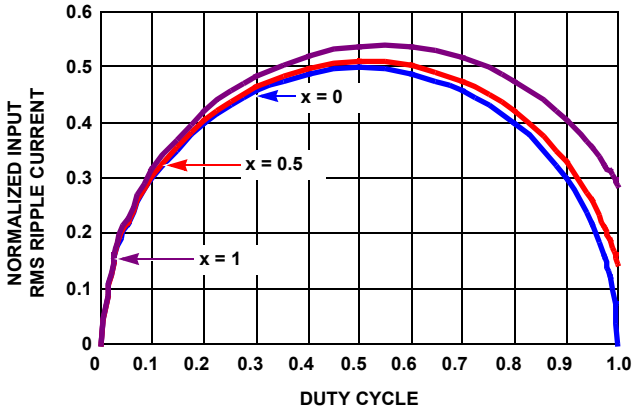

FIGURE 16. NORMALIZED INPUT RMS CURRENT FOR EFF = 1

The important parameters for the bulk input capacitors are the voltage rating and the RMS current rating. For reliable operation, select bulk capacitors with voltage and current ratings above the maximum input voltage and capable of supplying the RMS current required by the switching circuit. Their voltage rating should be at least 1.25x greater than the maximum input voltage, while a voltage rating of 1.5x is a preferred rating. Figure 16 is a graph of the input RMS ripple current, normalized relative to output load current, as a function of duty cycle that is adjusted for converter efficiency. The ripple current calculation is written as Equation 14:

$$I_{IN\_RMS} = \frac{\sqrt{(I_{MAX}^2 \cdot (D - D^2)) + \left(x^2 \cdot I_{MAX}^2 \cdot \frac{D}{12}\right)}}{I_{MAX}} \quad \text{(EQ. 14)}$$

Where:

- I_{MAX} is the maximum continuous I_{LOAD} of the converter
- x is a multiplier (0 to 1) corresponding to the inductor peak-to-peak ripple amplitude expressed as a percentage of I_{MAX} (0% to 100%)
- D is the duty cycle that is adjusted to take into account the efficiency of the converter

Duty cycle is written as Equation 15:

$$D = \frac{V_O}{V_{IN} \cdot EFF} \quad \text{(EQ. 15)}$$

In addition to the bulk capacitors, some low ESL ceramic capacitors are recommended to decouple between the drain of the high-side MOSFET and the source of the low-side MOSFET.

Selecting the Bootstrap Capacitor

The integrated driver features an internal bootstrap Schottky diode. Simply adding an external capacitor across the BOOT and PHASE pins completes the bootstrap circuit. The bootstrap capacitor voltage rating is selected to be at least 10V. Although the theoretical maximum voltage of the capacitor is PVCC-V_{DIODE} (voltage drop across the boot diode), large excursions below ground by the phase node requires at least a 10V rating for the bootstrap capacitor. The bootstrap capacitor can be chosen from Equation 16:

$$C_{BOOT} \geq \frac{Q_{GATE}}{\Delta V_{BOOT}} \quad \text{(EQ. 16)}$$

Where:

- Q_{GATE} is the amount of gate charge required to fully charge the gate of the upper MOSFET
- ΔV_{BOOT} is the maximum decay across the BOOT capacitor

As an example, suppose the high-side MOSFET has a total gate charge Q_g, of 25nC at V_{GS} = 5V, and a ΔV_{BOOT} of 200mV. The calculated bootstrap capacitance is 0.125µF; for a comfortable margin, select a capacitor that is double the calculated capacitance. In this example, 0.22µF will suffice. Use a low temperature-coefficient ceramic capacitor.

Driver Power Dissipation

Switching power dissipation in the driver is mainly a function of the switching frequency and total gate charge of the selected MOSFETs. Calculating the power dissipation in the driver for a desired application is critical to ensuring safe operation. Exceeding the maximum allowable power dissipation level will push the IC beyond the maximum recommended operating junction temperature of +125°C. When designing the application, it is recommended that the following calculation be performed to ensure safe operation at the desired frequency for the selected MOSFETs. The power dissipated by the drivers is approximated as Equation 17:

$$P = F_{sw}(1.5V_U Q_U + V_L Q_L) + P_L + P_U \quad \text{(EQ. 17)}$$

Where:

- F_{SW} is the switching frequency of the PWM signal
- V_U is the upper gate driver bias supply voltage
- V_L is the lower gate driver bias supply voltage
- Q_U is the charge to be delivered by the upper driver into the gate of the MOSFET and discrete capacitors
- Q_L is the charge to be delivered by the lower driver into the gate of the MOSFET and discrete capacitors
- P_L is the quiescent power consumption of the lower driver
- P_U is the quiescent power consumption of the upper driver

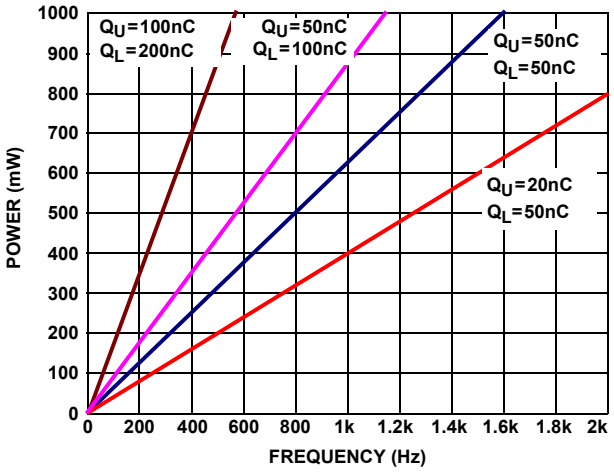

FIGURE 17. POWER DISSIPATION vs FREQUENCY

MOSFET Selection and Considerations

The choice of MOSFETs depends on the current each MOSFET will be required to conduct, the switching frequency, the capability of the MOSFETs to dissipate heat, and the availability and nature of heat sinking and air flow.

Typically, a MOSFET cannot tolerate even brief excursions beyond their maximum drain-to-source voltage rating. The MOSFETs used in the power stage of the converter should have a maximum V_{DS} rating that exceeds the sum of the upper voltage tolerance of the input power source and the voltage spike that occurs when the MOSFETs switch.

There are several power MOSFETs readily available that are optimized for DC/DC converter applications. The preferred high-side MOSFET emphasizes low gate charge so that the device spends the least amount of time dissipating power in the linear region. The preferred low-side MOSFET emphasizes low $r_{DS(ON)}$ when fully saturated to minimize conduction loss.

For the low-side MOSFET, (LS), the power loss can be assumed to be conductive only and is written as Equation 18:

$$P_{CON\_LS} \approx I_{LOAD}^{2} \cdot r_{DS(ON)\_LS} \cdot (1 - D) \quad \text{(EQ. 18)}$$

For the high-side MOSFET, (HS), its conduction loss is written as Equation 19:

$$P_{CON\_HS} = I_{LOAD}^{2} \cdot r_{DS(ON)\_HS} \cdot D \quad \text{(EQ. 19)}$$

For the high-side MOSFET, its switching loss is written as Equation 20:

$$P_{SW\_HS} = \frac{V_{IN} \cdot I_{VALLEY} \cdot t_{ON} \cdot F_{SW}}{2} + \frac{V_{IN} \cdot I_{PEAK} \cdot t_{OFF} \cdot F_{SW}}{2} \quad \text{(EQ. 20)}$$

Where:

- I_{VALLEY} is the difference of the DC component of the inductor current minus 1/2 of the inductor ripple current
- I_{PEAK} is the sum of the DC component of the inductor current plus 1/2 of the inductor ripple current
- t_{ON} is the time required to drive the device into saturation
- t_{OFF} is the time required to drive the device into cut-off

Layout Considerations

As a general rule, power layers should be close together, either on the top or bottom of the board, with the weak analog or logic signal layers on the opposite side of the board. The ground-plane layer should be adjacent to the signal layer to provide shielding. The ground plane layer should have an island located under the IC, the components connected to analog or logic signals. The island should be connected to the rest of the ground plane layer at one quiet point.

There are two sets of components in a DC/DC converter; the power components and the small signal components. The power components are the most critical because they switch large amount of energy. The small signal components connect to sensitive nodes or supply critical bypassing current and signal coupling.

The power components should be placed first and these include MOSFETs, input and output capacitors, and the inductor. Keeping the distance between the power train and the control IC short helps keep the gate drive traces short. These drive signals include the LGATE, UGATE, PGND, PHASE and BOOT.

When placing MOSFETs, try to keep the source of the upper MOSFETs and the drain of the lower MOSFETs as close as thermally possible (see Figure 18). Input high frequency capacitors should be placed close to the drain of the upper MOSFETs and the source of the lower MOSFETs. Place the output inductor and output capacitors between the MOSFETs and the load. High frequency output decoupling capacitors (ceramic) should be placed as close as possible to the decoupling target, making use of the shortest connection paths to any internal planes. Place the components in such a way that the area under the IC has less noise traces with high dV/dt and di/dt, such as gate signals and phase node signals.

VCC AND PVCC PINS

Place the decoupling capacitors as close as practical to the IC. In particular, the PVCC decoupling capacitor should have a very short and wide connection to the PGND pin. The VCC decoupling capacitor should be referenced to GND pin.

EN AND PGOOD PINS

These are logic signals that are referenced to the GND pin. Treat as a typical logic signal.

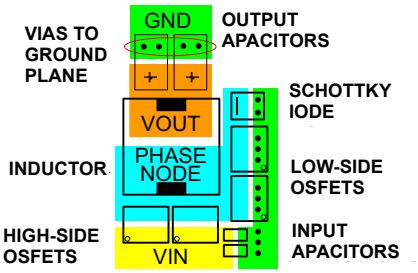

FIGURE 18. TYPICAL POWER COMPONENT PLACEMENT

OCSET AND VO PINS

The current-sensing network consisting of R_{OCSET}, R_O, and C_{SEN} needs to be connected to the inductor pads for accurate measurement of the DCR voltage drop. These components however, should be located physically close to the OCSET and VO pins with traces leading back to the inductor. It is critical that the traces are shielded by the ground plane layer all the way to the inductor pads. The procedure is the same for resistive current sense.

FB, SREF, REFIN, AND RTN PINS

The input impedance of these pins is high, making it critical to place the components connected to these pins as close as possible to the IC.

LGATE, PGND, UGATE, BOOT, AND PHASE PINS

The signals going through these traces are high dv/dt and high di/dt, with high peak charging and discharging current. The PGND pin can only flow current from the gate-source charge of the low-side MOSFETs when LGATE goes low. Ideally, route the trace from the LGATE pin in parallel with the trace from the PGND pin, route the trace from the UGATE pin in parallel with the trace from the PHASE pin. In order to have more accurate zero-crossing detection of inductor current, it is recommended to connect the PHASE pin to the drain of the low-side MOSFETs with Kelvin connection. These pairs of traces should be short, wide, and away from other traces with high input impedance; weak signal traces should not be in proximity with these traces on any layer.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
December 10, 2012	FN8390.0	Initial Release.

About Intersil

Intersil Corporation is a leader in the design and manufacture of high-performance analog, mixed-signal and power management semiconductors. The company's products address some of the fastest growing markets within the industrial and infrastructure, personal computing and high-end consumer markets. For more information about Intersil or to find out how to become a member of our winning team, visit our website and career page at www.intersil.com.

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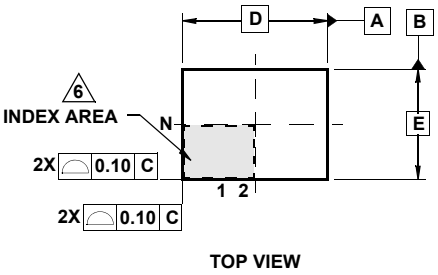
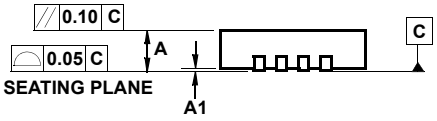
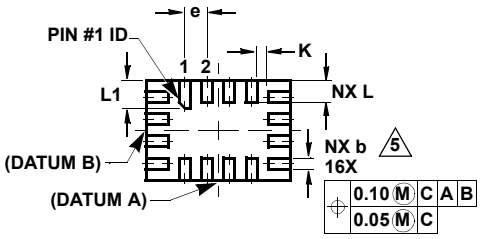
Ultra Thin Quad Flat No-Lead Plastic Package (UTQFN)



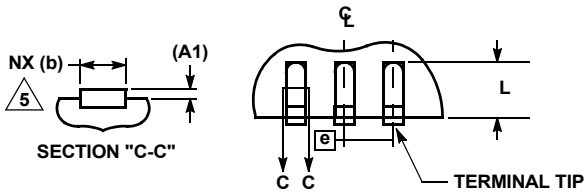
TOP VIEW

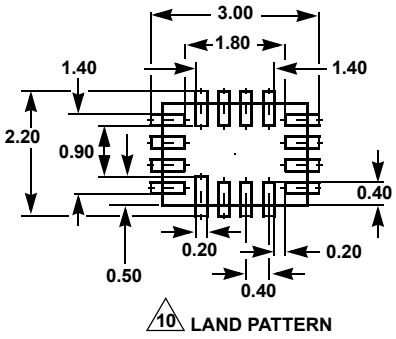


SIDE VIEW



BOTTOM VIEW





L16.2.6x1.8A

16 LEAD ULTRA THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.45	0.50	0.55	-
A1	-	-	0.05	-
A3		0.127 REF		-
b	0.15	0.20	0.25	5
D	2.55	2.60	2.65	-
E	1.75	1.80	1.85	-
e		0.40 BSC		-
K	0.15	-	-	-
L	0.35	0.40	0.45	-
L1	0.45	0.50	0.55	-
N		16		2
Nd		4		3
Ne		4		3
θ	0	-	12	4

Rev. 5 2/09

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on D and E side, respectively.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Maximum package warpage is 0.05mm.
8. Maximum allowable burrs is 0.076mm in all directions.
9. JEDEC Reference MO-255.
10. For additional information, to assist with the PCB Land Pattern Design effort, see Intersil Technical Brief TB389.