FAIRCHILD
A Schlumberger Company

μA8T26A • μA8T28 Quad 3-State Bus Transceivers

Interface Products

Description

μA8T26A and μA8T28 are Quad 3-State Bus Transceivers featuring MPU or MOS compatibility. Both parts feature high-impedance pnp inputs and high-speed operation made possible by the use of Schottky transistor technology.

These devices are useful as bus extenders in systems employing the F6800, F3870 or other comparable MPU families. Maximum input current of 200 μA at the device input pins assures proper operation despite limited drive capability of the MPU chip.

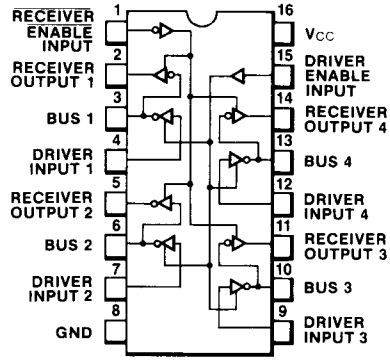
The μA8T26A/28 are identical to the NE8T26A/28 or the MC8T26A/28.

- **μA8T26A—INVERTING BUS**
- **μA8T28—NON-INVERTING**
- **MPU COMPATIBLE**
- **HIGH-IMPEDANCE pnp INPUTS**
- **HIGH-SPEED SCHOTTKY TECHNOLOGY**
- **+5 V SINGLE SUPPLY OPERATION**
- **3-STATE DRIVERS AND RECEIVERS**

Absolute Maximum Ratings	T_A = 25°C unless otherwise noted
Power Supply Voltage (V_{CC})	8.0 V
Input Voltage (V_I)	5.5 V
Junction Temperature (T_J)	
Ceramic DIP	175°C
Molded DIP	150°C
Operating Temperature	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Pin Temperature	
Molded DIP (Soldering, 10 s)	260°C
Ceramic DIP (Soldering, 60 s)	300°C

Connection Diagrams
16-Pin DIP

μA8T26A

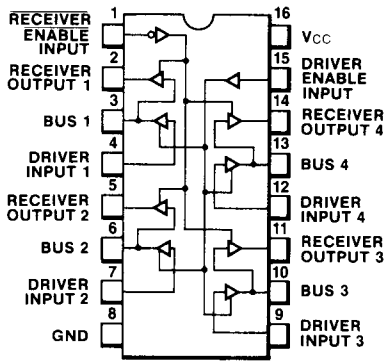


(Top View)

Order Information

Type	Package	Code	Part No.
μA8T26A	Ceramic DIP	6B	μA8T26ADM
μA8T26A	Ceramic DIP	6B	μA8T26ADC
μA8T26A	Molded DIP	9B	μA8T26APC

Connection Diagram
μA8T28

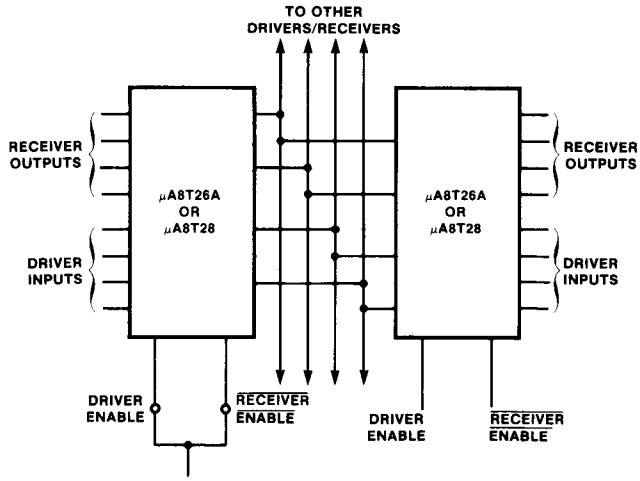


(Top View)

Order Information

Type	Package	Code	Part No.
μA8T28	Ceramic DIP	6B	μA8T28DM
μA8T28	Ceramic DIP	6B	μA8T28DC
μA8T28	Molded DIP	9B	μA8T28PC

Bidirectional Bus Application



DC Characteristics 4.75 V ≤ V_{CC} ≤ 5.25 V for 0°C ≤ T_A ≤ 70°C, and 4.5 V ≤ V_{CC} ≤ 5.5 V for −55°C ≤ T_A ≤ +125°C, unless otherwise noted

Symbol	Characteristic	Min	Typ	Max	Unit
	Input Current, LOW Logic State				
$I_{IL(\overline{RE})}$	Receiver Enable Input, $V_{IL(RE)}$ = 0.4 V			−200	μA
$I_{IL(DE)}$	Driver Enable Input, $V_{IL(DE)}$ = 0.4 V			−200	
$I_{IL(D)}$	Driver Input, $V_{IL(D)}$ = 0.4 V			−200	
$I_{IL(B)}$	Bus Receiver Input, $V_{IL(B)}$ = 0.4 V			−200	
	Input Disabled Current, LOW Logic State				
$I_{IL(D)DIS}$	Driver Input, $V_{IL(D)}$ = 0.4 V			−25	μA
	Input Current, HIGH Logic State				
$I_{IH(\overline{RE})}$	Receiver Enable Input, $V_{IH(RE)}$ = 5.25 V			25	μA
$I_{IH(DE)}$	Driver Enable Input, $V_{IH(DE)}$ = 5.25 V			25	
$I_{IH(D)}$	Driver Input, $V_{IH(D)}$ = 5.25 V			25	
$I_{IH(B)}$	Receiver Input, $V_{IH(B)}$ = 5.25 V (μA8T26 only)			100	
	Input Voltage, LOW Logic State				
$V_{IL(\overline{RE})}$	Receiver Enable Input			0.85	V
$V_{IL(DE)}$	Driver Enable Input			0.85	
$V_{IL(D)}$	Driver Input			0.85	
$V_{IL(B)}$	Receiver Input			0.85	
	Input Voltage, HIGH Logic State				
$V_{IH(RE)}$	Receiver Enable Input	2.0			V
$V_{IH(DE)}$	Driver Enable Input	2.0			
$V_{IH(D)}$	Driver Input	2.0			
$V_{IH(B)}$	Receiver Input	2.0			
	Output Voltage, LOW Logic State				
$V_{OL(B)}$	Bus Driver Output, $I_{OL(B)}$ = 48 mA			0.5	V
$V_{OL(R)}$	Receiver Output, $I_{OL(R)}$ = 20 mA			0.5	
	Output Voltage, HIGH Logic State				
$V_{OH(B)}$	Bus Driver Output, $I_{OH(B)}$ = −10 mA	2.4	3.1		V
$V_{OH(R)}$	Receiver Output, $I_{OH(R)}$ = −2.0 mA	2.4	3.1		
	Receiver Output, $I_{OH(R)}$ = −100 μA, VCC = 5.0 V	3.5			
	Output Disabled Leakage Current HIGH Logic State				
$I_{OHL(B)}$	Bus Driver Output, $V_{OH(B)}$ = 2.4 V			100	μA
$I_{OHL(R)}$	Receiver Output, $V_{OH(R)}$ = 2.4 V			100	

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DC Characteristics (Cont.) $4.75\ V \leq V_{CC} \leq 5.25\ V$ for $0°C \leq T_A \leq 70°C$, and $4.5\ V \leq V_{CC} \leq 5.5\ V$ for $-55°C \leq T_A \leq +125°C$, unless otherwise noted

Symbol	Characteristic	Min	Typ	Max	Unit
	Output Disabled Leakage Current LOW Logic State				
$I_{OLL(B)}$	Bus Output, $V_{OL(B)} = 0.5\ V$			−100	μA
$I_{OLL(R)}$	Receiver Output, $V_{OL(R)} = 0.5\ V$			−100	
	Input Clamp Voltage				
$V_{IC(DE)}$	Driver Enable Input $I_{IC(DE)} = -12\ mA$			−1.0	V
$V_{IC(RE)}$	$\overline{\text{Receiver Enable}}$ Input $I_{IC(RE)} = -12\ mA$			−1.0	
$V_{IC(D)}$	Driver Input $I_{IC(D)} = -12\ mA$			−1.0	
	Output Short-Circuit Current, $V_{CC} = 5.25\ V$, Note				
$I_{OS(B)}$	Bus Driver Output	−50	80	−150	mA
$I_{OS(R)}$	Receiver Output	−30	50	−75	
	Power Supply Current				
I_{CC}	$V_{CC} = 5.25\ V$		50	87	mA

Note
Only one output may be short-circuited at a time

μA8T26A AC Characteristics Unless otherwise noted, specifications apply at $T_A = 25°C$ and $V_{CC} = 5.0\ V$.

Symbol	Characteristic	Figure	Typ	Max	Unit
$t_{PLH(R)}$	Propagation Delay Time from Receiver (Bus) Input to HIGH Logic State Receiver Output	1	9	14	ns
$t_{PHL(R)}$	Propagation Delay Time from Receiver (Bus) Input to LOW Logic State Receiver Output	1	6	14	ns
$t_{PLH(D)}$	Propagation Delay Time from Driver Input to HIGH Logic State Driver (Bus) Output	2	10	14	ns
$t_{PHL(D)}$	Propagation Delay Time from Driver Input to LOW Logic State Driver (Bus) Output	2	10	14	ns
$t_{PLZ(RE)}$	Propagation Delay Time from $\overline{\text{Receiver Enable}}$ Input to HIGH Impedance (Open) Logic State Receiver Output	3	10	15	ns
$t_{PZL(RE)}$	Propagation Delay Time from $\overline{\text{Receiver Enable}}$ Input to LOW Logic Level Receiver Output	3	15	20	ns
$t_{PLZ(DE)}$	Propagation Delay Time from Driver Enable Input to HIGH Impedance Logic State Driver (Bus) Output	4	15	20	ns
$t_{PZL(DE)}$	Propagation Delay Time from Driver Enable Input to LOW Logic State Driver (Bus) Output	4	19	25	ns

μA8T28 AC Characteristics $T_A = 25°C$, $V_{CC} = 5.0\ V$ unless otherwise specified.

Symbol	Characteristic	Figure	Typ	Max	Unit
$t_{PLH(R)}$	Propagation Delay Time—Receiver ($C_L = 30\ pF$)	5	−12	17	ns
$t_{PHL(R)}$			−9	17	
$t_{PLH(D)}$	Propagation Delay Time—Driver ($C_L = 300\ pF$)	6	−13	17	ns
$t_{PHL(D)}$			−13	17	
$t_{PZL(RE)}$	Propagation Delay Time—Receiver Enable ($C_L = 30\ pF$)	7	−18	23	ns
$t_{PLZ(RE)}$			−13	18	
$t_{PZL(DE)}$	Propagation Delay Time—Driver Enable ($C_L = 300\ pF$)	8	−21	28	ns
$t_{PLZ(DE)}$			−18	23	

Fig. 1 μA8T26A Test Circuit and Waveforms for Propagation Delay Time from Bus (Receiver) Input to Receiver Output, $t_{PLH(R)}$ and $t_{PHL(R)}$

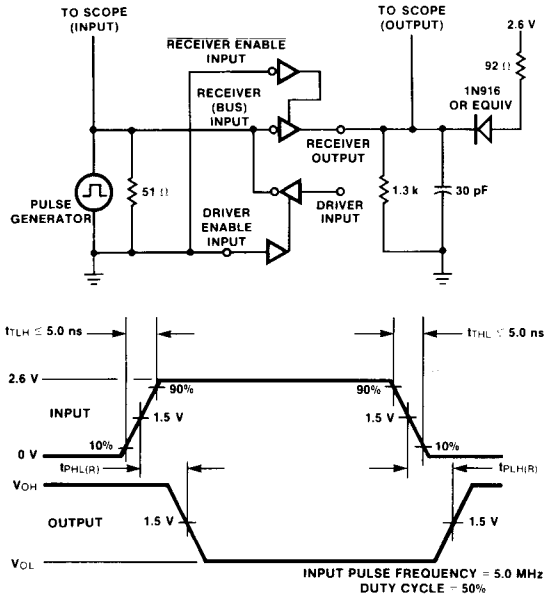

Fig. 2 μA8T26A Test Circuit and Waveforms for Propagation Delay Time from Driver Input to Bus (Driver) Output, $t_{PLH(D)}$ and $t_{PHL(D)}$

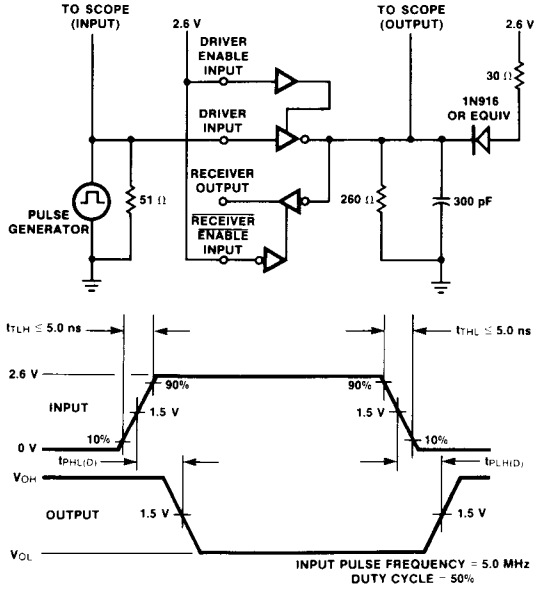

Fig. 3 μA8T26A Test Circuit and Waveforms for Propagation Delay Time from Receiver Enable Input to Receiver Output, $t_{PLZ(RE)}$ and $t_{PZL(RE)}$

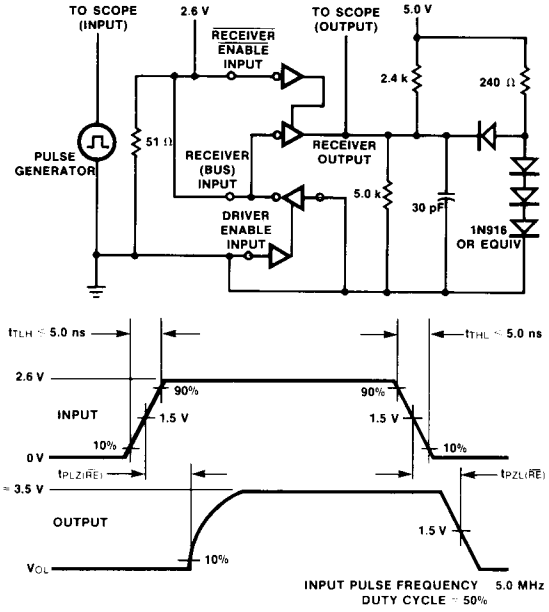

Fig. 4 μA8T26A Test Circuit and Waveforms for Propagation Delay Time from Driver Enable Input to Driver (Bus) Output, $t_{PLZ(DE)}$ and $t_{PZL(DE)}$

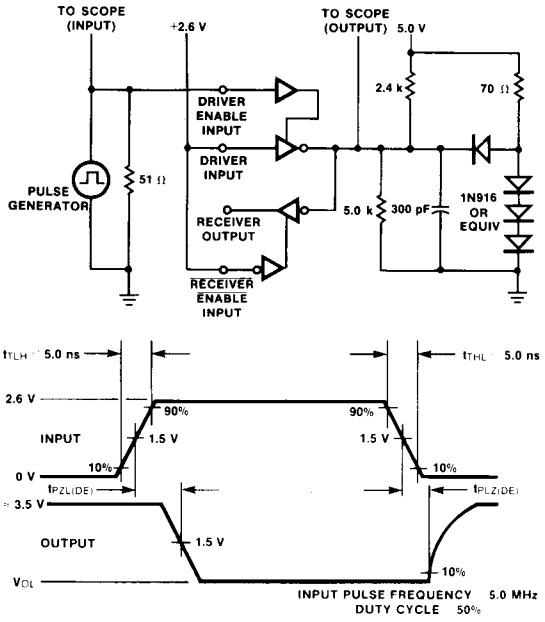

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Fig. 5 **μA8T28 Test Circuit and Waveforms for Propagation Delay Time from Bus (Receiver) Input to Receiver Output, $t_{PLH(R)}$ and $t_{PHL(R)}$**

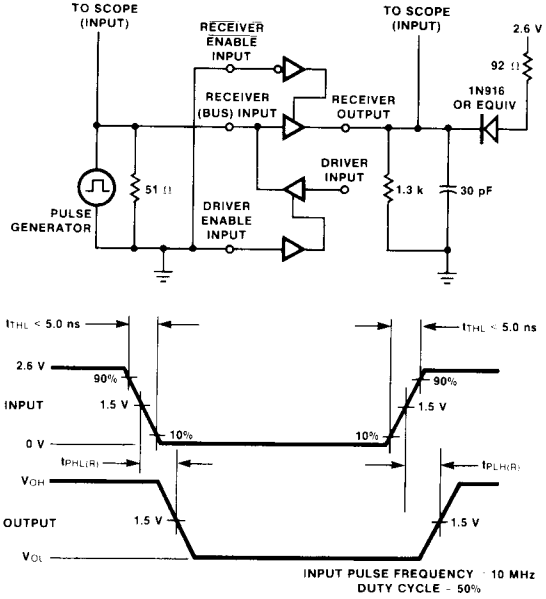


Fig. 6 **μA8T28 Test Circuit and Waveforms for Propagation Delay Time from Driver Input to Bus (Driver) Output, $t_{PLH(D)}$ and $t_{PHL(D)}$**

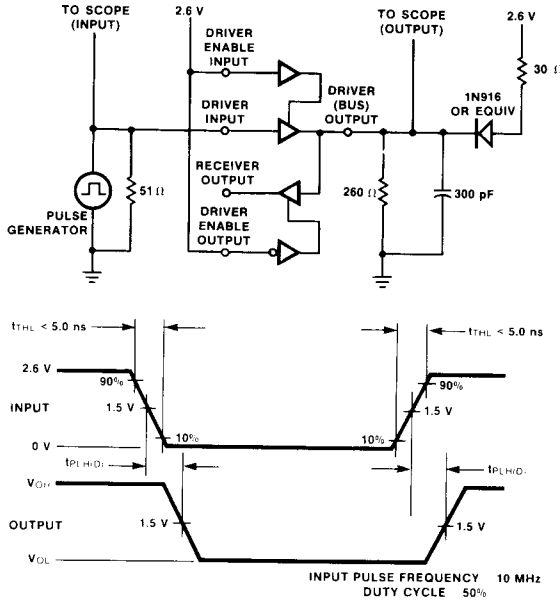


Fig. 7 **μA8T28 Test Circuit and Waveforms for Propagation Delay Time from Receiver Enable Input to Receiver Output, $t_{PLZ(RE)}$ and $t_{PZL(RE)}$**

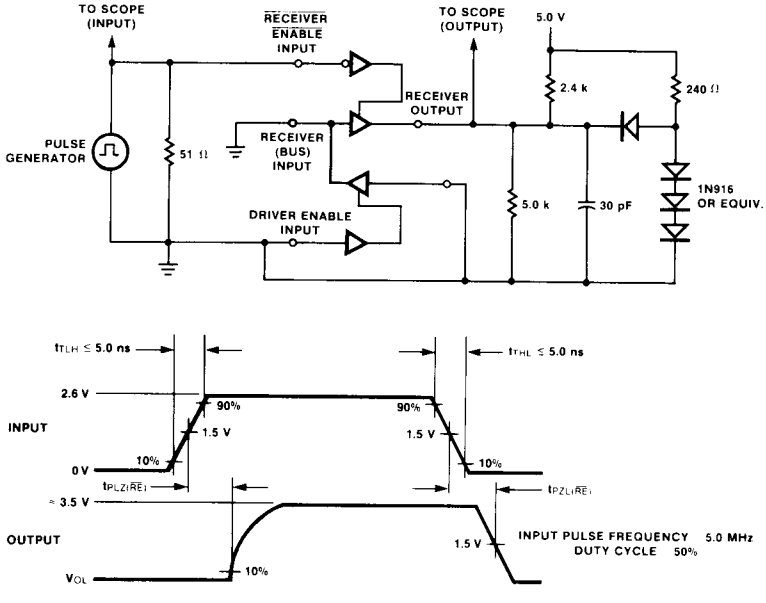
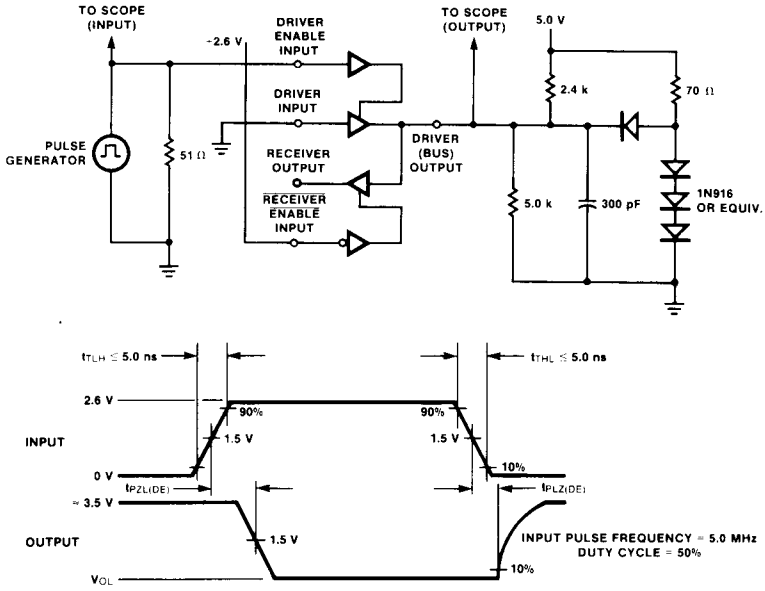


Fig. 8 μA8T28 Test Circuit and Waveforms for Propagation Delay Time from Driver Enable Input to Driver (Bus) Output, $t_{PLZ(DE)}$ and $t_{PZL(DE)}$



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