![Panasonic]

AN30185A

VIN = 2.9V to 5.5V 2ch,0.8A
General-purpose High Efficiency Power LSI

FEATURES

- High-speed response DC-DC Step-Down Regulator circuit that employs hysteretic control system : 2-ch (1.0 V, 0.8 A / 1.8 V, 0.8 A)
- LDO : 1-ch (0.9 V, 10 mA)
- Built-in external Pch MOSFET gate drive circuits
- Built-in Reset function
- Built-in Under Voltage Lockout function (UVLO)
- 24pin Plastic Quad Flat Non-leaded Package (Size : 4 × 4 mm, 0.5 mm pitch)

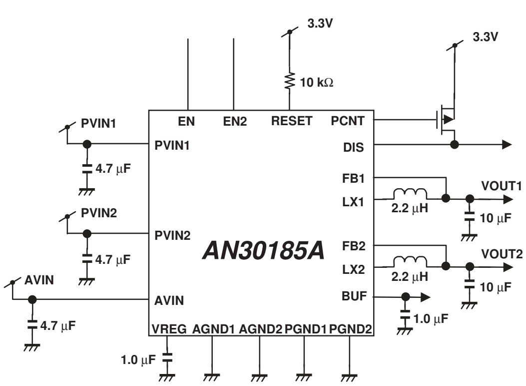
APPLICATIONS

High Current Distributed Power Systems such as SSD (Solid State Drive), Cellular Phone, etc.

DESCRIPTION

AN30185A is a power management LSI which has DC-DC step down regulators (2-ch) that employs hysteretic control system.
By this system, when load current changes suddenly, it responds at high speed and minimizes the changes of output voltage.
Since it is possible to use capacitors with small capacitance and it is unnecessary to use parts for phase compensation, this IC realizes downsizing of set and reducing in the number of external parts.
Output voltages are 1.0 V and 1.8 V. Each maximum current is 0.8 A.
This LSI has a LDO circuit, external Pch-MOSFET gate drive circuits and a reset circuit of input power supply voltage.

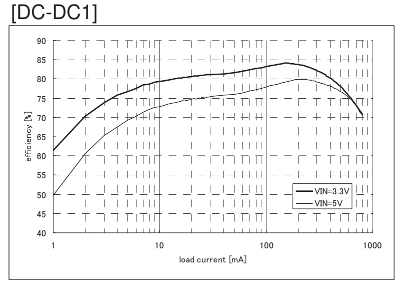
SIMPLIFIED APPLICATION



Notes) This application circuit is an example. The operation of mass production set is not guaranteed. You should perform enough evaluation and verification on the design of mass production set. You are fully responsible for the incorporation of the above application circuit and information in the design of your equipment.

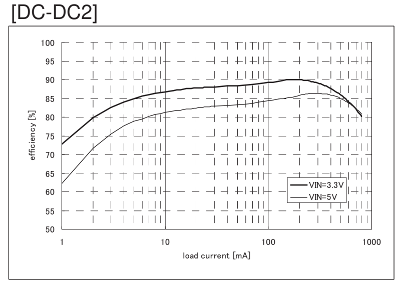
EFFICIENCY CURVE

[DC-DC1]



Condition : V_{IN}=3.3V or 5.0V , Vout=1.0V , Cout=10µF , Lout=2.2µH

[DC-DC2]



Condition : V_{IN}=3.3V or 5.0V , Vout=1.8V , Cout=10µF , Lout=2.2µH

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Notes
Supply voltage	V_{IN}	6.0	V	*1 *3
Operating free-air temperature	T_{opr}	– 40 to + 85	°C	*2
Operating junction temperature	T_j	– 40 to + 150	°C	*2
Storage temperature	T_{stg}	– 55 to + 150	°C	*2
Input Voltage Range	EN,EN2,FB1,FB2	– 0.3 to (V_{IN} + 0.3)	V	*1 *3
Output Voltage Range	LX1,LX2,PCNT,DIS, RESET,BUF,VREG	– 0.3 to (V_{IN} + 0.3)	V	*1 *3
ESD	HBM (Human Body Model)	2	kV	-

Notes) Do not apply external currents and voltages to any pin not specifically mentioned.
This product may sustain permanent damage if subjected to conditions higher than the above stated absolute maximum rating. This rating is the maximum rating and device operating at this range is not guaranteeable as it is higher than our stated recommended operating range. When subjected under the absolute maximum rating for a long time, the reliability of the product may be affected.
*1:The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.
*2:Except for the power dissipation, operating ambient temperature, and storage temperature, all ratings are for Ta = 25°C.
*3:V_{IN} is voltage for AVIN, PVIN1 = PVIN2,(V_{IN} + 0.3) V must not be exceeded 6 V.

POWER DISSIPATION RATING

PACKAGE	θ_{JA}	PD(Ta=25°C)	PD(Ta=85°C)	Notes
9pin Wafer level chip size package (WLCSP Type)	84.9 °C /W	1.472 W	0.765 W	*1

Note). For the actual usage, please refer to the PD-Ta characteristics diagram in the package specification, follow the power supply voltage, load and ambient temperature conditions to ensure that there is enough margin and the thermal design does not exceed the allowable value.
*1:Glass Epoxy Substrate(4 Layers) [Glass-Epoxy: 50 X 50 X 0.8t(mm)]
Die Pad Exposed , Soldered.

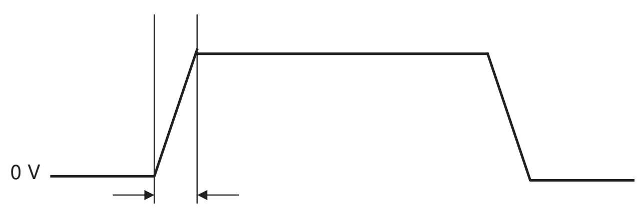
CAUTION

Although this has limited built-in ESD protection circuit, but permanent damage may occur on it.
Therefore, proper ESD precautions are recommended to avoid electrostatic damage to the MOS gates

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Supply voltage range	V_{IN}	2.9	3.3	5.5	V	*1 *2
Input Voltage Range	EN	– 0.3	—	V_{IN} + 0.3	V	*3
	EN2	– 0.3	—	V_{IN} + 0.3	V	*3
	FB1	– 0.3	—	V_{IN} + 0.3	V	*3
	FB2	– 0.3	—	V_{IN} + 0.3	V	*3
Output Voltage Range	LX1,LX2	– 0.3	—	V_{IN} + 0.3	V	*3
	PCNT	– 0.3	—	V_{IN} + 0.3	V	*3
	DIS	– 0.3	—	V_{IN} + 0.3	V	*3
	RESET	– 0.3	—	V_{IN} + 0.3	V	*3
	BUF	– 0.3	—	V_{IN} + 0.3	V	*3
	VREG	– 0.3	—	V_{IN} + 0.3	V	*3

Note) Do not apply external currents and voltages to any pin not specifically mentioned.
Voltage values, unless otherwise specified, are with respect to GND. GND is voltage for AGND1, AGND2, PGND1, PGND2. AGND1 = AGND2 = PGND1 = PGND2. Vin is voltage for AVIN, PVIN1, PVIN2. AVIN = PVIN1 = PVIN2.
*1 : Please set the rising time of power input pin to the following range.
In addition, please input the voltage with the rising time which has margin enough in consideration of the variation in external parts.
*2 : The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.
*3 : (V_{IN} + 0.3) V must not be exceeded 6 V.



100 µs < Tr < 1.5 ms
(Tr is the rise time from 0 V to the setup voltage of V_{IN}.)

ELECTRICAL CHARACTERISTICS

V_{IN} = AVIN = PVIN1 = PVIN2 = 3.3V
[DC-DC1] Cout = 10 µF (GRM21BB31A106K[Murata]) , Lout = 2.2 µH (NR3012T2R2M[Taiyo Yuden])
[DC-DC2] Cout = 10 µF (GRM21BB31A106K[Murata]) , Lout = 2.2 µH (NR3012T2R2M[Taiyo Yuden])
T_a = 25 °C ± 2 °C unless otherwise noted.

Parameter	Symbol	Conditions	Limits			Unit	Notes
			Min	Typ	Max		
[DC-DC1] (1.0 V DC/DC step-down regulator) [DC-DC2] (1.8 V DC/DC step-down regulator)							
Consumption current at active	IACT	EN = 3.3 V, I_{OUT1}, I_{OUT2}, $I_{OUT(BUF)}$ = 0 A	—	200	300	µA	—
EN pin Low-level input voltage	VENL	V_{IN} = 3.3 V	—	0	0.3	V	—
EN pin High-level input voltage	VENH	V_{IN} = 3.3 V	1.5	3.3	—	V	—
EN pin leak current	ILEAK EN	EN = 3.3 V	—	2.4	10	µA	—
EN2 pin Low-level input voltage	VEN2L	V_{IN} = 3.3 V	—	0	0.3	V	—
EN2 pin High-level input voltage	VEN2H	V_{IN} = 3.3 V	1.5	3.3	—	V	—
EN2 pin leak current	ILEAK EN2	EN2 = 3.3 V	—	2.0	10	µA	—
DC-DC1 output voltage	DD1 VOUT	I_{OUT1} = 450 mA	0.980	1.000	1.020	V	—
DC-DC2 output voltage	DD2 VOUT	I_{OUT2} = 500 mA	1.764	1.800	1.836	V	—
UVLO start voltage	VUVLO DET	V_{IN} = 3.3 V → 0 V	2.4	2.5	2.6	V	—
UVLO stop voltage	VUVLO RMV	V_{IN} = 0 V → 3.3 V	2.45	2.6	2.8	V	—
Reset detection voltage	VRST DET	V_{IN} = 3.3 V → 0 V	2.740	2.810	2.880	V	—
Reset cancel voltage	VRST RMV	V_{IN} = 0 V → 3.3 V	2.847	2.920	2.993	V	—
Reset ON resistance	RON RST	EN = 0 V	—	10	20	Ω	—
DIS discharge resistance	RON DIS	EN = 0 V	—	90	190	Ω	—
BUF output voltage	BUF VOUT	$I_{OUT(BUF)}$ = 10 µA	0.873	0.900	0.927	V	—

ELECTRICAL CHARACTERISTICS (Continued)

V_{IN} = AVIN = PVIN1 = PVIN2 = 3.3V
[DC-DC1] Cout = 10 μF (GRM21BB31A106K[Murata]) , Lout = 2.2 μH (NR3012T2R2M[Taiyo Yuden])
[DC-DC2] Cout = 10 μF (GRM21BB31A106K[Murata]) , Lout = 2.2 μH (NR3012T2R2M[Taiyo Yuden])
T_a = 25 °C ± 2 °C unless otherwise noted.

Parameter	Symbol	Conditions	Reference values			Unit	Notes
			Min	Typ	Max		
[DC-DC1] (1.0 V DC/DC step-down regulator) [DC-DC2] (1.8 V DC/DC step-down regulator)							
Consumption current at standby	ISTB	EN = 0 V	—	0	—	μA	*1
DC-DC1 line regulation	DD1 REGIN	V_{IN} = 2.9 V → 5.5 V I_{OUT1} = 450 mA	—	6	—	mV	*1
DC-DC2 line regulation	DD2 REGIN	V_{IN} = 2.9 V → 5.5 V I_{OUT2} = 500 mA	—	8	—	mV	*1
DC-DC1 load regulation	DD1 REGLD	I_{OUT1} = 10 μA → 800 mA	—	10	—	mV	*1
DC-DC2 load regulation	DD2 REGLD	I_{OUT2} = 10 μA → 800 mA	—	15	—	mV	*1
DC-DC1 output current limit	DD1 ILMT	FB1 = 1.0 V → 0.5 V	—	1.6	—	A	*1
DC-DC2 output current limit	DD2 ILMT	FB2 = 1.8 V → 0.9 V	—	1.6	—	A	*1
DC-DC1 efficiency 1	DD1 EFF1	V_{IN} = 3.3 V I_{OUT1} = 10 mA	—	77	—	%	*1
DC-DC1 efficiency 2	DD1 EFF2	V_{IN} = 5 V I_{OUT1} = 10 mA	—	71	—	%	*1
DC-DC1 efficiency 3	DD1 EFF3	V_{IN} = 3.3 V I_{OUT1} = 450 mA	—	80	—	%	*1
DC-DC1 efficiency 4	DD1 EFF4	V_{IN} = 5 V I_{OUT1} = 450 mA	—	77	—	%	*1
DC-DC2 efficiency 1	DD2 EFF1	V_{IN} = 3.3 V I_{OUT2} = 10 mA	—	86	—	%	*1
DC-DC2 efficiency 2	DD2 EFF2	V_{IN} = 5 V I_{OUT2} = 10 mA	—	80	—	%	*1
DC-DC2 efficiency 3	DD2 EFF3	V_{IN} = 3.3 V I_{OUT2} = 500 mA	—	85	—	%	*1
DC-DC2 efficiency 4	DD2 EFF4	V_{IN} = 5 V I_{OUT2} = 500 mA	—	84	—	%	*1
DC-DC1 output ripple voltage 1	DD1 VRPL1	I_{OUT1} = 10 mA	—	30	—	mV[p-p]	*1
DC-DC1 output ripple voltage 2	DD1 VRPL2	I_{OUT1} = 450 mA	—	7	—	mV[p-p]	*1
D-CDC2 output ripple voltage 1	DD2 VRPL1	I_{OUT2} = 10 mA	—	30	—	mV[p-p]	*1
DC-DC2 output ripple voltage 2	DD2 VRPL2	I_{OUT2} = 500 mA	—	7	—	mV[p-p]	*1

*1 : Typical Value checked by design.

ELECTRICAL CHARACTERISTICS (Continued)

V_{IN} = AVIN = PVIN1 = PVIN2 = 3.3V
[DC-DC1] Cout = 10 μF (GRM21BB31A106K[Murata]) , Lout = 2.2 μH (NR3012T2R2M[Taiyo Yuden])
[DC-DC2] Cout = 10 μF (GRM21BB31A106K[Murata]) , Lout = 2.2 μH (NR3012T2R2M[Taiyo Yuden])
T_a = 25 °C ± 2 °C unless otherwise noted.

Parameter	Symbol	Conditions	Reference values			Unit	Notes
			Min	Typ	Max		
[DC-DC1] (1.0 V DC/DC step-down regulator) [DC-DC2] (1.8 V DC/DC step-down regulator)							
DC-DC1 load transient response	DD1 DVAC	I_{OUT1} = 50 mA ↔ 200 mA Δ t = 1 μs	—	25	—	mV	*1
DC-DC2 load transient response	DD2 DVAC	I_{OUT2} = 10 mA ↔ 250 mA Δ t = 1 μs	—	25	—	mV	*1
DC-DC1 operating frequency	DD1 FSW	I_{OUT1} = 450 mA	—	1.2	—	MHz	*1
DC-DC2 operating frequency	DD2 FSW	I_{OUT2} = 500 mA	—	1.2	—	MHz	*1
DC-DC1 discharge resistance	DD1 RDIS	EN = 0 V	—	100	—	Ω	*1
DC-DC2 discharge resistance	DD2 RDIS	EN = 0 V	—	150	—	Ω	*1
DC-DC1 Pch-MOS ON resistance	DD1 RONP	—	—	0.25	—	Ω	*1
DC-DC2 Pch-MOS ON resistance	DD2 RONP	—	—	0.3	—	Ω	*1
DC-DC1 Nch-MOS ON resistance	DD1 RONN	—	—	0.2	—	Ω	*1
DC-DC2 Nch-MOS ON resistance	DD2 RONN	—	—	0.25	—	Ω	*1
DC-DC1 start time	DD1 TSTU	Capacitive load : 26 μF I_{OUT1} = 0 A The time until 90 % from 10 % of target value.	—	0.1	—	ms	*1
DC-DC2 start time	DD2 TSTU	Capacitive load : 24 μF I_{OUT2} = 0 A The time until 90 % from 10 % of target value.	—	0.15	—	ms	*1

*1 : Typical Value checked by design.

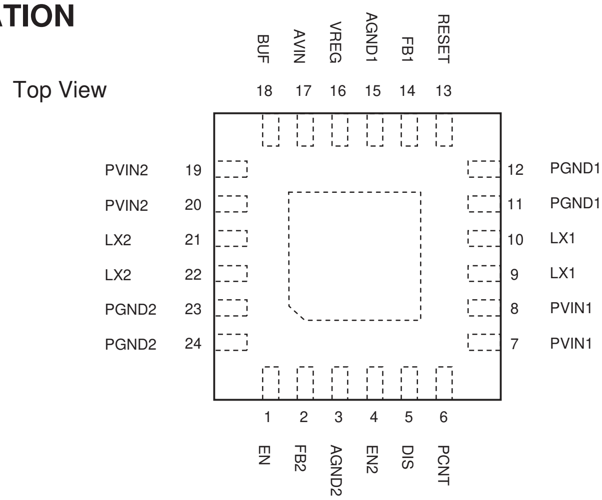
ELECTRICAL CHARACTERISTICS (Continued)

V_{IN} = AVIN = PVIN1 = PVIN2 = 3.3V
[DC-DC1] Cout = 10 µF (GRM21BB31A106K[Murata]) , Lout = 2.2 µH (NR3012T2R2M[Taiyo Yuden])
[DC-DC2] Cout = 10 µF (GRM21BB31A106K[Murata]) , Lout = 2.2 µH (NR3012T2R2M[Taiyo Yuden])
T_a = 25 °C ± 2 °C unless otherwise noted.

Parameter	Symbol	Conditions	Reference values			Unit	Notes
			Min	Typ	Max		
[DC-DC1] (1.0 V DC/DC step-down regulator) [DC-DC2] (1.8 V DC/DC step-down regulator)							
BUF line regulation	BUF REG IN	V_{IN} = 2.9V → 5.5V $I_{OUT(BUF)}$ = 10 µA	—	0	—	mV	*1
BUF load regulation	BUF REG LD	$I_{OUT(BUF)}$ = 10 µA → 10 mA	—	5	—	mV	*1
BUD output current limit	BUF ILMT	BUF = 0V	—	10	—	mA	*1
BUF PSRR	BUF PSR	$I_{OUT(BUF)}$ = 10 µA f = 10 kHz	—	–50	—	dB	*1
BUF load transient response 1	BUF DVAC 1	$I_{OUT(BUF)}$ = 10 µA → 10 mA Δ t = 1 µs	—	160	—	mV	*1
BUF load transient response 2	BUF DVAC 2	$I_{OUT(BUF)}$ = 10 mA → 10 µA Δ t = 1 µs	—	100	—	mV	*1
BUF discharge resistance	BUF RDIS	EN = 0 V	—	80	—	Ω	*1
BUF start time	BUF TSTU	$I_{OUT(BUF)}$ = 0 A The time until 90 % from 10 % of target value.	—	50	—	µs	*1
Reset delay	RST DLY	—	—	30	—	ms	*1
PCNT sink current	IPCNT	PCNT = 3.3 V	—	2.5	—	µA	*1
Timer latch time	TLAT CH	—	—	1	—	ms	*1
DC-DC1 Ground-short detection voltage	DD1 SCP	FB1 = 1.0 V → 0 V	—	0.5	—	V	*1
DC-DC2 Ground-short detection voltage	DD2 SCP	FB2 = 1.8 V → 0 V	—	0.9	—	V	*1
TSD operating temperature	TJSO	Temperature error detection	—	160	—	°C	*1

*1 : Typical Value checked by design.

PIN CONFIGURATION

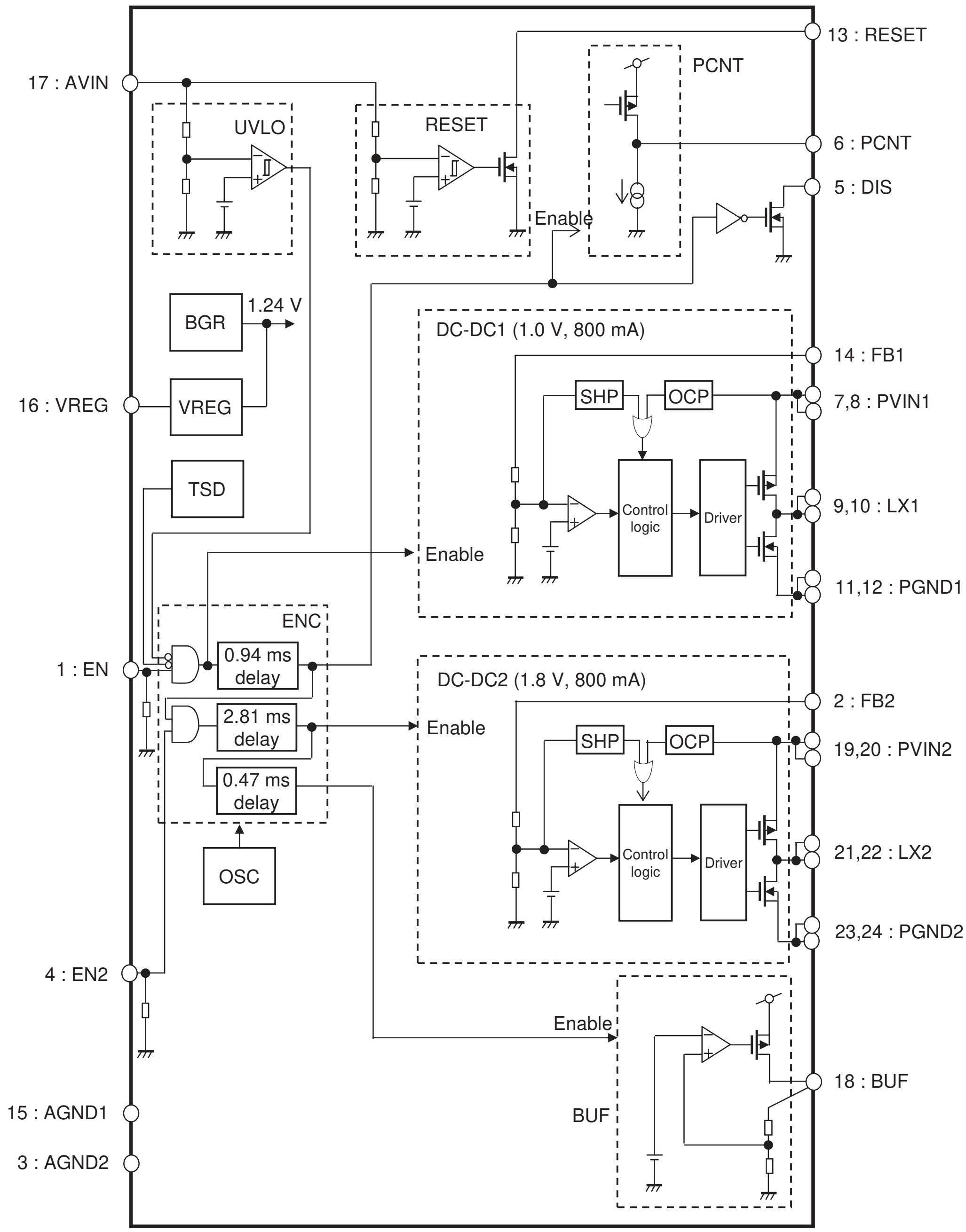


PIN FUNCTION

Pin No.	Pin name	Type	Description
1	EN	Input	ON/OFF control pin
2	FB2	Input	Feed Back pin (for DC-DC2)
3	AGND2	Ground	Ground pin
4	EN2	Input	DCDC2 and BUF control pin
5	DIS	Output	Discharge pin (open drain)
6	PCNT	Output	External Pch MOSFET gate control pin
7	PVIN1	Power supply	Power supply pin (for DC-DC1)
8	PVIN1	Power supply	Power supply pin (for DC-DC1)
9	LX1	Output	Driver output pin (for DC-DC1)
10	LX1	Output	Driver output pin (for DC-DC1)
11	PGND1	Ground	Ground pin (for DC-DC1)
12	PGND1	Ground	Ground pin (for DC-DC1)
13	RESET	Output	Reset output pin (open drain)
14	FB1	Input	Feed Back pin (for DC-DC1)
15	AGND1	Ground	Ground pin
16	VREG	Output	LDO output pin (Power supply for internal control circuit / 2.55 V)
17	AVIN	Power supply	Power supply pin
18	BUF	Output	LDO output pin (0.9 V)
19	PVIN2	Power supply	Power supply pin (for DC-DC2)
20	PVIN2	Power supply	Power supply pin (for DC-DC2)
21	LX2	Output	Driver output pin (for DC-DC2)
22	LX2	Output	Driver output pin (for DC-DC2)
23	PGND2	Ground	Ground pin (for DC-DC2)
24	PGND2	Ground	Ground pin (for DC-DC2)

Notes) Concerning detail about pin description, please refer to OPERATION and APPLICATION INFORMATION section.

FUNCTIONAL BLOCK DIAGRAM



Notes) This block diagram is for explaining functions. Part of the block diagram may be omitted, or it may be simplified.

OPERATION

1. Pin Setting For Start / Stop Control

EN	High		Low	
EN2	High	Low	High	Low
DC-DC1(1.0V)	ON	ON	OFF	OFF
External Pch-MOSFE Gate control circuit	ON	ON	OFF	OFF
DC-DC2(1.8V)	ON	OFF	OFF	OFF
BUF(0.9V)	ON	OFF	OFF	OFF

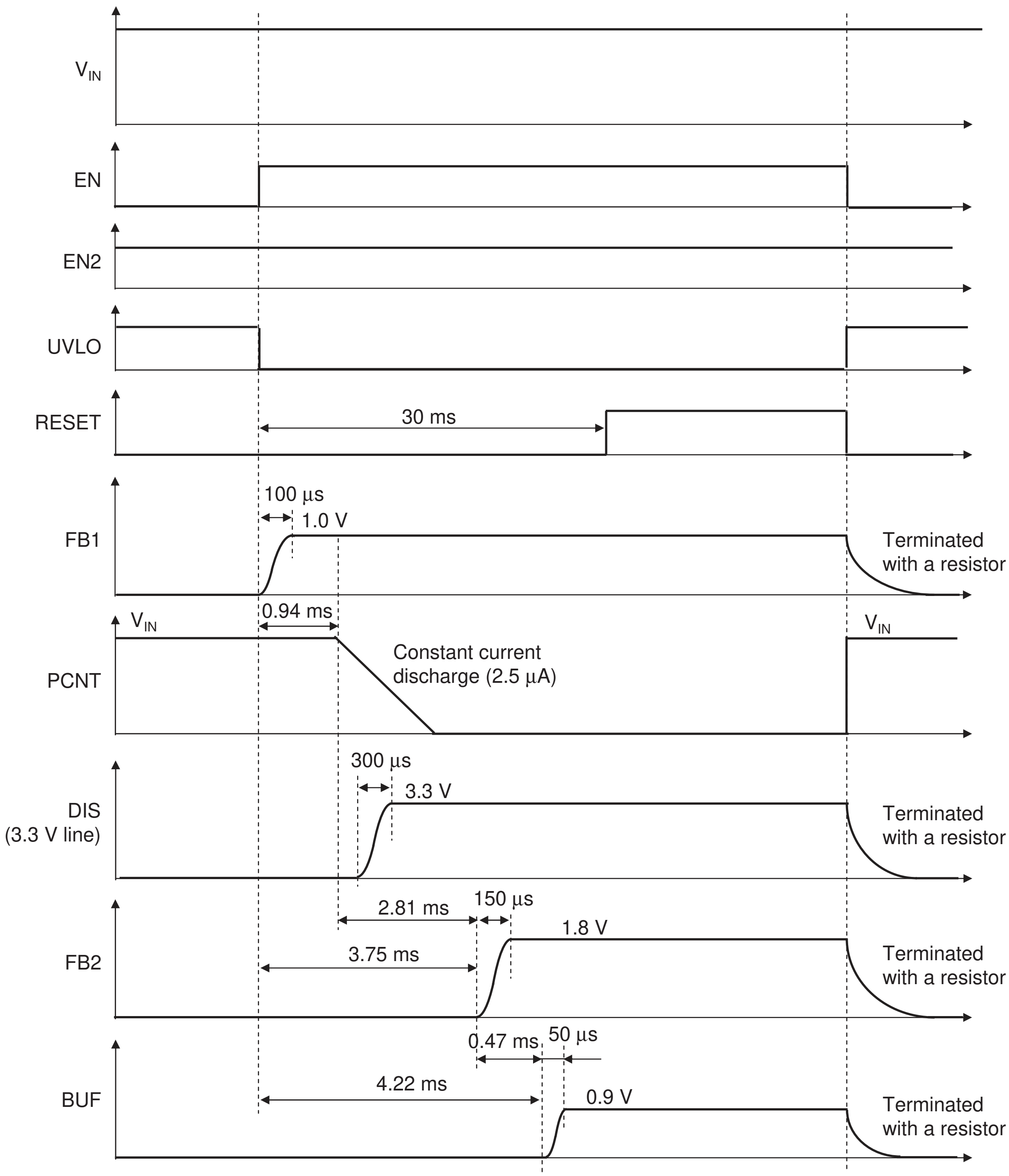
EN pin is the main control pin. When EN pin becomes High, DC-DC1 and external Pch-MOSFET gate control circuit turn on,and DC-DC2 and BUF become controllable by EN2 pin.
EN2 pin is the control pin for DC-DC2 and BUF. When EN2 pin becomes High, DC-DC2 and BUF turn on.
Even if EN2 is High under the condition that EN is Low, DC-DC2 and BUF do not turn on.

OPERATION (Continued)

2. Start / Stop Control Timing Chart

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Start / Stop control sequence by EN pin under the condition that EN2 pin is fixed to High is as follows.



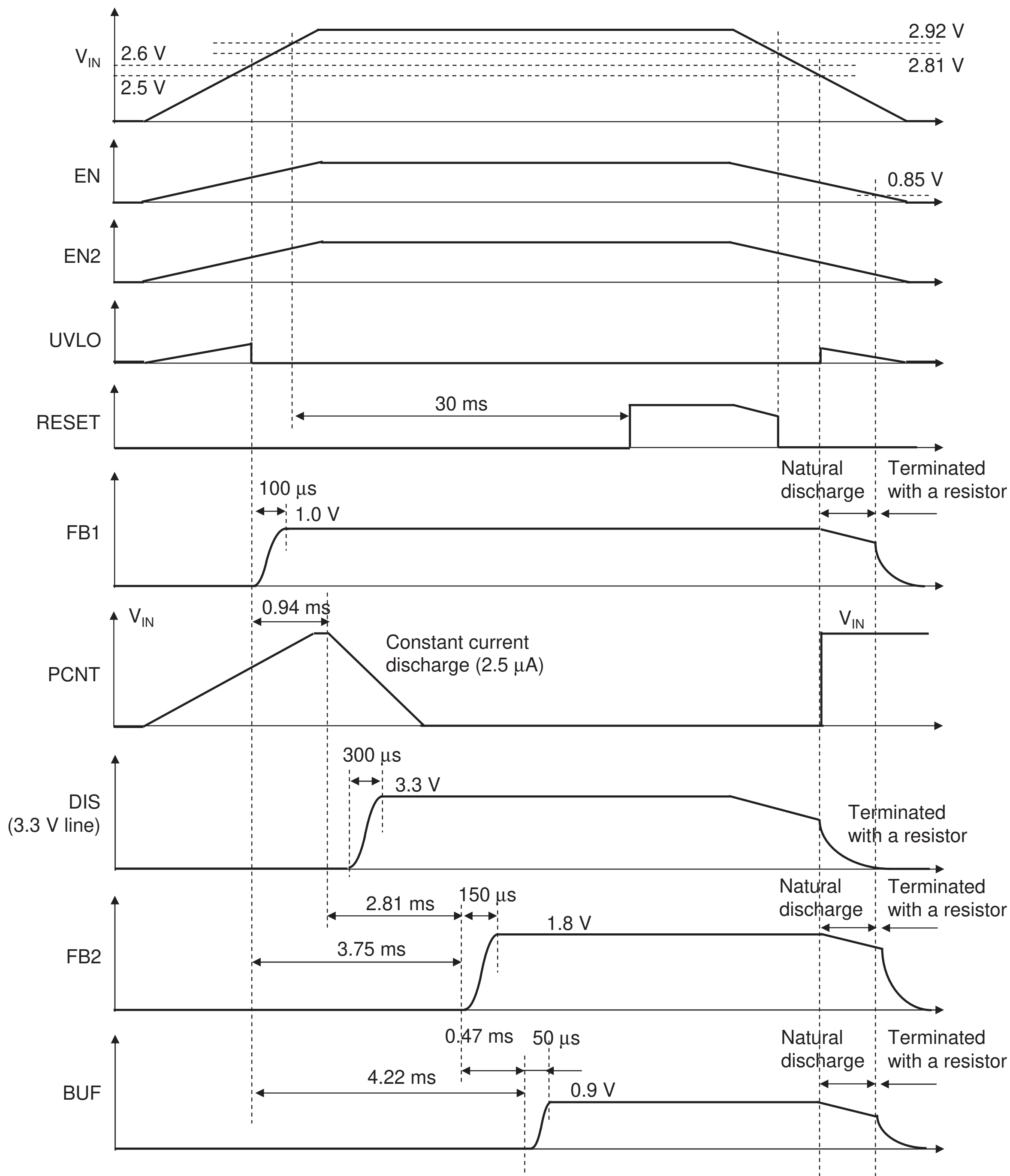
Note) All values given in the above figure are typical values.

OPERATION (Continued)

2. Start / Stop Control Timing Chart

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Start / Stop sequence in case that EN pin and EN2 pin are connected to power supply (V_{IN}) is as follows.



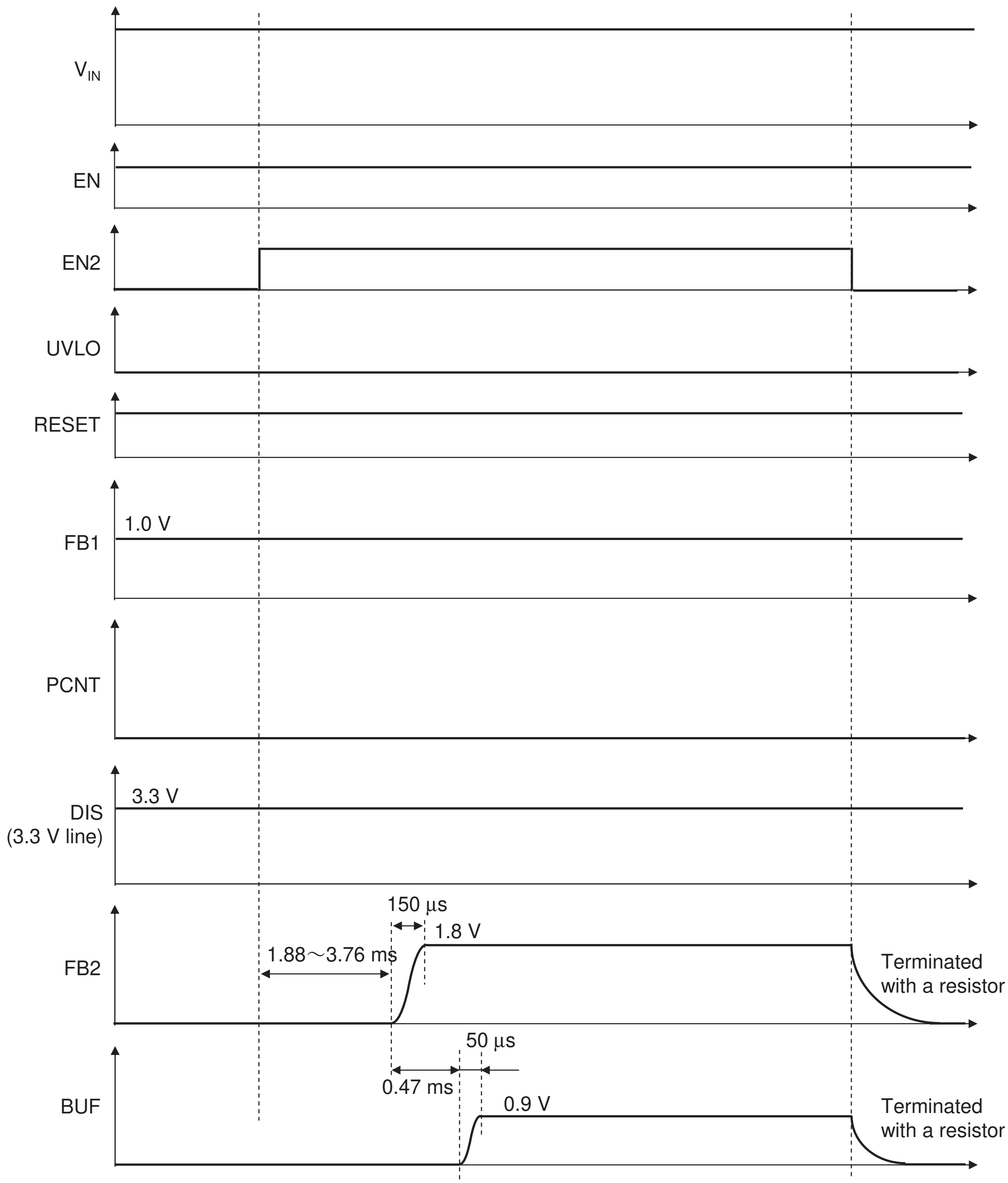
Note) All values given in the above figure are typical values.

OPERATION (Continued)

2. Start / Stop Control Timing Chart

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Start / Stop control sequence by EN2 pin under the condition that EN pin is fixed to High is as follows.



Note) All values given in the above figure are typical values.

OPERATION (Continued)

3. Protection

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

- UVLO function
  When power supply rises to 2.6 V or higher at EN = High, UVLO is released, and the operation of each function starts.
  Since this function's hysteresis is 100 mV, UVLO detects when power supply falls to 2.5 V or lower, then each
  function shuts down.

- Reset function
  RESET pin shifts to High at 30 ms delay after power supply rises to 2.92 V or higher.
  (Output type : Nch MOS open drain)
  Since this function's hysteresis is 110 mV, RESET pin shifts to Low when power supply falls to 2.81 V or lower.(No delay in case of High → Low)

- DC-DC1 (Output voltage : 1.0 V)
  When UVLO is released, DC-DC1 starts and outputs 1.0 V. Soft-start function operates for 1 ms after startup.
  Since output voltage rises slowly, limiting input current, it is possible to prevent rush current and overshoot.
  When UVLO detects, DC-DC1 turns off. When EN pin shifts to Low, an output pin (FB1) is terminated with a resistor.

- External Pch-MOSFET gate control function
  PCNT pin is discharged by the constant current (2.5 µA) at 0.94 ms delay after UVLO is released.
  By connecting the gate of Pch MOSFET to PCNT pin, it is possible to turn on this FET softly.
  At the same time, the termination with a resistor of DIS pin is released.
  Just after UVLO detects, PCNT pin voltage becomes V_{IN} and DIS pin is terminated with a resistor.

- DC-DC2 (Output voltage : 1.8 V)
  When both EN pin and EN2 pin are fixed to High, DC-DC2 turns on and outputs 1.8 V. Start-up timing is as follows.
  1) In case that EN pin becomes Low → High when EN2 pin is fixed to High
     → 3.75 ms delay from UVLO release
  2) In case that EN2 pin becomes Low → High within 3.75 ms from UVLO release when EN pin is fixed to High
     → 3.75 ms delay from UVLO release
  3) In case that EN2 pin becomes Low → High after 3.75 ms from UVLO release when EN pin is fixed to High
     → 1.88 ms to 3.76 ms delay from when EN2 pin becomes Low → High

  DC-DC2 has the same soft-start function as DC-DC1 and starts, preventing rush current and overshoot.
  DC-DC2 stops because UVLO detects. When EN pin shifts to Low, an output pin (FB2) is terminated with a resistor.
  DC-DC2 also stops when EN2 pin becomes Low, and the output pin is terminated with a resistor.

- BUF (Output voltage : 0.9 V)
  BUF pin outputs 0.9 V when both EN pin and EN2 pin are fixed to High. Start-up timing is 0.47 ms delay after DC-DC2
  turns on. BUF starts, preventing rush current and overshoot.
  BUF stops because UVLO detects. BUF is terminated with a resistor when EN pin shifts to Low.
  BUF also stops when EN2 pin becomes Low, and the output pin is terminated with a resistor.

OPERATION (Continued)

3. Protection

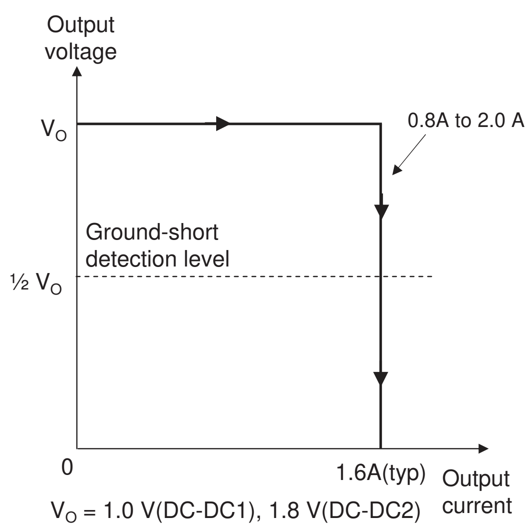
Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Ground-short protection function

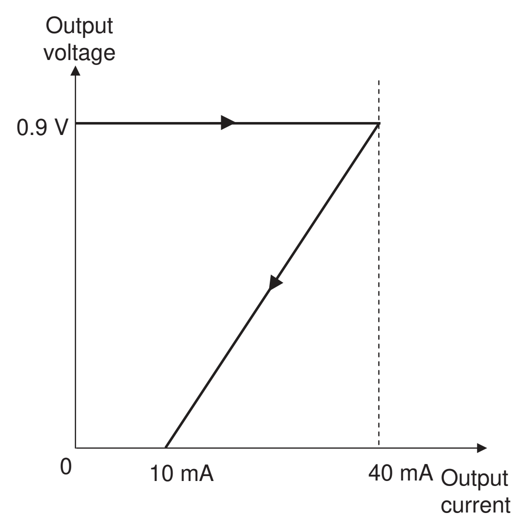
DC-DC1 and DC-DC2 have ground-short detection circuits respectively. When output voltage falls to 50% or lower Of target value (DC-DC1 : 0.5 V, DC-DC2 : 0.9 V), it shifts to the protection sequence shown in [3.Protection]. However, even if BUF pin shorts to GND, BUF does not shift to the protection sequence.

Over-current limit function

DC-DC1, DC-DC2 and BUF have over-current limit circuits respectively. This function limits the output current which exceeds the setup value. The over-current limit characteristics are as follows.



a) DC-DC1/2



b) BUF

The output currents of DC-DC1 and DC-DC2 are limited to 1.6 A(typ) regardless of the output voltage.
BUF has limit characteristics, which the output current decreases as the output voltage falls.
The peak input current is 40 mA(typ). The input current at BUF = 0 V is 10 mA(typ).

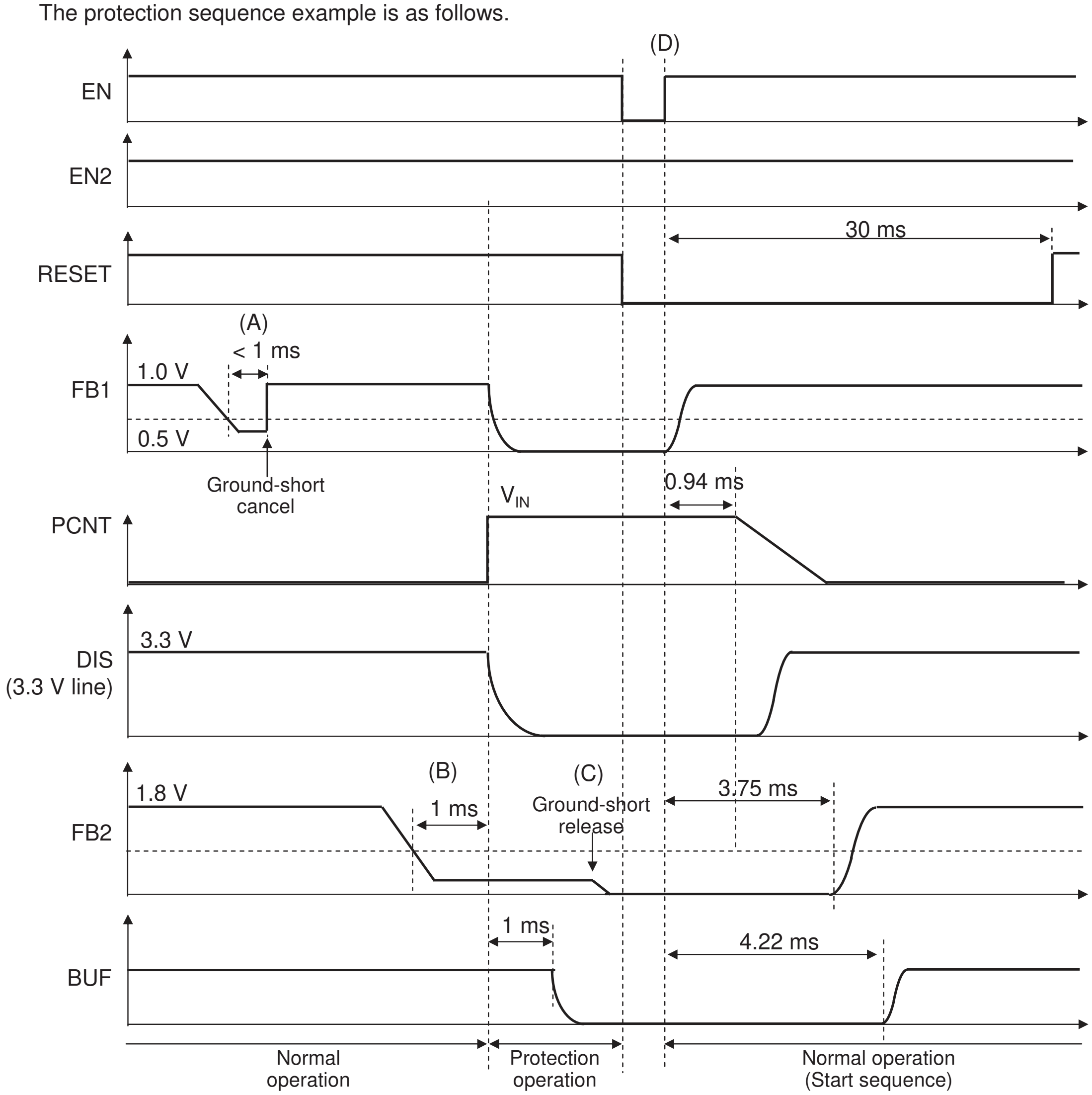
OPERATION (Continued)

3. Protection

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Protection Sequence

When the following state continues for 1 ms(typ), AN30185A shifts to the protection sequence.
— Any of DCDC1 and DCDC2 shorts to GND. (Output voltage is 50% or lower of target value.)
— TSD circuit detects abnormal state.
When this LSI shifts to the protection sequence, it is latched to the state at which each function is shut down.
It recovers from the protection sequence by applying to EN pin again or releasing UVLO again.
The protection sequence example is as follows.



In (A) of the above figure, DCDC1 output shorts to GND. However, this LSI doesn't shift to protection sequence because the term of ground-short is 1 ms or shorter.
In (B) of the above figure, DCDC2 output shorts to GND. After ground-short state continues for 1 ms, this LSI shifts to protection sequence, DCDC1, DCDC2 and external Pch-MOSFET gate drive circuits shift to OFF state, and BUF shifts to OFF state after another 1 ms and are latched.
Even if ground-short is released, the operation of each circuit does not recover (C).
During the protection sequence, RESET pin is not set to Low.
In (D) of the above figure, they recover to normal start sequence after EN is input again.

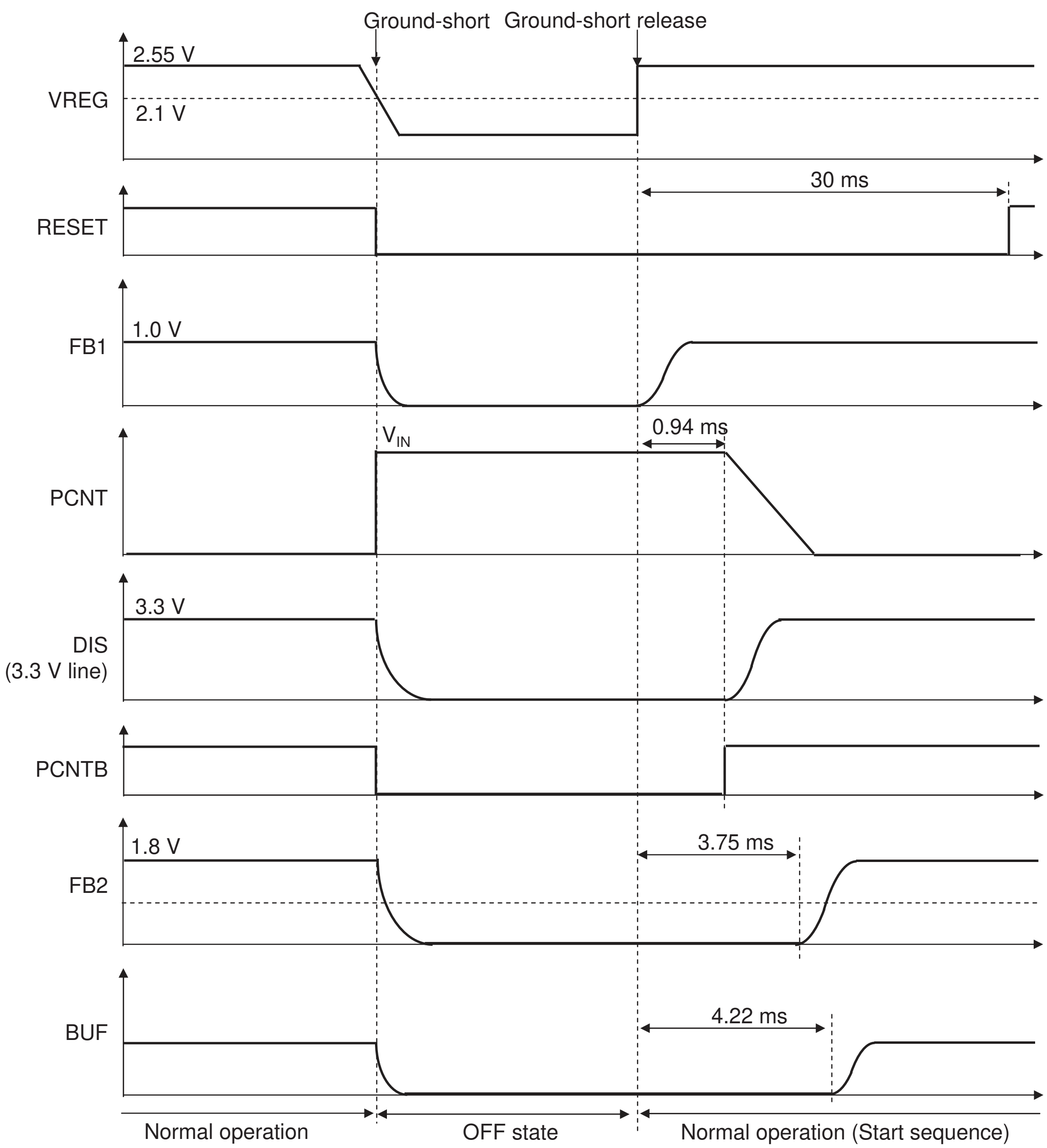
OPERATION (Continued)

3. Protection

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

VREG pin Ground Short Operation

VREG pin is an output pin of LDO used in internal circuits. The operation of each function stops just after VREG pin Is shorted to GND. Since each function is not latched unlike the case of [3.Protection : Protection sequence], it recovers by the release of ground-short.
The operation is as follows.



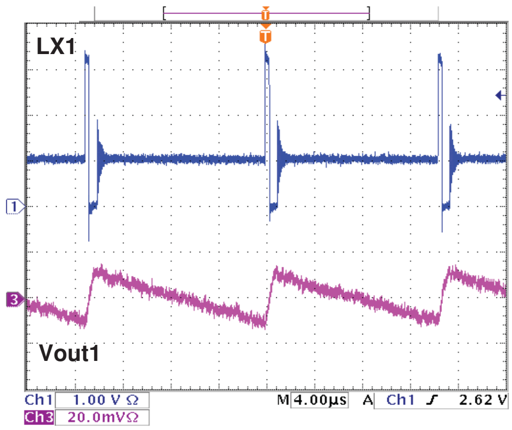
TYPICAL CHARACTERISTICS CURVES

(1) Output ripple voltage

VIN = 3.3 V , Cout = 10 µF (GRM21BB31A106K[Murata]) , Lout = 2.2 µH (NR3012T2R2M[Taiyo Yuden])

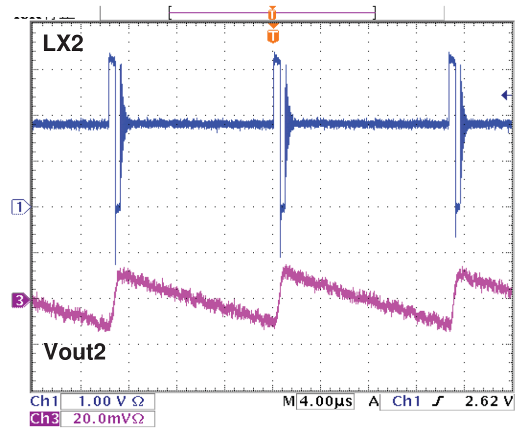
DC-DC1

Iout1 = 10 mA



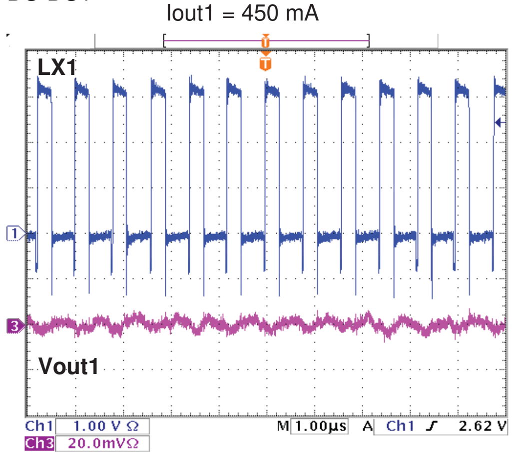
DC-DC2

Iout2 = 10 mA



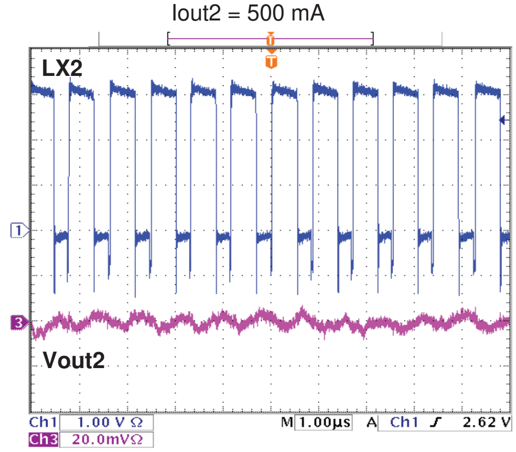
DC-DC1

Iout1 = 450 mA



DC-DC2

Iout2 = 500 mA



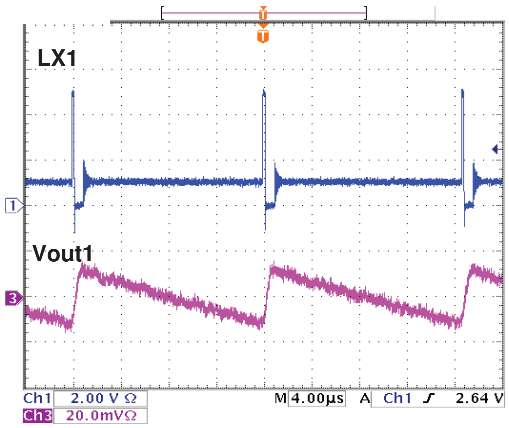
TYPICAL CHARACTERISTICS CURVES (Continued)

(1) Output ripple voltage

VIN = 5.0 V , Cout = 10 µF (GRM21BB31A106K[Murata]) , L = 2.2 µH (NR3012T2R2M[Taiyo Yuden])

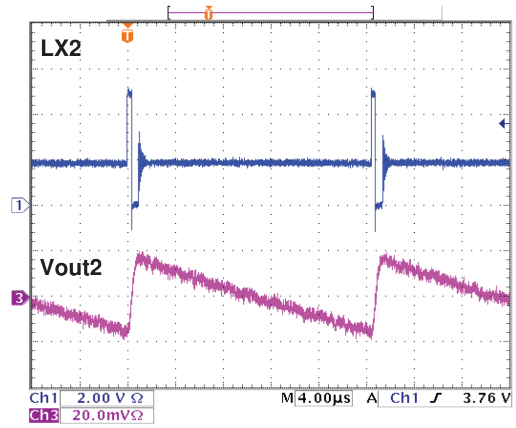
DC-DC1

Iout1 = 10 mA



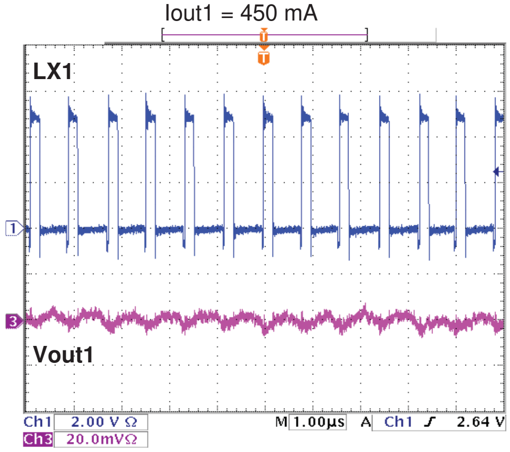
DC-DC2

Iout2 = 10 mA



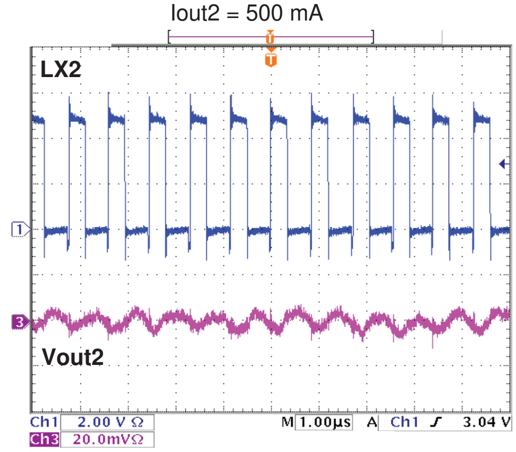
DC-DC1

Iout1 = 450 mA



DC-DC2

Iout2 = 500 mA



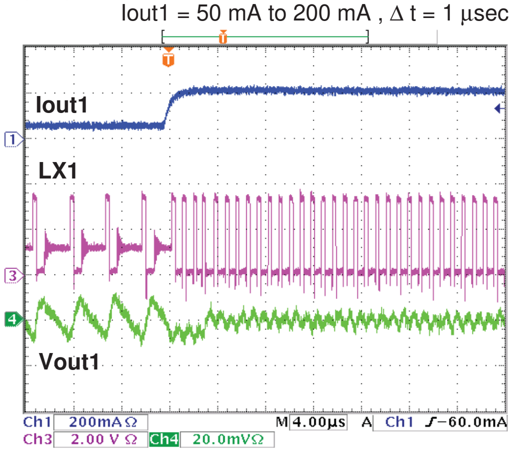
TYPICAL CHARACTERISTICS CURVES (Continued)

(2) Load transient response

VIN = 3.3 V , Cout = 10 µF (GRM21BB31A106K[Murata]) , Lout = 2.2 µH (NR3012T2R2M[Taiyo Yuden])

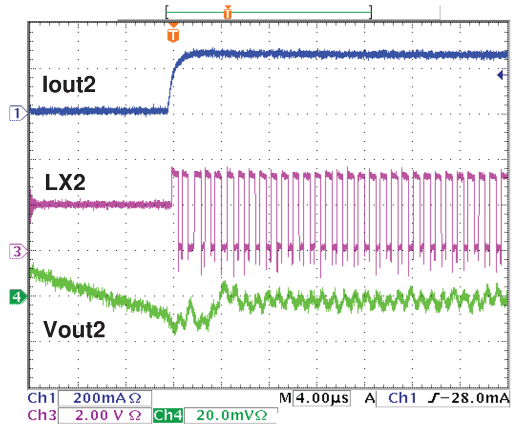
DC-DC1

Iout1 = 50 mA to 200 mA , Δ t = 1 µsec



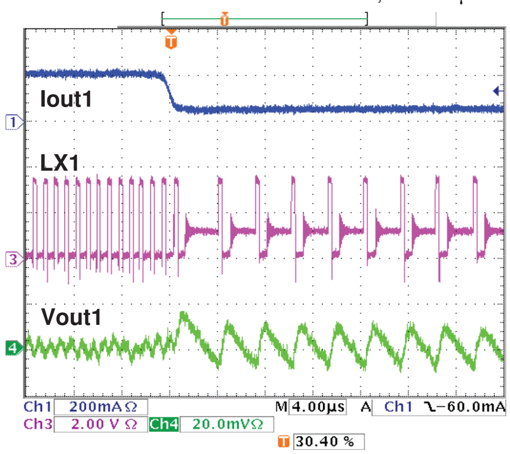
DC-DC2

Iout2 = 10 mA to 250 mA , Δ t = 1 µsec



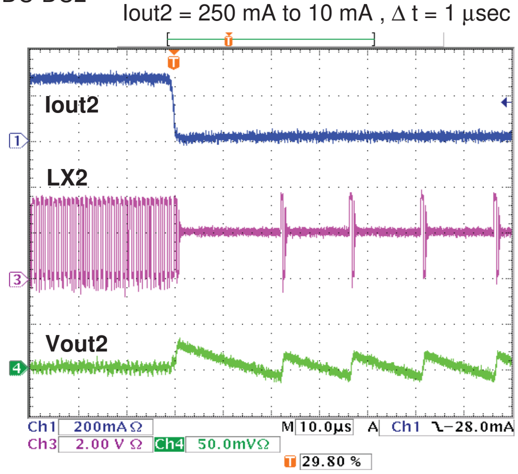
DC-DC1

Iout1 = 200 mA to 50 mA , Δ t = 1 µsec



DC-DC2

Iout2 = 250 mA to 10 mA , Δ t = 1 µsec



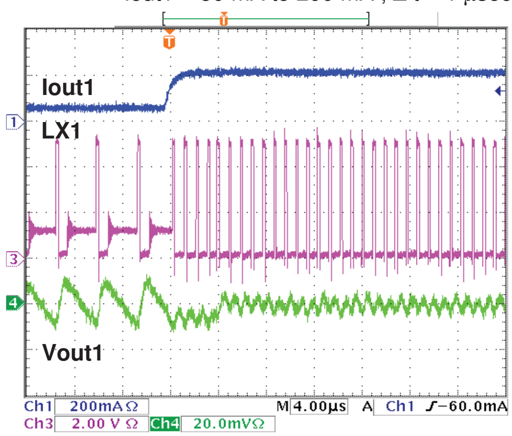
TYPICAL CHARACTERISTICS CURVES (Continued)

(2) Load transient response

VIN = 5.0 V , Cout = 10 µF (GRM21BB31A106K[Murata]) , Lout = 2.2 µH (NR3012T2R2M[Taiyo Yuden])

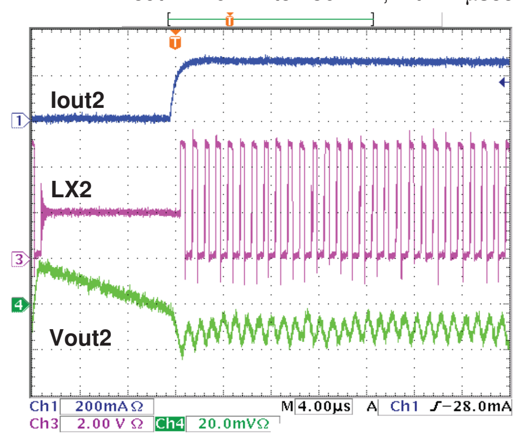
DC-DC1

Iout1 = 50 mA to 200 mA , Δ t = 1 µsec



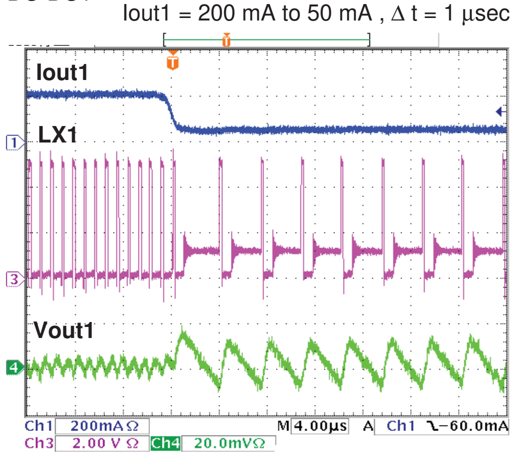
DC-DC2

Iout2 = 10 mA to 250 mA , Δ t = 1 µsec



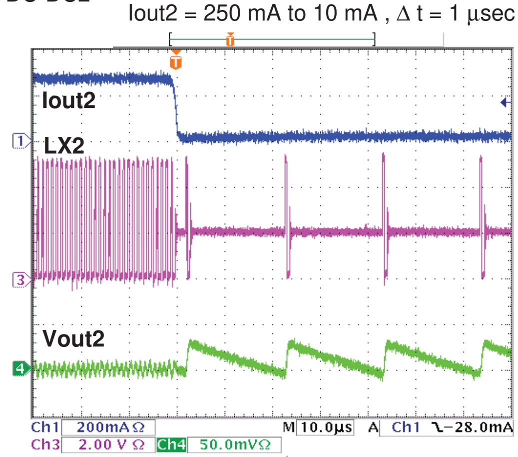
DC-DC1

Iout1 = 200 mA to 50 mA , Δ t = 1 µsec



DC-DC2

Iout2 = 250 mA to 10 mA , Δ t = 1 µsec

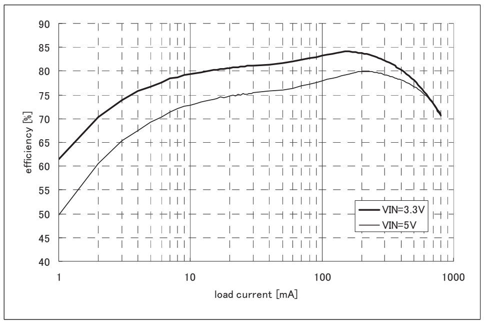


TYPICAL CHARACTERISTICS CURVES (Continued)

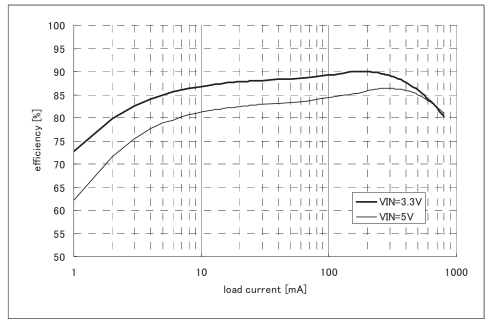
(3) Efficiency

VIN = 3.3 V or 5.0V , Cout = 10 µF (GRM21BB31A106K[Murata]) , Lout = 2.2 µH (NR3012T2R2M[Taiyo Yuden])

DC-DC1



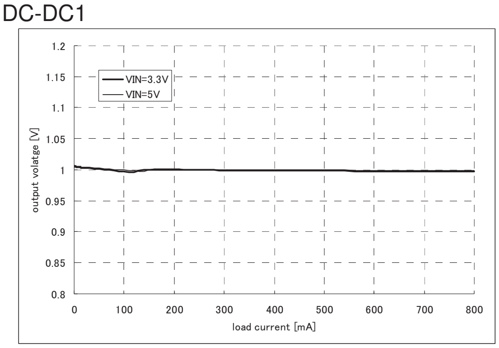
DC-DC2



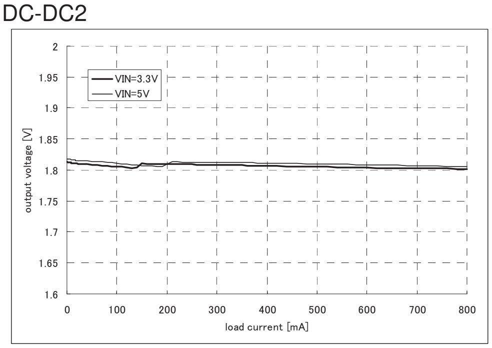
(4) Load regulation

VIN = 3.3 V or 5.0V , Cou t= 10 µF (GRM21BB31A106K[Murata]) , Lout = 2.2 µH (NR3012T2R2M[Taiyo Yuden])

DC-DC1



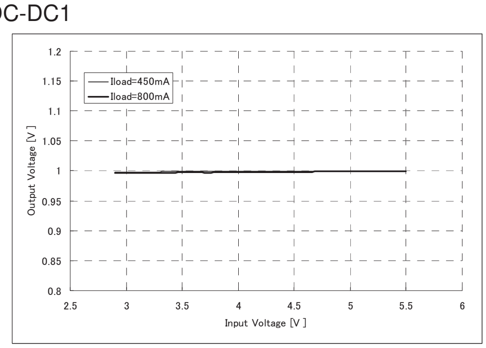
DC-DC2



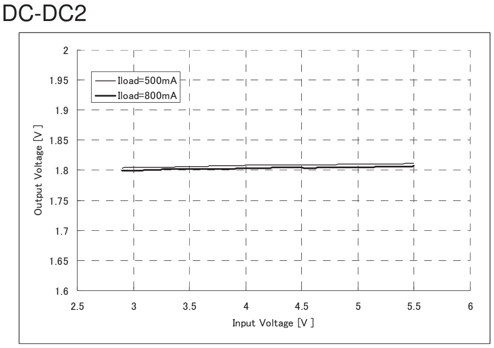
(5) Line regulation

Cout = 10 µF (GRM21BB31A106K[Murata]) , Lout = 2.2 µH (NR3012T2R2M[Taiyo Yuden])

DC-DC1

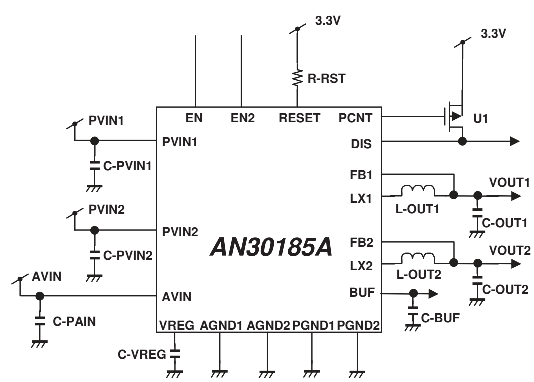


DC-DC2



APPLICATIONS INFORMATION

1. Application circuit



2. Layout of Evaluation Board

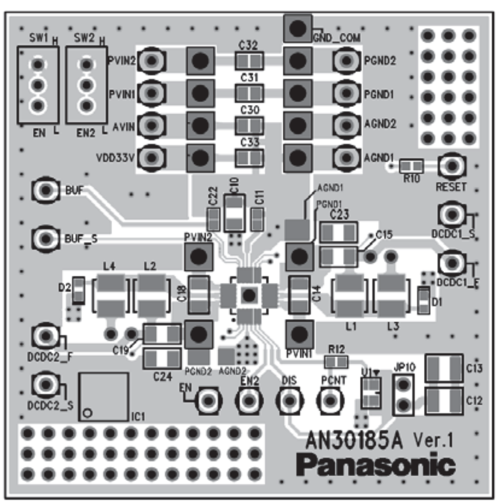


Figure : Top Layer with silk screen
(Top View) with Evaluation board

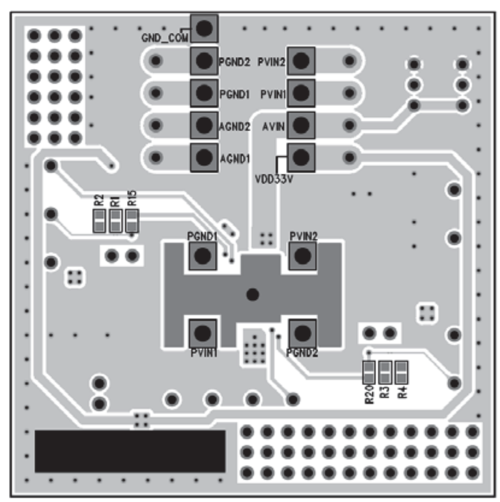


Figure : Bottom Layer with silk screen
(Bottom View)with Evaluation board

Notes) This application circuit and layout is an example. The operation of mass production set is not guaranteed. You should perform enough evaluation and verification on the design of mass production set. You are fully responsible for the incorporation of the above application circuit and information in the design of your equipment.

APPLICATIONS INFORMATION (Continued)

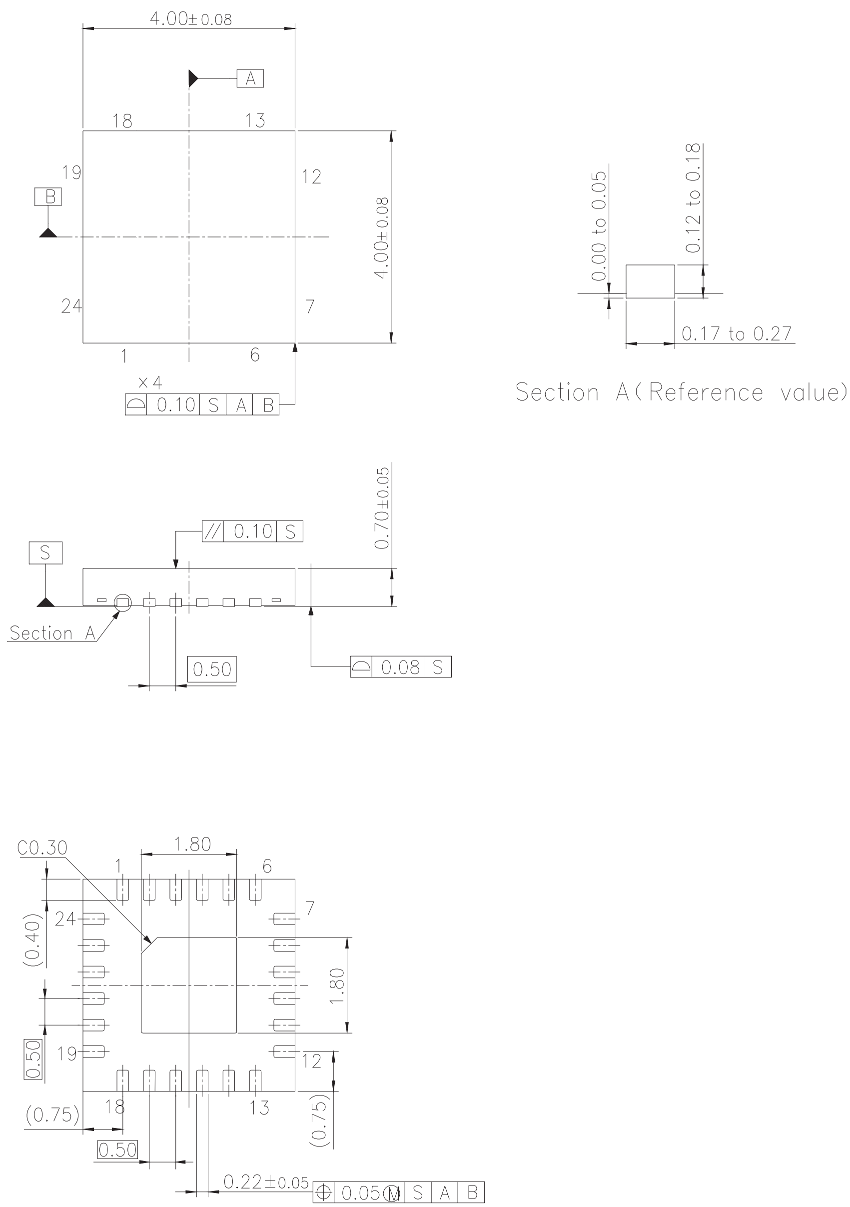
3. Recommended Component

Reference Designator	QTY	Value	Manufacturer	Part Number
C-PVIN1	1	4.7 μF	Murata	GRM21BB31A475KA74L
C-PVIN2	1	4.7 μF	Murata	GRM21BB31A475KA74L
CAVIN	1	4.7 μF	Murata	GRM21BB31A475KA74L
C-VREG	1	1 μF	Murata	GRM155B31A105KE15D
C-BUF	1	1 μF	Murata	GRM155B31A105KE15D
C-VOUT1	1	10 μF	Murata	GRM21BB31A106KE18L
C-VOUT2	1	10 μF	Murata	GRM21BB31A106KE18L
L-OUT1	1	2.2 μH	TAIYO YUDEN	NR3012T2R2M
L-OUT2	1	2.2 μH	TAIYO YUDEN	NR3012T2R2M
U1	1	—	Panasonic	MTM76111
R-RST	1	10 KΩ	Panasonic	ERA3ARW103V

PACKAGE INFORMATION (Reference Data)

Package Code : HQFN024-P-0404

Unit:mm



Body Material	:	Br / Sb Free Epoxy Resin
Lead Material	:	Cu Alloy
Lead Finish Method : Au Plating		

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Be sure to read the notes to descriptions and the usage notes in the book.

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Any applications other than the standard applications intended.
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(2) Traffic control equipment (such as for automobile, airplane, train, and ship)
(3) Medical equipment for life support
(4) Submarine transponder
(5) Control equipment for power plant
(6) Disaster prevention and security device
(7) Weapon
(8) Others : Applications of which reliability equivalent to (1) to (7) is required
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USAGE NOTES

1. When designing your equipment, comply with the range of absolute maximum rating and the guaranteed operating conditions (operating power supply voltage and operating environment etc.). Especially, please be careful not to exceed the range of absolute maximum rating on the transient state, such as power-on, power-off and mode-switching. Otherwise, we will not be liable for any defect which may arise later in your equipment.

   Even when the products are used within the guaranteed values, take into the consideration of incidence of break down and failure mode, possible to occur to semiconductor products. Measures on the systems such as redundant design, arresting the spread of fire or preventing glitch are recommended in order to prevent physical injury, fire, social damages, for example, by using the products.

2. Comply with the instructions for use in order to prevent breakdown and characteristics change due to external factors (ESD, EOS, thermal stress and mechanical stress) at the time of handling, mounting or at customer's process. When using products for which damp-proof packing is required, satisfy the conditions, such as shelf life and the elapsed time since first opening the packages.

3. Pay attention to the direction of LSI. When mounting it in the wrong direction onto the PCB (printed-circuit-board), it might smoke or ignite.

4. Pay attention in the PCB (printed-circuit-board) pattern layout in order to prevent damage due to short circuit between pins. In addition, refer to the Pin Description for the pin configuration.

5. Perform a visual inspection on the PCB before applying power, otherwise damage might happen due to problems such as a solder-bridge between the pins of the semiconductor device. Also, perform a full technical verification on the assembly quality, because the same damage possibly can happen due to conductive substances, such as solder ball, that adhere to the LSI during transportation.

6. Take notice in the use of this product that it might break or occasionally smoke when an abnormal state occurs such as output pin-VCC short (Power supply fault), output pin-GND short (Ground fault), or output-to-output-pin short (load short) .

   And, safety measures such as an installation of fuses are recommended because the extent of the above-mentioned damage and smoke emission will depend on the current capability of the power supply.

7. The protection circuit is for maintaining safety against abnormal operation. Therefore, the protection circuit should not work during normal operation.

   Especially for the thermal protection circuit, if the area of safe operation or the absolute maximum rating is momentarily exceeded due to output pin to VCC short (Power supply fault), or output pin to GND short (Ground fault), the LSI might be damaged before the thermal protection circuit could operate.

8. Unless specified in the product specifications, make sure that negative voltage or excessive voltage are not applied to the pins because the device might be damaged, which could happen due to negative voltage or excessive voltage generated during the ON and OFF timing when the inductive load of a motor coil or actuator coils of optical pick-up is being driven.

9. The product which has specified ASO (Area of Safe Operation) should be operated in ASO

10. Verify the risks which might be caused by the malfunctions of external components.

11. Connect the metallic plates on the back side of the LSI with their respective potentials (AGND, PVIN, LX). The thermal resistance and the electrical characteristics are guaranteed only when the metallic plates are connected with their respective potentials.

Request for your special attention and precautions in using the technical information and semiconductors described in this book

(1) If any of the products or technical information described in this book is to be exported or provided to non-residents, the laws and regulations of the exporting country, especially, those with regard to security export control, must be observed.

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Consult our sales staff in advance for information on the following applications:
- Special applications (such as for airplanes, aerospace, automotive equipment, traffic signaling equipment, combustion equipment, life support systems and safety devices) in which exceptional quality and reliability are required, or if the failure or malfunction of the products may directly jeopardize life or harm the human body.

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Even when the products are used within the guaranteed values, take into the consideration of incidence of break down and failure mode, possible to occur to semiconductor products. Measures on the systems such as redundant design, arresting the spread of fire or preventing glitch are recommended in order to prevent physical injury, fire, social damages, for example, by using the products.

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