XILINXPWR-081 (HPA-081)

Single-Channel Linear Regulator Power Management Solution Providing I_{CCINT} up to 1.4 A from V_{IN} = 3.3 V and 800 mA from V_{IN} = 5.0 V

SUPPORTS:

- Spartan™-3 Design 3 (PR215) - http://focus.ti.com/lit/ml/slva176/slva176.pdf
- Spartan™-II Design 2 (PR209) - http://focus.ti.com/lit/ml/slva170/slva170.pdf
  - Board requires significant modification to match PR209
- Spartan™-IIE Design 2 (PR210) - http://focus.ti.com/lit/ml/slva171/slva171.pdf
  - Board requires significant modification to match PR210

FEATURES:

- Independent linear regulators allow higher power dissipation than an integrated dual-channel solution.
- Linear regulator solution saves cost and space over a switching DC/DC solution.
- Control cost by using lower current LDOs from the TPS79xxx family for U2, U3 and U4 to meet specific application requirements.
- Linear regulators start-up fast, allowing large in-rush currents for charging decoupling capacitors and FPGA start-up. The current draw on the input power supply is minimized by the use of the:
  - External SVS, U1, which monitors the input rail and prevents the regulator from enabling until the input bulk capacitors (not shown in the schematic) are fully charged.
  - Soft-start circuit consisting of the external NMOS transistor Q4, TPS3803-01 supervisory IC (SVS) and supporting passive components to provide 10 ms rise time for V_{CCINT}.
  - Soft-start circuit consisting of the external PMOS transistor Q3 and supporting passive components to provide 10 ms rise time for V_{CCO}.
  - Sequential sequencing of V_{CCINT}, V_{CCAUX} then V_{CCO}.
    - the discrete SVS circuit formed by bipolar transistors Q1 and Q2 and supporting passives enables the V_{CCAUX} regulator, U4.
    - V_{CCAUX} enables the V_{CCO} regulator, U3.
- The design meets Xilinx's V_{CCINT} and V_{CCO} start-up profile requirements, where applicable, including monotonic voltage ramp, in-rush current and power voltage ramp time requirements.

IMPORTANT WEB LINKS:

- Link to the TI home page for Xilinx FPGA power management solutions at http://www.ti.com/xilinxfpga for more information and other reference designs.

- Link to datasheets at http://focus.ti.com/lit/ds/symlink/TPS78601.pdf, http://focus.ti.com/lit/ds/symlink/tps79601.pdf, http://focus.ti.com/lit/ds/symlink/tps79401.pdf, and http://focus.ti.com/lit/ds/symlink/tps3809k33.pdf.
- Link to application note SLVA118 http://focus.ti.com/lit/an/slva118/slva118.pdf to explore the thermal considerations when using linear regulators.
- Link to application note SLVA156 http://focus.ti.com/lit/an/slva156/slva156.pdf for more details on the soft-start circuit.
- Link to application note SLVA159 http://focus.ti.com/lit/an/slva159a/slva159a.pdf when using 3.3-V JTAG ports.

IMPLEMENTATION NOTES:

- **Sequencing:** Although Xilinx FPGAs **do NOT require it**, this reference design employs sequencing. This practice is consistent with good power supply design and prevents the input power supply from being pulled down due to supporting in-rush currents for charging large capacitive loads all at once.
- **V_{CCO} minimum ramp time:** Met by soft-start circuit consisting of the external PMOS transistor Q3 and supporting passive components.
- **Power Dissipation/Thermal Issues:** The DDPAK packaged regulators in this design are limited to 3W @ $T_A = 55^o$ C and no airflow, due to power dissipation limitation of the package.
    - Refer to the application section of the datasheet for maximum power dissipation at different ambient conditions as well as guidance on sizing the ground plane area underneath the package for heatsinking.
    - The linear regulator's output current can be computed by rearranging the following equation:
      $P_{Dmax} = (V_{IN} - V_{CCINT}) * I_{CCINTmax}$.

      As an example, with V_{CCINT} = 1.2V and P_{Dmax} = 3 W:
        - $I_{CCINTmax} = P_{Dmax} /(V_{IN} - V_{CCINT})$.
        - $I_{CCINTmax}$ = 1.4 A when V_{IN} = 3.3 V so use the TPS78601 for U2.
        - $I_{CCINTmax}$ = 789 mA when V_{IN} = 5.0 V so use the TPS79601 for U2.
- **Soft Start Circuitry:**
    - NMOS transistor Q4 should be selected so that its threshold voltage, V_{TH}, is at least 0.9 V below V_{IN} or lower (e.g., $V_{TH} < 5.0\ V - 1.2\ V = 3.8\ V$ or $V_{TH} < 3.3\ V - 1.2\ V = 2.1\ V$). In addition, the transistor's R_{DSon} should be low enough, when driven by V_{IN}, that the voltage drop across the transistor at maximum current (e.g., $I_{CCINTmax}*R_{DSon}$) does not cause V_{CCINT} to fall below its -5% tolerance.
    - PMOS transistor Q3 should be selected so that its threshold voltage, V_{TH}, is at least 0.9 V below the V_{CCO} voltage or lower (e.g., $V_{TH} < 3.3\ V - 0.9\ V = 2.4\ V$). In addition, the transistor's R_{DSon} should be low enough, when driven by V_{CCO} = 3.3 V, that the voltage drop across the transistor at

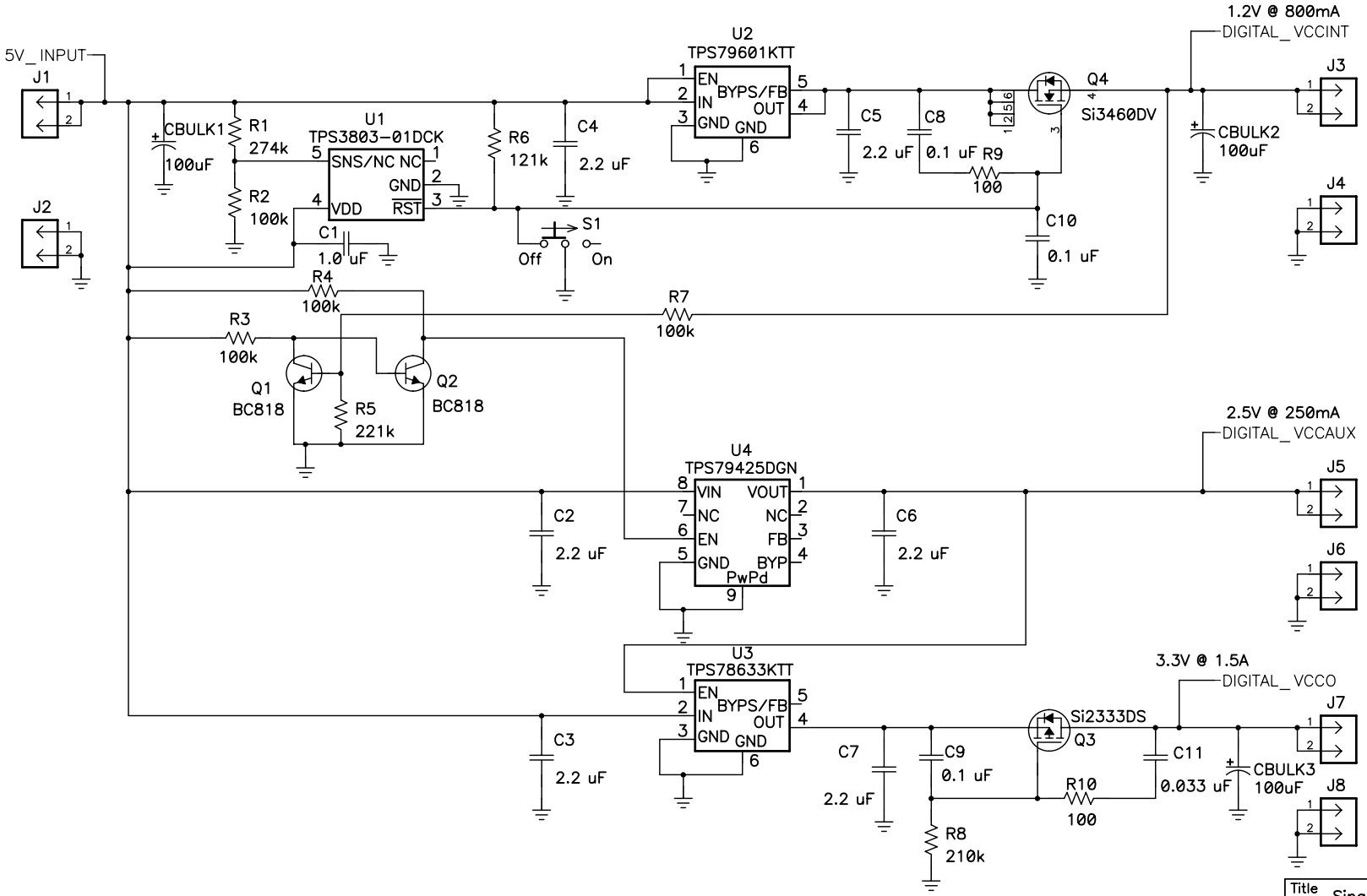
maximum current (e.g., I_{CCO}*R_{DSon}) does not cause V_{CCO} to fall below its -5% tolerance.

- The source of Q4 and the drain of Q3 each need at least 10 uF of capacitance in order for the soft-start circuits to work properly. The additional bulk bypass capacitance (not shown in the schematic) required for each rail of the FPGA will most likely meet this requirement.

- **Modifications:**
  - Adapt for 3.3 V input supply by:
    - Omitting U3 V_{CCO} linear regulator,
    - Replacing U2, TPS79601 1-A linear regulator, with TPS78601 1.5-A linear regulator,
    - Replacing U1 SVS, TPS3809K33, with TPS3809L30,
    - Resizing R4 to XXX.
  - For a low-cost, discrete Supply Voltage Supervisory Circuit alternative to U1, please see reference design PR286 (Active-High Reset Output) or PR281 (Active-Low Reset Output).
- **3.3V Configuration**
  - The Spartan-3 FPGA configuration and JTAG ports commonly use signals with a 2.5-V swing. Alternatively, it is possible to use 3.3-V signals simply by adding a few external resistors. The 3.3-V signals can cause a reverse current that flows from certain configurations and JTAG input pins, through the FPGA, to the V_{CCAUX} power rail. Therefore, please refer to application note SLVA159 http://focus.ti.com/lit/an/slva159a/slva159a.pdf for implementation guidance.

QUESTIONS?

- Send an email to **fpgasupport@list.ti.com**



Title	Single-chanel LDO (TPS79xxx) Design	
Size: B	Number: HPA081	Rev: B
Date: 08/05/04		Drawn by:
Filename: hpa081b.sch		Sheet: of

Filename: HPA081A_bom.xls

Date: 05/04/2004

HPA081A BOM

COUNT	RefDes	DESCRIPTION	SIZE	MFR	PART NUMBER
1	C1	Capacitor, Ceramic, 1.0-uF, 6.3-V, X5R, 10%	603	muRata	GRM188R60J105KA01
1	C11	Capacitor, Ceramic, 0.033-uF, 16-V, X7R, 10%	603	muRata	GRM188R71C333KA01
6	C2 - C7	Capacitor, Ceramic, 2.2-uF, 6.3-V, X5R, 10%	805	muRata	GRM21BR60J225KC01
3	C8, C9, C10	Capacitor, Ceramic, 0.1-uF, 25-V, X7R, 10%	603	muRata	GRM188R71E104KA01
3	CBULK1, CBULK2, CBULK3	Capacitor, Tantalum, 100-uF, 10-V, 95-milliohm, 20%	7343 (D)	Vishay	594D107X0010C2T
8	J1 - J8	Header, 2-pin, 100mil spacing, (36-pin strip)	0.100 x 2	Sullins	PTC36SAAN
2	Q1, Q2	Bipolar, NPN, 30-V, 800-mA, 310-mW	SOT23		BC818
1	Q3	MOSFET, P-ch, -12 V, 4 A, 51 milliohm	SOT23	Vishay	Si2333DS
1	Q4	MOSFET, N-ch, 60-V,3.2-A, 100-milliOhms	TSOP-6	Vishay	Si3460DV
1	R1	Resistor, Chip, 274k-Ohms, 1/16-W, 1%	603	Std	Std
4	R2, R3, R4, R7	Resistor, Chip, 100k-Ohms, 1/16-W, 1%	603	Std	Std
1	R5	Resistor, Chip, 221k-Ohms, 1/16-W, 1%	603	Std	Std
1	R6	Resistor, Chip, 121k-Ohms, 1/16-W, 1%	603	Std	Std
1	R8	Resistor, Chip, 210k-Ohms, 1/16-W, 1%	603	Std	Std
2	R9, R10	Resistor, Chip, 100-Ohms, 1/16-W, 1%	603	Std	Std
1	S1	Switch, 1P2T, Slide, PC-mount, 200-mA	79900	E_Switch	EG1218
1	U1	IC, Voltage Detector, Adj - V	SOP-5 (DCK)	TI	TPS3803-01DCK
1	U2	IC, Ultra Low-Noise, High PSRR, Fast RF Adj V 1.0A LDO Linear Regulator	DDPAK-5	TI	TPS79601KTT
1	U3	IC, Ultra Low-Noise, High PSRR, Fast RF 3.3V 1.5A LDO Linear Regulator	DDPAK-5	TI	TPS78633KTT
1	U4	IC, Utralow-Noise, High PSRR, Fast RF 250 mA, LDO Linear Regulators, 2.5V	DGN	TI	TPS79425DGN
1	--	PCB, 2.85 In x 2.6 In x .062 In		Any	HPA081

Notes:

1. These assemblies are ESD sensitive, ESD precautions shall be observed.
2. These assemblies must be clean and free from flux and all contaminants.
   Use of no clean flux is not acceptable.
3. These assemblies must comply with workmanship standards IPC-A-610 Class 2.
4. Ref designators marked with an asterisk ('**') cannot be substituted.
   All other components can be substituted with equivalent MFG's components.

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