MDT1040AIS-LVDS	1024 x 768	LVDS Interface	TFT Module
(MCT104A0W1024768LML)	**Specification**		
Version: 1	**Date: 31/10/2016**		
Revision			
1	25/10/2017	First issue.	

Display Features			
Display Size	10.4"		
Resolution	1024 x 768		
Orientation	Landscape		
Appearance	RGB		
Logic Voltage	3.3V		
Interface	LVDS		
Brightness	350 cd/m^2		
Touchscreen	N/A		
Module Size	236.00 x 176.90 x 5.70 mm		
Operating Temperature	-20°C ~ +70°C		
Pinout	20 - Way Connector	Box Quantity	Weight / Display
Pitch	---	---	---

RoHS compliant

Display Accessories	
Part Number	**Description**
MCIB14/16	HDMI-to-LVDS interface board, with voltage generation.

Optional Variants	
Appearances	**Voltage**

Summary

The MDT1040AIS-LVDS is a color active matrix thin film transistor (TFT) liquid crystal display (LCD) that uses amorphous silicon TFT as a switching device. It is composed of a TFT LCD panel, a timing controller, voltage reference, common voltage, column driver, and row driver circuit. This TFT LCD has a 10.4-inch diagonally measured active display area with XGA resolution (1,024 horizontal by 768 vertical pixels array).

General Specifications

- Size: 10.4 inch

- Dot Matrix: 1024 x R.G.B. x 768 dots

- Module dimension: 236.0*176.9*5.7 mm

- Active area: 211.2 *158.4 mm

- Dot pitch: 0.20625 x 0.20625 mm

- LCD type: TFT, Normally White, Transmissive

- Gray scale inversion direction: 6 o'clock

- Backlight Type: LED ,Normally White

- Interface: LVDS

- With /Without TP: Without TP

- Surface: Anti-Glare

*Color tone slight changed by temperature and driving voltage.

Interface

Signal Connector Type

Item	Description
Type/Part Number	MSB24013P20HA (Manufacture by STM)
Mating Receptacle / Type (Reference)	P24013P20 or compatible

Signal Connector Pin Assignment

Pin No.	Symbol	Description	Note
1	VDD	Power Supply, 3.3V (typical)	-
2	VDD	Power Supply, 3.3V (typical)	-
3	VSS	Ground	-
4	REV	Reverse Scan selection {High:2.5(min), 3.3(typ),3.6(max); Low: 0.5(max)}	(1)
5	Rin1-	-LVDS differential data input (R0-R5,G0)	-
6	Rin1+	+LVDS differential data input (R0-R5,G0)	-
7	VSS	Ground	-
8	Rin2-	-LVDS differential data input (G1-G5,B0-B1)	-
9	Rin2+	+LVDS differential data input (G1-G5,B0-B1)	-
10	VSS	Ground	-
11	Rin3-	-LVDS differential data input (B2-B5,HS,VS,DE)	-
12	Rin3+	+LVDS differential data input (B2-B5,HS,VS,DE)	-
13	VSS	Ground	-
14	ClkIN-	-LVDS differential clock input	-
15	ClkIN+	+LVDS differential clock input	-
16	GND	Ground	-
17	Rin4-	-LVDS differential data input (R6-R7,G6-G7,B6-B7)	-
18	Rin4+	+VDS differential data input (R6-R7,G6-G7,B6-B7)	-
19	SEL68	6/8 bits LVDS data input selection(H:8bits L/NC:6bits)	-
20	Bist	Internal use	-

Note (1) REV = LOW/NC   (2) REV = High
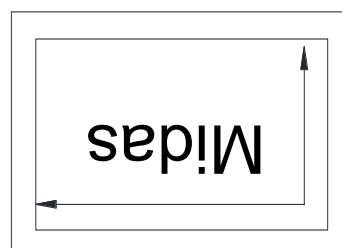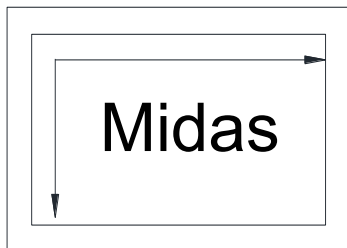
LVDS Receiver

Signal Electrical Characteristics For LVDS Receiver
The built-in LVDS receiver is compatible with (ANSI/TIA/TIA-644) standard.
Table 8 LVDS Receiver Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Differential Input High Threshold	Vth	-	-	+100	mV	VCM =+1.2V
Differential Input Low Threshold	Vtl	-100	-	-	mV	VCM =+1.2V
Magnitude Differential Input	|VID|	200	-	600	mV	-
Common Mode Voltage	VCM	1.0	1.2	1.4	V	Vth – Vtl=200 mV
Common Mode Voltage Offset	ΔVCM	-50	-	+50	mV	Vth – Vtl=200 mV

Note:(1) Input signals shall be low or Hi- resistance state when VDD is off.

(2) All electrical characteristics for LVDS signal are defined and shall be measured at the interface connector of LCD
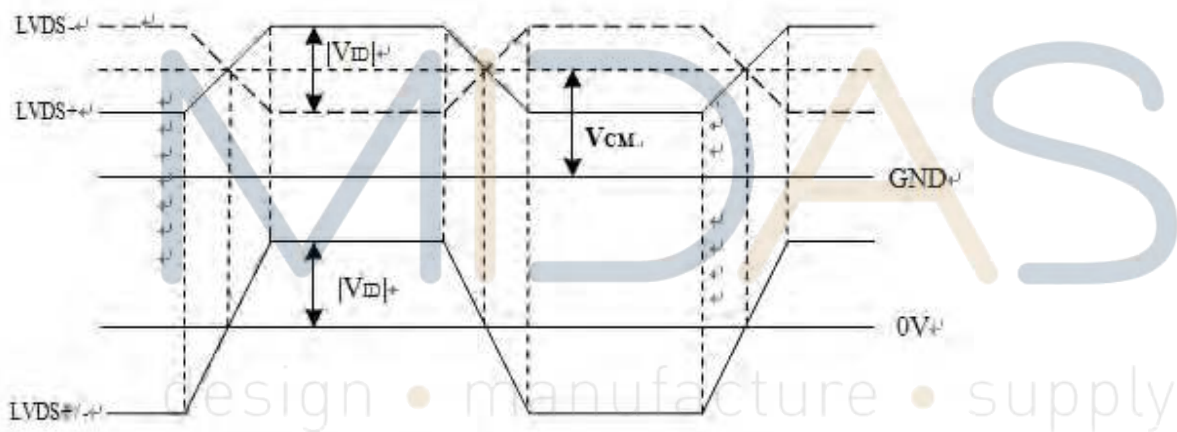
Figure 1 Voltage Definitions
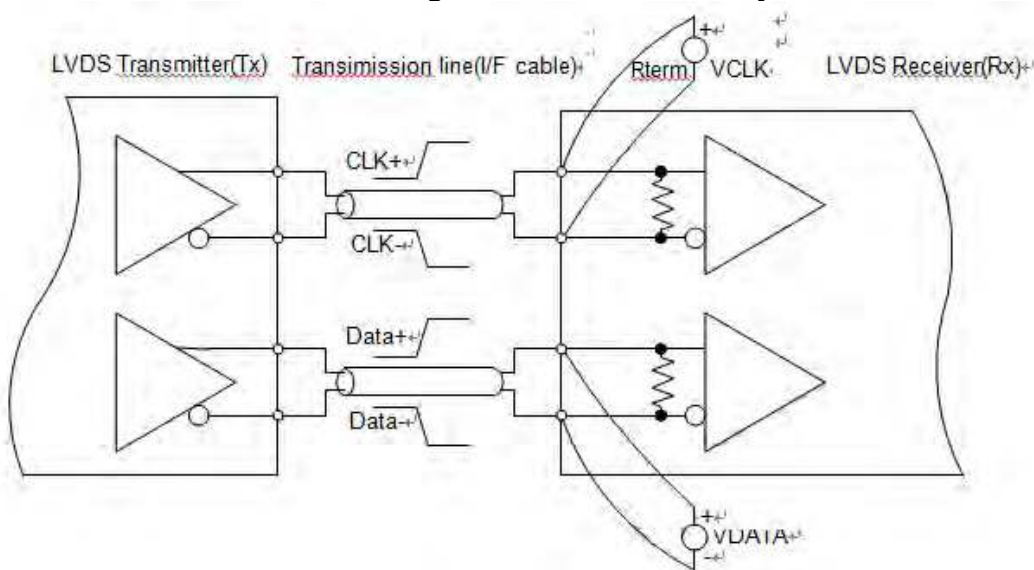

Figure 2 Measurement System
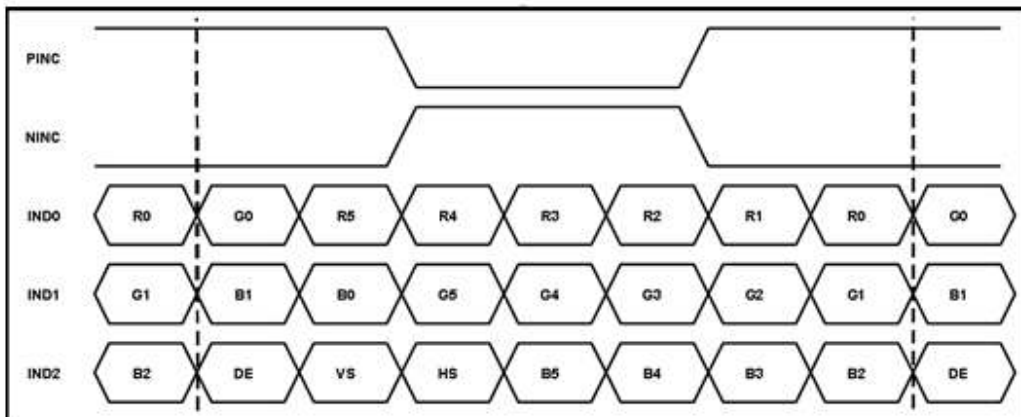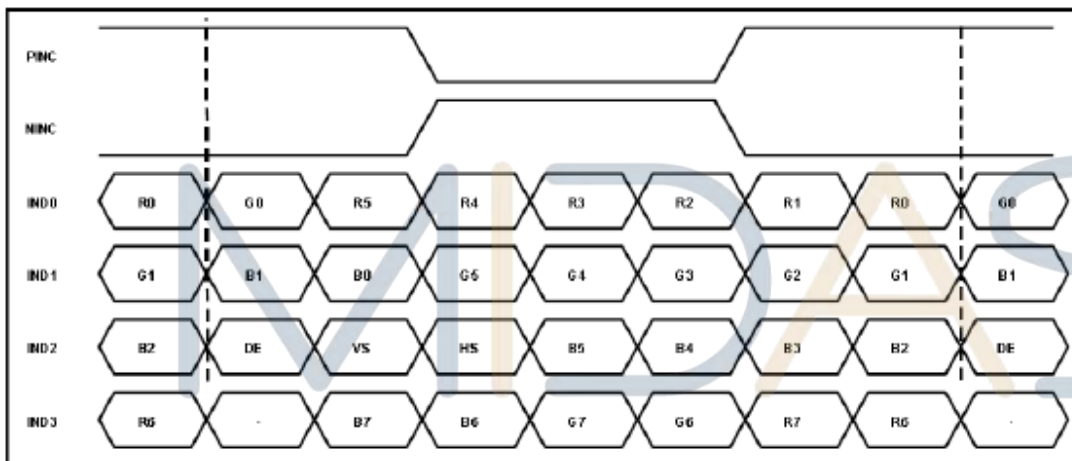
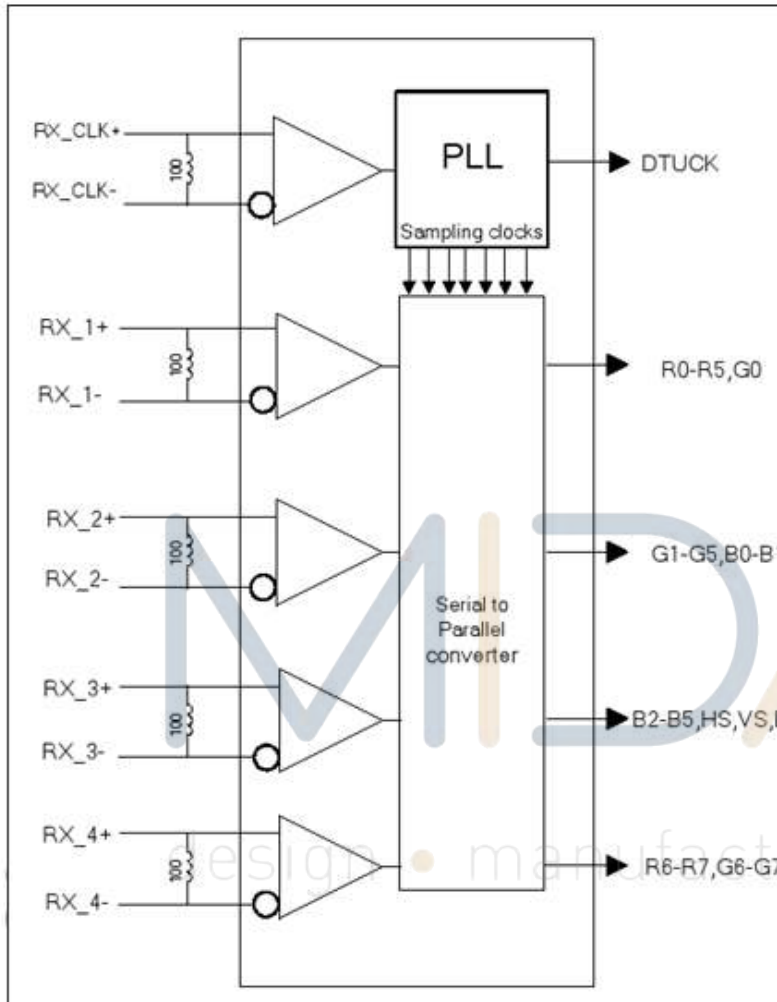**Figure 3 Data Mapping (6 Bit)**

Figure 4 Data Mapping (8 Bit)

LVDS Receiver Internal Circuit

Figure 4 LVDS Receiver Internal Circuit shows the internal block diagram of the LVDS receiver.
This LCD module equips termination resistors for LVDS link.

Figure 5 LVDS Receiver Internal Circuit

Backlight Connector Type

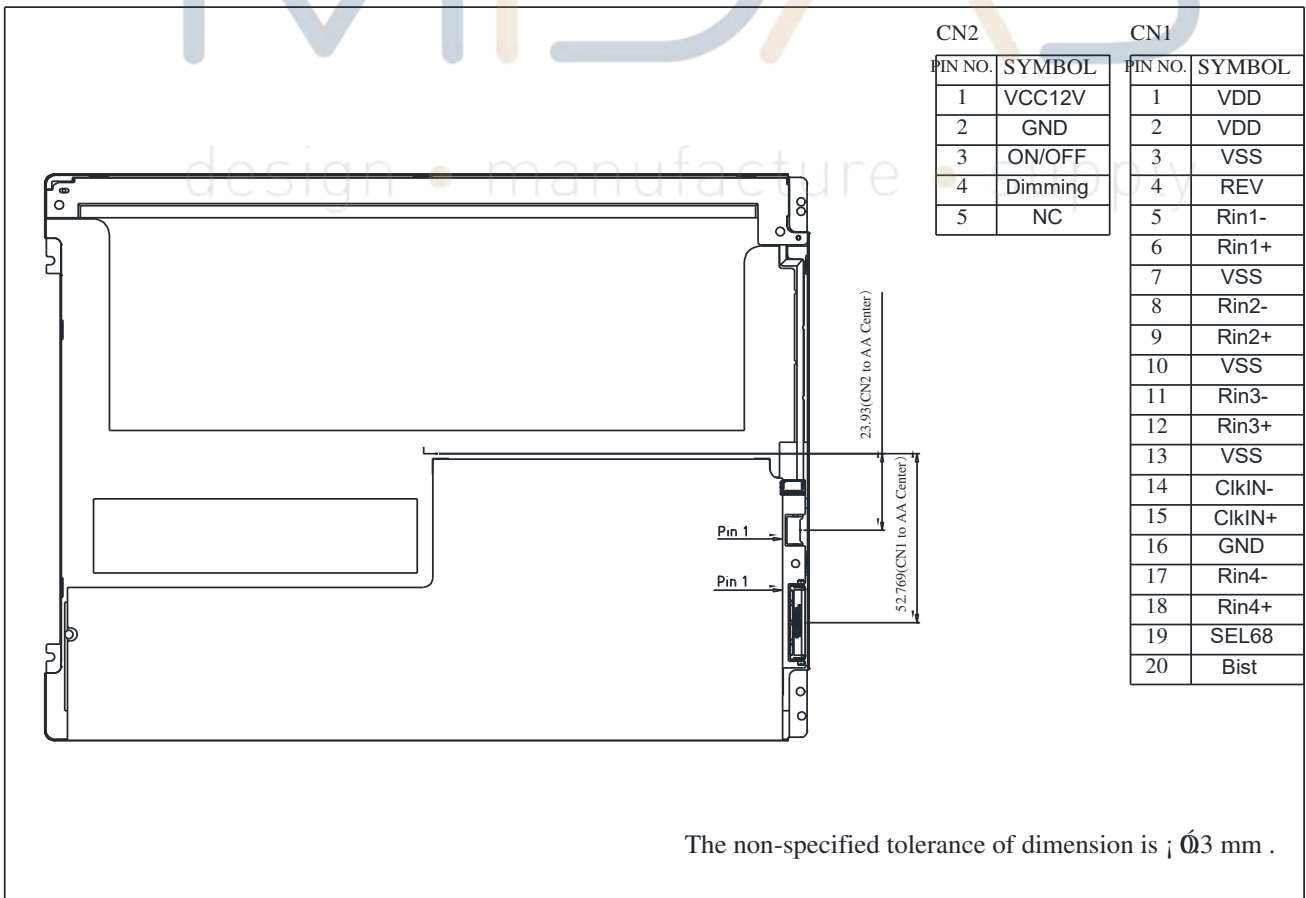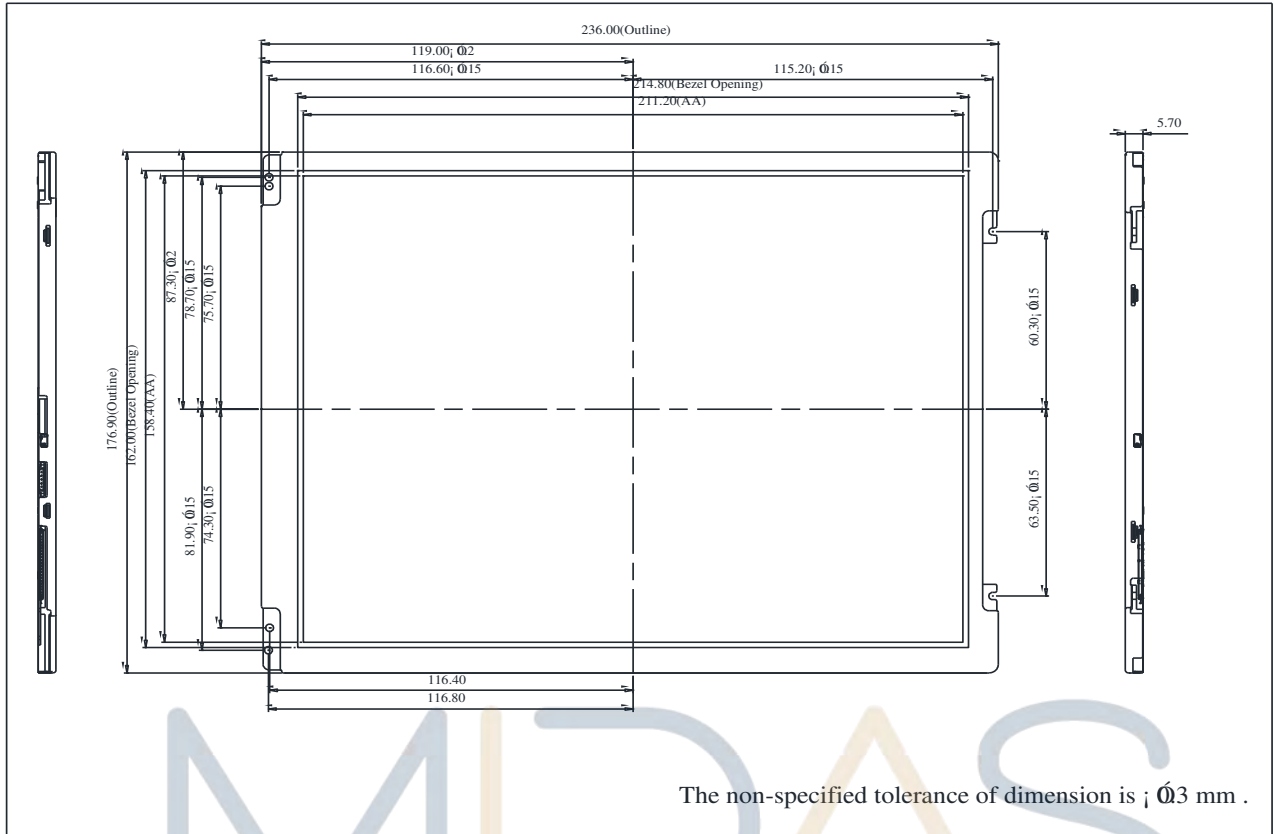| Item	Description
Type	MSB24038P5A (Manufacture by STM)
Mating Receptacle / Type (Reference)	P24038P5

Backlight Connector Pin Assignment

Pin No.	Symbol	Signal name
1	VCC	12V
2	GND	GND
3	ON/OFF	5V-ON,0V-OFF
4	Dimming	PWM Dimming or Analog Dimming
5	NC	NC

Contour Drawing

The non-specified tolerance of dimension is ±0.3 mm .

CN2	
PIN NO.	SYMBOL
1	VCC12V
2	GND
3	ON/OFF
4	Dimming
5	NC

CN1	
PIN NO.	SYMBOL
1	VDD
2	VDD
3	VSS
4	REV
5	Rin1-
6	Rin1+
7	VSS
8	Rin2-
9	Rin2+
10	VSS
11	Rin3-
12	Rin3+
13	VSS
14	ClkIN-
15	ClkIN+
16	GND
17	Rin4-
18	Rin4+
19	SEL68
20	Bist

The non-specified tolerance of dimension is ±0.3 mm .

Block Diagram
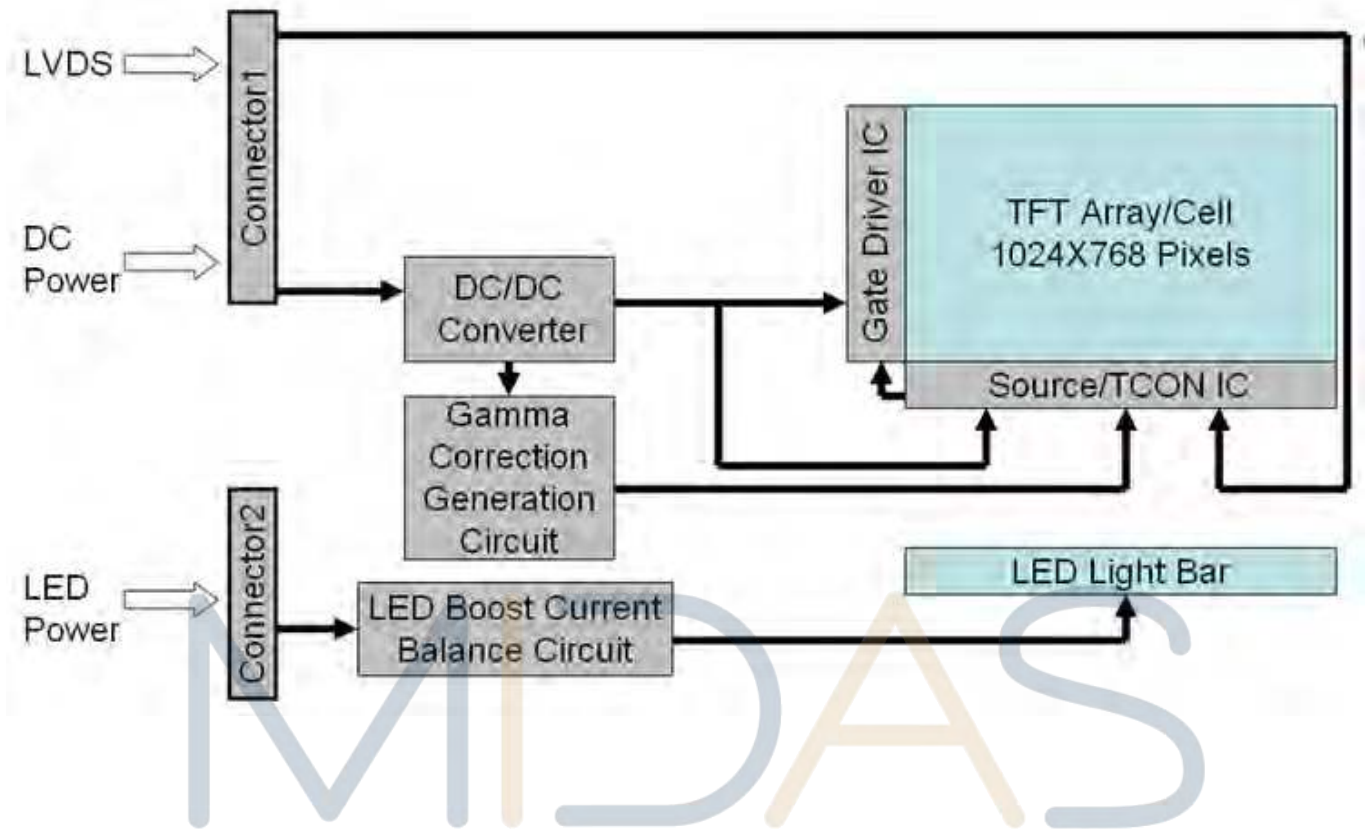
Absolute Maximum Ratings

Item	Symbol	Min	Typ	Max	Unit
Operating Temperature	TOP	-20	—	+70	℃
Storage Temperature	TST	-30	—	+80	℃

Note: Device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above
1.   Temp. ≦60℃, 90% RH MAX. Temp.＞60℃, Absolute humidity shall be less than 90% RH at 60℃

Electrical Characteristics

Input power specifications are as follows.

Table 1 Power Consumption

| Item		Symbol	Min.	Typ.	Max.	Units	Note
LCD Drive Voltage (Logic)		VDD	3.0	3.3	3.6	V	(2), (4)
VDD Current	Black Pattern	IDD	-	TBD	(0.25)	A	(3),(4)
VDD Power Consumption	Black Pattern	PDD	-	-	(0.84)	W	
Rush Current		Irush	-	-	1.5	A	(1),(4)
Allowable Logic/LCD Drive Ripple Voltage		VDDrp	-	-	(200)	mV	(4)

Note (1) Measure Condition

Figure 15 VDD Rising Time
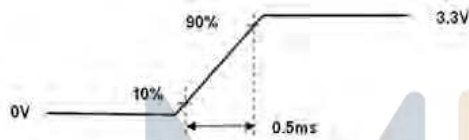
Note (2) VDD Power Dip Condition

If VTH＜VDD≤Vmin，then td≤10ms；when the voltage return to normal our panel must revive automatically
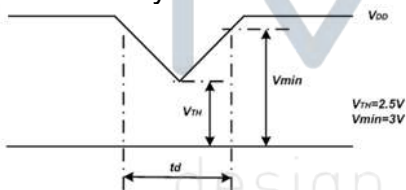
Note (3) Frame Rate=60Hz, VDD=3.3V,DC Current.

Note (4) Operating temperature 25℃, humidity 55%RH.

Power ON/OFF Sequence

VDD power on/off sequence is as follows. Interface signals are also shown in the chart.

Signals from any system shall be Hi- resistance state or low level when VDD is off.
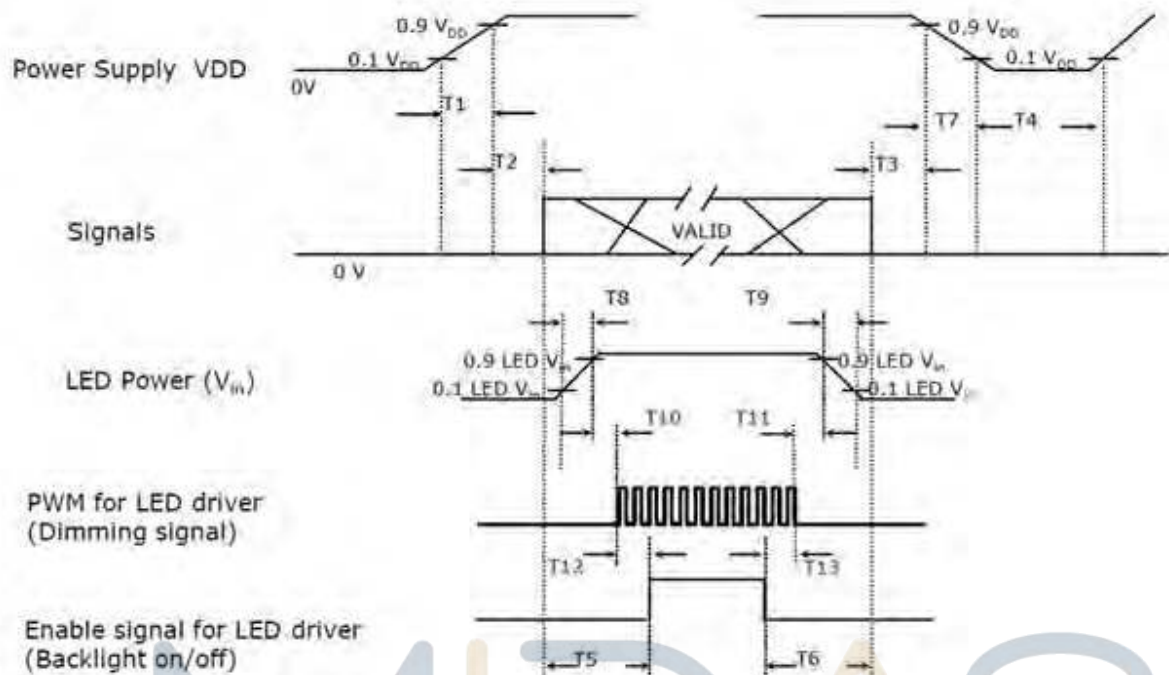
Figure 17 Power Sequence

Table 2 Power Sequencing Requirements

Power ON/OFF Sequence					
Items	Symbol	MIN	TYP	MAX	Unit
VDD rising time from 10% to 90%	T1	0.5	-	10	ms
Delay from VDD to valid data at power ON	T2	30	-	50	ms
Delay from valid data OFF to VDD OFF at power OFF	T3	0	-	50	ms
VDD OFF time for windows restart	T4	500	-	-	ms
Delay from valid data to B/L enable at power ON	T5	200	-	-	ms
Delay from valid data off to B/L disable at power Off	T6	200	-	-	ms
VDD falling time from 90% to 10%	T7	0.5	-	10	ms
LED Vin rising time from 10% to 90%	T8	0.5	-	10	ms
LED Vin falling time from 90% to 10%	T9	0.5	-	10	ms
Delay from LED driver Vin rising time 90% to PWM ON	T10	0	-	-	ms
Delay from PWM Off to LED driver Vin falling time 10%,Must keep rule	T11	0	-	-	ms
Delay from PWM ON to B/L Enable ON, Must keep rule	T12	0	-	-	ms
Delay from B/L Enable Off to PWM Off	T13	0	-	-	ms

Parameter Guideline Of LED Backlight

Table 3 Parameter Guideline for LED Backlight

Item	Symbol		Min.	Typ.	Max.	Units	Note
LED Input Voltage	V_LED		10.8	12	12.6	V	(2),(3)
LED Power Consumption	P_LED		-	-	(2.88)	W	(2),(3)
LED Forward Voltage	VF		2.8	3.2	3.6	V	
LED Forward Current	IF		-	20	30	mA	
PWM Signal Voltage	VPW M_EN	High	4.5	5	5.5	V	(2)
		Low	0	-	0.4		
LED Enable Voltage	VLED_EN	High	2.0	5	5.5	V	
		Low	0	-	0.4		
Input PWM Frequency	FPWM		100	-	1K	Hz	
LED Life Time	LT		30,000	-	-	Hours	(1)(2)
Duty Ratio	PWM		5	-	100	%	(2)

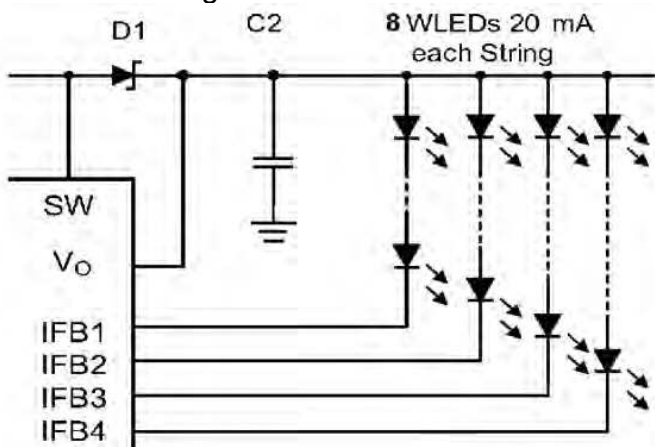Note (1) The LED life time define as the estimated time to 50% degradation of initial luminous.
Note (2) Operating temperature 25℃, humidity 55%RH.
Note (3) A higher LED power supply voltage will result in better power efficiency. Keep the V_LED between 12V and 12.6V is strongly recommended.
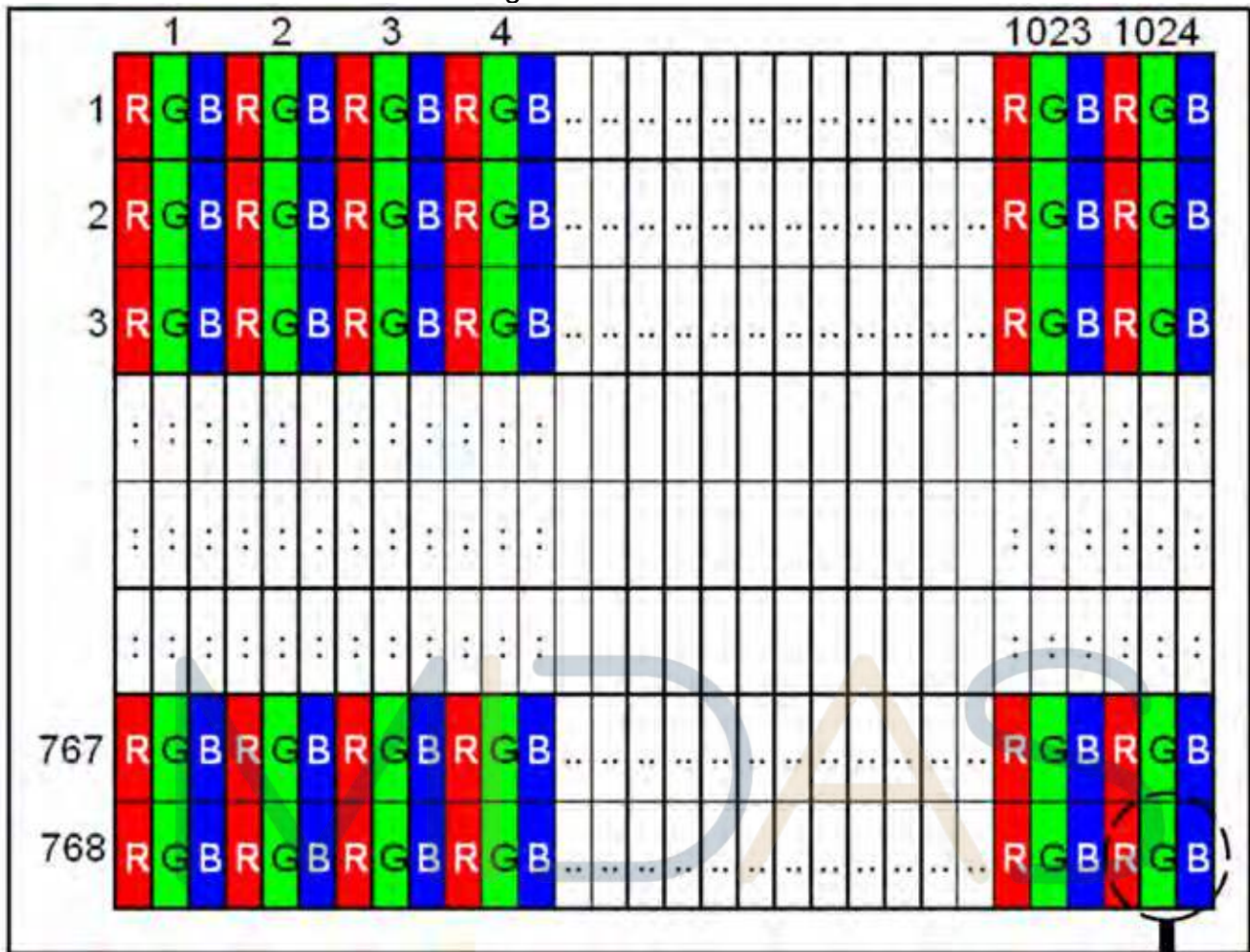
Figure 8 LED Rush Current Measure Condition
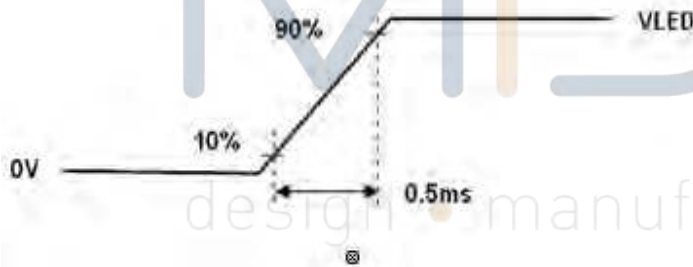
LED Circuit Diagram

Pixel Format Image

Figure 1 shows the relationship of the input signals and LCD pixel format image.

Figure 1 Pixel Format

Interface Timings

Timing Characteristics Synchronization method should be DE mode. Table 1 Interface Timings

Parameter	Symbol	Unit	Min.	Typ.	Max.
LVDS Clock Frequency	Fclk	MHz	(52)	(65)	(71)
H Total Time	HT	Clocks	(1,114)	(1,344)	(1,400)
H Active Time	HA	Clocks	1,024	1,024	1,024
H Blanking Time	HBL	Clocks	(90)	(320)	(376)
V Total Time	VT	Lines	(778)	(806)	(845)
V Active Time	VA	Lines	768	768	768
V Blanking Time	VBL	Lines	(10)	(38)	(77)
Frame Rate	Vsync	Hz	55	60	65

Note: H Blanking Time and V Blanking Time can not be changed at every frame.

Optical Characteristics

Item		Symbol	Condition.	Min	Typ.	Max.	Unit	Remark
Response time		Tr	θ=0° 、Φ=0°	-	16	-	.ms	Note 3,5
		Tf						
Contrast ratio		CR	At optimized viewing angle	720	900	-	-	Note 4,5
Color Chromaticity	White	Wx	θ=0° 、Φ=0	0.26	0.31	0.36		Note 2,6,7
		Wy		0.28	0.33	0.38		
Viewing angle	Hor.	ΘR	CR≧10	70	75	-	Deg.	Note 1
		ΘL		70	75	-		
	Ver.	ΦT		70	75	-		
		ΦB		70	75	-		
Brightness		-	-	300	350	-	cd/m²	Center of display

Ta=25±2℃,

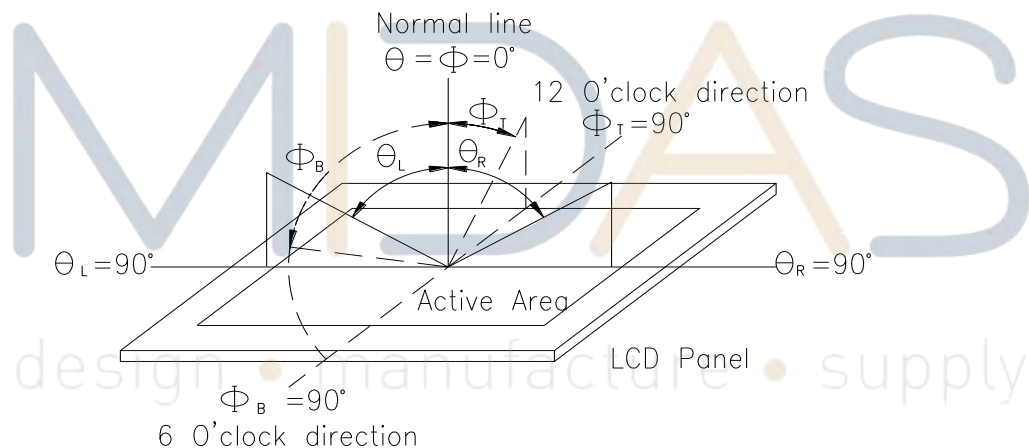Note 1: Definition of viewing angle range

Fig.11.1. Definition of viewing angle

Note 2: Test equipment setup:
After stabilizing and leaving the panel alone at a driven temperature for 10 minutes, the measurement should be executed. Measurement should be executed in a stable, windless, and dark room. Optical specifications are measured by Topcon BM-7orBM-5 luminance meter 1.0° field of view at a distance of 50cm and normal direction.
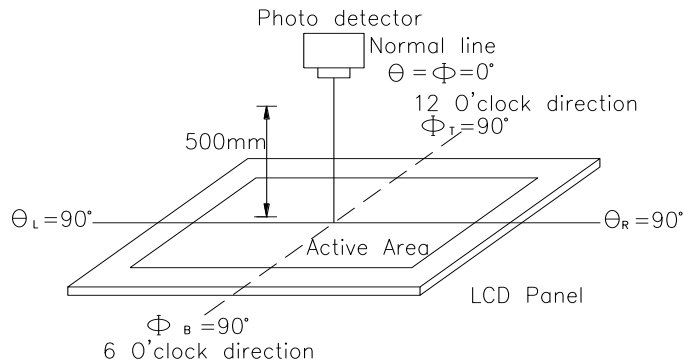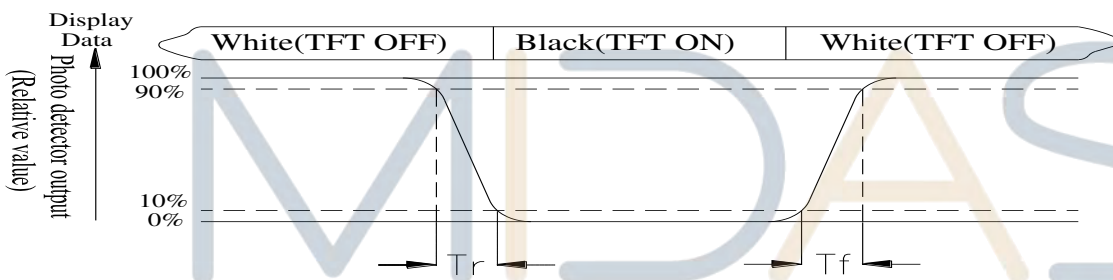
Fig. 11.2.   Optical measurement system setup

Note 3: Definition of Response time:

The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time, Tr, is the time between photo detector output intensity changed from 90%to 10%. And fall time, Tf, is the time between photo detector output intensity changed from 10%to 90%

Note 4: Definition of contrast ratio:

The contrast ratio is defined as the following expression.

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

Note 5: White Vi = Vi50 ± 1.5V

Black Vi = Vi50 ± 2.0V

"±" means that the analog input signal swings in phase with VCOM signal.

"±" means that the analog input signal swings out of phase with VCOM signal.

The 100% transmission is defined as the transmission of LCD panel when all the input terminals of module are electrically opened.

Note 6: Definition of color chromaticity (CIE 1931)

Color coordinates measured at the center point of LCD

Note 7: Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

Reliability

Content of Reliability Test (Wide temperature, -20℃~70℃)

Environmental Test			
Test Item	**Content of Test**	**Test Condition**	**Note**
High Temperature storage	Endurance test applying the high storage temperature for a long time.	80℃ 200hrs	2
Low Temperature storage	Endurance test applying the low storage temperature for a long time.	-30℃ 200hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	70℃ 200hrs	——
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-20℃ 200hrs	1
High Temperature/ Humidity Operation	The module should be allowed to stand at 60℃,90%RH max	60℃,90%RH 96hrs	1,2
Thermal shock resistance	The sample should be allowed stand the following 10 cycles of operation -20℃　　25℃　　70℃ 30min　5min　30min 1 cycle	-20℃/70℃ 10 cycles	——
Vibration test	Endurance test applying the vibration during transportation and using.	Total fixed amplitude : 1.5mm Vibration Frequency : 10~55Hz One cycle 60 seconds to 3 directions of X,Y,Z for Each 15 minutes	3
Static electricity test	Endurance test applying the electric stress to the terminal.	VS=±600V(contact) ,±800v(air), RS=330Ω CS=150pF 10 times	——

Note1: No dew condensation to be observed.

Note2: The function test shall be conducted after 4 hours storage at the normal
        Temperature and humidity after remove from the test chamber.

Note3: The packing have to including into the vibration testing.