User's Guide

SNVA273B–October 2007–Revised May 2013

AN-1687 LM20125 Evaluation Board

1 Introduction

The LM20125 is a full featured buck switching regulator capable of driving up to 5A of load current. The nominal 500 kHz switching frequency of the LM20125 reduces the size of the power stage components while still allowing for highly efficient operation. The LM20125 is capable of converting an input voltage between 2.95 V and 5.5 V down to an output voltage as low as 0.8 V. Fault protection features include cycle-by-cycle current limit, output power good, and output over-voltage protection. The dual function soft-start/tracking pin can be used to control the startup response of the LM20125, and the precision enable pin can be used to easily sequence the LM20125 in applications with sequencing requirements. The LM20125 is available in a 16-pin HTSSOP package with an exposed pad for enhanced thermal performance.

The LM20125 evaluation board has been designed to balance overall solution size with the efficiency of the regulator. The evaluation board measures just under 1.3” x 1.1” on a two layer PCB, with all components placed on the top layer. The power stage and compensation components of the LM20125 evaluation board have been optimized for an input voltage of 5 V, but for testing purposes, the input can be varied across the entire operating range. The output voltage of the evaluation board is nominally 1.2 V, but this voltage can be easily changed by replacing one of the feedback resistors (R_{FB1} or R_{FB2}). The control loop compensation of the LM20125 evaluation board has been designed to provide a stable solution over the entire input and output voltage range with a reasonable transient response. The EN pin must be above 1.18 V (typ) on the board to initiate switching. If the EN function is not necessary, the EN pin should be externally tied to V_{IN}.

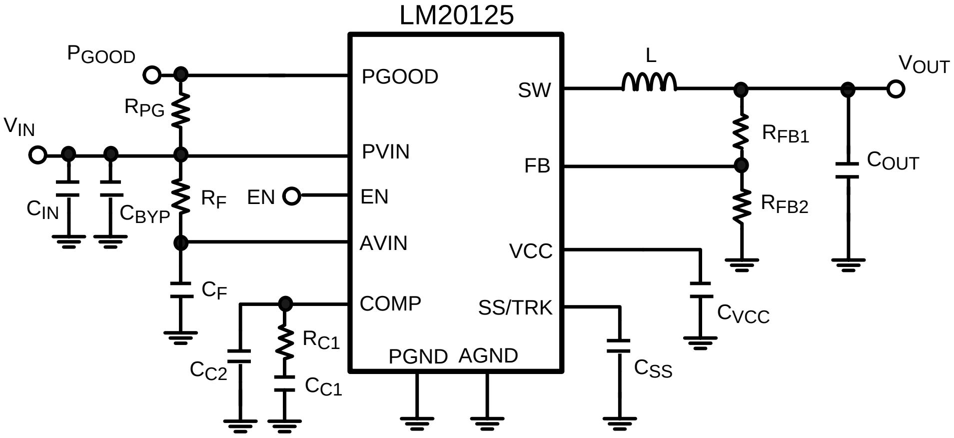


Figure 1. Evaluation Board Schematic

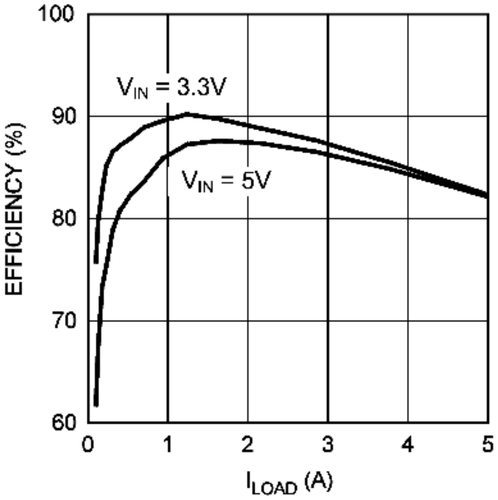
2 Bill of Materials

Designator	Description	Part Number	Qty	Manufacturer
U1	Synchronous Buck Regulator	LM20125	1	Texas Instruments
C_{IN}	100 µF, 1210, X5R, 6.3 V	GRM32ER60J107ME20	1	Murata
C_{BYP}	1 µF, 0603, X5R, 6.3 V	GRM188R60J105KA01	1	Murata
C_{OUT}	100 µF, 1210, X5R, 6.3 V	GRM32ER60J107ME20	1	Murata
L	1 µH, 6 mΩ	MSS1038-102NL	1	Coilcraft
R_F	1Ω, 0603	CRCW06031R0J-e3	1	Vishay-Dale
C_F	100 nF, 0603, X7R, 16 V	GRM188R71C104KA01	1	Murata
CV_{VCC}	1 µF, 0603, X5R, 6.3 V	GRM188R60J105KA01	1	Murata
R_{PG}	10 kΩ, 0603	CRCW06031002F-e3	1	Vishay-Dale
R_{C1}	4.64 kΩ, 0603	CRCW06034641F-e3	1	Vishay-Dale
C_{C1}	3.3 nF, 0603, X7R, 25 V	VJ0603Y332KXXA	1	Vishay-Vitramon
C_{C2}	OPEN	OPEN	0	N/A
C_{SS}	33 nF, 0603, X7R, 25 V	VJ0603Y333KXXA	1	Vishay-Vitramon
R_{FB1}	4.99 kΩ, 0603	CRCW06034991F-e3	1	Vishay-Dale
R_{FB2}	10 kΩ, 0603	CRCW06031002F-e3	1	Vishay-Dale
Test Points	Test Points	160-1026-02-01-00	7	Cambion

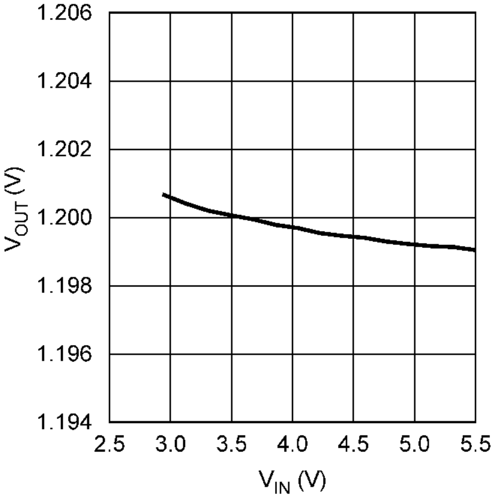
3 Connection Descriptions

Terminal Silkscreen	Description
V_{IN}	This terminal is the input voltage to the device. The device will operation over the input voltage range of 2.95 V to 5.5 V. The absolute maximum voltage rating for this pin is 6 V.
GND	This terminal is the ground connection to the device. There are two different GND connections on the PCB. One should be used for the input supply and the other for the load.
V_{OUT}	This terminal connects to the output voltage of the power supply and should be connected to the load.
EN	This terminal connects to the enable pin of the device. This terminal should be connected to V_{IN} or driven externally. If driven externally, a voltage typically greater than 1.18 V will enable the device. The operating voltage for this pin should not exceed 5.5 V. The absolute maximum voltage rating on this pin is 6 V.
SS/TRACK	This terminal provides access to the SS/TRK pin of the device. Connections to this terminal are not needed for most applications. The feedback pin of the device will track the voltage on the SS/TRK pin if it is driven with an external voltage source that is below the 0.8 V reference. The voltage on this pin should not exceed 5.5 V during normal operation. The absolute maximum voltage rating on this pin is 6 V.
PGOOD	This terminal connects to the power good output of the device. There is a 10 kΩ pull-up resistor from this pin to the input voltage. The voltage on this pin should not exceed 5.5 V during normal operation and has an absolute maximum voltage rating of 6 V.

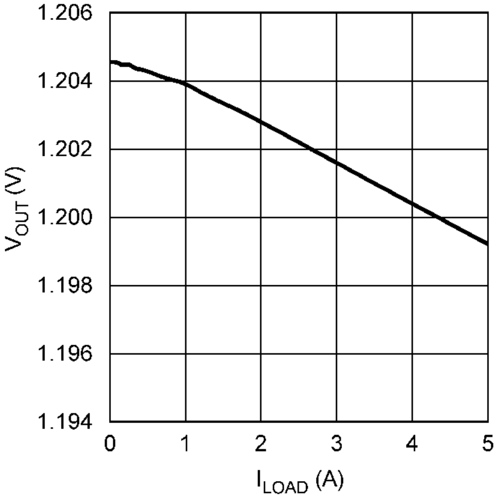
4 Performance Characteristics



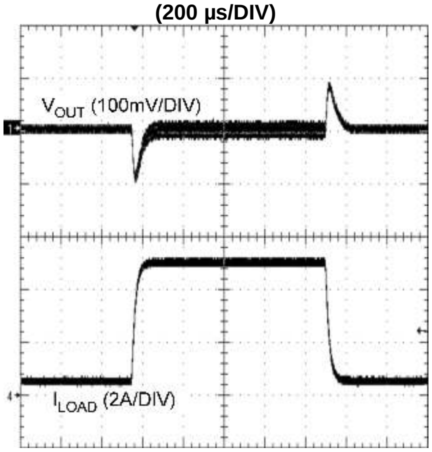
Efficiency vs Load



Line Regulation (I_{LOAD} = 5A)

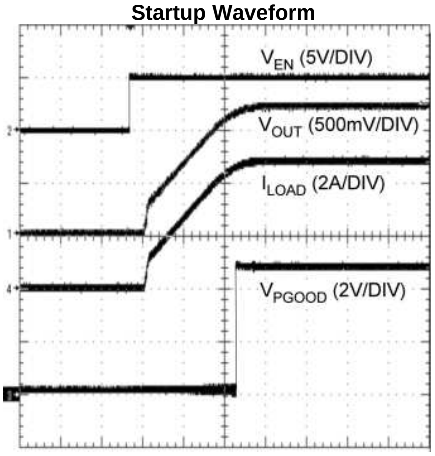


Load Regulation (V_{IN} = 5 V)



0.5A to 5A Load Transient Response (200 µs/DIV)

Startup Waveform



5 Component Selection

This section provides a walk-through of the design process of the LM20125 evaluation board. Unless otherwise indicated, all equations assume units of Amps (A) for current, Farads (F) for capacitance, Henries (H) for inductance, and Volts (V) for voltages.

5.1 Input Capacitor

The required RMS current rating of the input capacitor for a buck regulator can be estimated by Equation 1:

$$I_{CIN(RMS)} = I_{OUT}\sqrt{D(1 - D)} \tag{1}$$

The variable D refers to the duty cycle, and can be approximated by:

$$D = \frac{V_{OUT}}{V_{IN}} \tag{2}$$

From Equation 3, it follows that the maximum $I_{CIN(RMS)}$ requirement occurs at a full 5A load current with the system operating at 50% duty cycle. Under this condition, the maximum $I_{CIN(RMS)}$ is given by:

$$I_{CIN(RMS)} = 5A\sqrt{0.5 \text{ x } 0.5} = 2.5A \tag{3}$$

Ceramic capacitors feature a very large I_{RMS} rating in a small footprint, making a ceramic capacitor ideal for this application. A 100 µF X5R ceramic capacitor from Murata with a 5.4A I_{RMS} rating provides the necessary input capacitance for the evaluation board. For improved bypassing, a small 1 µF high frequency capacitor is placed in parallel with the 100 µF bulk capacitor to filter high frequency noise pulses on the supply.

5.2 AV_{IN} Filter

An RC filter should be added to prevent any switching noise on PV_{IN} from interfering with the internal analog circuitry connected to AV_{IN}. These can be seen on the schematic as components R_F and C_F. There is a practical limit to the size of the resistor R_F as the AV_{IN} pin will draw a short 60mA burst of current during startup, and if R_F is too large the resulting voltage drop can trigger the UVLO comparator. For the demo board, a 1Ω resistor is used for R_F ensuring that UVLO will not be triggered after the part is enabled. A recommended 1 µF C_F capacitor coupled with the 1 Ω resistor provides roughly 16dB of attenuation at the 1 MHz switching frequency.

5.3 Inductor

As per the device-specific data sheet recommendations, the inductor value should initially be chosen to give a peak-to-peak ripple current equal to roughly 30% of the maximum output current. The peak-to-peak inductor ripple current can be calculated by Equation 4:

$$\Delta I_{P-P} = \frac{(V_{IN} - V_{OUT}) \times D}{L \times f_{SW}} \tag{4}$$

Rearranging this equation and solving for the inductance reveals that for this application (V_{IN} = 5 V, V_{OUT} = 1.2 V, f_{SW} = 500 kHz, and I_{OUT} = 5A), the nominal inductance value is roughly 1.22 µH. A final inductance of 1 µH is selected to minimize the inductor size and DC resistance. This results in a peak-to-peak ripple current of 1.8A and 2.24A when the converter is operating from 5 V and 3.3 V, respectively. Once an inductance value is calculated, an actual inductor needs to be selected based on a trade-off between physical size, efficiency, and current carrying capability. For the LM20125 evaluation board, a Coilcraft MSS1038-102NL inductor offers a good balance between efficiency (6 mΩ DCR), size, and saturation current rating (9A I_{SAT} rating). If the output voltage of the evaluation board is increased there is a chance the device may hit current limit at 5A output. To avoid current limit with higher output voltages the value of the inductor should be increased to reduce the ripple current.

5.4 Output Capacitor

The value of the output capacitor in a buck regulator influences the voltage ripple that will be present on the output voltage, as well as the large signal output voltage response to a load transient. Given the peak-to-peak inductor current ripple (ΔI_{P-P}) the output voltage ripple can be approximated by Equation 5:

$$\Delta V_{OUT} = \Delta I_{P-P} \times \left[R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}} \right] \tag{5}$$

The variable R_{ESR} above refers to the ESR of the output capacitor. As can be seen in Equation 5, the ripple voltage on the output can be divided into two parts, one of which is attributed to the AC ripple current flowing through the ESR of the output capacitor and another due to the AC ripple current actually charging and discharging the output capacitor. The output capacitor also has an effect on the amount of droop that is seen on the output voltage in response to a load transient event.

For the evaluation board, a Murata 100 µF ceramic capacitor is selected for the output capacitor to provide good transient and DC performance in a relatively small package. From the technical specifications of this capacitor, the ESR is roughly 2 mΩ, and the effective in-circuit capacitance is approximately 55 µF (reduced from 100 µF due to the 1.2 V DC bias). With these values, the peak-to-peak voltage ripple on the output when operating from a 5 V input can be calculated to be 12 mV.

5.5 C_{SS}

A soft-start capacitor can be used to control the startup time of the LM20125 voltage regulator. The startup time of the regulator when using a soft-start capacitor can be estimated by Equation 6:

$$t_{SS} = \frac{0.8V \times C_{SS}}{I_{SS}} \tag{6}$$

For the LM20125, I_{SS} is nominally 5 µA. For the evaluation board, the soft-start time has been designed to be roughly 5 ms, resulting in a C_{SS} capacitor value of 33 nF.

5.6 C_{VCC}

The C_{VCC} capacitor is necessary to bypass an internal 2.7 V sub-regulator. This capacitor should be sized equal to or greater than 1 µF, but less than 10 µF. A value of 1 µF is sufficient for most applications..

5.7 C_{C1}

The capacitor, C_{C1} is used to set the crossover frequency of the LM20125 control loop. Since this board was optimized to work well over the full input, output voltage, and frequency range, the value of C_{C1} was selected to be 3.3 nF. Once the operating conditions for the device are known, the transient response can be optimized by reducing the value of C_{C1} and calculating the value for R_{C1} as outlined in Section 5.8.

5.8 R_{C1}

Once the value of C_{C1} is known, resistor R_{C1} is used to place a zero in the control loop to cancel the output filter pole. This resistor can be sized according to Equation 7:

$$R_{C1} = \left[\frac{C_{C1}}{C_{OUT}} \times \left[\frac{I_{OUT}}{V_{OUT}} + \frac{1 - D}{f_{SW} \times L} + \frac{15 \times D}{V_{IN}}\right]\right]^{-1} \tag{7}$$

For stability purposes, the device should be compensated for the maximum output current expected in the application.

5.9 C_{C2}

A second compensation capacitor, C_{C2}, can be used in some designs to provide a high frequency pole, useful for cancelling a possible zero introduced by the ESR of the output capacitor. For the LM20125 evaluation board, the C_{C2} footprint is unpopulated, as the low ESR ceramic capacitor used on the output does not contribute a zero to the control loop before the crossover frequency. If the ceramic capacitor on the evaluation board is replaced with a different capacitor having significant ESR, the required value of the capacitor C_{C2} can be estimated by Equation 8:

$$C_{C2} = \frac{C_{OUT} \times R_{ESR}}{R_{C1}} \tag{8}$$

5.10 R_{FB1} and R_{FB2}

The resistors labeled R_{FB1} and R_{FB2} create a voltage divider from V_{OUT} to the feedback pin that is used to set the output of the voltage regulator. Nominally, the output of the LM20125 evaluation board is set to 1.2 V, giving resistor values of R_{FB1} = 4.99 kΩ and R_{FB2} = 10 kΩ. If a different output voltage is required, the value of R_{FB1} can be adjusted according to Equation 9:

$$R_{FB1} = \left(\frac{V_{OUT}}{0.8} - 1\right) \times R_{FB2} \tag{9}$$

R_{FB2} does not need to be changed from its value of 10 kΩ.

6 PCB Layout

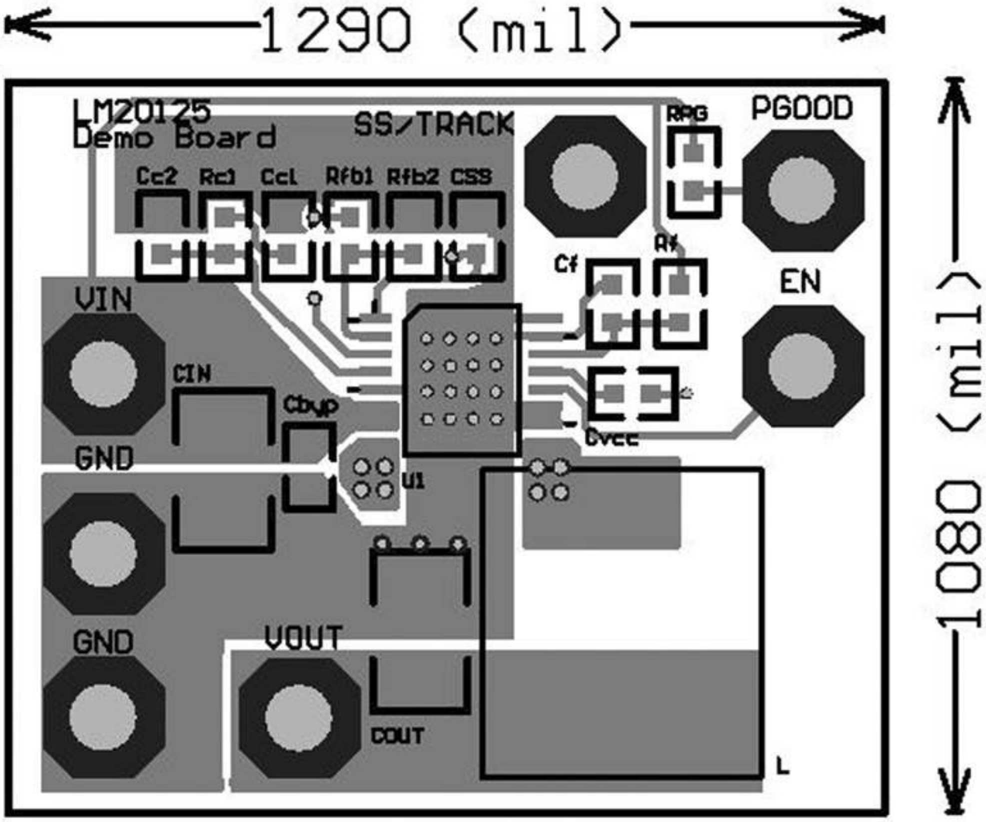


Figure 2. Top Layer

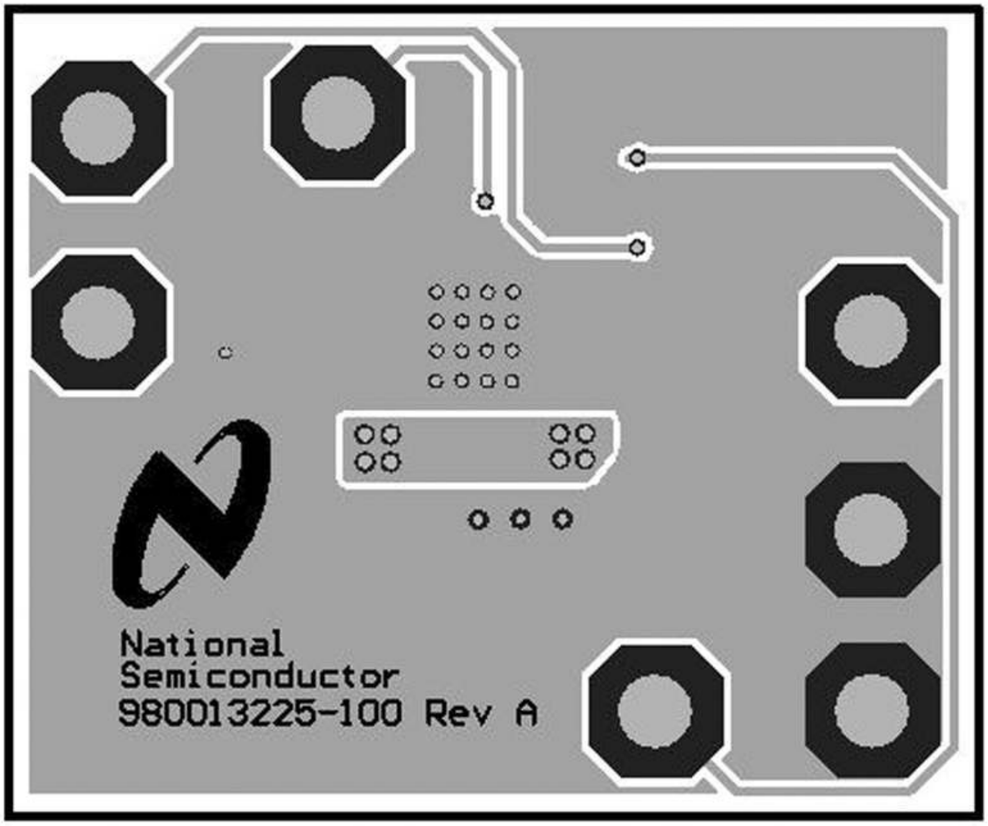


Figure 3. Bottom Layer

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