Quick Start Guide for testing the AD6649 IF Diversity Receiver Customer Evaluation Board Using the FPGA based Capture Board HSC-ADC-EVALCZ



Figure 1: AD6649 Evaluation Board with HSC-ADC_EVALCZ Data Capture Board

Equipment Needed

- ► Analog signal source and anti-aliasing filter
- ► Analog Clock Source
- ► PC
- ► USB 2.0 port recommended (USB 1.1-compatible)
- ► AD6649 evaluation board
- ► HSC-ADC-EVALCZ FPGA Based Data Capture Board

Documents Needed

- ► AD6649 Datasheet
- ► VisualAnalog Converter Evaluation Tool User Manual, AN-905
- ▶ High Speed ADC SPI Control Software User Manual, AN-878
- ▶ Interfacing to High Speed ADCs via SPI, AN-877

Software Needed

- ► VisualAnalog
- ► SPIController

All documents and software are available at <u>http://www.analog.com/fifo</u>. For any questions please send an email to <u>highspeed.converters@analog.com</u>.

AD6649 Filter Modes

The AD6649 IF diversity receiver supports 2 different filter modes. The first mode supports a 95MHz output bandwidth at 245.76MSPS with the fixed-frequency NCO and low latency FIR filter. The second mode supports a 100MHz output bandwidth at 245.76MSPS with a tunable NCO and high performance FIR filter. The evaluation platform supports both of these modes.

Testing

- **1.** Connect the AD6649 evaluation board and the HSC-ADC-EVALCZ board together as shown in Figure 1.
- **2.** Connect one 6V, 2A switching power supply (such as the CUI EPS060250UH-PHP-SZ supplied) to the AD6649 board.
- **3.** Make sure a jumper is installed on header J9 at the 2.5V position on the HSC-ADC-EVALCZ evaluation board to set the FPGA I/O voltage to 2.5V. Connect one 6V, 2A switching power supply (such as the CUI EPS060250UH-PHP-SZ supplied) to the HSC-ADC-EVALCZ board.
- 4. Connect the HSC-ADC-EVALCZ board to the PC with a USB cable. (Connect to J6.)
- 5. On the ADC evaluation board, make sure that jumpers are installed on headers P105, P108, P104, P107, P110, and P103 for the default setup.
- 6. On the ADC evaluation board, provide a clean, low jitter clock source to connector J506 at the desired ADC conversion rate. If the AD6649 input clock divider is used provide a clock into connector J506 at the appropriate rate which will be divided to your desired clock rate. The input clock level should be between 10dBm and 14dBm.
- 7. On the ADC evaluation board, use a clean signal generator with low phase noise to provide an input signal to the analog input at connector J301 (Channel A) and/or J303 (Channel B). Use a 1 m, shielded, RG-58, 50 Ω coaxial cable to connect the signal generator. For best results use a narrow-band, band-pass filter with 50 Ω terminations and an appropriate center frequency. (ADI uses TTE, Allen Avionics, and K&L band-pass filters.) In order for the input level to be near the ADC's full scale, the generator level should be set to 8dBm to 12dBm – this level depends on the input frequency and any losses in bandpass filters.
- 8. Open VisualAnalog on the PC. "AD6649" should be listed in the status bar of the "New Canvas" window. Select the template that corresponds to the type of testing that you are performing. Select 'Yes' when VisualAnalog prompts for programming the FPGA. The 'DONE' LED should illuminate on the HSC-ADC-EVALCZ board indicating that the FPGA has been correctly programmed. (If Visual Analog does not prompt for programming the FPGA select the ADC Data Capture Settings window and click on the 'Capture Board' tab. In the FPGA box select program to configure the FPGA.)

- **9.** Next open the SPI Controller software. If prompted for a configuration file, select the file titled AD6649spiR03.cfg. If not, check the title bar of the window to see which configuration is loaded. If necessary, choose "Cfg Open" from the "File" menu and select the configuration file named above. Note that the CHIP ID(1) field may be filled whether the correct SPI Controller configuration file is loaded or not.
- **10.** Click the New DUT button (**N**) in SPI Controller.
- **11.** Set the DCO Clk Delay Enable checkbox in the FLEXOUTPUT DELAY(17) panel on the ADCBase0 tab as shown below. In addition, set the DCO Clk Delay register to the '600ps additional delay on DCO pin'. These settings align the output timing with the input timing on the capture FPGA.

SPIController 1	.0.57.3 : USB Ezu	sb-0 : CS 1 :	AD6649spiR03.cfg : AD6649spiR03.cal			
File Config Help						
	£					
Global ADCBase 0 ADC A ADC	B					
Duty Cycle Stabilizer	Master Sync En	PATT1(1A-19)				
CLK DIV(B) Phase - clk cycles delayed	Sync Mode © Continuous Mode © Next Sync Mode	USER TEST PATT2(1C-1B) 0 E hex				
Divide ratio	OUTPUT ADJUST(15) Output Port LVDS Drive Current	USER TEST PATT3(1E-1D) 0 _E hex				
FLEX OUTPUT PHASE(16)	MODES(8)	USER TEST PATT4(20-1F)				
VREF(18) Vref Adjust 1.75V pk-pk	Full Pwr dn Standby					
FLEX OUTPUT DELAY	(17)					
CCO Clk Delay Enable						
DCO Clk Delay						
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12. The AD6649 defaults to the fixed frequency NCO and low latency FIR filter. To place the part in this mode the SPI settings for the ADC A and ADC B tabs should be set as shown below. For this mode the following checkboxes should be checked:

KANAS MAIN(50) 'Fir Low Latency Mode En'

NCO CONTROL(51-57) 'NCO Phase Dither Enable', 'NCO Amplitude Dither Enable', 'Enable Sync NCO1 to NCO2'

The NCO frequency should be set to '40000000'

MISC EXTRA (5A) 'Low Latency NCO (Fs/4 only)'

SPIController 1.0.71.3 : USB Ezusb-0 : CS 1 : Al	06649spiR03.cfg : AD6649spiR03.cal			
File Config Help				
Global ADCBase 0 ADCA MODES(8) Int Pwt Dn Mode Power Down Standby OFFSET(10) 0 Standby Offset Ad(LSBs) 0 V	TESTID(D) Reset PN Long Gen Reset PN Shot Gen Test User Mode Continuous Output Mode I Output Test Mode Output Test Mode Off-Normal Operation I BIST Enable BIST Inddin reset MISR(24/25) MSB Performance MIN(50) Fit Low Latency Mode En Reduce Output Gain by 50% Datapath Gain OdB	DC CORRECTION CTRL(40) Freeze DC Correction En DC Correction on ADC D abapeth DC Correction Bandwidth Select 2387.32 Hz DC LEVEL(41/42) MSB LSB 00000000 00000000 Read SYNC EXTRA(59) Sync Position Sample Capture on negative edge Sync Capture	NCO CONTROL(51-57) ✓ NCO Amplitude Dither Enable ✓ NCO Amplitude Dither Enable ✓ Invert Output Spectrum ✓ Enable Sync NCO1 to NCO2 Primary NCO Freq. #4000000 E Finary NCO Freq. #000000 E Primary NCO Iffet \$00000 E Primary NCO Utext Primary NCO Iffet \$00000 E Primary NCO Utext Primary NCO Utext	SYNC CONTROL(58) NCD1 Sync En NCD1 Sync Mode Continuous Mode Rest Sync Mode FIR Sync En FIR Sync Mode Next Sync Mode NCD2 Sync Mode Continuous Mode NCD2 Sync Mode NCD2 Sync Mode NCD2 Sync Mode
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13. To place the AD6649 in the mode that uses the tunable NCO and high performance FIR filter, the SPI settings for the ADC A and ADC B tabs should be set as shown below. For this mode the following checkboxes should be checked:

NCO CONTROL(51-57) 'NCO Phase Dither Enable', 'NCO Amplitude Dither Enable', 'Enable Sync NCO1 to NCO2'

The NCO frequency should be set to '40000000'

SPIController 1.0.71.3 : USB Ezusb-0 : CS 1 : AD6649spiR03.cfg : AD6649spiR03.cal File Config Help 🔲 🖪 🔲 🔳 🔜 🔛 Global ADCBase 0 ADCA ADCB OUTPUT MODE(14) TEST IO(D) DC CORRECTION CTRL(40) NCO CONTROL(51-57) SYNC CONTROL(58) MODES(8) Int Pwr Dn Mode Freeze DC Correction En DC Correction on ADC Datapath 🔽 NCO Phase Dither Enable NC01 Sync En NC01 Sync Mode Reset PN Long Gen Disable ADC Dig. Output Normal VCO Amplitude Dither Enable Output Invert C Power Down C Standby Invert Output Spectrum
 Enable Sync NC01 to NC02 Continuous Mode DC Correction Bandwidth Select Test User Mode C Next Sync Mode Data Format 2387.32 Hz 🔻 Continuous Output Mode 💌 Primary NCO Freq. Offset Binary
 2V's Compliment Output Test Mode 40000000 E hex Gray Code Off-Normal Operation -OFFSET(10) DC LEVEL(41/42) Offset Adj(LSBs) Primary NCO Offset TEST BIST(E) MSB LSB 00000000 00000000 0 🗸 0000 Read E hex BIST Enable BIST held in reset FIR Sync En FIR Sync Mode Continuous Mode FAST DETECT CTRL(45) SYNC EXTRA(59) MISB(24/25) Force a value on Fast Detect pin
 Fast Detect Force Value
 Coarse Fast Detect En
 Fine Fast Detect Enable C Next Sync Mode Sync Position Sample 00000000 000000000 _____Read MSB LSB NCO2 Sync En NCO2 Sync Mod Capture on negative edge -Sync Edge Detect MAIN(50) Continuous Mode Sync on high level of sync pin 💌 C Next Sync Mode ED THRESHOLD/DWELL TIME(46-4C) Fir Low Latency Mode En Reduce Output Gain by 50% Bypass All Blocks and Output 9 Bit Data MISCEXTRA(5A) Raw Fast Detect Upper Threshold -NC01 Select n High Latency NC0
 Low Latency NC0(Fs/4 only) Datapath Gain FD Upper Threshold OdB -0 E hex FD Lower Threshold E hex FD Dwell Time Counter 0 E hex 2/8/2011 8:48:32 AM

MISC EXTRA (5A) 'High Latency NCO'

14. If the NCO is set to a value other than '4000000' (fs/4) then Visual Analog allows input of the Nyquist zone and NCO frequency in order to find the output signal harmonics correctly after the AD6649 frequency conversion. To enable this mode click on the 'FFT Analysis Settings' button and enable the Advanced calculations feature for the AD6649. Enter the Nyquist zone of the input signal and the NCO frequency – Visual Analog can then accurately find the signal harmonics in the FFT spectrum. (Images are noted with an 'I').

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- **15.** Click the Run button (▶) in VisualAnalog.
- **16.** Adjust the amplitude of the input signal so that the fundamental is at the desired level. (Examine the "Fund Power" reading in the left panel of the VisualAnalog FFT window.)
- 17. If desired, click on File>Save Form as in the FFT window to save the FFT plot.

Troubleshooting

- ► The FFT plot appears abnormal...
 - ✓ If you see a normal noise floor when you disconnect the signal generator from the analog input, be sure you are not overdriving the ADC. Reduce input level if necessary.
 - ✓ In VisualAnalog, Click on the Settings button in the "Input Formatter" block. Check that "Number Format" is set to the correct encoding (2's compliment by default).

► The FFT plot appears normal, but performance is poor.

- \checkmark Make sure you are using an appropriate filter on the analog input.
- ✓ Make sure the signal generators for the clock and the analog input are clean (low phase noise).
- ✓ If you are using non-coherent sampling, change the analog input frequency slightly.
- ✓ Make sure the SPI config file matches the product being evaluated.
- ► The FFT window remains blank after the Run button is clicked.
 - ✓ Make sure the evaluation board is securely connected to the HSC-ADC-EVALCZ board
 - ✓ Repeat steps 8 through 12.
 - ✓ Make sure the FPGA has been programmed by verifying that the 'D6' LED is illuminated on the HSC-ADC-EVALCZ board.
 - ✓ Make sure the correct FPGA program was installed.

► VisualAnalog indicates that the "FIFO capture timed out."

- ✓ Make sure all power and USB connections are secure.
- ✓ Repeat steps 11 through 16.
- \checkmark Double check that the encode clock source is present at connector J506.
- Revision: 0 July 26, 2010
- Revision: A December 14, 2010
- Revision: B February 8, 2011
- Revision: C October 24, 2013