

PD70101/PD70201
Datasheet
Power over Ethernet 802.3af/at PD Controller
October 2019



Contents

1	Revision History	1
1.1	Revision 3.0	1
1.2	Revision 2.0	1
1.3	Revision 1.9	1
1.4	Revision 1.8	1
1.5	Revision 1.7	1
1.6	Revision 1.6	1
1.7	Revision 1.5	1
1.8	Revision 1.4	1
1.9	Revision 1.3	1
1.10	Revision 1.2	2
1.11	Revision 1.1	2
1.12	Revision 1.0	2
2	Product Overview	3
2.1	Features	4
2.2	Applications	5
3	Functional Descriptions	7
4	Electrical Specifications	8
4.1	Absolute Maximum Ratings	8
4.2	Thermal Properties	9
4.3	Electrical Characteristics	10
5	Pin Configuration	18
6	Package Specifications	21
7	Theory of Operation	23
7.1	Detection	23
7.2	Physical Layer Classification	23
7.3	Two-Events Detection and AT Flag	23
7.4	Soft Start and Inrush Current Protection	24
7.5	Over-Current Protection	25
7.6	Power Good	25
7.7	Start-up Supply	26
7.8	PD Interface Thermal Protection	26
7.9	Bulk Capacitor Discharge	26
7.10	DC-DC Start-up	26
7.11	Current Limit and Short Circuit Protection	27

7.12	Low Power Mode Operation	27
7.13	Input (VPP and VCC) Under Voltage Lock Out	27
7.14	External Enable	28
8	Ordering Information	29

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 3.0

Revision 3.0 was published in October 2019. The following is the summary of changes in this revision.

- Microsemi logo was added to the pin out figures.
- Made formatting changes to application figures.
- Divided Electrical Characteristics table under ten different titles.

1.2 Revision 2.0

Revision 2.0 was published in January 2017. The following is the summary of changes.

- Changed MSL from 1 to 3.
- Updated formatting and disclaimer.

1.3 Revision 1.9

Revision 1.9 was published in November 2015. In this revision, the maximum value for VSW-START was added.

1.4 Revision 1.8

Revision 1.8 was published in May 2015. The following is the summary of changes in this revision.

- Updated differential amplifier and GND connection in figures 2 and 3.
- Added the differential amplifier input (VSN, VSP) to Absolute Maximum Ratings table.

1.5 Revision 1.7

Revision 1.7 was published in November 2014. The following is the summary of changes in this revision.

- Updated information continuous operation load current parameter.
- Updated Pin 3 description.

1.6 Revision 1.6

Revision 1.6 was published in March 2014. Updated differential amplifier gain in figure 2

1.7 Revision 1.5

Revision 1.5 was published in February 2014. In this revision, minor formatting corrections were made.

1.8 Revision 1.4

Revision 1.4 was published in February 2014. There were general updates in this revision.

1.9 Revision 1.3

Revision 1.3 was published in November 2013. The following are the changes in this revision.

- Updated Vcc disable.
- Added note 5 and removed A from 70101A in the package pin out details.

1.10 Revision 1.2

Revision 1.2 was published in June 2012. In this revision, Switching Frequency Accuracy specification limits and the equation in note 3 were updated.

1.11 Revision 1.1

Revision 1.1 was published in February 2012. In this revision, the document's format and address were updated.

1.12 Revision 1.0

Revision 1.0 was the production release of this document published in September 2011.

2 Product Overview

The PD70101 and PD70201 devices are integrated Powered Device (PD) interface and PWM controllers for a DC-DC converter used in IEEE802.3af and IEEE802.3at applications. The PD70101 can be used for IEEE802.3af or IEEE802.3at Type 1 applications, while the PD70201 can also be used in IEEE802.3at Type 2 applications.

A single PD70201 can be used in 4-pair applications that consume up to 47.7 W.

These devices have a number of features designed to improve efficiency and reliability:

Detection and Classification: The front-end interface includes detection and classification circuitry. The detection signature resistor is disconnected upon completion of the detection phase. The system then begins the classification phase. Classification can be configured for Classes 0 to 4 via an external resistor. The PD70201 includes a twoevents classification identification circuit which generates a flag to inform the PD application whether the Power Source Equipment (PSE) is Type 1 or Type 2.

Capacitor: A current-limited internal MOSFET switch charges the input capacitor of the DC-DC converter. This capacitor is discharged in a timely manner when the input power is removed.

Gate drivers: The PWM DC-DC controller has two built-in gate drivers designed to swing between VCC and GND. These 2 out-of-phase driver stages can be configured for synchronous rectification or active clamp.

Peak current mode control: The DC-DC converter employs peak current mode control for better line and load step response. The switching frequency can be set from 100 kHz to 500 kHz, enabling a size and efficiency trade off.

Maximum duty cycle is limited to 50% to reduce the power MOSFET switch voltage to two times the input voltage; a 150 V rated MOSFET can be used for the primary side switch. The secondary synchronous MOSFET voltage rating depends on the output voltage and can be higher or lower than the primary side MOSFET switch.

Soft-start circuit: The devices include a soft-start circuit to control the output voltage rise time (user settable) at start-up, and to limit the inrush current. An integrated startup bias circuit powers the DC-DC controller, until the device starts up by the voltage generated by the bootstrap circuit.

Low Voltage Protection Warning and Monitoring: Dual Under Voltage Lock Out (UVLO), which monitors both the PoE Port Input Voltage and VCC, ensures reliable operation during any system disturbances. The PoE port UVLO has a programmable threshold and hysteresis to enable tailoring to the desired turn-on and turn-off voltage.

An internal current sense amplifier with a Kelvin connection allows the use of an extremely low resistor to measure the current sense threshold voltage (200 mV) which optimizes efficiency.

Low Power Mode operation is provided to improve efficiency under light loads such as when the PD is in standby. The user can define at what power level the unit enters low power mode by means of a single resistor value.

2.1 Features

The PD70101/PD70201 device has the following key features.

- IEEE802.3af and IEEE802.3at compliant
- Support for 4-pair applications of up to 47.7 W with a single IC
- Two-events classification identification with a level signal indicating Type 1 or Type 2 PSE
- Less than 10 μ A (typical) offset current during detection
- Signature resistor is disconnected upon detection
- Programmable classification setting with a single resistor
- Integrated 0.6 Ω isolating MOSFET switch with inrush current limit
- Power off DC-DC input capacitor discharge
- 100 kHz to 500 kHz adjustable DC-DC switching frequency
- DC-DC frequency can be synchronized to external clock
- Supports low power mode operation for higher efficiency 50% maximum duty cycle
- Soft-start circuit to control the output voltage rise time
- Two out-of-phase driver stages for efficient synchronous rectification or active clamp
- PoE port input UVLO with programmable threshold and hysteresis
- Internal differential amplifier simplifying non-isolated step down converter
- Over load and short circuit protection

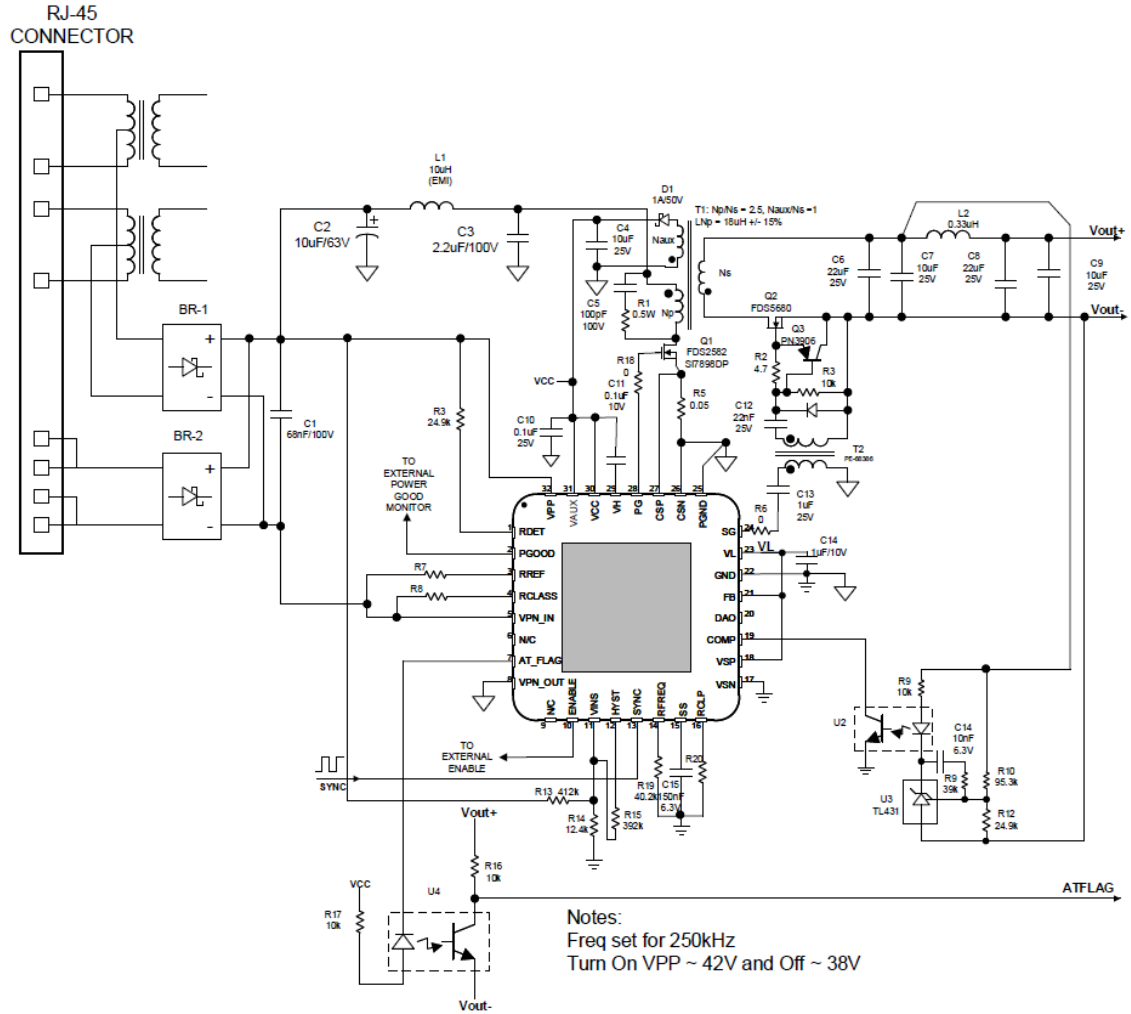
2.2 Applications

The following are the applications of the PD70101/PD70201 device.

- IEEE802.3at and IEEE802.3af powered devices such as IP phones, WLAN access points, and network cameras.
- 48 V input telcom/networks hot swappable power supply.

The following figures illustrate the typical applications of the PD70101/PD70201 device.

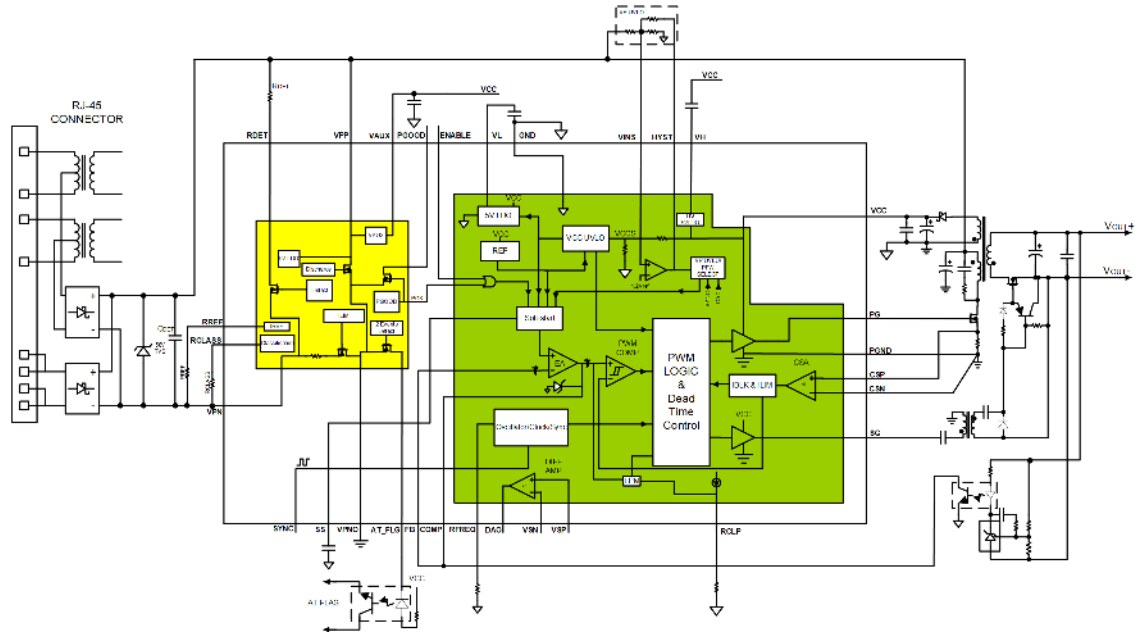
Figure 1 • 12 V, 2 A Output Isolated Flyback with Secondary Synchronous Rectification



3 Functional Descriptions

The following figure shows the functional block diagram of PD70101/PD70201 device.

Figure 3 • Functional Block Diagram



4 Electrical Specifications

The following section describes the electrical specifications of the PD70101/PD70201 device.

4.1 Absolute Maximum Ratings

The following table lists the absolute maximum ratings of the PD70101/PD70201 device.

Table 1 • Absolute Maximum Ratings

Parameter	Value	Units
VPP, RDET, VPN_OUT (with respect to VPN_IN)	-0.3 to 74	V _{DC}
RREF, RCLASS (with respect to VPN_IN)	-0.3 to 6	V
PGOOD, AT_FLAG, VAUX (with respect to VPN_OUT)	-0.3 to 74	W
VCC (with respect to PGND)	-0.3 to 40	V _{DC}
PG, SG (with respect to PGND)	-0.3 to 20	V _{DC}
VL, VSN, VSP (with respect to PGND)	-0.3 to 6	V
VH (with respect to VCC)	-0.3 to VCC - 6	V _{DC}
All Other Pins (with respect to GND)	-0.3 to VL +0.3	V _{DC}
ESD (HBM) Protection at all I/O pins*	±1	kV
Maximum Junction Temperature (T _{JMAX})	150	°C
Operational Ambient Temperature	-40 to 85	°C
Storage Temperature Range	-65 to 150	°C
Peak Package Solder Reflow Temperature (40 seconds maximum exposure), MSL3	260	°C

Exceeding these ratings could cause damage to the device. All voltages are with respect to VPN_IN. Currents are positive into, negative out of specified terminal. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions are not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

Note: *All pins except pin 2 (PGOOD) and pin 31 (VAUX). Pin 2 and 31 ESD Protection is ±150 V HBM.

4.2 Thermal Properties

The following table lists the thermal specifications of the PD70101/PD70201 device.

Table 2 • Thermal Properties

Symbol	Thermal Resistance	Min	Typ	Max	Units
θ_{JC}	Junction to case		5		°C/W
θ_{JP}	Junction to pad		4		°C/W
θ_{JA}	Junction to ambient		23		°C/W

Note: The θ_{Jx} numbers assume no forced airflow. Junction temperature is calculated using $T_J = T_A + (P_D \times \theta_{JA})$. In particular, θ_{JA} is a function of the PCB construction. The stated number above is for a four-layer board in accordance with JESD-51 (JEDEC) with thermal vias.

4.3 Electrical Characteristics

This section describes the electrical characteristics of the PD70101/PD70201 device.

The following specifications apply over the operating ambient temperature of $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ (except where otherwise noted with $V_{PP} = 48\text{ V}$; $V_{EN} = \text{HIGH}$, $f_s = 250\text{ kHz}$). Production tests were performed at $25\text{ }^{\circ}\text{C}$. Unless otherwise specified, V_{PP} is with respect to VPN_IN and VCC is with respect to $PGND$.

Table 3 • PD Interface

Symbol	Parameter	Test Conditions/Comment	Min	Typ	Max	Units
Power Supply						
V_{PP}	Input voltage		0	55	57	V
Detection Mode						
DET_{RANGE}	Detection voltage range	Measured between V_{PP} and VPN_{IN}	1.3		10.1	V
R_{DET-ON}	Detection switch ON resistance	$2.5\text{ V} \leq (\Delta V_{PP} \text{ to } VPN_{IN}) \leq 10.1\text{ V}$ Measured between R_{DET} and VPN_{IN}			50	Ω
$R_{DET-OFF}$	Detection is disconnected	Measured between V_{PP} and VPN_{IN}	10.1		12.8	V
$R_{DET-OFF}$	Detection switch OFF resistance	$12.8\text{ V} \leq (\Delta V_{PP} \text{ to } VPN_{IN}) \leq 57.0\text{ V}$ Measured between R_{DET} and VPN_{IN}	2.0			$M\Omega$
I_{OFFSET}	Input offset current	$2.5\text{ V} \leq V_{PP} \leq 10.1\text{ V}$ $-40\text{ }^{\circ}\text{C} \leq T_J \leq 85\text{ }^{\circ}\text{C}$			16	μA
I_{OFFSET}		$2.5\text{ V} \leq V_{PP} \leq 10.1\text{ V}$ $-40\text{ }^{\circ}\text{C} \leq T_J \leq 55\text{ }^{\circ}\text{C}$			10	μA
$V_{RDET-ON}$	RDET reconnection level	Measured between V_{PP} and VPN_{IN}	1.95	3.0	4.85	V
Classification Mode						
$V_{TH-LOW-ON}$	Classification current source, turn ON threshold range measured at V_{PP}	Turn on for any I_{CLASS} while V_{PP} increases	11.4		13.7	V
V_{HST}	Classification disconnection minimum hysteresis voltage	Hysteresis between $V_{TH-low-on}$ and $V_{TH-low-off}$		1		V
$V_{TH-HIGH-OFF}$	Classification current source, turn OFF threshold range measured at V_{PP}	Turn off while V_{PP} increases	20.9		23.9	V
$I_{CLASS-LIM}$	Current limit threshold		50	68	80	mA
$I_{CLASS-DIS}$	Input current IPP when classification function is disabled	Class 0 $R_{CLASS} = \text{Open}$			3.0	mA
$I_{CLASS-EN}$	Input current IPP when classification function is enabled	Class 1 $R_{CLASS} = 133\ \Omega \pm 1\%$	9.5	10.5	11.5	mA
		Class 2 $R_{CLASS} = 69.8\ \Omega \pm 1\%$	17.5	18.5	19.5	mA
		Class 3 $R_{CLASS} = 45.3\ \Omega \pm 1\%$	26.5	28.0	29.5	mA
		Class 4 $R_{CLASS} = 30.9\ \Omega \pm 1\%$	38.0	40.0	42.0	mA

Symbol	Parameter	Test Conditions/Comment	Min	Typ	Max	Units
	RCLASS Voltage		1.142		1.278	V
Mark						
V _{MARK}	Mark, working range	VPP failing edge	4.9		10.1	V
I _{MARK}	Mark current		0.25		4	mA

Table 4 • Isolation Switch

Symbol	Parameter	Test Conditions/Comment	Min	Typ	Max	Units
V _{SW-START}	Isolation Switch MOSFET switches from off to I _{LIM-LOW}		36		42	V
V _{SW-OFF}	Isolation Switch MOSFET switched off		30.5		34.5	V
I _{LIM-LOW}	Startup current limit, I _{LIM-LOW}		130	240	330	mA
V _{DIFF}	VPN_IN to VPN_OUT Threshold voltage for I _{LIM-LOW} to I _{LIM-HIGH} switchover	When VPNIN to VPNOOUT ≤ V _{DIFF} , Isolating switch switches over from I _{LIM-LOW} to I _{LIM-HIGH}			0.7	V
OCP	Over current protection limit current		1500	1800	2000	mA
I _{LOAD}	Continuous operation load	Isolating switch at I _{LIM-HIGH} PD70101			450	mA
		PD70201			1123	
SW-RD _{SON}	Isolated Switch On resistance at I _{LIM-HIGH}	Total resistance between VPNIN and VPNOOUT Isolating switch at I _{LIM-HIGH}			0.6	Ω

Table 5 • DC/DC Capacitor Discharger

Symbol	Parameter	Test Conditions/Comment	Min	Typ	Max	Units
C _{IN}	DC/DC input capacitance	For reference only Guaranteed by design (not tested in production)		220	264	μF
	Discharge current	7.0 V ≤ V _{PP} to V _{PNOUT} ≤ 30 V	22.8	32	50	mA
AT_FLAG						
	Output low voltage	I _{OL} = 0.75 mA			0.4	V
		I _{OL} = 5 mA			2.5	V
	Leakage current	V _{AT_FLAG} = 57 V			1.7	μA
PGOOD						
	Output low voltage	I _{OL} = 0.75 mA			0.4	V
		I _{OL MAX} = 5 mA			2.5	V
	Leakage current	V _{PGOOD} = 57 V			1.7	μA
PD Interface Thermal Shutdown						
	Thermal Shutdown Temperature ¹		180	200	220	°C
VAUX (respect to VPN_OUT)						
VAUX-OFF	VAUX output voltage off (leakage current)	PGOOD = High impedance Load = 1 MΩ			1	V
VAUX-ON	VAUX output voltage on	Isolating switch at I _{LIM-HIGH} and PGOOD = Low	9.8	10.5	11.8	V
I _{VAUXP}	Output current peak	Capacitor = 30 μF When T _{LOAD} ≤ 5 mS Isolating switch at I _{LIM-HIGH} and PGOOD = Low	0		10	mA
I _{VAUXC}	Output continuous current	When T _{LOAD} ≤ 10 mS Isolating switch at I _{LIM-HIGH} and PGOOD = Low	0		2	mA
I _{VAUX}	VAUX output current limit	Isolating switch at I _{LIM-HIGH} and PGOOD = Low	10		32	mA

Table 6 • DC/DC Controller

Symbol	Parameter	Test Conditions/Comment	Min	Typ	Max	Units
VCC						
VCC	Maximum Input Operating Voltage				20	V
IVCC	Input Current	VCC < VCC_UVLO or ENABLE = Low. See Note 5		250	2000	μA
		V _{ENABLE} and V _{INS} = High; V _{VCC} < VCC_UVLO_UP; -40 °C ≤ Temp ≤ +55 °C. See Note 5			4.5	mA
		VCC > VCC_UVLO and ENABLE = High, No Load on PG, SG, VL, and FSW = 500 kHz.			3	mA
VCC_UVLO	VCC UVLO Rising Threshold	VCC raising edge	8.85	9.15	9.5	V
VCC_UVLO	VCC UVLO Falling Threshold	VCC falling edge	7	7.3	7.6	V
POE Port Input UVLO						
VINS	UVLO Threshold		1.171	1.200	1.229	V
	VINS Input Current		-0.1		0.1	μA
HYST-V _{OH}	HYST Output High Voltage	I _{SOURCE} = 1 mA	2.8			V
HYST-V _{OL}	HYST Output Low Voltage	I _{SINK} = 3 mA			0.4	V
Internal LDO's						
VL	5 V LDO	I _L < 5 mA	4.75	5	5.25	V
VH	-5 V LDO	Reference to VCC		-5		V
Soft-Start						
I _{SS_CHG}	Soft-start charging current ²	R _{FFREQ} = 33.2 kΩ; V _{SOFTSTART} = 0.5 V	32	36	40	μA
I _{SS_DIS}	Soft-start discharging current	V _{SOFTSTART} = 0.5 V; % of I _{SS_CHG}		10		%
V _{SS_CH}	Soft-start completion threshold ¹	% of 1.2 V	90		95	%
V _{SS_DISCH}	Soft-start discharge completion threshold ¹			50		mV
R _{SS_DISCH}	Soft-start discharge FET on resistance			50		Ω
t _{DISCH}	Soft-start discharge FET on time ¹	1 cyc = 1/F _{FFREQ}		32		cyc
Switching Frequency and Synchronization						
F _{FFREQ}	Switching frequency range		100		500	kHz
F _{FFREQ}	Switching frequency accuracy ³	R _{FFREQ} = 33.2k	285	315	345	kHz
F _{SYNC}	Synchronization frequency range	F _{SYNC} > 2x F _{FFREQ}	200		1000	kHz
V _{SYNC-HIGH}	Synchronization voltage high threshold		2.4		5	V

Symbol	Parameter	Test Conditions/Comment	Min	Typ	Max	Units
V _{SYNC-LOW}	Synchronization voltage low threshold				0.8	V
PW _{SYNC_MIN}	Synchronization minimum pulse width		100			ns
PW _{SYNC_MAX}	Synchronization maximum PWM duty				90	%
I _{SYNC}	Synchronization input current		-1.3		1.3	μA

Table 7 • Error Amplifier

Symbol	Parameter	Test Conditions/Comment	Min	Typ	Max	Units
Gain _{DC_OPL}	DC Open Loop Gain ¹	R _{LOAD} = 100k	70	100		dB
AV _{UGBW}	Unity Gain Bandwidth ¹	C _{LOAD} = 10 pF	2	5		MHz
I _{COMP_OUT}	Output Sourcing Current	0.2 V ≤ V _{COMP} ≤ 1.3 V	110		620	μA
I _{COMP_IN}	Output Sink Current	0.2 V ≤ V _{COMP} ≤ 1.3 V	145		495	μA
V _{EA_CMR}	Input Common Mode Range		0		2	V
V _{FB}	Feedback Voltage	COMP shorted to FB	1.171	1.200	1.229	V
I _{FB}	FB Pin Input Current		-50		50	nA
V _{COMP}	Output Clamp Voltage		1.8	2.1	2.6	V

Table 8 • PWM Comparator

Symbol	Parameter	Test Conditions/Comment	Min	Typ	Max	Units
V _{RCLP}	RCLP Voltage Range		0		1	V
Low Power Mode (Skip Pulse Mode)						
	Low Power Skip Mode Threshold ^{1,4}	V _{COMP} Rising (% of V _{RCLP})		95		%
		V _{COMP} Falling (% of V _{RCLP})		90		%

Table 9 • Current Sense Amplifier and Current Limit

Symbol	Parameter	Test Conditions/Comment	Min	Typ	Max	Units
Gain _{CSA}	Gain	Measure at DC	4.75	5.0	5.25	V/V
V _{CSA_CMR}	Input Common Mode Range		0		2.0	V
	Output Rise/Fall time ¹	10% to 90%			75	ns
t _{BLANK}	Blanking Time ¹		50		100	ns
V _{LIM_TH}	Current Limit Threshold		1.1	1.2	1.3	V
V _{IMAX_TH}	Current Maximum Threshold		1.7	1.8	1.9	V

Table 10 • Differential Amplifier

Symbol	Parameter	Test Conditions/Comment	Min	Typ	Max	Units
Gain _{DA}	Gain	Measured at DC	6.86	7.0	7.14	V/V
A _V	Unity Gain			5		MHz
UGBW _{DA}	Bandwidth ¹					
V _{DA_CMR}	Common Mode Range		0		3.5	V
	Input Offset Voltage		-7		7	mV
	Input Bias Current		-1		1	μA

Table 11 • Output Drivers

Symbol	Parameter	Test Conditions/Comment	Min	Typ	Max	Units
PG R _{ds}	Primary Gate (PG)			10		Ω
ONH	High On Resistance					
PG R _{ds}	Primary Gate (PG)			5		Ω
ONL	Low On Resistance					
SG R _{ds}	Secondary Gate			10		Ω
ONH	(SG) High On Resistance					
SG R _{ds}	Secondary Gate			10		Ω
ONL	(SG) Low On Resistance					
T _{DEAD}	Dead Time – PG low to SG high or SG low to PG high	C _{LOAD} On PG and SG = 1000 pF		110		ns
	PG Minimum On Time				120	ns
	PG Maximum Duty Cycle		44.5		50	%

Table 12 • Logic (ENABLE Pin)

Symbol	Parameter	Test Conditions/Comment	Min	Typ	Max	Units
V _{HI}	Logic High Threshold		2.0			V
V _{LO}	Logic Low Threshold				0.8	V
	Input Current		-1		1	μA

Table 13 • PWM Controller Thermal Shutdown

Symbol	Parameter	Test Conditions/Comment	Min	Typ	Max	Units
T _{SD}	Thermal Shutdown Threshold ¹			157		°C
V _{LO}	Threshold Hysteresis ¹			15	30	°C

Notes:

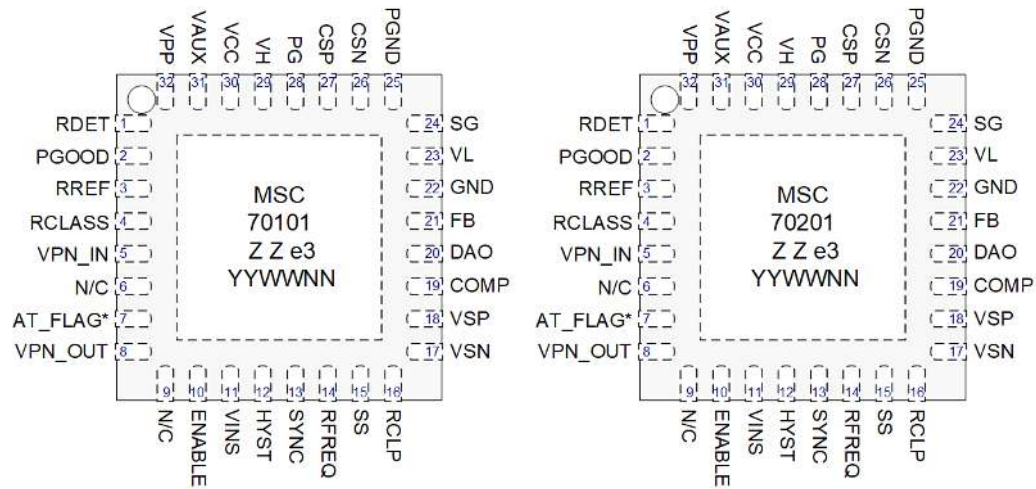
1. Guaranteed by design
2. Soft start charge current equation: $I_{ss_chg} = 1.2 V/R_{FREQ}$

$$Freq = \frac{1}{(90pF \times R_{FREQ}) + 150ns}$$

3. Switching frequency equation: where Freq is [Hz]
4. Low power mode clamp equation: $V_{CLAMP} = 0.3 * (R_{RCLP}/R_{FREQ})$
5. Minimum and maximum current are guaranteed by design.

5 Pin Configuration

The following illustration shows the device pin diagram from the top views.



ZZ = Random character with no meaning and e3 = 2nd level interconnect.

YY = Year, WW = Week, NNN = Trace Code

The following table lists the pin descriptions of the PD70101/PD70201 device.

Table 14 • Pin Descriptions

Pin Number	PD70101 Pin Name	PD70201 Pin Name	Description
1	RDET	RDET	Valid Detection Resistor: Connect a 24.9 kΩ, 1% resistor from this pin to VPP.
2	PGOOD	PGOOD	Open Drain Output (active low): This flag is generated to indicate the power rails (VPN_OUT) are ready.
3	RREF	RREF	Bias current resistor for the PD Interface. Connect a 240k 1% resistor between this pin and VPN_IN.
4	RCLASS	RCLASS	Power Classification Setting: Connect external class resistor between this pin and VPN_IN.
5	VPN_IN	VPN_IN	VPort Negative Input: Connected to the isolating switch input N-channel MOSFET source.
6	N/C	N/C	Not Used.
7	N/C	AT_FLAG	Open Drain Output (active low): This flag indicates if the chip detects an IEEE 802.3at compliant PSE.
8	VPN_OUT	VPN_OUT	VPort Negative Output: Connected to the isolating switch output. N-channel MOSFET Drain.
9	N/C	N/C	Not Used.
10	ENABLE	ENABLE	

Pin Number	PD70101 Pin Name	PD70201 Pin Name	Description
			Logic level Enable input for DC-DC controller. Pulling this pin to VL turns on the DC-DC controller. This allows the DC-DC controller to be turned on without power to the PD interface.
11	VINS	VINS	VPP input voltage sensing for UVLO comparator. Connect to an external resistor divider from VPP to GND. Threshold is 1.2 V reference.
12	HYST	HYST	Output of the VINS/UVLO comparator. This pin is used for VPP UVLO hysteresis programming.
13	SYNC	SYNC	External Clock synchronization for the DC-DC controller. Connect an external clock as defined in the EC table to this pin to synchronize the DC-DC converter switching frequency to this clock. PG rising edge is synchronized with the clock rising edge.
14	RFREQ	RFREQ	DC-DC Switching Frequency Setting. Connect a resistor from this pin to GND to set the switching frequency.
15	SS	SS	Soft-start: Connect a capacitor from this pin to GND to set the soft-start time of the DC-DC converter. This capacitor is charged with an internal current source to 1.2 V.
16	RCLP	RCLP	Low Power Mode Clamp. Connect a resistor from this pin to GND to program the LPM clamping voltage or connect this pin to GND to disable LPM.
17	VSN	VSN	Differential Amplifier's negative input. Connect this to the junction of a resistor divider from Vo- to GND for the Direct Buck converter application.
18	VSP	VSP	Differential Amplifier's positive input. Connect this to the junction of a resistor divider from Vo+ to GND for the Direct Buck converter application.
19	COMP	COMP	Error Amplifier Output. Short to FB pin when driven directly with an optoisolator for Isolated DC-DC Converter. Connect to FB via RC compensation networks for Non-Isolated Direct Buck Converter.
20	DAO	DAO	Differential Amplifier Output. Connect to FB (externally) for Non-Isolated Direct Buck Converter.
21	FB	FB	Inverting Input of the Error Amplifier. Connect to opto-coupler for Isolated DC-DC. Connect to RC compensation networks for Non-isolated DC-DC
22	GND	GND	This is Analog GND. Connect to a local AGND plane. Soft-start capacitor and the frequency setting resistor return to this local GND plane.
23	VL	VL	5 V (GND reference) internal LDO Output. Connect a 1 μ F or higher ceramic cap from VL to GND.
24	SG	SG	Secondary Gate Driver. Output is the compliment of PG output. Leave open (NC) if not used. SG is low when in Low Power Skip Mode.
25	PGND	PGND	

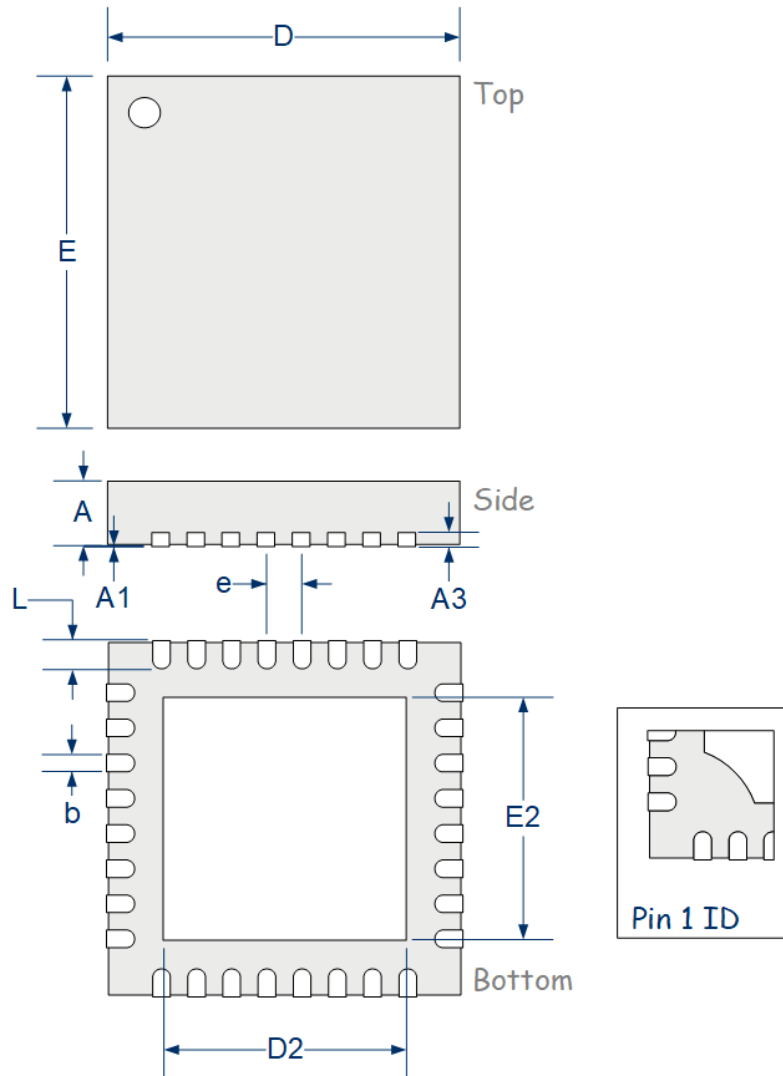
Pin Number	PD70101 Pin Name	PD70201 Pin Name	Description
			This is the Power Ground. Connect to a local PGND plane. Input, VCC decoupling capacitors, PG and SG drivers. Primary current sense resistor return to this PGND.
26	CSN	CSN	Negative Input of the Current Sense Amplifier. Kelvin connect to the PGND side of the primary current sense resistor.
27	CSP	CSP	Positive Input of the Current Sense Amplifier. Kelvin connect to the Non-PGND side of the primary current sense resistor.
28	PG	PG	Primary Gate Driver. Connect to the gate of the primary side Power MOSFET, directly or via a resistor.
29	VH	VH	5V High side (VCC reference) internal LDO Output. Connect a 0.1 μ F or higher ceramic cap from VH to VCC.
30	VCC	VCC	Input Supply to the DC-DC Controller. Connect a 4.7 μ F or higher ceramic capacitor from this pin to PGND. Alternately an parallel combination of 1 μ F ceramic and an greater than 10 μ F electrolytic capacitor can be used.
31	VAUX	VAUX	Auxiliary voltage reference to VPN_OUT; this voltage can be used for DC-DC startup when operated with a bootstrapped voltage source. For applications with POE power only connect directly to VCC; for applications using multiple power sources (such as a wall adaptor), connect to VCC pin through a small, low current, 30 V rated schottky diode.
32	VPP	VPP	This is the positive terminal of the POE input port. Connect to the positive terminal of the input bridges at the CDET positive side.
EP	Exposed Pad	Exposed Pad	Thermal Pad; electrically connected to VPN_IN. For proper thermal management should be tied to a large copper fill or plane that is electrically connected to VPN_IN.

6 Package Specifications

The following section describes the package information of the PD70101/PD70201 device.

The PD70101/PD70201 package is halogen free and meets RoHS2 and REACH standards.

Figure 4 • Package Outline Diagram



Dimensions do not include protrusions; these shall not exceed 0.155 mm (0.006") on any side. Lead dimension shall not include solder coverage. Dimensions are in millimeters. Inches are for reference only.

The following table lists the dimensions for the PD70101/PD70201 package.

Table 15 • Package Dimensions

Dimension	Millimeters		Inches	
	Min	Max	Min	Max
A	0.80	1.00	0.031	0.039
A1	0	0.05	0	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	5.00 BSC		0.197 BSC	
D2	3.30	3.60	0.130	0.142
E	5.00 BSC		0.197 BSC	
E2	3.30	3.60	0.130	0.142
e	0.50 BSC		0.02 BSC	
L	0.30	0.50	0.012	0.020

7 Theory of Operation

The PD70101/PD70201 device theory of operation is described in the following sections.

The PD70101/PD70201 IC integrates IEEE 802.3af/at compliant PD front-end functions including Detection, Physical Layer Classification, Two-events Classification (PD70201 only), Power Good, Soft Start Current Limiting, Over-Current Protection, and Bulk Capacitor Discharge with a PWM controller. The integrated PWM controller function provides a PWM controller solution with a minimum requirement of external components.

7.1 Detection

IEEE 802.3af/at-compliant detection is provided by means of a 24.9 k Ω resistor connected between VPP and RDET pin. RDET pin is connected to VPN_IN via an open drain MOSFET with a maximum specified R_{DS(on)} of 50 Ω . Internal logic monitors VPP to VPN_IN and connects the RDET pin to VPN_IN when the rising VPP to VPN_IN voltage is between 1.1 V and 10.1 V. When rising VPP to VPN_IN voltages exceed 10.1 V, the MOSFET is switched off. Once above 10.1 V, falling VPP to VPN_IN voltage between 2.45 V and 4.85 V will reconnect RDET pin to VPN_IN.

7.2 Physical Layer Classification

Physical Layer (hardware) Classification per IEEE 802.3af/at is generated via a regulated reference voltage of 1.2 V, switched onto the RCLASS pin. Internal logic monitors the VPP to VPN_IN voltage and connects the 1.2 V reference to RCLASS pin at a rising VPP to VPN_IN voltage threshold between 11.4 V and 13.7 V. Once VPP to VPN_IN has exceeded the rising threshold, there is a 1 V typical hysteresis between the VPP rising (turn-on) threshold and the VPP falling (turn-off) threshold.

The 1.2 V reference stays connected to the RCLASS pin until the VPP to VPN_IN rising voltage exceeds the upper turn-off threshold of 20.9 V to 23.9 V. The 1.2 V reference voltage is disconnected from the RCLASS pin at VPP to VPN_IN voltages above the upper threshold.

Classification current signature is provided via a resistor connected between RCLASS pin and VPN_IN. The classification current is therefore the current drawn by the PD70101/PD70201 IC during the classification phase, and is simply the 1.2 V reference voltage divided by the RCLASS resistor value. The maximum current available at the RCLASS pin is current limited to 68 mA (typical).

7.3 Two-Events Detection and AT Flag

The PD70201 IC provides IEEE 802.3at Type 2 compliant detection of the two events classification signature, and generation of the AT flag. This feature is available on the PD70201 IC only.

The two events classification signature is a means by which an IEEE 802.3at Type 2 Power Source can inform a compliant PD that it is AT Type 2 compliant, and as such is capable of providing AT Type 2 power levels.

The Power Source communicates the Type 2-compliant signature by toggling the VPP to VPN_IN voltage twice (2 events) during the Physical Layer Classification phase. The VPP to VPN_IN voltage is toggled

from the Physical Layer Classification's voltage level (13.5 V to 20.9 V) down to a voltage Mark level. Voltage Mark level is specified as a VPP to VPN_IN voltage of 4.9 V to 10.1 V.

PD70201 IC recognizes a VPP to VPN_IN falling edge from Classification level to Mark level as being one event of the Two-Events Signature. If two such falling edges are detected, PD70201 will assert AT flag by means of an open drain MOSFET connected between AT_FLAG pin and VPN_OUT.

AT_FLAG pin is active low; a low impedance state between AT_FLAG and VPN_OUT indicates a valid Two-Events Classification Signature was received, and the Power Source is AT Type 2 compliant.

AT_FLAG MOSFET is capable of 5 mA of current and can be pulled up to VPP.

7.4 Soft Start and Inrush Current Protection

PD70101/PD70201 IC contains an internal isolation switch that provides ground isolation between power source and PD application during Detection and Classification phases. The isolation switch is a N-channel MOSFET, wired in a common source configuration where the MOSFET's Source is connected to Power Source ground at VPN_IN, and the MOSFET's Drain is connected to application's primary ground at VPN_OUT.

Internal logic monitors VPP to VPN_IN voltage and keeps the MOSFET in a high impedance state until VPP to VPN_IN voltage reaches turn-on threshold of 36 V to 42 V. Once VPP to VPN_IN voltage exceeds this threshold, the MOSFET is switched into one of two modes.

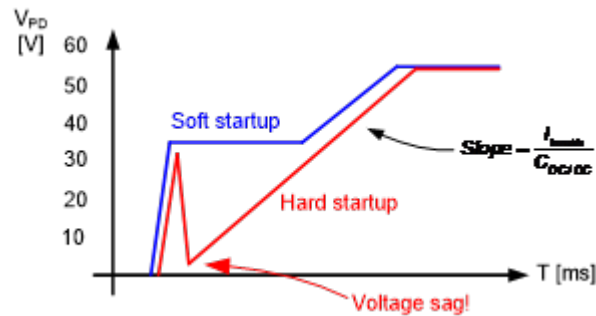
Mode into which the MOSFET is switched is determined by the voltage developed across the MOSFET, or put another way, the VPN_OUT to VPN_IN differential voltage. Two modes are defined below:

Table 16 • Isolation Switch Modes

VPN_OUT to VPN_IN	Mode	Description
≥ 0.7 V	Soft start	Limits VPN_OUT current to 240 mA (typical)
≤ 0.7 V	Normal operating	Limits VPN_OUT current to 1.8 A (typical)

By controlling the MOSFET current based on VPN_OUT to VPN_IN voltage, inrush currents generated by fully discharged bulk capacitors can be limited. This method limits current to a maximum of 350 mA, compliant with IEEE 802.3af/at specification.

Soft Start current limiting is required to reduce occurrences of voltage sag at the PD input during device power-up. A comparison is shown in [figure 3 \(see page 7\)](#).

Figure 5 • Comparison of Input Voltages without Soft-start (Hard Startup) and Soft-start (Soft Startup)


Once bulk capacitance has charged up to a point where V_{PN_OUT} to V_{PN_IN} differential voltage is less than 0.7 V, the isolation MOSFET is switched into normal operating mode with MOSFET current limit set at 1.8 A (typical), to provide overcurrent protection.

PD70101 and PD70201 ICs are different in their respective isolation MOSFET's continuous current handling capability. The maximum isolation MOSFET's continuous current handling capability is 450 mA for PD70101 and 1123 mA for PD70201.

An adequate heatsink for the PD70101/PD70201 IC's exposed pad must be provided to achieve these current levels without damaging the IC. A large, heavy copper fill area and/or a heavy ground plane with Thermal Vias are recommended.

Internal logic monitoring V_{PP} to V_{PN_IN} will place the isolation switch MOSFET in a high impedance state if voltage between V_{PP} and V_{PN_IN} drops below 31 V to 34 V.

7.5 Over-Current Protection

An over-current protection is provided on the PD70101/PD70201 IC using the Isolation Switch MOSFET, which limits the V_{PN_OUT} current to 1.8 A during normal operation. See previous description of Soft Start.

7.6 Power Good

During Soft Start mode, the PD70101/PD70201 IC monitors V_{PN_OUT} to V_{PN_IN} differential voltage. When this voltage is less than 0.7 V (maximum), the IC enters normal operation mode and the isolation switch current limit is increased to 1.8 A (typical). At this same 0.7 V (maximum) threshold the Power Good signal is asserted by means of an open drain MOSFET between PGOOD and V_{PN_OUT} .

PGOOD pin is active low; a low impedance state between PGOOD and V_{PN_OUT} indicates the Soft Start mode has finished and the isolation switch has transitioned into normal operating mode.

PGOOD MOSFET can handle current of 5 mA and can be pulled up to V_{PP} .

The application load should begin after no less than 80 ms after PGOOD is activated.

7.7 Start-up Supply

PD70101/PD70201 IC provides a 10.5 V (typical) regulated output used as a start-up supply for the integrated DC/DC controller when VCC is provided via a bootstrap winding. This regulated supply is available at VAUX pin, and is referenced to VPN_OUT pin. The VAUX start-up supply is current-limited at 10 mA (minimum).

For stability, the start-up regulator requires a minimum of 4.7 μ F ceramic capacitor connected directly between VAUX and PGND pins (most applications will connect PGND to VPN_OUT).

For applications where power to the DC-DC controller is provided by POE only, the VAUX pin is connected directly to VCC. For applications which have alternate power sources (such as a wall adaptor), the VAUX pin output is connected to the VCC pin through a series diode. This diode is typically a low current diode with a 30 V rating.

7.8 PD Interface Thermal Protection

Both PD70101 and PD70201 IC contain temperature sensors which individually monitor both the isolation MOSFET and the classification current source for over temperature conditions. In case of an over temperature condition, the sensor will activate protection circuitry which will disconnect its respective monitored function.

7.9 Bulk Capacitor Discharge

The bulk capacitor discharge circuitry eliminates the need to place a diode in series with the VPP line to prevent an application's bulk capacitance from discharging through the detection resistor and the isolation switch MOSFET's body diode. Discharge current through the detection resistor can cause failure of the detection signature in cases where a PD is connected and the bulk capacitance is not fully discharged.

During normal operation, PD70101/PD70201 IC continuously monitors voltage at VPP to VPN_IN. Should VPP to VPN_IN voltage fall below isolation switch turn-off threshold (31 V to 34 V), isolation switch MOSFET is immediately placed in a high-impedance state. At this point the internal logic monitors the voltage at VPP to VPN_OUT.

If VPP to VPN_OUT voltage is between 1.5 V to 32 V, minimum 23 mA constant current source is connected across the VPP and VPN_OUT pins. This constant current source provides bulk capacitor discharge.

A 220 μ F bulk capacitance can be discharged from 32 V to 1.5 V in a maximum period of 292 ms.

7.10 DC-DC Start-up

The DC-DC controller starts up when it receives the PGOOD high signal from the front-end, or ENABLE goes high provided that VCC UVLO have passed. When the PGOOD signal or ENABLE goes high, the start-up sequence begins with ramping up the SS pin from GND to 1.2 V. For isolated applications the output voltage may reach the maximum level before the SS reaches 1.2 V, depending on the output loading condition. In applications with lighter loads, the output reaches regulation level sooner than in heavy loads, as in this mode the SS voltage directly controls the peak inductor current; hence the energy is

delivered to the load. The external secondary error amplifier regulates the output voltage and controls the peak inductor current via the opto-coupler across the isolation barrier. For non-isolated applications, because the internal error amplifier is used to close the regulation loop, the output reaches the regulation level when SS reaches 1.2 V.

An additional internal offset is added to the FB to ensure that COMP does not reach its upper limit because of amplifier input offset. This offset is removed (slowly to avoid overshoot) when the SS ramp is complete.

Low Power mode is not supported during SS ramp as it is not necessary.

7.11 Current Limit and Short Circuit Protection

The DC-DC converter is a peak current mode controller; an internal current sense amplifier with a gain of 5 monitors the voltage across an external current sense resistor and regulates the output based on the current through the resistor. If the output of the internal current sense amplifier reaches 1.2 V, the converter will truncated the PWM output, and thus limit the output current.

If the output of the internal current sense amplifier reaches 1.8 V, the controller enters hiccup mode by discharging the SS capacitor with a constant current that equals 10% of the charging current during ramp up.

This discharge continues until $V_{SS} = 50$ mV where an internal $\sim 50 \Omega$ MOSFET connected to SS turns on for 25 clock cycles to ensure the SS capacitor fully discharges to GND before ramping back up and restart. The converter will exit the hiccup mode when the over current condition is removed.

7.12 Low Power Mode Operation

The devices offer a pulse skipping operation for light load condition, referred to as Low Power Mode (LPM), to improve the efficiency of light load operation by reducing the power dissipation especially in high frequency switching. Using an external resistor from RCLP pin to GND, the user can program the output power when the unit enters pulse skipping.

Pulse skipping mode is disabled until SS ramp is completed, regardless of the LPM status.

7.13 Input (VPP and VCC) Under Voltage Lock Out

The PD interface circuit offers an internal PGOOD signal that can be used to start the DC-DC converter; however, the threshold of the PGOOD is fixed at $VPN_OUT - VPN_IN \leq 0.7$ V. This may not fit all possible applications. Therefore, the device offers an option to have a programmable UVLO which is tied to level of $VPP - VPN_OUT$, plus a programmable hysteresis. The voltage developed across a simple resistor divider is sensed at VINS, and will enable/disable the PWM controller at a nominal 1.2 V threshold. A third resistor connected between VINS and HYST pins allows programmable hysteresis. This feature enables the end user to tailor to any desired systems application's requirement for turn on and turn off time. In addition to the VPP sensing for UVLO, the devices also have VCC UVLO to ensure that the PWM controller is always properly powered during operation. These features provide robust solutions under various systems disturbances.

7.14 External Enable

The PD interface circuit provides an internal PGOOD signal that is used to enable the DC-DC converter when powered by the PoE input; however, for applications that require input power from a wall adaptor, the internal PGOOD signal is not functional. For these applications an external enable input is provided, allowing a non-PoE power source (such as a wall adaptor) the ability to start the DC-DC converter. The Enable pin is active high, and is driven by a 5 V maximum signal referenced to GND. When the DC-DC converter is powered by the PD interface (PoE power), the Enable pin will not disable the controller. It may be tied to ground or left floating when not used.

8 Ordering Information

The following table lists the ordering information of the PD70101/PD70201 device.

Table 17 • Ordering Information

Ambient Temperature	Type	Package	Part Number	Packaging Type
-40 °C to 85 °C	RoHS compliant, Pb-free, Matte Tin Pin Finish	QFN 5x5 Plastic 32-pin	PD70101ILQ (IEEE802.3af)	Bulk/Tube
			PD70101ILQ-TR (IEEE802.3af)	Tape and Reel
			PD70201ILQ (IEEE802.3at)	Bulk/Tube
			PD70201ILQ-TR (IEEE802.3at)	Tape and Reel

**Microsemi Headquarters**

One Enterprise, Aliso Viejo,
CA 92656 USA

Within the USA: +1 (800) 713-4113

Outside the USA: +1 (949) 380-6100

Sales: +1 (949) 380-6136

Fax: +1 (949) 215-4996

Email: sales.support@microsemi.com

www.microsemi.com

© 2019 Microsemi. All rights reserved. Microsemi and the Microsemi logo are trademarks of Microsemi Corporation. All other trademarks and service marks are the property of their respective owners.

Microsemi makes no warranty, representation, or guarantee regarding the information contained herein or the suitability of its products and services for any particular purpose, nor does Microsemi assume any liability whatsoever arising out of the application or use of any product or circuit. The products sold hereunder and any other products sold by Microsemi have been subject to limited testing and should not be used in conjunction with mission-critical equipment or applications. Any performance specifications are believed to be reliable but are not verified, and Buyer must conduct and complete all performance and other testing of the products, alone and together with, or installed in, any end-products. Buyer shall not rely on any data and performance specifications or parameters provided by Microsemi. It is the Buyer's responsibility to independently determine suitability of any products and to test and verify the same. The information provided by Microsemi hereunder is provided "as is, where is" and with all faults, and the entire risk associated with such information is entirely with the Buyer. Microsemi does not grant, explicitly or implicitly, to any party any patent rights, licenses, or any other IP rights, whether with regard to such information itself or anything described by such information. Information provided in this document is proprietary to Microsemi, and Microsemi reserves the right to make any changes to the information in this document or to any products and services at any time without notice.

Microsemi, a wholly owned subsidiary of Microchip Technology Inc. (Nasdaq: MCHP), offers a comprehensive portfolio of semiconductor and system solutions for aerospace & defense, communications, data center and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions; setting the world's standard for time; voice processing devices; RF solutions; discrete components; enterprise storage and communication solutions; security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, California, and has approximately 4,800 employees globally. Learn more at www.microsemi.com.

PD-000391083