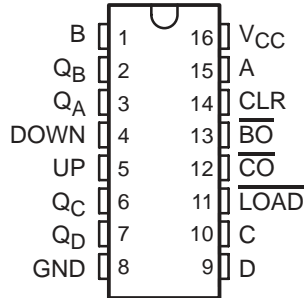


# SN54HC193, SN74HC193 4-BIT SYNCHRONOUS UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

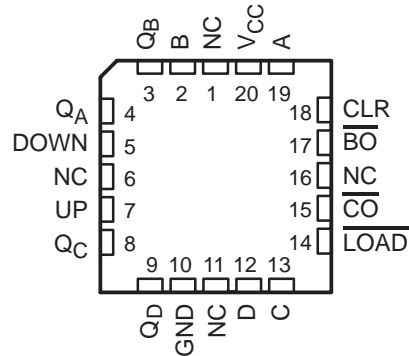
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- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 80- $\mu$ A Max  $I_{CC}$
- Typical  $t_{pd} = 20$  ns
- $\pm 4$ -mA Output Drive at 5 V
- Low Input Current of 1  $\mu$ A Max
- Look-Ahead Circuitry Enhances Cascaded Counters
- Fully Synchronous in Count Modes
- Parallel Asynchronous Load for Modulo-N Count Lengths
- Asynchronous Clear

SN54HC193 . . . J OR W PACKAGE  
SN74HC193 . . . D, N, NS, OR PW PACKAGE  
(TOP VIEW)



SN54HC193 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## description/ordering information

The 'HC193 devices are 4-bit synchronous, reversible, up/down binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidentally with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple-clock) counters.

## ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube of 25	SN74HC193N	SN74HC193N
	SOIC – D	Tube of 40	SN74HC193D	HC193
		Reel of 2500	SN74HC193DR	
		Reel of 250	SN74HC193DT	
	SOP – NS	Reel of 2000	SN74HC193NSR	HC193
	TSSOP – PW	Tube of 90	SN74HC193PW	HC193
Reel of 2000		SN74HC193PWR		
Reel of 250		SN74HC193PWT		
-55°C to 125°C	CDIP – J	Tube of 25	SNJ54HC193J	SNJ54HC193J
	CFP – W	Tube of 150	SNJ54HC193W	SNJ54HC193W
	LCCC – FK	Tube of 55	SNJ54HC193FK	SNJ54HC193FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

# SN54HC193, SN74HC193 4-BIT SYNCHRONOUS UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

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## description/ordering information (continued)

The outputs of the four flip-flops are triggered on a low-to-high-level transition of either count (clock) input (UP or DOWN). The direction of counting is determined by which count input is pulsed while the other count input is high.

All four counters are fully programmable; that is, each output may be preset to either level by placing a low on the load ( $\overline{\text{LOAD}}$ ) input and entering the desired data at the data inputs. The output changes to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers simply by modifying the count length with the preset inputs.

A clear (CLR) input has been provided that forces all outputs to the low level when a high level is applied. The clear function is independent of the count and  $\overline{\text{LOAD}}$  inputs.

These counters were designed to be cascaded without the need for external circuitry. The borrow ( $\overline{\text{BO}}$ ) output produces a low-level pulse while the count is zero (all outputs low) and DOWN is low. Similarly, the carry ( $\overline{\text{CO}}$ ) output produces a low-level pulse while the count is maximum (9 or 15), and UP is low. The counters then can be cascaded easily by feeding  $\overline{\text{BO}}$  and  $\overline{\text{CO}}$  to DOWN and UP, respectively, of the succeeding counter.

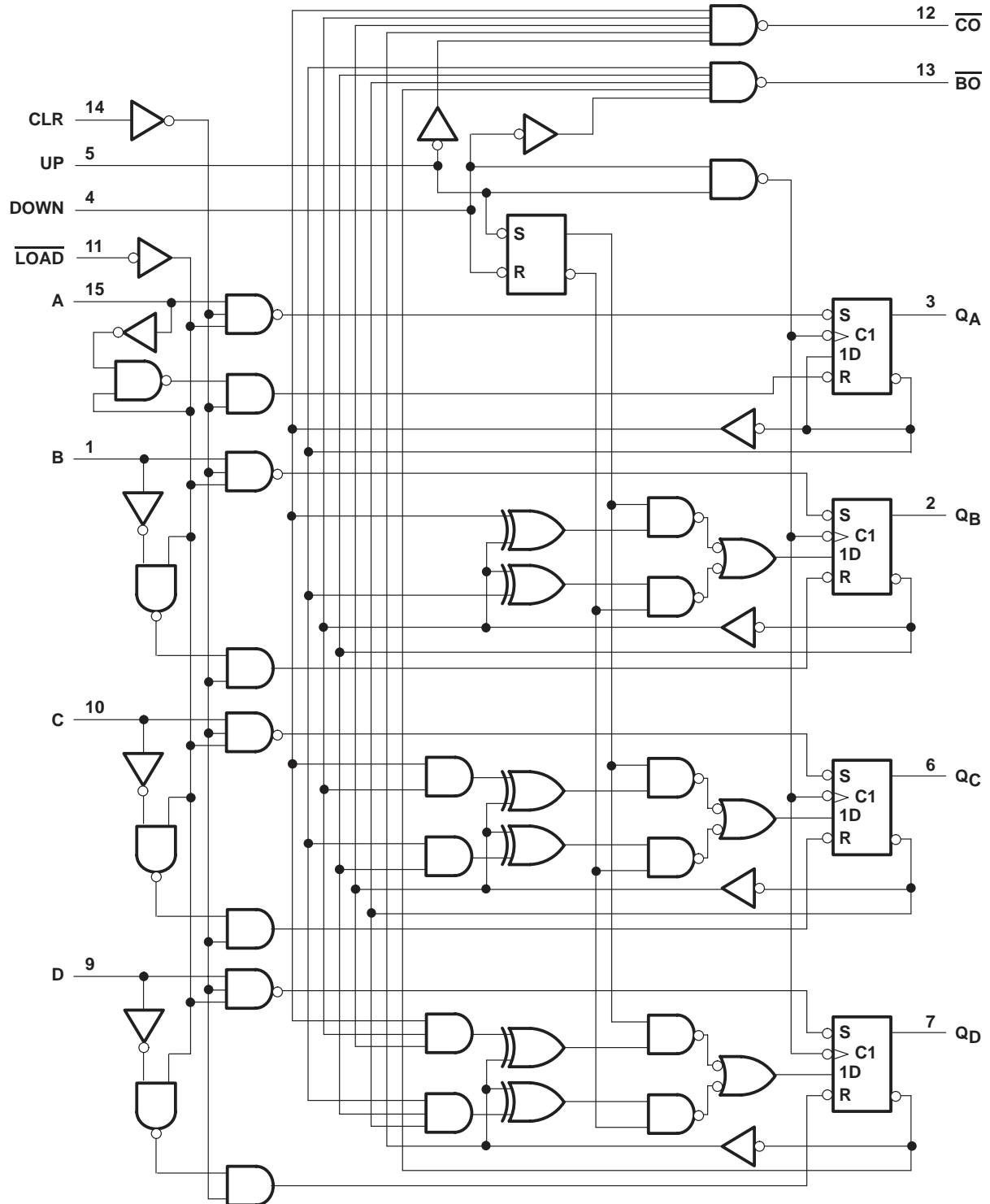


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# SN54HC193, SN74HC193 4-BIT SYNCHRONOUS UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

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logic diagram (positive logic)



Pin numbers shown are for the D, J, N, NS, PW, and W packages.

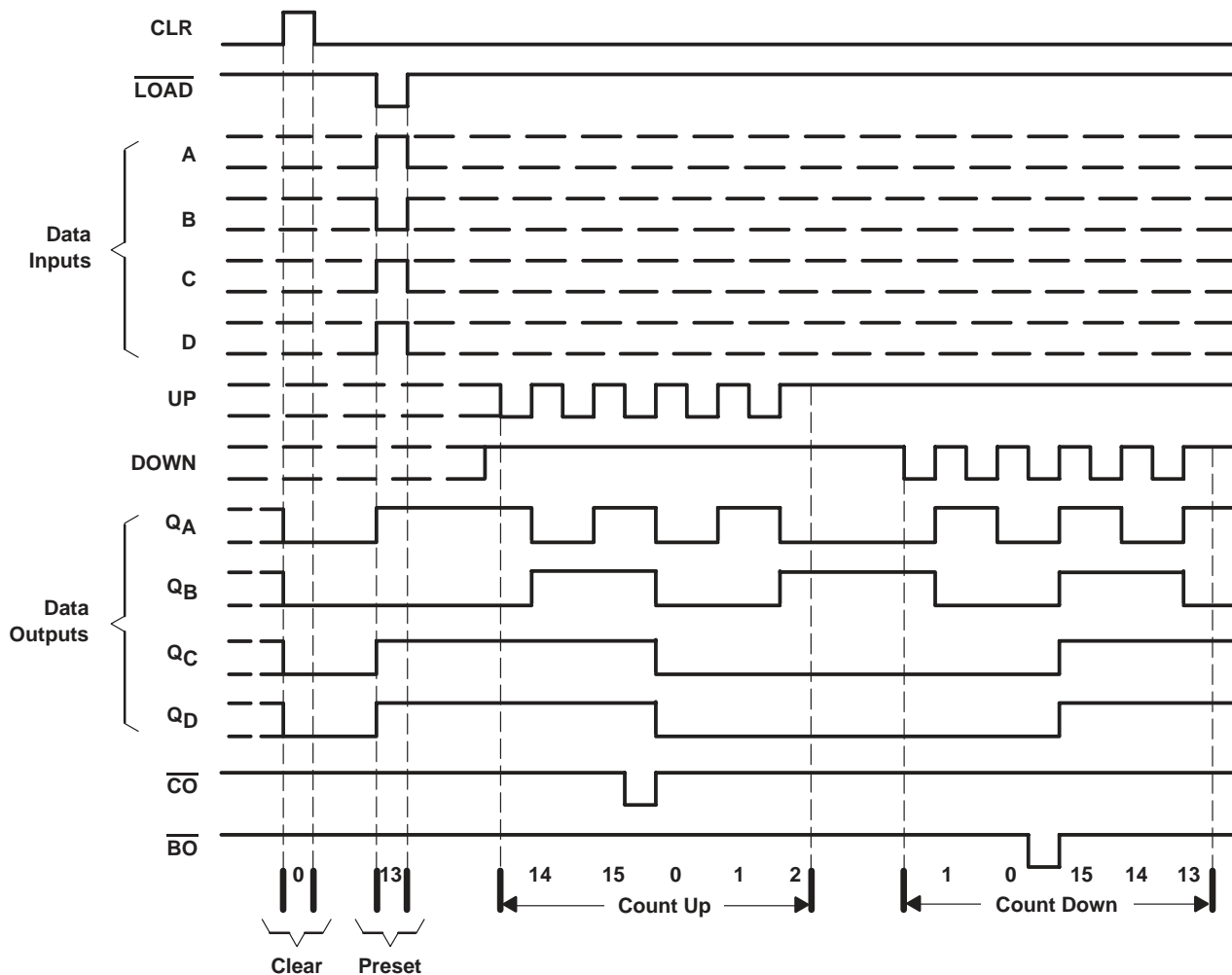
# SN54HC193, SN74HC193 4-BIT SYNCHRONOUS UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

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## typical clear, load, and count sequence

The following sequence is illustrated below:

1. Clear outputs to 0
2. Load (preset) to binary 13
3. Count up to 14, 15, carry, 0, 1, and 2
4. Count down to 1, 0, borrow, 15, 14, and 13



- NOTES: A. CLR overrides  $\overline{\text{LOAD}}$ , data, and count inputs.  
 B. When counting up, count-down input must be high; when counting down, count-up input must be high.



# SN54HC193, SN74HC193 4-BIT SYNCHRONOUS UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	–0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) (see Note 1) .....	±20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) (see Note 1) .....	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	±25 mA
Continuous current through $V_{CC}$ or GND .....	±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package .....	73°C/W
N package .....	67°C/W
NS package .....	64°C/W
PW package .....	108°C/W
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 3)

		SN54HC193			SN74HC193			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	2	5	6	2	5	6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2$ V		1.5	$V_{CC} = 2$ V		1.5	V
		$V_{CC} = 4.5$ V		3.15	$V_{CC} = 4.5$ V		3.15	
		$V_{CC} = 6$ V		4.2	$V_{CC} = 6$ V		4.2	
$V_{IL}$	Low-level input voltage	$V_{CC} = 2$ V			$V_{CC} = 2$ V		0.5	V
		$V_{CC} = 4.5$ V			$V_{CC} = 4.5$ V		1.35	
		$V_{CC} = 6$ V			$V_{CC} = 6$ V		1.8	
$V_I$	Input voltage	0		$V_{CC}$	0		$V_{CC}$	V
$V_O$	Output voltage	0		$V_{CC}$	0		$V_{CC}$	V
$\Delta t/\Delta v$ ‡	Input transition rise/fall time	$V_{CC} = 2$ V			$V_{CC} = 2$ V		1000	ns
		$V_{CC} = 4.5$ V			$V_{CC} = 4.5$ V		500	
		$V_{CC} = 6$ V			$V_{CC} = 6$ V		400	
$T_A$	Operating free-air temperature	–55		125	–40		85	°C

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

‡ If this device is used in the threshold region (from  $V_{ILmax} = 0.5$  V to  $V_{IHmin} = 1.5$  V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at  $t_f = 1000$  ns and  $V_{CC} = 2$  V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.



# SN54HC193, SN74HC193

## 4-BIT SYNCHRONOUS UP/DOWN COUNTERS

### (DUAL CLOCK WITH CLEAR)

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HC193		SN74HC193		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -20 μA	2 V	1.9	1.998		1.9		1.9	V	
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I <sub>OH</sub> = -4 mA	4.5 V	3.98	4.3		3.7		3.84		
			6 V	5.48	5.8		5.2		5.34		
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20 μA	2 V		0.002	0.1		0.1		V	
			4.5 V		0.001	0.1		0.1			0.1
			6 V		0.001	0.1		0.1			0.1
		I <sub>OL</sub> = 4 mA	4.5 V		0.17	0.26		0.4			0.33
			6 V		0.15	0.26		0.4			0.33
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0		6 V		±0.1	±100		±1000		±1000	nA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0		6 V			8		160		80	μA
C <sub>i</sub>			2 V to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V <sub>CC</sub>	T <sub>A</sub> = 25°C		SN54HC193		SN74HC193		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	2 V		4.2		2.8		3.3	MHz
		4.5 V		21		14		17	
		6 V		24		16		19	
t <sub>w</sub>	CLR high	2 V		120		180		150	ns
		4.5 V		24		36		30	
		6 V		21		31		26	
	LOAD low	2 V		120		180		150	
		4.5 V		24		36		30	
		6 V		21		31		26	
	UP or DOWN high or low	2 V		120		180		150	
		4.5 V		24		36		30	
		6 V		21		31		26	
t <sub>su</sub>	Data before LOAD inactive	2 V		110		165		140	ns
		4.5 V		22		33		28	
		6 V		19		28		24	
	CLR inactive before UP↑ or DOWN↑	2 V		110		165		140	
		4.5 V		22		33		28	
		6 V		19		28		24	
	LOAD inactive before UP↑ or DOWN↑	2 V		110		165		140	
		4.5 V		22		33		28	
		6 V		19		28		24	
t <sub>h</sub>	Data after LOAD inactive	2 V		5		5		5	ns
		4.5 V		5		5		5	
		6 V		5		5		5	



**SN54HC193, SN74HC193**  
**4-BIT SYNCHRONOUS UP/DOWN COUNTERS**  
**(DUAL CLOCK WITH CLEAR)**

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switching characteristics over recommended operating free-air temperature range,  $C_L = 50 \text{ pF}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			SN54HC193		SN74HC193		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{max}$			2 V	4.2	8		2.8		3.3	MHz	
			4.5 V	21	55		14		17		
			6 V	24	60		16		19		
$t_{pd}$	UP	$\overline{CO}$	2 V		75	165		250		205	ns
			4.5 V		24	33		50		41	
			6 V		20	28		43		35	
	DOWN	$\overline{BO}$	2 V		75	165		250		205	
			4.5 V		24	33		50		41	
			6 V		20	28		43		35	
	UP or DOWN	Any Q	2 V		190	250		375		315	
			4.5 V		40	50		75		63	
			6 V		35	43		64		54	
	$\overline{LOAD}$	Any Q	2 V		190	260		390		325	
			4.5 V		40	52		78		65	
			6 V		35	44		66		55	
$t_{PHL}$	CLR	Any Q	2 V		170	240		360		300	ns
			4.5 V		36	48		72		60	
			6 V		31	41		61		51	
$t_t$		Any	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

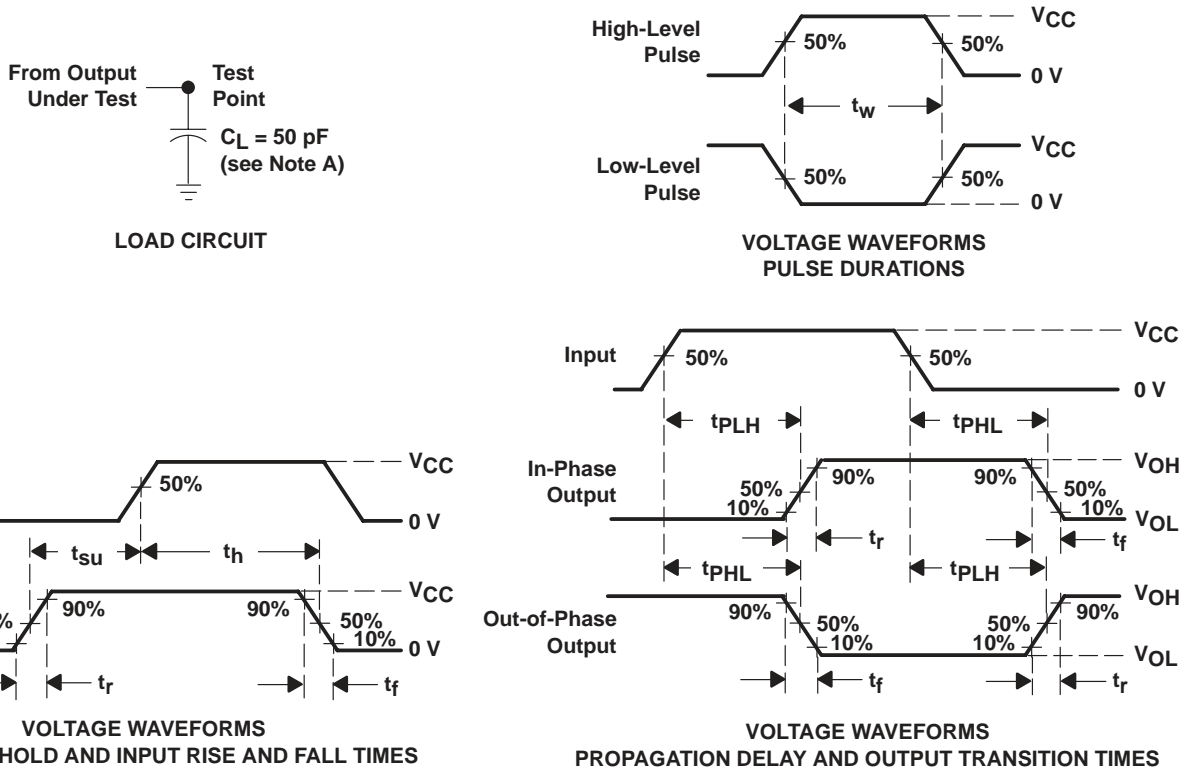
operating characteristics,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	No load	50	pF

**SN54HC193, SN74HC193**  
**4-BIT SYNCHRONOUS UP/DOWN COUNTERS**  
**(DUAL CLOCK WITH CLEAR)**

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**PARAMETER MEASUREMENT INFORMATION**



- NOTES:
- A.  $C_L$  includes probe and test-fixture capacitance.
  - B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 6 \text{ ns}$ ,  $t_f = 6 \text{ ns}$ .
  - C. For clock inputs,  $f_{max}$  is measured when the input duty cycle is 50%.
  - D. The outputs are measured one at a time with one input transition per measurement.
  - E.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

**Figure 1. Load Circuit and Voltage Waveforms**



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-87724012A	NRND	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 87724012A SNJ54HC 193FK	
5962-8772401EA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8772401EA SNJ54HC193J	<a href="#">Samples</a>
SN54HC193J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54HC193J	<a href="#">Samples</a>
SN74HC193D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC193	<a href="#">Samples</a>
SN74HC193DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC193	<a href="#">Samples</a>
SN74HC193DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC193	<a href="#">Samples</a>
SN74HC193DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC193	<a href="#">Samples</a>
SN74HC193DT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC193	<a href="#">Samples</a>
SN74HC193N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74HC193N	<a href="#">Samples</a>
SN74HC193NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74HC193N	<a href="#">Samples</a>
SN74HC193NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC193	<a href="#">Samples</a>
SN74HC193PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC193	<a href="#">Samples</a>
SN74HC193PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC193	<a href="#">Samples</a>
SN74HC193PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC193	<a href="#">Samples</a>
SN74HC193PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC193	<a href="#">Samples</a>
SNJ54HC193FK	NRND	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 87724012A SNJ54HC	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
										193FK	
SNJ54HC193J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8772401EA SNJ54HC193J	<b>Samples</b>

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN54HC193, SN74HC193 :**

- Catalog: [SN74HC193](#)
- Automotive: [SN74HC193-Q1](#), [SN74HC193-Q1](#)
- Military: [SN54HC193](#)

## NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC193DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC193NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74HC193PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC193DR	SOIC	D	16	2500	333.2	345.9	28.6
SN74HC193NSR	SO	NS	16	2000	367.0	367.0	38.0
SN74HC193PWR	TSSOP	PW	16	2000	367.0	367.0	35.0

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

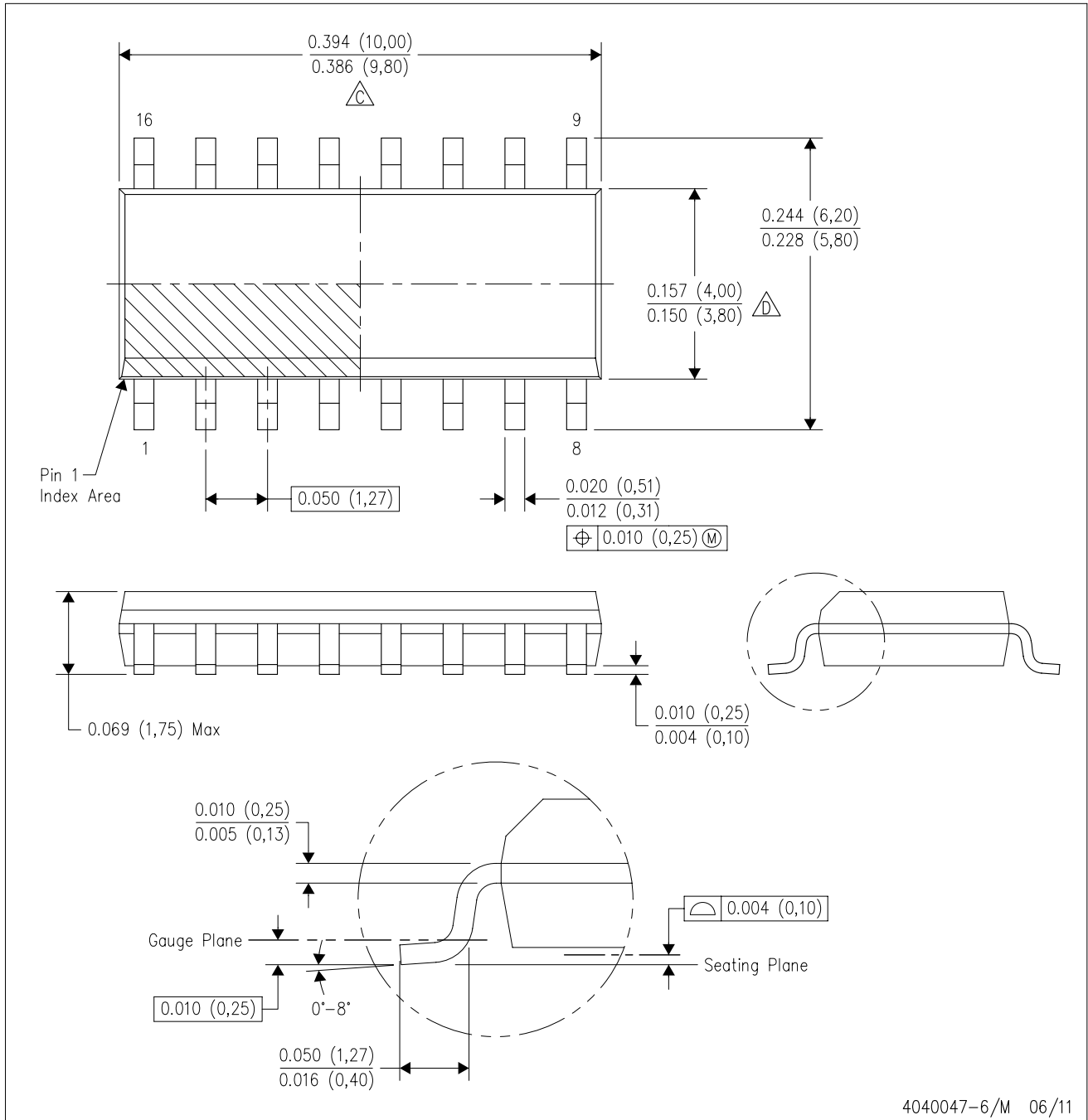


- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDSO-G16)

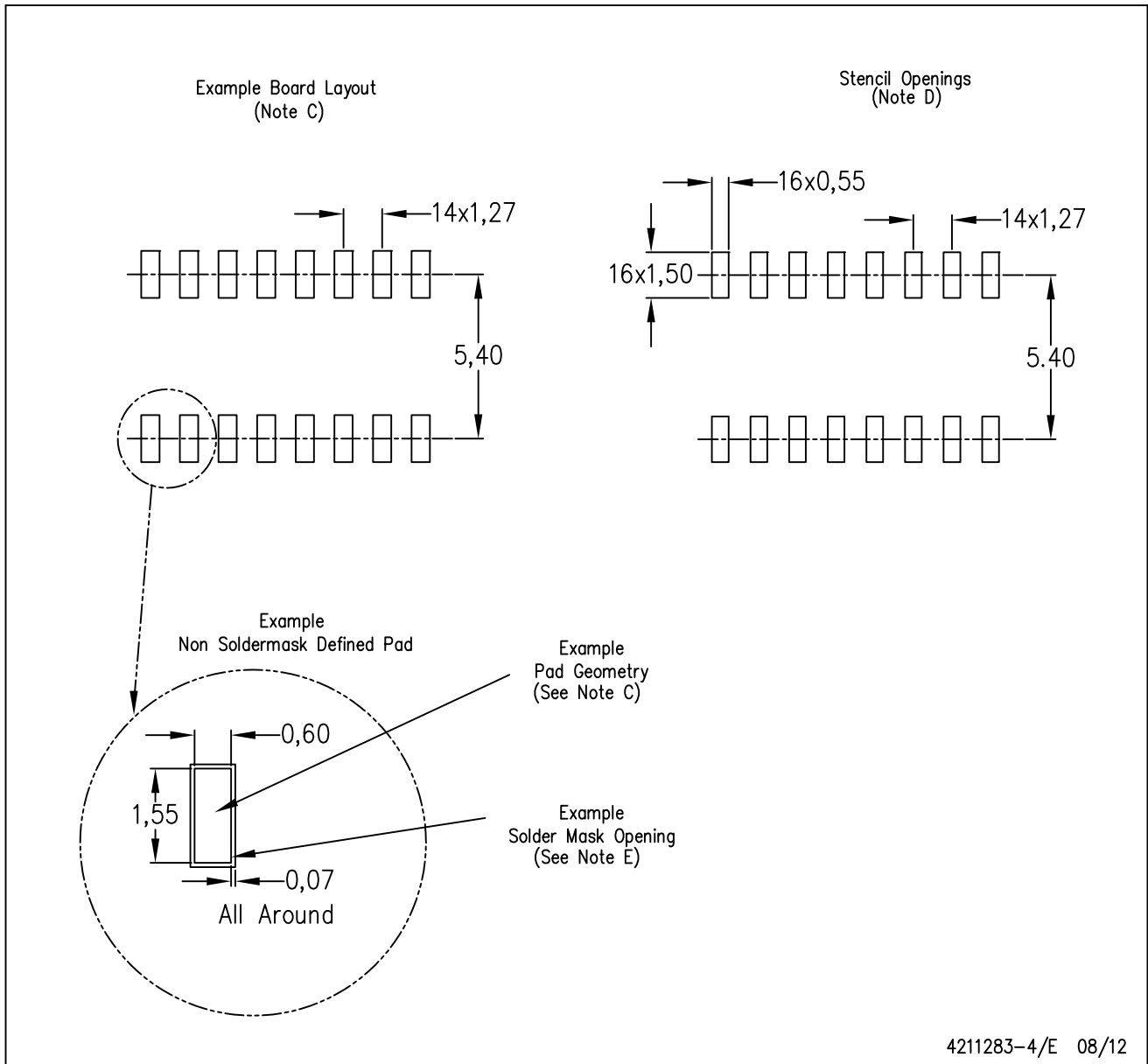
PLASTIC SMALL OUTLINE



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.  
 D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.  
 E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

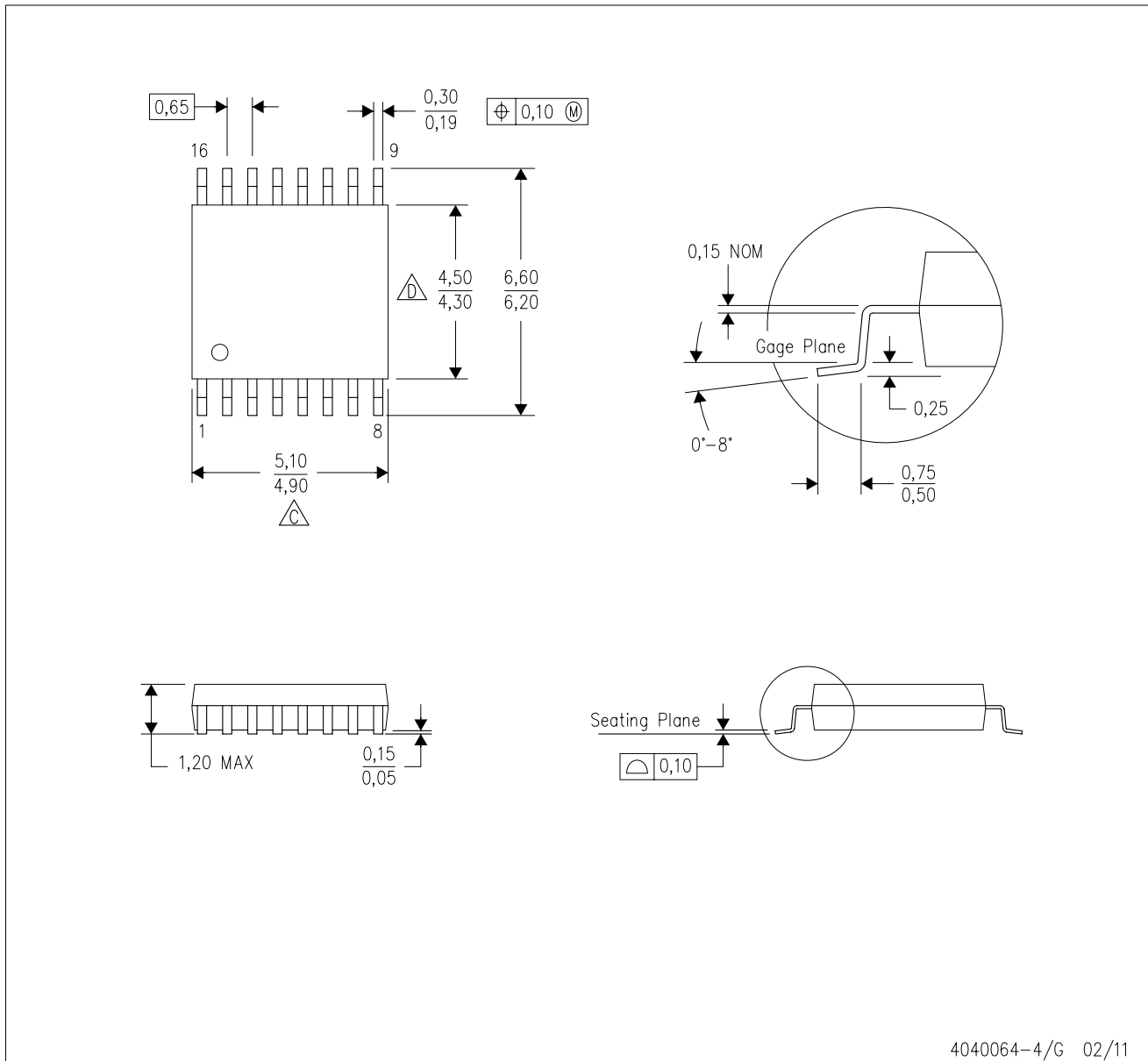
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G16)

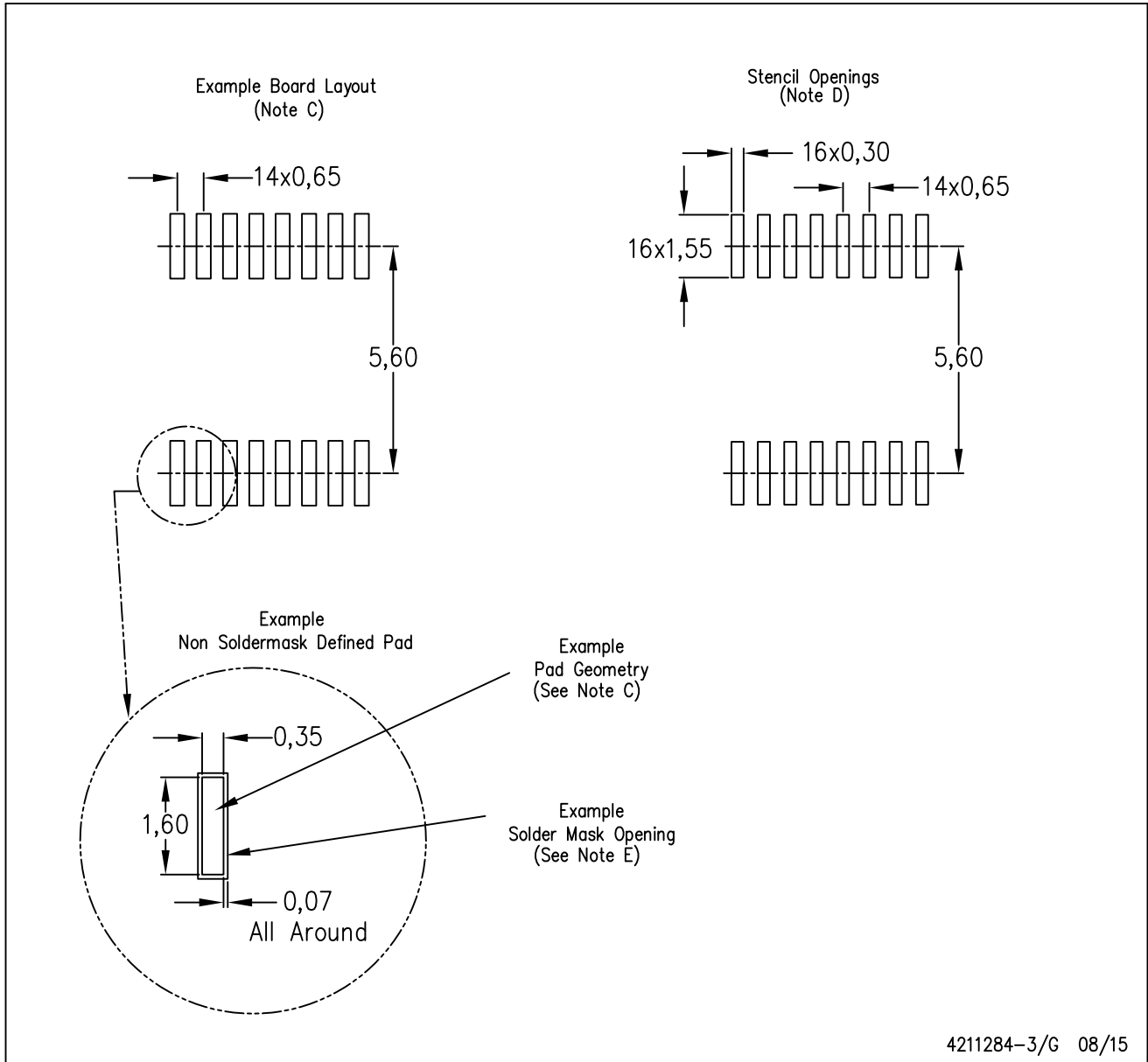
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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