



**MX573ABC212M500**  
**Ultra-Low Jitter 212.5MHz LVC MOS XO**  
**ClockWorks® FUSION**

**General Description**

The MX573ABC212M500 is an ultra-low phase jitter XO with LVC MOS output optimized for high line rate applications.

**Applications**

- Fibre Channel 10G/12G SERDES

**Features**

- 212.5MHz LVC MOS
- Typical phase noise:
  - 80fs (Integration range: 1.875MHz-20MHz)
- ±50ppm total frequency stability
- -40°C to +85°C temperature range
- Industry standard 6-Pin 7mm x 5mm LGA package

**Absolute Maximum Ratings**

Supply Voltage (VIN).....	+4.6V
Lead Temperature (soldering, 10s).....	260°C
Storage Temperature (T <sub>s</sub> ).....	125°C
ESD Rating (HBM).....	2kV

**Operating Ratings**

Supply Voltage (VIN).....	+2.375V to +3.63V
Ambient Temperature (TA).....	-40°C to +85°C

**Electrical Characteristics**

VDD = 2.375 - 3.63V, TA = -40°C to +85°C, output terminated with 50 Ohms to VDD/2.<sup>1</sup>

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
IDD	Supply Current				95	mA
F0	Center Frequency			212.5		MHz
	Frequency Stability	Note 2			±50	ppm
∅j	Phase Noise	Integration Range (12kHz to 20MHz) Integration Range (1.875MHz to 20MHz)		175 80		fsRMS
Tstart	Start-Up Time				20	ms
TR/TF	Rise/Fall time		100		500	ps
	Duty Cycle		45		55	%
VIH	Input High Voltage	3.3V Operation	2		VDD + 0.3	V
VIL	Input Low Voltage	3.3V Operation	-0.3		0.8	V
VOH	Output High Voltage	LVC MOS output levels	VDD - 0.8			V
VOL	Output Low Voltage	LVC MOS output levels			0.6	V

**Notes:**

1. Guaranteed after thermal equilibrium.
2. Inclusive of initial accuracy, temperature drift, aging, shock, vibration.

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February 04, 2017  
 MX573AB1-4816

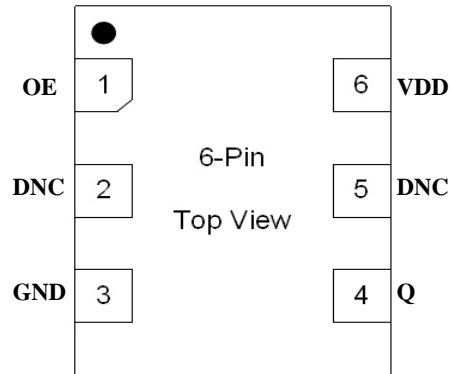
Revision 1.0  
[tcghelp@microchip.com](mailto:tcghelp@microchip.com)

## Ordering Information

Ordering Part Number	Marking Line 1	Marking Line 3	Shipping	Package
MX573ABC212M500	MX573AB	C212M500	Tube	6-Pin 7mm x 5mm LGA
MX573ABC212M500 TR	MX573AB	C212M500	Tape and Reel	6-Pin 7mm x 5mm LGA

Devices are Green and RoHS compliant. Sample material may have only a partial top mark.

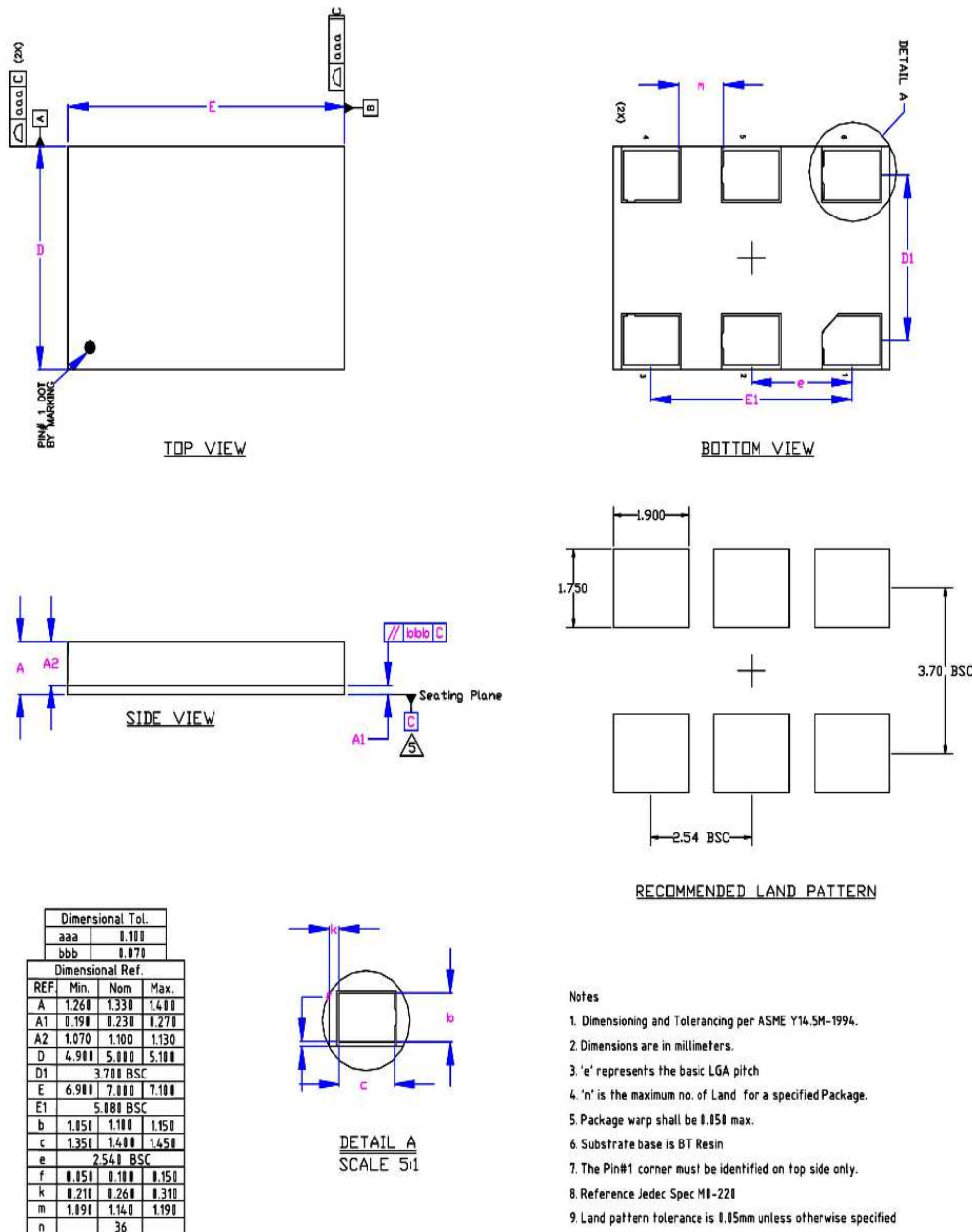
## Pin Configuration



## Pin Description

Pin Number	Pin Name	Pin Type	Pin Level	Pin Function
1	OE	I, SE	LVC MOS	Output Enable, disables output to tri-state, 0 = Disabled, 1 = Enabled, 50k Ohms Pull-Up
2	DNC			Make no connection, leave floating.
3	GND	PWR		Power Supply Ground
4, 5	Q, DNC	O, SE	LVC MOS	Clock Output Frequency = 212.5MHz
6	VDD	PWR		Power Supply

### Package Information and Recommended Land Pattern for 6-Pin LGA<sup>3</sup>



**6-Pin LGA (7x5mm)**

**Note:**

3. Package information is correct as of the publication date. For updates and most current information, go to [www.microchip.com](http://www.microchip.com).

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