



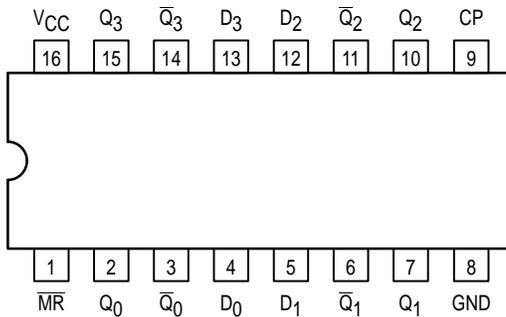
# MC54/74F175

## QUAD D FLIP-FLOP

The MC54/74F175 is a high-speed quad D flip-flop. The device is useful for general flip-flop requirements where both true and complementary outputs are required and clock and clear inputs are common to all flip-flops. The information on the D inputs is stored during the LOW-to-HIGH clock transition. Both true and complemented outputs of each flip-flop are provided. A Master Reset input resets all flip-flops, independent of the Clock or D inputs when LOW.

- Four Edge-triggered D-type Inputs
- Buffered Positive Edge-triggered Common Clock
- Buffered Asynchronous Common Reset
- True and Complementary Outputs
- ESD > 4000 Volts

### CONNECTION DIAGRAM DIP (TOP VIEW)



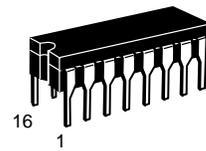
### FUNCTION TABLE

Inputs	Outputs	
@ $t_n$ , $\overline{MR} = H$	@ $t_n + 1$	
$D_n$	$Q_n$	$\overline{Q}_n$
L	L	H
H	H	L

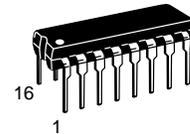
$t_n$  = Bit time before clock positive-going transition  
 $t_n + 1$  = Bit time after clock positive-going transition  
 H = HIGH Voltage Level  
 L = LOW Voltage Level

### QUAD D FLIP-FLOP

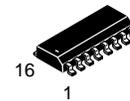
### FAST™ SCHOTTKY TTL



**J SUFFIX**  
 CERAMIC  
 CASE 620-09



**N SUFFIX**  
 PLASTIC  
 CASE 648-08

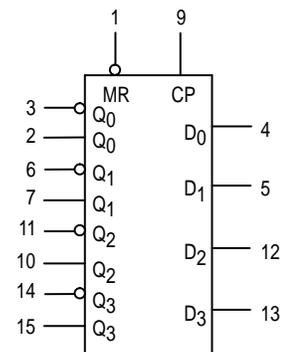


**D SUFFIX**  
 SOIC  
 CASE 751B-03

### ORDERING INFORMATION

MC54FXXXJ Ceramic  
 MC74FXXXN Plastic  
 MC74FXXXD SOIC

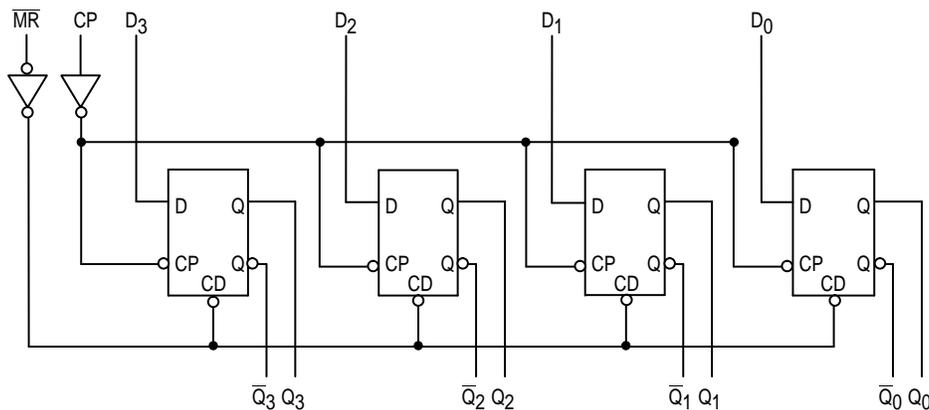
### LOGIC SYMBOL



$V_{CC}$  = PIN 16  
 GND = PIN 8

# MC54/74F175

## LOGIC DIAGRAM



**NOTE:**

This diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## FUNCTIONAL DESCRIPTION

The F175 consists of four edge-triggered D flop-flops with individual D inputs and Q and  $\bar{Q}$  outputs. The Clock and Master Reset are common. The four flip-flops will store the state of their individual D inputs, one setup time before, on the LOW-to-HIGH clock (CP) transition, causing individual Q and

$\bar{Q}$  outputs to follow. A LOW input on the Master Reset (MR) will force all Q outputs LOW and  $\bar{Q}$  outputs HIGH independent of Clock or Data inputs. The F175 is useful for general logic applications where a common Master Reset and Clock are acceptable.

## GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V <sub>CC</sub>	Supply Voltage	54, 74	4.5	5.0	5.5	V
T <sub>A</sub>	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I <sub>OH</sub>	Output Current — High	54, 74			-1.0	mA
I <sub>OL</sub>	Output Current — Low	54, 74			20	mA

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage	
V <sub>IL</sub>	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage	
V <sub>IK</sub>	Input Clamp Diode Voltage			-1.2	V	I <sub>IN</sub> = -18 mA	V <sub>CC</sub> = MIN
V <sub>OH</sub>	Output HIGH Voltage	54, 74	2.5	3.4	V	I <sub>OH</sub> = -1.0 mA	V <sub>CC</sub> = 4.50 V
		74	2.7	3.4	V	I <sub>OH</sub> = -1.0 mA	V <sub>CC</sub> = 4.75 V
V <sub>OL</sub>	Output LOW Voltage		0.35	0.5	V	I <sub>OL</sub> = 20 mA	V <sub>CC</sub> = MIN
I <sub>IH</sub>	Input HIGH Current			20	μA	V <sub>IN</sub> = 2.7 V	V <sub>CC</sub> = MAX
				100	μA	V <sub>IN</sub> = 7.0 V	V <sub>CC</sub> = MAX
I <sub>IL</sub>	Input LOW Current			-0.6	mA	V <sub>IN</sub> = 0.5 V	V <sub>CC</sub> = MAX
I <sub>OS</sub>	Output Short Circuit Current (Note 2)	-60		-150	mA	V <sub>OUT</sub> = 0 V	V <sub>CC</sub> = MAX
I <sub>CC</sub>	Power Supply Current		22.5	34	mA	D <sub>n</sub> = $\overline{MR}$ = 4.5 V CP = $\sqrt{\quad}$	V <sub>CC</sub> = MAX

**NOTES:**

- For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
- Not more than one output should be shorted at a time, nor for more than 1 second.

# MC54/74F175

## AC CHARACTERISTICS

Symbol	Parameter	54/74F			54F		74F		Unit
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0 V C <sub>L</sub> = 50 pF			T <sub>A</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0 V ± 10% C <sub>L</sub> = 50 pF		T <sub>A</sub> = 0°C to +70°C V <sub>CC</sub> = 5.0 V ± 10% C <sub>L</sub> = 50 pF		
		Min	Typ	Max	Min	Max	Min	Max	
f <sub>max</sub>	Maximum Clock Frequency	100	140		100		100		MHz
t <sub>PLH</sub>	Propagation Delay	3.5	5.0	6.5	3.5	8.5	3.5	7.5	ns
t <sub>PHL</sub>	CP to Q <sub>n</sub> or $\overline{Q}_n$	4.0	6.5	8.5	4.0	10.5	4.0	9.5	
t <sub>PHL</sub>	Propagation Delay $\overline{MR}$ to $\overline{Q}_n$	4.5	9.0	11.5	4.5	15	4.5	13	ns
t <sub>PLH</sub>	Propagation Delay $\overline{MR}$ to $\overline{Q}_n$	4.0	6.5	8.5	4.0	10	4.0	9.0	ns

## AC OPERATING REQUIREMENTS

Symbol	Parameter	54/74F			54F		74F		Unit
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0 V			T <sub>A</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0 V ± 10%		T <sub>A</sub> = 0°C to +70°C V <sub>CC</sub> = 5.0 V ± 10%		
		Min	Typ	Max	Min	Max	Min	Max	
t <sub>S(H)</sub>	Setup Time, HIGH or LOW	3.0			3.0		3.0		ns
t <sub>S(L)</sub>	D <sub>n</sub> to CP	3.0			3.0		3.0		
t <sub>H(H)</sub>	Hold Time, HIGH or LOW	1.0			1.0		1.0		ns
t <sub>H(L)</sub>	D <sub>n</sub> to CP	1.0			1.0		1.0		
t <sub>W(H)</sub>	CP Pulse Width, HIGH	4.0			4.0		4.0		ns
t <sub>W(L)</sub>	or LOW	5.0			5.0		5.0		
t <sub>W(L)</sub>	$\overline{MR}$ Pulse Width, LOW	5.0			5.0		5.0		ns
t <sub>rec</sub>	Recovery Time, $\overline{MR}$ to CP	5.0			5.0		5.0		ns