AUTOMOTIVE N-Channel 40V 175°C MOSFET

FEATURES

- AEC-Q101 Qualified
- 100% UIS and R_g Tested
- 175°C Operating Junction Temperature
- Wettable Flank Package
- RoHS Compliant
- Halogen-free according to IEC 61249-2-21

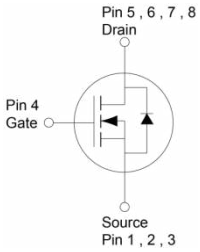
APPLICATIONS

- 12V Automotive Systems
- Solenoid and Motor Control
- Automotive Transmission Control
- DC-DC Converters

PRODUCT SUMMARY			
PARAMETER		**VALUE**	**UNIT**
V_{DS}		40	V
$R_{DS(on)}$ (max)	V_{GS} = 10V	3.3	mΩ
	V_{GS} = 7V	5.1	
Q_g		87	nC

Pb-Free RoHS COMPLIANT HALOGEN FREE

PDFN56U



Note: MSL 1 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)				
PARAMETER		**SYMBOL**	**LIMIT**	**UNIT**
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current (Note 1)	T_C = 25°C	I_D	121	A
	T_A = 25°C		21	
Pulsed Drain Current		I_{DM}	484	A
Single Pulse Avalanche Current (Note 2)		I_{AS}	36	A
Single Pulse Avalanche Energy (Note 2)		E_{AS}	194	mJ
Total Power Dissipation	T_C = 25°C	P_D	107	W
	T_C = 125°C		36	
Total Power Dissipation	T_A = 25°C	P_D	3.1	W
	T_A = 125°C		1	
Operating Junction and Storage Temperature Range		T_J, T_{STG}	- 55 to +175	°C

THERMAL RESISTANCE			
PARAMETER	**SYMBOL**	**MAXIMUM**	**UNIT**
Thermal Resistance – Junction to Case	$R_{\Theta JC}$	1.4	°C/W
Thermal Resistance – Junction to Ambient	$R_{\Theta JA}$	48	°C/W

Thermal Performance Note: $R_{\Theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case-thermal reference is defined at the solder mounting surface of the drain pins. $R_{\Theta JC}$ is guaranteed by design while $R_{\Theta CA}$ is determined by the user's board design. The $R_{\Theta JA}$ limit presented here is based on mounting on a 1 in^2 pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)						
PARAMETER	**CONDITIONS**	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**
Static						
Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250μA	BV_{DSS}	40	--	--	V
Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA	$V_{GS(TH)}$	1.8	2.5	3.8	V
Gate-Source Leakage Current	V_{GS} = ±20V, V_{DS} = 0V	I_{GSS}	--	--	±100	nA
Drain-Source Leakage Current	V_{GS} = 0V, V_{DS} = 40V	I_{DSS}	--	--	1	μA
	V_{GS} = 0V, V_{DS} = 40V T_J = 125°C		--	--	100	
	V_{GS} = 0V, V_{DS} = 40V T_J = 175°C		--	--	500	
Drain-Source On-State Resistance (Note 3)	V_{GS} = 10V, I_D = 21A	$R_{DS(on)}$	--	2.2	3.3	mΩ
	V_{GS} = 10V, I_D = 21A, T_J = 125°C		--	3.8	5.7	
	V_{GS} = 10V, I_D = 21A, T_J = 175°C		--	4.8	7.3	
	V_{GS} = 7V, I_D = 17A		--	2.5	5.1	
Forward Transconductance (Note 3)	V_{DS} = 10V, I_D = 21A	g_{fs}	--	68	--	S
Dynamic (Note 4)						
Total Gate Charge	V_{GS} = 10V, V_{DS} = 20V, I_D = 21A	Q_g	--	87	--	nC
Total Gate Charge	V_{GS} = 7V, V_{DS} = 20V, I_D = 17A	Q_g	--	64	--	
Gate-Source Charge		Q_{gs}	--	20	--	
Gate-Drain Charge		Q_{gd}	--	23	--	
Input Capacitance	V_{GS} = 0V, V_{DS} = 20V, f = 1.0MHz	C_{iss}	--	4917	--	pF
Output Capacitance		C_{oss}	--	484	--	
Reverse Transfer Capacitance		C_{rss}	--	276	--	
Gate Resistance	f = 1.0MHz	R_g	0.5	1.7	3.4	Ω
Switching (Note 4)						
Turn-On Delay Time	V_{GS} = 10V, V_{DS} = 20V, I_D = 21A, R_G = 2Ω	$t_{d(on)}$	--	10	--	ns
Rise Time		t_r	--	24	--	
Turn-Off Delay Time		$t_{d(off)}$	--	49	--	
Fall Time		t_f	--	23	--	
Source-Drain Diode						
Diode Forward Voltage (Note 3)	V_{GS} = 0V, I_S = 21A	V_{SD}	--	--	1	V
Reverse Recovery Time	I_S = 21A, di/dt = 100A/μs	t_{rr}	--	30	--	ns
Reverse Recovery Charge		Q_{rr}	--	20	--	nC

Notes:

1. Silicon limited current only.
2. L = 0.3mH, V_{GS} = 10V, V_{DD} = 25V, R_G = 50Ω, I_{AS} = 36A, Starting T_J = 25°C
3. Pulse test: Pulse Width ≤ 300μs, duty cycle ≤ 2%.
4. Switching time is essentially independent of operating temperature.

ORDERING INFORMATION

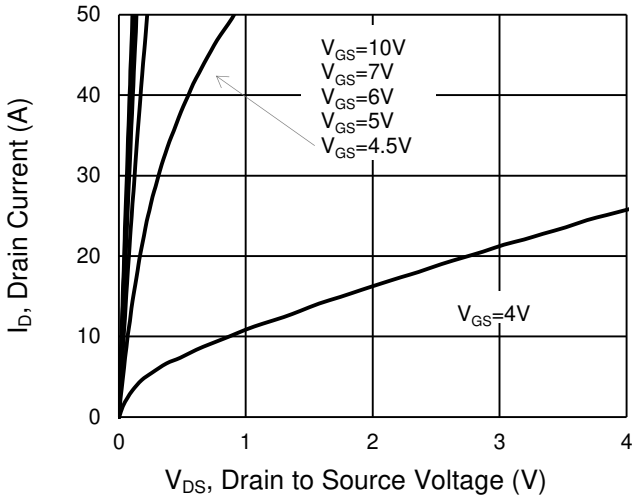
ORDERING CODE	PACKAGE	PACKING
TQM033NB04CR RLG	PDFN56U	2,500pcs / 13” Reel
TQM033NB04CR-V RLG	PDFN56U	2,500pcs / 13” Reel

Notes:
V : HOT test

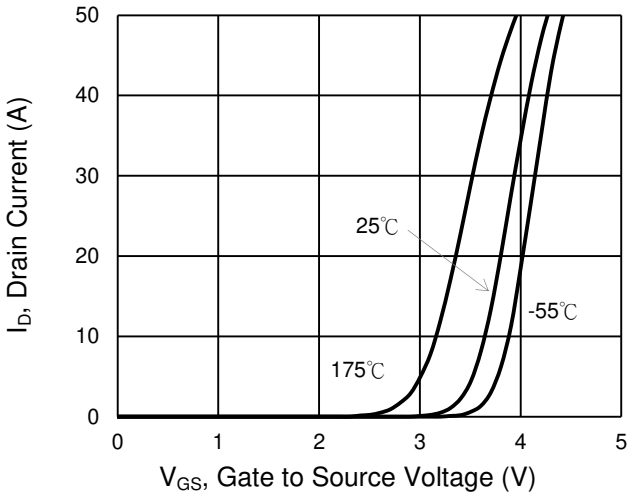
CHARACTERISTICS CURVES

(T_A = 25°C unless otherwise noted)

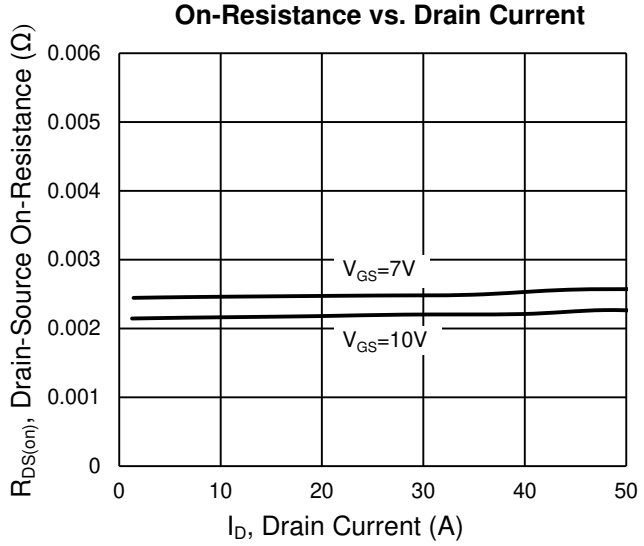
Output Characteristics



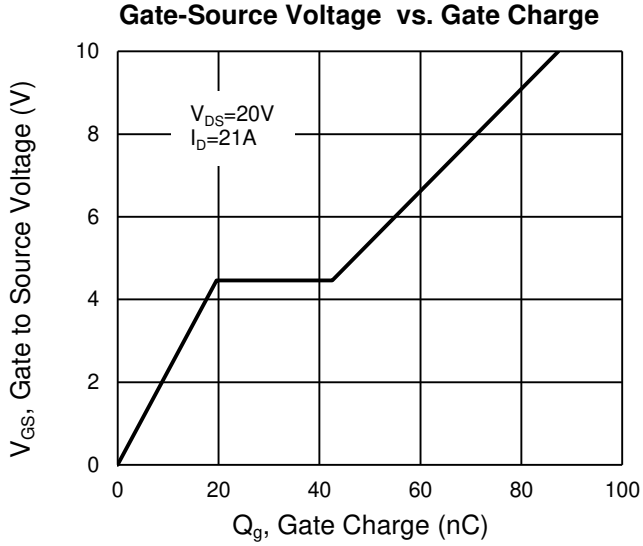
Transfer Characteristics



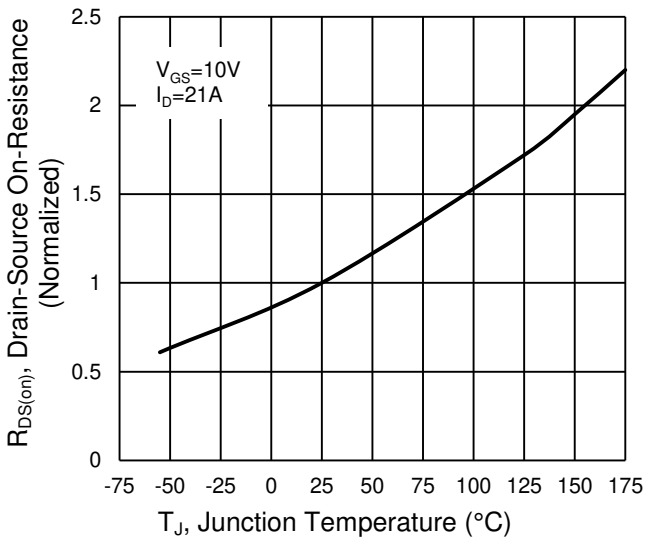
On-Resistance vs. Drain Current



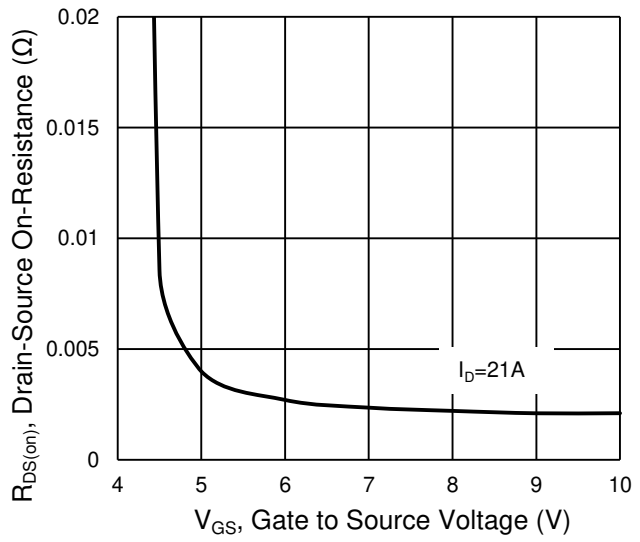
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature



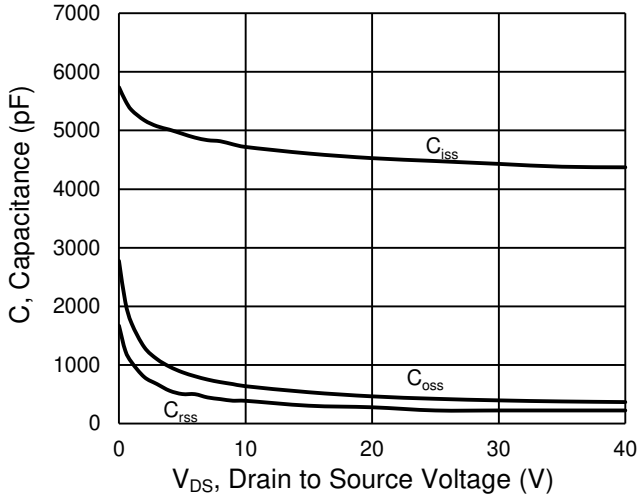
On-Resistance vs. Gate-Source Voltage



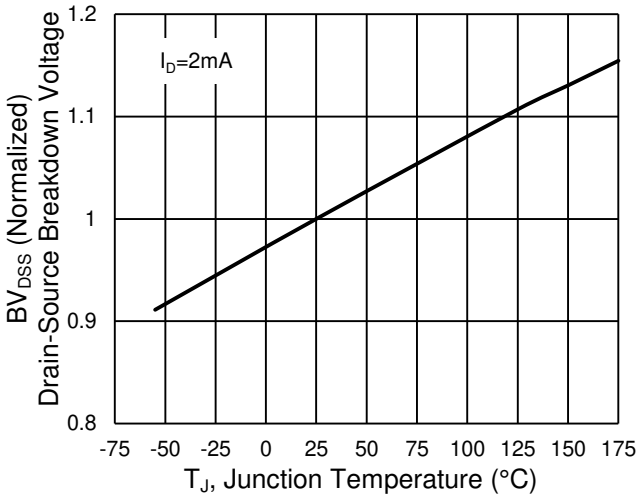
CHARACTERISTICS CURVES

(T_A = 25°C unless otherwise noted)

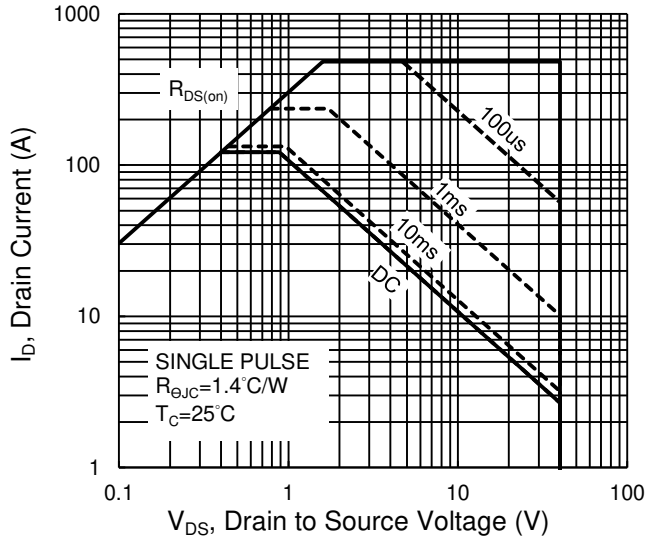
Capacitance vs. Drain-Source Voltage



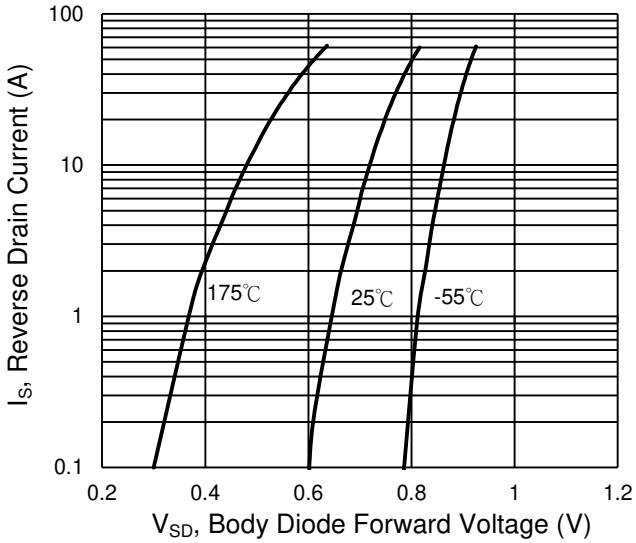
BV_{DSS} vs. Junction Temperature



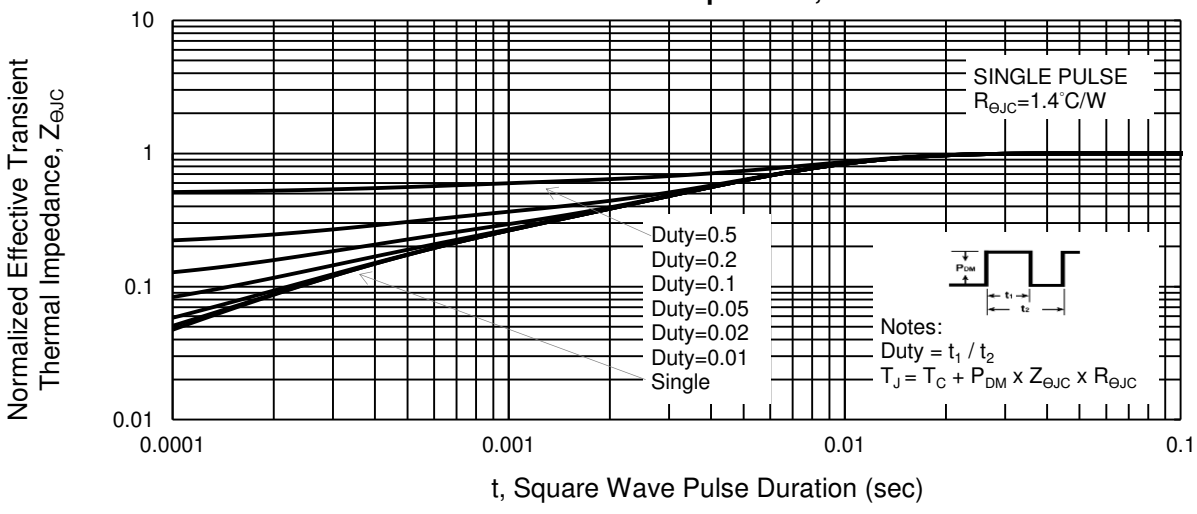
Maximum Safe Operating Area, Junction-to-Case



Source-Drain Diode Forward Current vs. Voltage

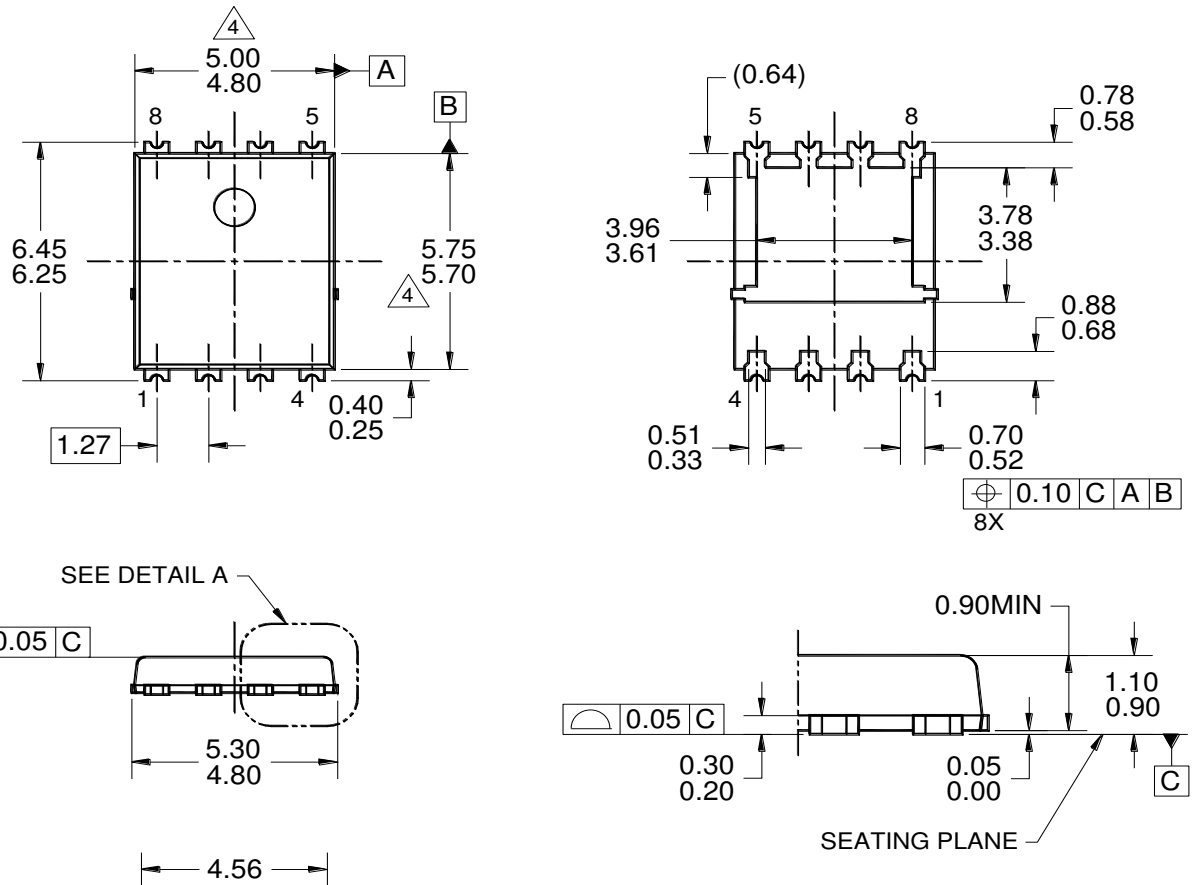


Normalized Thermal Transient Impedance, Junction-to-Case



PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

PDFN56U



NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PACKAGE OUTLINE REFERENCE: JEITA ED-7500B, EIAJ SC-111BB.

4 MOLDED PLASTIC BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

5. DWG NO. REF: HQ2SD07-PDFN56U-023 REV A.

P/N	=	MARKING CODE
Y	=	YEAR CODE
WW	=	WEEK CODE (01~52)
L	=	LOT CODE (1~9, A~Z)
F	=	FACTORY CODE
_	=	AEC-Q101 QUALIFIED

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