FAIRCHILD SEMICONDUCTOR®

October 2007

USB1T1103
Universal Serial Bus Peripheral Transceiver with Voltage Regulator

Features

- Complies with Universal Serial Bus Specification 2.0
- Integrated 5V to 3.3V voltage regulator for powering VBus
- Utilizes digital inputs and outputs to transmit and receive USB cable data
- Supports full speed (12Mbits/s) data rates
- Ideal for portable electronic devices
- MLP technology package (16 terminal) with HBCC footprint
- 15kV contact HBM ESD protection on bus terminals

Description

This chip provides a USB Transceiver functionality with a voltage regulator that is compliant to USB Specification Rev 2.0. this integrated 5V to 3.3V regulator allows interfacing of USB Application specific devices with supply voltages ranging from 1.65V to 3.6V with the physical layer of Universal Serial Bus. It is capable of operating at 12Mbits/s (full speed) data rates and hence is fully compliant to USB Specification Rev 2.0. The Vbusmon terminal allows for monitoring the Vbus line.

The USB1T1103 also provides exceptional ESD protection with 15kV contact HBM on D+,D- terminals

Applications

- PDA
- PC Peripherals
- Cellular Phones
- MP3 Players
- Digital Still Camera
- Information Appliance

Ordering Information

Part Number	Package Number	Product code Top Mark	Pb-Free	Package Description	Packing Method
USB1T1103MPX	MLP14D	$Y&Z&2&T USB1103	Yes	14-Terminal Molded Leadless Package (MLP), 2.5mm Square	3K Units on Tape and Reel
USB1T1103MHX	MLP16HB	$Y&Z&2&T USB1103	Yes	16-Terminal Molded Leadless Package (MHBCC), JEDEC MO-217,3mm Square	3K Units on Tape and Reel

Pb-Free package per JEDEC J-STD-020B.

Typical Application

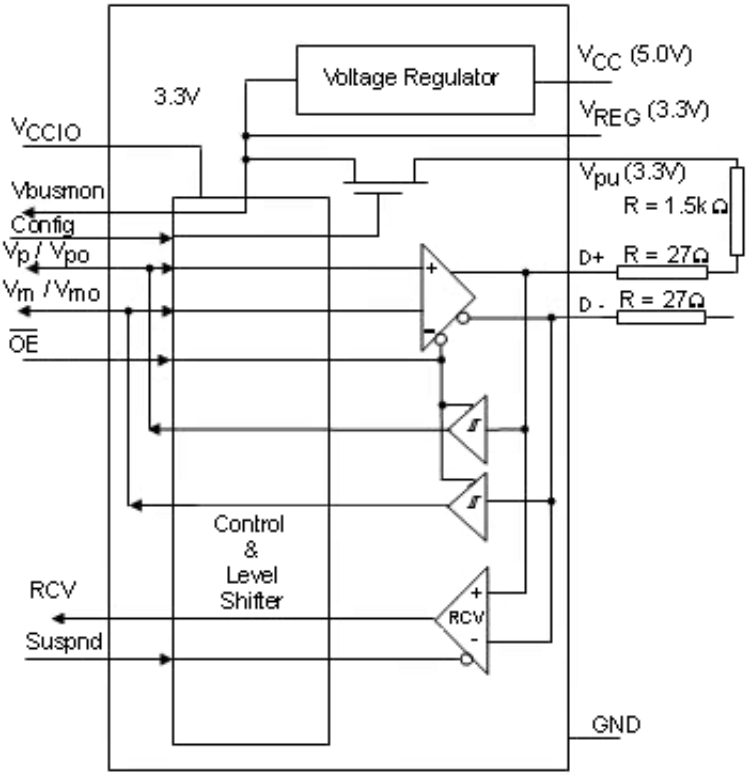


Figure 1. Logic Diagram

Connection Diagrams

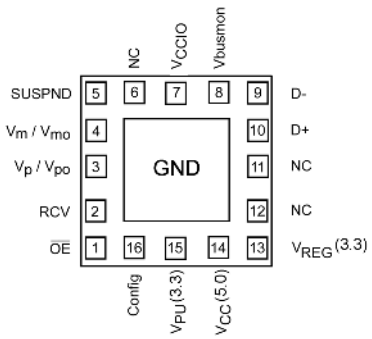


Figure 2. MLP16 GND Exposed Diepad (Bottom View)

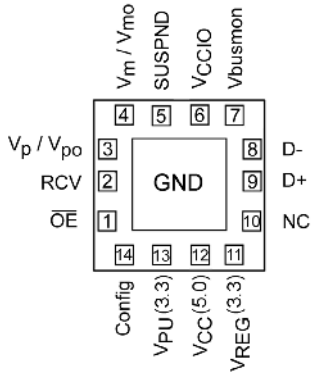


Figure 3. MLP14 GND Exposed Diepad (Bottom View)

Terminal Descriptions

Terminal Number		Terminal Name	I/O	Terminal Description
MLP14	MLP16			
1	1	OE	I	Output Enable: Active LOW enables the transceiver to transmit data on the bus. When not active the transceiver is in the receive mode (CMOS level is relative to V_{CCIO})
2	2	RCV	O	Receive Data Output: Non-inverted CMOS level output for USB differential Input (CMOS output level is relative to V_{CCIO}). Driven LOW when SUSPN is HIGH; RCV output is stable and preserved during SE0 condition.
3	3	V_p/V_{po}	I/O	Single-ended D+ receiver output V_P (CMOS level relative to V_{CCIO}): Used for external detection of SE0, error conditions, speed of connected device; Terminal also acts as drive data input V_{po} (see Table 1 and Table 2). Output drive is 4 mA buffer.
4	4	V_m/V_{mo}	I/O	Single-ended D- receiver output V_m (CMOS level relative to V_{CCIO}): Used for external detection of SE0, error conditions, speed of connected device; Terminal also acts as drive data input V_{mo} (see Table 1 and Table 2). Output drive is 4 mA buffer.
5	5	SUSPND	I	Suspend: Enables a low power state (CMOS level is relative to V_{CCIO}). While the SUSPND terminal is active (HIGH) it will drive the RCV terminal to logic “0” state.
—	6	NC		No Connect
6	7	V_{CCIO}		Supply Voltage for digital I/O terminals (1.65V to 3.6V): When not connected the D+ and D- terminals are in 3-STATE. This supply bus is totally independent of V_{CC} (5V) and V_{REG} (3.3V), and must never exceed the V_{REG} (3.3) voltage. For V_{CCIO} disconnected the O+/O- terminals are HIGH Impedance and the V_{PU} (3.3V) is turned off.
7	8	Vbusmon	O	Vbus monitor output (CMOS level relative to V_{CCIO}): When Vbus > 4.1V then Vbusmon = HIGH and when Vbus < 3.6V then Vbusmon = LOW. If SUSPND = HIGH then Vbusmon is pulled HIGH.
9, 8	10, 9	D+, D-	AI/O	Data +, Data -: Differential data bus conforming to the USB standard. Terminals are HIGH Impedance for bus powered mode when Vbus < 3.6V. For ByPass Mode then HIGH Impedance when V_{REG}/ Vbus < V_{REG} minimum.
10	11	NC		No Connect
—	12	NC		No Connect
11	13	V_{REG} (3.3V)		Internal Regulator Option: Regulated supply output voltage (3.0V to 3.6V) during 5V operation; decoupling capacitor of at least 0.1 µF is required. Regulator ByPass Option: Used as supply voltage input for 3.3V operation.
12	14	V_{CC} (5.0V)		Internal Regulator Option: Used as supply voltage input (4.0V to 5.5V); can be connected directly to USB line Vbus. Regulator ByPass Option: Connected to V_{REG} (3.3V)
13	15	V_{PU} (3.3V)		Pull-up Supply Voltage (3.3V ± 10%): Connect an external 1.5kΩ resistor on D+ (FS data rate); Terminal function is controlled by Config input terminal: Config = LOW - V_{PU} (3.3V) is floating (HIGH Impedance) for zero pull-up current. Config = HIGH - V_{PU} (3.3V) = 3.3V; internally connected to V_{REG} (3.3V). V_{PU} is OFF in disable mode.
14	16	Config	I	USB connect or disconnect software control input. Configures 3.3V to external 1.5kΩ resistor on D+ when HIGH.
Exposed Diepad	Exposed Diepad	GND	GND	GND supply down bonded to exposed diepad to be connected to the PCB GND.

Functional Description

The USB1T1103 transceiver is designed to convert CMOS data into USB differential bus signal levels and to convert USB differential bus signal to CMOS data.

To minimize EMI and noise the outputs are edge rate controlled with the rise and fall times controlled and defined for full speed data rates only (12Mbits/s). The rise, fall times are balanced between the differential terminals to minimize skew.

The USB1T1103 differs from earlier USB Transceiver in that the V_p/V_m and V_{po}/V_{mo} terminals are now I/O terminals rather than discrete input and output terminals. Table 1 describes the specific terminal functionality selection. Table 2 and Table 3 describe the specific Truth Tables for Driver and Receiver operating functions.

The USB1T1103 also has the capability of various power supply configurations, including a disable mode for V_{CCIO} disconnected, to support mixed voltage supply applications (see Table 4) and Section 2.1 for detailed descriptions.

Functional Tables

Table 1. Function Select

SUSPND	OE	D+, D-	RCV	V_p/V_{po}	V_m/V_{mo}	Function
L	L	Driving & Receiving	Active	V_{po} Input	V_{mo} Input	Normal Driving (Differential Receiver Active)
L	H	Receiving (1)	Active	V_p Output	V_m Output	Receiving
H	L	Driving	Inactive(2)	V_{po} Input	V_{mo} Input	Driving during Suspend (Differential Receiver Inactive)
H	H	3 STATE(1)	Inactive(2)	V_p Output	V_m Output	Low Power State

Notes:

1. Signal levels is function of connection and/or pull-up/pull-down resistors.
2. For SUSPND = HIGH mode the differential receiver is inactive and the output RCV is forced LOW. The out-of-suspend signaling (K) is detected via the single-ended receivers of the V_p/V_{po} and V_m/V_{mo} terminals.

Table 2. Driver Function ($\overline{OE}$ = L) using Differential Input Interface

V_m/V_{mo}	V_p/V_{po}	Data (D+ / D-)
L	L	SE0 (3)
L	H	Differential Logic 1
H	L	Differential Logic 0
H	H	Illegal State

Notes:

3. SE0 = Single Ended Zero

Table 3. Receiver Function ($\overline{OE}$ = H)

D+, D-	RCV	V_p/V_{po}	V_m/V_{mo}
Differential Logic 1	H	H	L
Differential Logic 0	L	L	H
SE0	X	L	L

Notes:

4. X = Don't Care
5. RCV(0) denotes the signal level on output RCV just prior to the SE0 or SE1 event. This level is stable during the SE0 or SE1 event period.

Power Supply Configurations and Options

The three modes of power supply operation are:

Normal Mode: Regulated Output and Regulator Bypass

1. Regulated Output: V_{CCIO} is connected and V_{CC}(5.0) is connected to 5V (4.0V to 5.5V) and the internal voltage regulator then produces 3.3V for the USB connections.
2. Internal Regulator Bypass Mode: V_{CCIO} is connected and both V_{CC}(5.0) and V_{REG}(3.3) are connected to a 3.3V source (3.0V to 3.6V).

In both cases, for normal mode, the V_{CCIO} is an independent voltage source (1.65V to 3.6V) that is a function of the external circuit configuration.

Sharing Mode: V_{CCIO} is only supply connected. V_{CC} and V_{REG} are not connected. In this mode, the D+ and D- terminals are 3-STATE and the USB1T1103 allows external signals up to 3.6V to share the D+ and D- bus lines. Internally the circuitry limits leakage from D+ and D- terminals (maximum 10µA) and V_{CCIO} such that device is in low power (suspended) state. Terminals Vbusmon and RCV are forced LOW as an indication of this mode with Vbusmon being ignored during this state.

Disable Mode: V_{CCIO} is not connected. V_{CC} is connected, or V_{CC} and V_{REG} are connected. 0V to 3.3V in this mode D+ and D- are 3-STATE and V_{PU} is HIGH Impedance (switch is turned off). The USB1T1103 allows external signals up to 3.6V to share the D+ and D- bus lines. Internally the circuitry limits leakage from D+ and D- pins (maximum 10µ A).

A summary of the Supply Configurations is described in Table 4.

Table 4. Power Supply Configuration Options

Terminals	Disable	Sharing	Normal (Regulated Output)	Normal (Regulator Bypass)
V_{CC} (5V)	Connected to 5V source	Not Connected or <3.6V	Connected to 5V Source	Connected to V_{REG} (3.3V) [Max Drop of 0.3V] (2.7V to 3.6V)
V_{REG} (3.3V)	3.3V, 300µA Regulated Output	Not Connected	3.3V, 300µA Regulated Output	Connected to 3.3V Source
V_{CCIO}	≤0.5V	1.65V to 3.6V Source	1.65V to 3.6V Source	1.65V to 3.6V Source
V_{PU} (3.3V)	3-STATE (off)	3-STATE (off)	3.3V Available if Config = HIGH	3.3V Available if Config = HIGH
D =, D-	3-STATE (off)	3-STATE	Function of Mode Set Up	Function of Mode Set Up
V_p/V_{po}, V_m/V_{mo}	Invalid [I]	L	Function of Mode Set Up	Function of Mode Set Up
RCV	Invalid [I]	L	Function of Mode Set Up	Function of Mode Set Up
Vbusmon	Invalid [I]	L	Function of Mode Set Up	Function of Mode Set Up
OE, SUSPND, Config	Hi-Z	Hi-Z	Function of Mode Set Up	Function of Mode Set Up

Notes:

6. Invalid [I] I/O are to be 3-STATE, outputs to be LOW.

ESD Protection

ESD Performance of the USB1T1103

- HBM D+/D-: 15.0kV
- HBM, all other terminals (Mil-Std 883E): 6.5kV

ESD Protection: D+/D- Terminals

Since the differential terminals of a USB transceiver may be subjected to extreme ESD voltages, additional immunity has been included in the D+ and D- terminals without compromising performance. The USB1T1103 differential terminals have ESD protection to the following limits:

- 15kV using the contact Human Body Model
- 8kV using the Contact Discharge method as specified in IEC 61000-4-2

Human Body Model

Figure 3 shows the schematic representation of the Human Body Model ESD event. Figure 4 is the ideal waveform representation of the Human Body Model.

IEC 61000-4-2, IEC 60749-26 and IEC 60749-27

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment and evaluates the equipment in its entirety for ESD immunity. Fairchild Semiconductor has evaluated this device using the IEC 6100-4-2 representative system model depicted in Figure 5. Under the additional standards set forth by the IEC, this device is also compliant with IEC 60749-26 (HBM) and IEC 60749-27 (MM).

Additional ESD Test Conditions

For additional information regarding our product test methodologies and performance levels, please contact Fairchild Semiconductor.

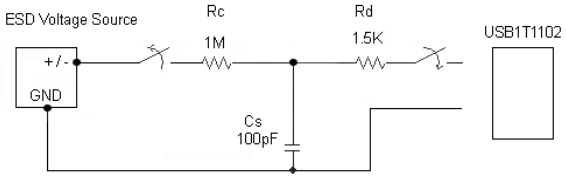


Figure 3. Human Body ESD Test Model

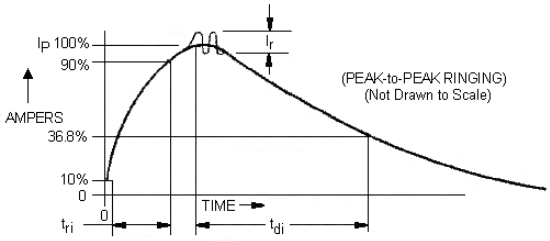


Figure 4. HBM Current Waveform

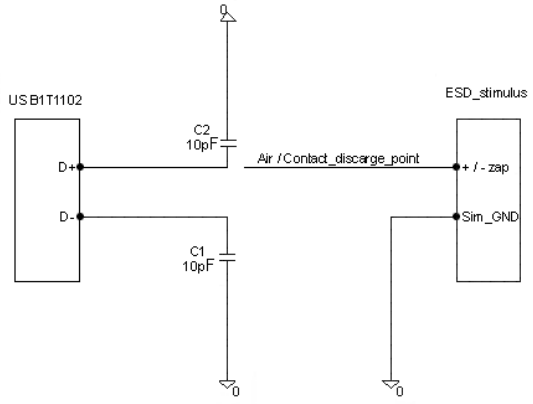


Figure 5. IEC 61000-4-2 ESD Test Model

Absolute Maximum Ratings

The “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The “Recommended Operating Conditions” table defines the conditions for actual device operation.

Symbol	Parameter	Min.	Max.	Unit
V_{CC} (5V)	Supply Voltage	-0.5	+6.0	V
V_{CCIO}	I/O Supply Voltage	-0.5	+4.6	V
I_{LU}	Latch-up Current, V_I = -1.8V to +5.4V		150	mA
I_{IK}	DC Input Current, V_I<0		-18	mA
V_I	DC Input Voltage(4)	-0.5	V_{CCIO} +0.5	V
I_{OK}	DC Output Diode Current, V_O >V_{CC} or V_O <0		±18	mA
V_O	DC Output Voltage(5)	-0.5	V_{CCIO}+0.5	V
I_O	Output Source or Sink Current, V_O + 0 to V_{CC}			
	Current for D+,D- Terminals		±12	mA
	Current for RCV, V_M/V_P		±12	mA
I_{CC},I_{GND}	DC V_{CC} or GND Current		±100	mA
V_{ESD}	ESD Immunity Voltage			
	Contact HBM			
	Terminals D+,D-, I_{LI} < 1µA		±15	kV
	All other Terminals I_{LI} < 1µA		±6.5	kV
T_{STG}	Storage Temperature	-40	+150	C
P_{TOT}	Power Dissipation			
	I_{CC} (5V)		48	mW
	I_{CCIO}		9	mW

Notes:

7. IO Absolute Maximumun Rating must be observed.
8. Per ESD Methodology described on page 6.

Recommended Operation Conditions

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	4.0	5.5	V
V_{CC10}	I/O DC Voltage	1.65	3.6	V
V_I	DC Input Voltage Range	0	V_{CCIO} +5.5	V
$V_{AI/O}$	DC Input Range for AI/O, Terminal D+ and D-	0	3.6	V
T_A	Operating Ambient Temperature	-40	+85	°C

DC Electrical Characteristics

Supply Terminals

Over recommended range of supply voltage and operating free air temperature (unless otherwise noted).
V_{CC} (5V) = 4.0V to 5.5V or V_{REG} (3.3V) = 3.0V to 3.6V, V_{CCIO} = 1.65V to 3.6V.

Symbol	Parameter	Conditions	Limits -40ºC to +85ºC			Units
			Min.	Typ.	Max.	
V_{REG} (3.3V)	Regulated Supply Output	Internal Regulator Option; $I_{LOAD} \leq 300$ µA	3.0(9)(10)	3.3	3.6	V
I_{CC}	Operating Supply Current (V_{CC}5.0)	Transmitting and Receiving at 12 Mbits/s; C_{LOAD} = 50 pF (D+, D-)		4.0(11)	8.0	mA
I_{CCIO}	I/O Operating Supply Current	Transmitting and Receiving at 12 Mbits/s		1.0(11)	2.0	mA
$I_{CC\ (IDLE)}$	Supply Current during FS IDLE and SE0 (V_{CC}5.0)	IDLE: $V_{D+} \leq 2.7V$, $V_{D-} \leq 0.3V$; SE0: $V_{D+} \leq 0.3V$, $V_{D-} \leq 0.3V$			300(12)	µA
$I_{CCIO\ (STATIC)}$	I/O Static Supply Current	IDLE, SUSPND or SE0			20.0	µA
$I_{CC(DISABLE)}$	Disable Supply Current	V_{CCIO} = 0V V_{CC} Connected			25.0	µA
$I_{CC(SUSPND)}$	Suspend Supply Current USB1T1103	SUSPND = HIGH $\overline{OE}$ = HIGH $V_m = V_p$ = OPEN			25.0(12)	µA
$I_{CCIO(SHARING)}$	I/O Sharing Mode Supply Current	V_{CC} (5V) Not Connected			20.0	µA
$I_{D+\ (SHARING)}$ $I_{D+/-}$	Sharing Mode Load Current on D+/D- Terminals	V_{CC} (5V) Not Connected Config = LOW; $V_{D\pm}$ = 3.6V			10.0	µA
$I_{D+(DISABLE)}$ $I_{D+/-}$	Disable Mode Load Current on D+/D- Terminals	V_{CCIO} Not Connected or 0V Config = $V_D \pm$ = 3.6V LOW or HIGH			10.0	µA
V_{CCTH}	V_{CC} Threshold Detection Voltage	$1.65V \leq V_{CCIO} \leq 3.6V$				V
		Supply Lost			3.6	
		Supply Present	4.1			
V_{CCHYS}	V_{CC} Threshold Detection Hysteresis Voltage	V_{CCIO} = 1.8V		70.0		mV
V_{CCIOTH}	V_{CCIO} Threshold Detection Voltage	$2.7V \leq V_{REG} \leq 3.6V$				V
		Supply Lost			0.5	
		Supply Present	1.4			
$V_{CCIOHYS}$	V_{CCIO} Threshold Detection Hysteresis Voltage	V_{REG} = 3.3V		450		mV
V_{REGTH}	Regulated Supply Threshold Detection Voltage	$1.65V \leq V_{CCIO} \leq V_{REG}$ $2.7V \leq V_{REG} \leq 3.6V$				V
		Supply Lost			0.8	
		Supply Present	2.4(14)			
V_{REGHYS}(15)	Regulated Supply Threshold Detection Hysteresis Voltage	V_{CCIO} = 1.8V		450		mV

Notes:

9. I_{LOAD} includes the pull-up resistor current via terminal V_{PU}
10. The minimum voltage in Suspend mode is 2.7V.
11. Not tested in production, value based on characterization.
12. Excludes any current from load and V_{PU} current to the 1.5kΩ resistor.
13. Includes current between V_{pu} and the 1.5k internal pull-up resistor.
14. When V_{CCIO} < 2.7V, minimum value for V_{REGTH} = 2.0V for supply present condition.
15. DC electrical measurements should be taken with unused inputs and I/O pins connected to a valid logic level. This applies for all modes of device operation defined in the Functional Tables on Page 4.

DC Electrical Characteristics

Digital Terminals – excludes D+, D- Terminals

Over recommended range of supply voltage and operating free air temperature (unless otherwise noted).

V_{CCIO} = 1.65V to 3.6V.

Symbol	Parameter	Conditions	Limits -40C° to +85°C		Units
			Min.	Max.	
Input Levels					
V_{IL}	LOW Level Input Voltage			0.3*V_{CCIO}	V
V_{IH}	HIGH Level Input Voltage		0.6*V_{CCIO}		V
Output Levels					
V_{OL}	LOW Level Output Voltage	I_{OL} = 2 mA		0.4	V
		I_{OL} = 100 =µA		0.15	
V_{OH}	HIGH Level Output Voltage	I_{OH} = 2 mA	V_{CCIO} - 0.4		V
		I_{OH} = 100 =µA	V_{CCIO}- 0.15		
Leakage Current					
I_{LI}	Input Leakage Current	V_{CCIO} = 1.65V to 3.6V		±1.0(16)	µA
Capacitance					
C_{IN}, $C_{I/O}$	Input Capacitance	Terminal to GND		10.0	pF

Notes:

16. If $V_{CCIO} \geq V_{REG,}$ leakage current is higher than specified.

DC Electrical Characteristics

Analog I/O Terminals – D+, D- Terminals

Over recommended range of supply voltage and operating free air temperature (unless otherwise noted).
V_{CC} = 4.0V to 5.5V or V_{REG} = 3.0V to 3.6V.

Symbol	Parameter	Conditions	Limits -40°C to +85°C			Units
			Min.	Typ.	Max.	
Input Levels – Differential Receiver						
V_{DI}	Differential Input Sensitivity	$\lvert V_{I(D+)} - V_{I(D-)} \rvert$	0.2			V
V_{CM}	Differential Common Mode Voltage		0.8		2.5	V
Input Levels – Single-ended Receiver						
V_{IL}	LOW Level Input Voltage				0.8	V
V_{IH}	HIGH Level Input Voltage		2.0			V
V_{HYS}	Hysteresis Voltage		0.30		0.7	V
Output Levels						
V_{OL}	LOW Level Output Voltage	R_L = 1.5kΩ to 3.6V			0.3	V
V_{OH}	HIGH Level Output Voltage(17)	R_L = 15kΩ to GND	2.8		3.6	V
Leakage Current						
I_{OFF}	Input Leakage Current Off State				±1.0	µA
	CAPACITANCE					
$C_{I/O}$	I/O Capacitance	Terminal to GND			20.0	pF
Resistance						

Symbol	Parameter	Conditions	Limits -40°C to +85°C			Units
			Min.	Typ.	Max.	
Z_{DRV}	Driver Output Impedance[18]		34.0	41.0	44.0	Ω
Z_{IN}	Driver Input Impedance		10.0			MΩ
R_{SW}	Switch Resistance				10.0	Ω
V_{TERM}	Termination Voltage[19][20]	R_{PU} Upstream Port	3.0		3.6	V

Notes:

17. If V_{OH} minimum = V_{REG} - 0.2V.
18. Includes external resistors of 27Ω on both D+ and D- terminals.
19. This voltage is available at terminal V_{PU} and V_{REG}.
20. Minimum voltage is 2.7V in the suspend mode.

AC Electrical Characteristics

A I/O Terminals Full Speed

Over recommended range of supply voltage and operating free air temperature (unless otherwise noted).
V_{CC} = 4.0V to 5.5V or V_{REG} = 3.0V to 3.6V, V_{CCIO} = 1.65V to 3.6V, C_L = 50 pF; R_L = 1.5K on D+ to V_{PU}.

Symbol	Parameter	Conditions	Limits -40°C to +85°C			Unit
			Min.	Typ.	Max.	
Driver Characteristics						
t_R	Output Rise Time	C_L = 50 - 125 pF 10% to 90%	4.0		20.0	ns
t_F	Output Fall Time	Figure 8, 12	4.0		20.0	
t_{RFM}	Rise/Fall Time Match	t_F/ t_R Excludes First Transition from Idle State	90.0		111.1	%
V_{CRS}	Output Signal Crossover Voltage [21]	Excludes First Transition from Idle State see Waveform	1.3		2.0	V
Driver Timing						
t_{PLH} t_{PHL}	Propagation Delay (V_p/V_{po}, V_m/V_{mo} to D+/D-)	Figures 9,12			18.0	ns
t_{PHZ} t_{PLZ}	Driver Disable Delay ($\overline{OE}$ to D+/D-)	Figures 11,12			15.0	ns
t_{PZH} t_{PZL}	Driver Enable Delay ($\overline{OE}$ to D+/D-)	Figures 11,13			15.0	ns
Receiver Timing						
t_{PLH} t_{PHL}	Propagation Delay (Diff) (D+/D- to Rev)	Figures 10,14			15.0	ns
t_{PLH} t_{PHL}	Single-Ended Receiver Propagation Delay (D+/D- to V_p/ V_{po}, V_m/V_{mo})	Figures 10,14			18.0	ns

NOTES:

21. Not production tested; limits guaranteed by design.

Typical Application Configurations

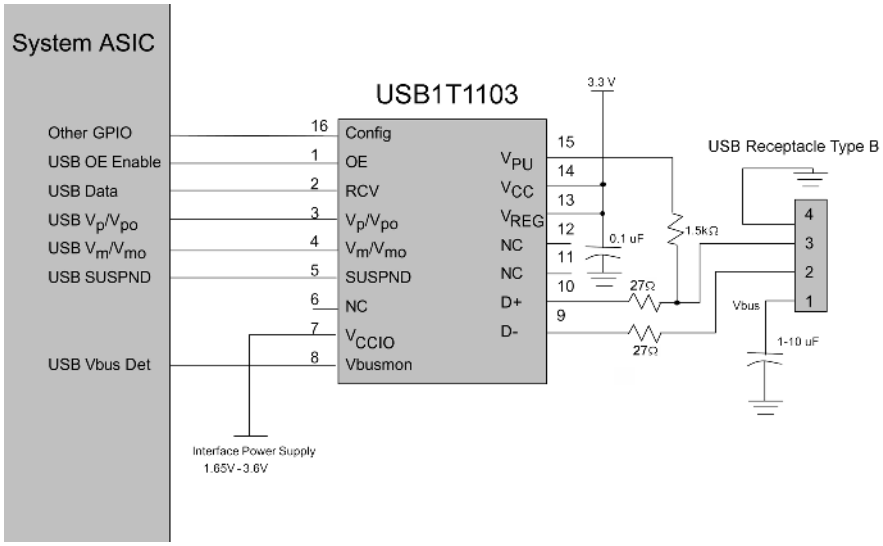


Figure 6. Upstream Connection in Bypass Mode with Differential Outputs

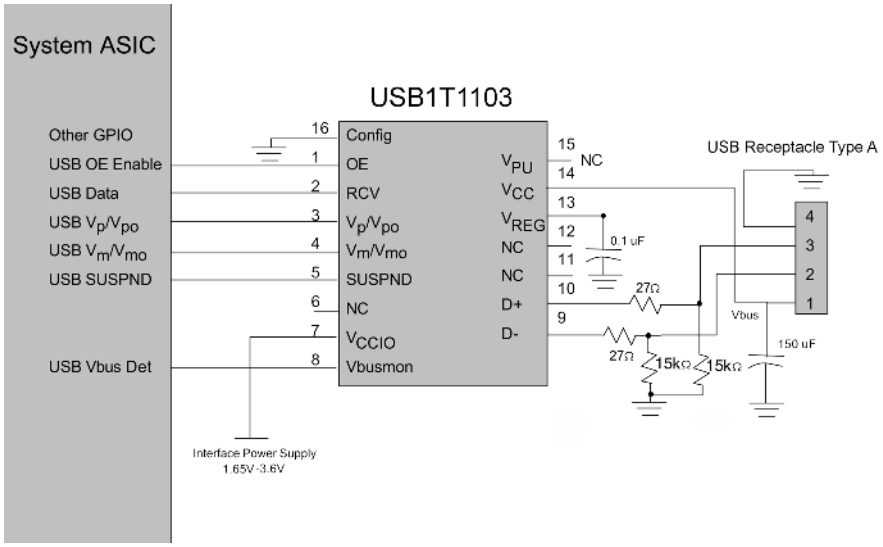


Figure 7. Downstream Connection in Normal Mode with Differential Outputs

AC Waveforms

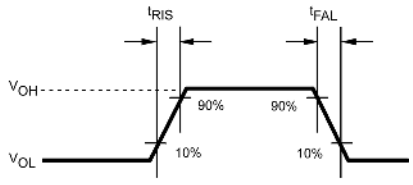


Figure 8. Rise and Fall Times

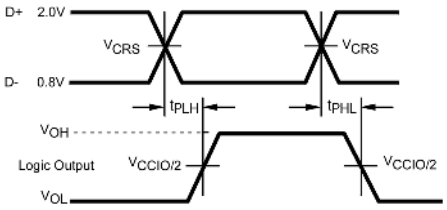


Figure 10. D+/D- to R_{CV}, V_{po}/V_p and V_{mo}/V_m

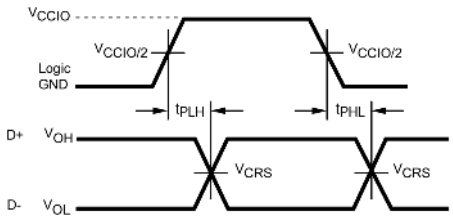


Figure 9. V_{po}, V_{mo} to D+/D-

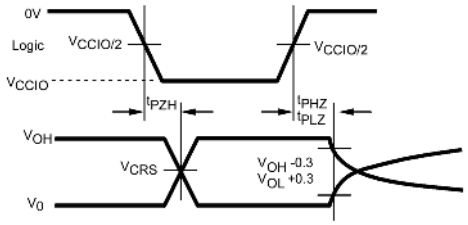
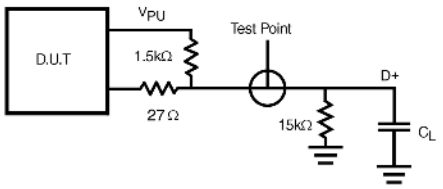


Figure 11. $\overline{OE}$ to D+/D-

Test Circuits and Waveforms



C_L = 50 pF Full Speed Propagation Delays

C_L = -125 pF Edge Rates only

Figure 12. Load for D+/D-

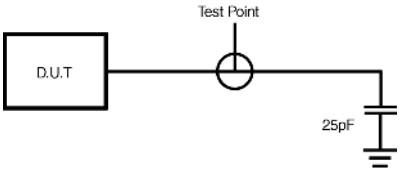
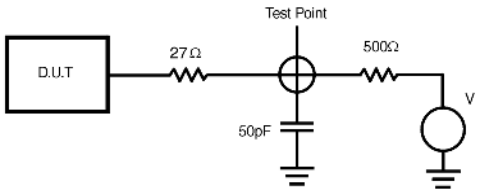


Figure 14. Load for V_m/V_{mo}, V_p/V_{po} and RCV



V = 0 for t_{PZH}, t_{PHZ}

V = V_{REG} for t_{PZL}

Figure 13. Load for Enable and Disable Times

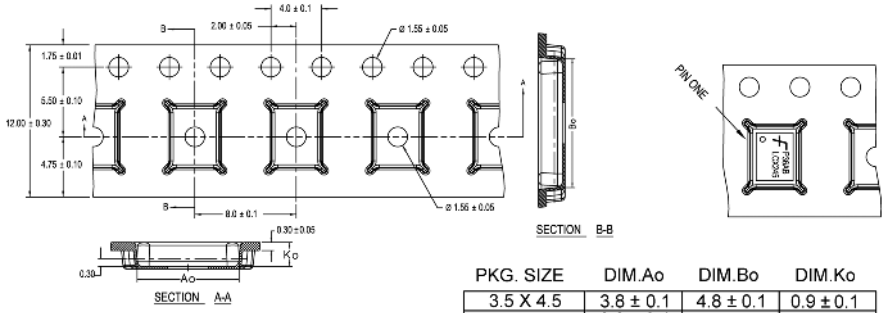
Tape and Reel Specification

Tape Format for MHBCC and MLP

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
MHX/MPX	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	2500/3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

TAPE DIMENSIONS

Dimensions are in inches (millimeters) unless otherwise specified.



PKG. SIZE	DIM.Ao	DIM.Bo	DIM.Ko
3.5 X 4.5	3.8 ± 0.1	4.8 ± 0.1	0.9 ± 0.1
3.0 X 3.0	3.3 ± 0.1	3.3 ± 0.1	0.9 ± 0.1
2.5 X 4.5	2.8 ± 0.1	4.8 ± 0.1	0.9 ± 0.1
2.5 X 3.5	2.8 ± 0.1	3.8 ± 0.1	0.9 ± 0.1
2.5 X 3.0	2.8 ± 0.1	3.3 ± 0.1	0.9 ± 0.1
2.5 X 2.5	2.8 ± 0.1	2.8 ± 0.1	0.9 ± 0.1

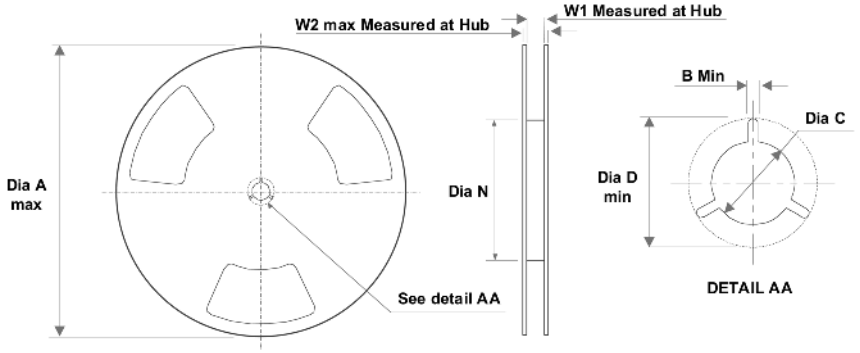
DIMENSIONS ARE IN MILLIMETERS

NOTES: unless otherwise specified

1. Cummulative pitch for feeding holes and cavities (chip pockets) not to exceed 0.008[0.20] over 10 pitch span.
2. Smallest allowable bending radius.
3. Thru hole inside cavity is centered within cavity.
4. Tolerance is ±0.002[0.05] for these dimensions on all 12mm tapes.
5. Ao and Bo measured on a plane 0.120[0.30] above the bottom of the pocket.
6. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
7. Pocket position relative to sprocket hole measured as true position of pocket. Not pocket hole.
8. Controlling dimension is millimeter. Diemension in inches rounded.

REEL DIMENSIONS

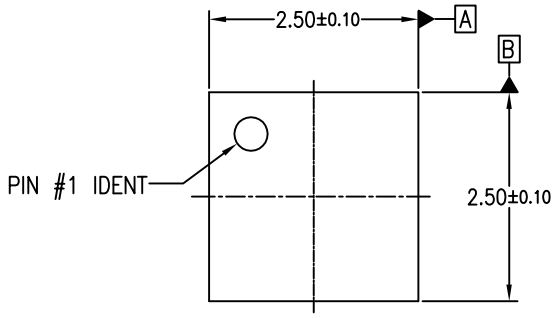
Dimensions are in inches (millimeters) unless otherwise specified.



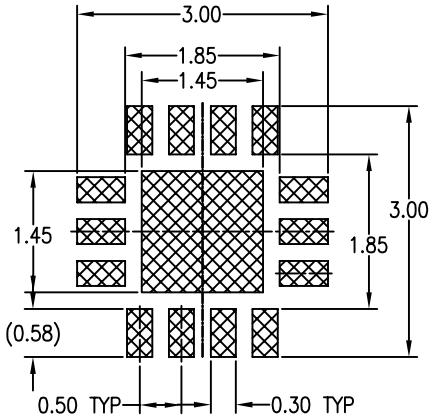
Tape Size	A	B	C	D	N	W1	W2
12 mm	13.0	0.059	0.512	0.795	7.008	0.488	0.724
	330	(1.50)	(13.00)	(20.20)	(178)	(12.4)	(18.4)

REVISIONS

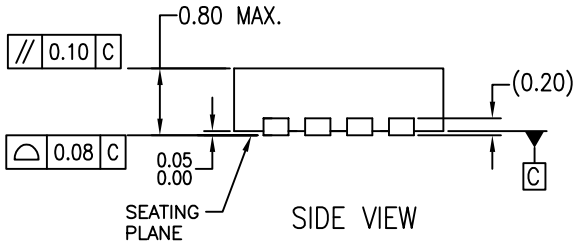
LTR	DESCRIPTION	EDCN	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL		25-2-2004	FEITAN



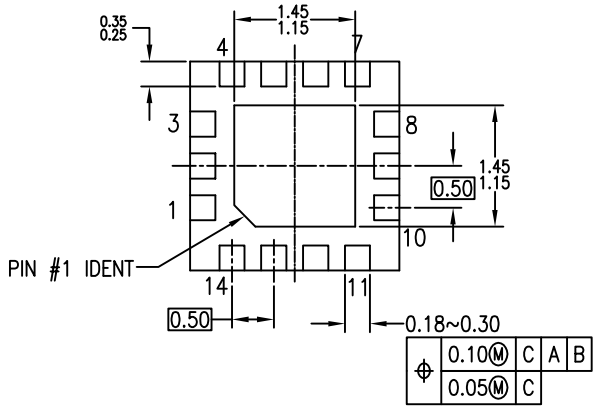
TOP VIEW



RECOMMENDED LAND PATTERN



SIDE VIEW



BOTTOM VIEW

NOTES:

A. NO JEDEC REGISTRATION
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

APPROVALS	DATE
DRAWN FEITAN	09-02-2004
DFTG. CHK.	
ENGR. CHK.	

FAIRCHILD SEMICONDUCTOR® Bayan Lepas, FIZ, 11900, Penang, Malaysia.

14LD, MLP, 2.5MM SQUARE

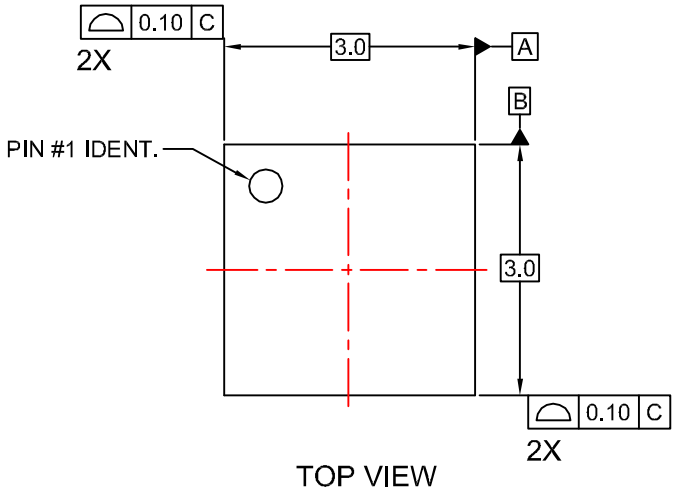
PROJECTION INCH [MM]

SCALE	SIZE	DRAWING NUMBER	REV
N/A	N/A	MKT-MLP14D	A

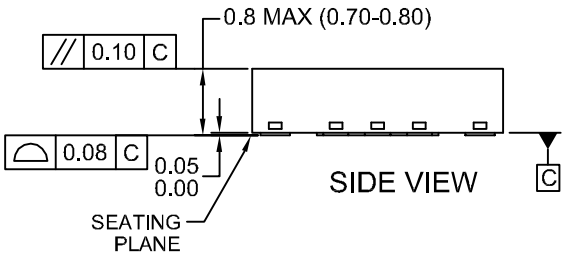
DO NOT SCALE DRAWING | SHEET 1 of 1

MLP14DrevA

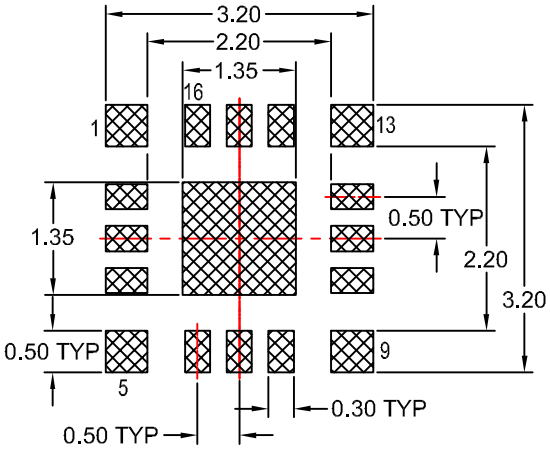
REVISIONS			
NBR	DESCRIPTION	DATE	DRAWN/SITE
A	RELEASE TO DOCUMENT CONTROL	14-11-2003	FEITAN
2	UPDATED DRAWING AND ADDED NON ASME TOLERANCE REFERENCE VALUES FOR BODY DIMS.	12-3-2008	L. England
3	Fixed min package thickness typo in side view.	4-29-2009	L. England
4	Removed extra squares on Bottom View.	7-6-2009	L. England



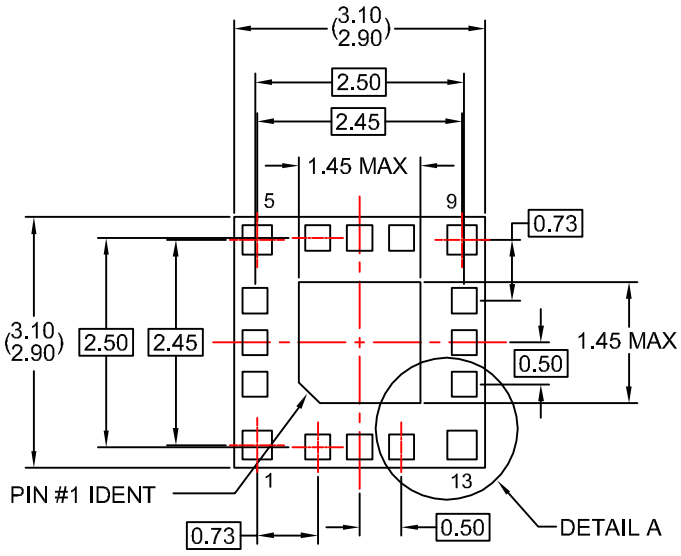
TOP VIEW



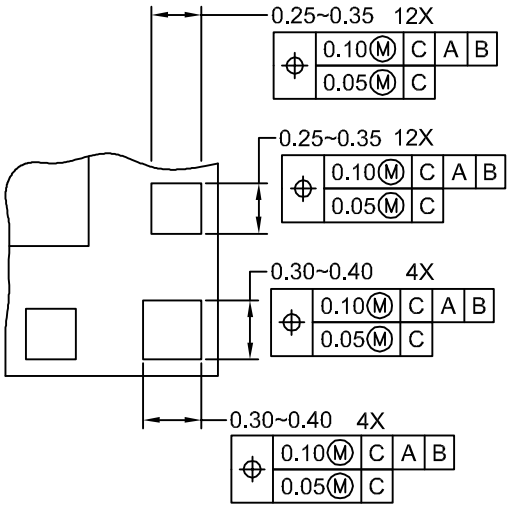
SIDE VIEW



RECOMMENDED LAND PATTERN



BOTTOM VIEW



DETAIL A

NOTES:

A. SIMILAR TO JEDEC REGISTRATION MO-217,
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994
D. LANDPATTERN RECOMMENDATION IS PER FSC INTERNAL DESIGN
E. DRAWING FILENAME: MLP16HBrev4

APPROVALS	DATE
DRAWN L. England	7-6-2009
DFTG. CHK. S. Martin	7-6-2009
ENGR. CHK.	

FAIRCHILD SEMICONDUCTOR®

16LD, MLP, JEDEC MO-217 EQUIVALENT, 3MM SQUARE

PROJECTION INCH [MM]

SCALE	SIZE	DRAWING NUMBER	REV
N/A	N/A	MKT-MLP16HB	4

DO NOT SCALE DRAWING | SHEET 1 of 1

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