TEXAS INSTRUMENTS

SN74VMEH22501A-EP

SCES625A – FEBRUARY 2005 – REVISED NOVEMBER 2015

SN74VMEH22501A-EP 8-Bit Universal Bus Transceiver and Two 1-Bit Bus Transceivers With Split LVTTL Port, Feedback Path, and 3-State Outputs

1 Features

- Controlled Baseline
  - One Assembly/Test Site, One Fabrication Site
- Enhanced Diminishing Manufacturing Sources (DMS) Support
- Enhanced Product-Change Notification
- Qualification Pedigree(1)
- Member of the Texas Instruments Widebus™ Family
- UBT™ Transceiver Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Modes
- OEC™ Circuitry Improves Signal Integrity and Reduces Electromagnetic Interference (EMI)
- Compliant With VME64, 2eVME, and 2eSST Protocols Validated at T_A = –40°C to 85°C
- Bus Transceiver Split LVTTL Port Provides a Feedback Path for Control and Diagnostics Monitoring
- I/O Interfaces are 5-V Tolerant
- B-Port Outputs (–48 mA/64 mA)
- Y and A-Port Outputs (–12 mA/12 mA)
- I_{off}, Power-Up 3-State, and BIAS V_{CC} Support Live Insertion
- Bus Hold on 3A-Port Data Inputs
- 26-Ω Equivalent Series Resistor on 3A Ports and Y Outputs
- Flow-Through Architecture Facilitates Printed Circuit Board Layout
- Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

2 Applications

- Industrial Controls
- Telecommunications
- Instrumentation Systems

3 Description

The SN74VMEH22501A-EP 8-bit universal bus transceiver has two integral 1-bit three-wire bus transceivers and is designed for 3.3-V V_{CC} operation with 5-V tolerant inputs. The UBT transceiver allows transparent, latched, and flip-flop modes of data transfer, and the separate LVTTL input and outputs on the bus transceivers provide a feedback path for control and diagnostics monitoring. This device provides a high-speed interface between cards operating at LVTTL logic levels and VME64, VME64x, or VME320(2) backplane topologies.

Device Information(3)

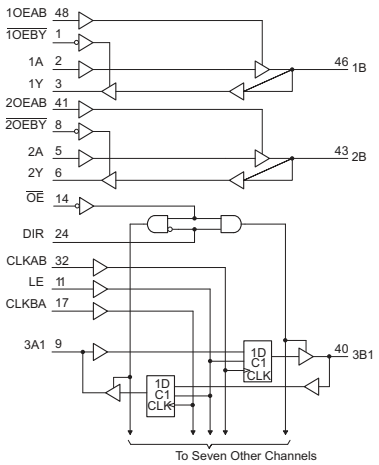
PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74VMEH22501A-EP	TSSOP (48)	4.40 mm × 9.70 mm
	TVSOP (48)	6.10 mm × 12.50 mm

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

(2) VME320 is a patented backplane construction by Arizona Digital, Inc.

(3) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic)



Pin numbers shown for DGG and DGV

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (February 2005) to Revision A	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Removed *Ordering Information* table.	1
• Added junction temperature and removed package thermal impedance from *Absolute Maximum Ratings*	6
• Added different conditions and results for I and M versions to the *Specifications*	7
• Updated the V_{CC} test condition for $I_{OZ(PU/PD)}$	8
• Added *Community Resources*	32

5 Description (continued)

The SN74VMEH22501A-EP device is pin-for-pin compatible to the SN74VMEH22501 device (SCES357), but operates at a wider operating temperature range.

High-speed backplane operation is a direct result of the improved OEC circuitry and high drive that has been designed and tested into the VME64x backplane model. The B-port I/Os are optimized for driving large capacitive loads and include pseudo-ETL input thresholds (½ V_{CC} ±50 mV) for increased noise immunity. These specifications support the 2eVME protocols in VME64x (ANSI/VITA 1.1) and 2eSST protocols in VITA 1.5.

With proper design of a 21-slot VME system, a designer can achieve 320-MB transfer rates on linear backplanes and, possibly, 1-GB transfer rates on the VME320 backplane.

All inputs and outputs are 5-V tolerant and are compatible with TTL and 5-V CMOS inputs.

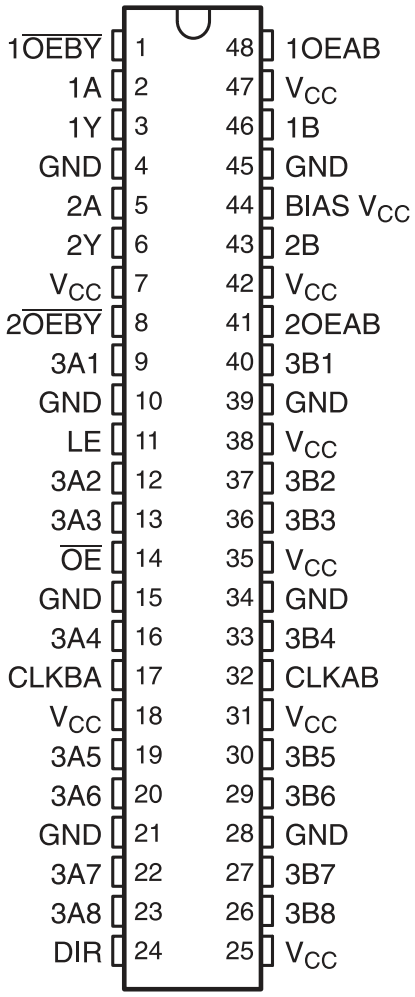
Active bus-hold circuitry holds unused or undriven 3A-port inputs at a valid logic state. Bus-hold circuitry is not provided on 1A or 2A inputs, any B-port input, or any control input. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

This device is fully specified for live-insertion applications using I_{off}, power-up 3-state, and BIAS V_{CC}. The I_{off} circuitry prevents damaging current to backflow through the device when it is powered off/on. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict. The BIAS V_{CC} circuitry precharges and preconditions the B-port input/output connections, preventing disturbance of active data on the backplane during card insertion or removal, and permits true live-insertion capability.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, output-enable ($\overline{OE}$ and $\overline{OEBY}$) inputs should be tied to V_{CC} through a pullup resistor and output-enable (OEAB) inputs should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the drive capability of the device connected to this input.

6 Pin Configuration and Functions

DGG or DGV Package
48-Pin TSSOP or TVSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
1$\overline{OEBY}$	1	I	Active low control output for 1Y bus
1A	2	I	Data in to 1B
1Y	3	O	Data out
GND	4	—	Ground
2A	5	I	Data in to 2B
2Y	6	O	Data out
VCC	7	I	Power supply input for internal circuits
2$\overline{OEBY}$	8	I	Active low control output for 2Y bus
3A1	9	I/O	Data in/out
GND	10	—	Ground
LE	11	I	Latch Enable pin for UBT
3A2	12	I/O	Data in/out

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
3A3	13	I/O	Data in/out
$\overline{OE}$	14	I	Active low enable pin for UBT
GND	15	—	Ground
3A4	16	I/O	Data in/out
CLKBA	17	I	Clock for 3B data to 3A bus
VCC	18	I	Power supply input for internal circuits
3A5	19	I/O	Data in/out
3A6	20	I/O	Data in/out
GND	21	—	Ground
3A6	22	I/O	Data in/out
3A8	23	I/O	Data in/out
DIR	24	—	Direction control for UBT
VCC	25	I	Power supply input for internal circuits
3B8	26	I/O	Data in/out
3B7	27	I/O	Data in/out
GND	28	—	Ground
3B6	29	I/O	Data in/out
3B5	30	I/O	Data in/out
VCC	31	I	Power supply input for internal circuits
CLKAB	32	I	Clock for 3A data to 3B bus
3B4	33	I/O	Data in/out
GND	34	—	Ground
VCC	35	I	Power supply input for internal circuits
3B3	36	I/O	Data in/out
3B2	37	I/O	Data in/out
VCC	38	I	Power supply input for internal circuits
GND	39	—	Ground
3B1	40	I/O	Data in/out
2OEAB	41	I	Active high control output for 2B bus
VCC	42	I	Power supply input for internal circuits
2B	43	I/O	Data in/out
BIAS VCC	44	I	Power supply input for internal circuits
GND	45	—	Ground
1B	46	I/O	Data in/out
VCC	47	I	Power supply input for internal circuits
1OEAB	48	I	Active high control output for 1B bus

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{CC}, BIAS V_{CC}	Supply voltage		–0.5	4.6	V
V_I	Input voltage (2)		–0.5	7	V
V_O	Voltage applied to any output in the high-impedance or power-off state (2)		–0.5	7	V
V_O	Voltage applied to any output in the high or low state (2)	3A port or Y output	–0.5	V_{CC} + 0.5	V
		B port	–0.5	4.6	
I_O	Output current in the low state	3A port or Y output		50	mA
		B port		100	
I_O	Output current in the high state	3A port or Y output		–50	mA
		B port		–100	
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0 or V_O > V_{CC}, B port		–50	mA
T_J	Junction temperature		–55	150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

see (1)(2)

			MIN	NOM	MAX	UNIT
V_{CC}, BIAS V_{CC}	Supply voltage		3.15	3.3	3.45	V
V_I	Input voltage	Control inputs or A port		V_{CC}	5.5	V
		B port		V_{CC}	5.5	
V_{IH}	High-level input voltage	Control inputs or A port	2			V
		B port	0.5 V_{CC} + 50 mV			
V_{IL}	Low-level input voltage	Control inputs or A port			0.8	V
		B port			0.5 V_{CC} – 50 mV	
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current	3A port and Y output			–12	mA
		B port			–48	
I_{OL}	Low-level output current	3A port and Y output			12	mA
		B port			64	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		20			µs/V
T_A	Operating ambient temperature	I version	–40		85	°C
		M version	–55		125	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

(2) Proper connection sequence for use of the B-port I/O precharge feature is GND and BIAS V_{CC} = 3.3 V first, I/O second, and V_{CC} = 3.3 V last, because the BIAS V_{CC} precharge circuitry is disabled when any V_{CC} pin is connected. The control inputs can be connected at any time, but normally are connected during the I/O stage. If B-port precharge is not required, any connection sequence is acceptable, but generally, GND is connected first.

7.4 Thermal Information

THERMAL METRIC(1)		SN74VMEH22501A-EP		UNIT
		DGV (TVSOP)	DGG (TSSOP)	
		48 PINS	48 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance, JEDEC 4-layer high-K board	73.9	62.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.1	15.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	37.3	30.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.9	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	36.8	29.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

over recommended operating free-air temperature range for A and B ports (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IK}		V_{CC} = 3.15 V	I_I = –18 mA			–1.2	V
V_{OH}	3A port, any B ports, and Y outputs	V_{CC} = 3.15 V to 3.45 V	I_{OH} = –100 µA	V_{CC} – 0.2			V
	3A port and Y outputs	V_{CC} = 3.15 V	I_{OH} = –6 mA	2.4			
			I_{OH} = –12 mA	2			
	Any B port	V_{CC} = 3.15 V	I_{OH} = –24 mA	2.4			
			I_{OH} = –48 mA	2			
V_{OL}	3A port, any B ports, and Y outputs	V_{CC} = 3.15 V to 3.45 V	I_{OL} = 100 µA			0.2	V
	3A port and Y outputs	V_{CC} = 3.15 V	I_{OL} = 6 mA			0.55	
			I_{OL} = 12 mA; I version; T_A = –40 to 85°C			0.8	
			I_{OL} = 12 mA; M version; T_A = –55 to 125°C			0.84	
	Any B port	V_{CC} = 3.15 V	I_{OL} = 24 mA			0.4	
			I_{OL} = 48 mA			0.55	
			I_{OL} = 64 mA; I version			0.6	
			I_{OL} = 64 mA; M version			0.7	
I_I	Control inputs, 1A and 2A	V_{CC} = 3.45 V	V_I = V_{CC} or GND			±1	µA
		V_{CC} = 0 or 3.45 V	V_I = 5.5 V			5	
I VERSION							
I_{OZH}(2)	3A port, any B port, and Y outputs	V_{CC} = 3.45 V; T_A = –40°C to 85°C	V_O = V_{CC} or 5.5 V			5	µA
I_{OZL}(2)	3A port and Y outputs	V_{CC} = 3.45 V; T_A = –40°C to 85°C	V_O = GND			–5	µA
	Any B port	V_{CC} = 3.45 V; T_A = –40°C to 85°C	V_O = GND			–20	
M VERSION							
I_{OZH}(2)	3A port, any B port, and Y outputs	V_{CC} = 3.45 V; T_A = –55°C to 125°C	V_O = V_{CC} or 5.5 V			15	µA
I_{OZL}(2)	3A port and Y outputs	V_{CC} = 3.45 V; T_A = –55°C to 125°C	V_O = GND			–8	µA
	Any B port	V_{CC} = 3.45 V; T_A = –55°C to 125°C	V_O = GND			–35	
GENERAL PARAMETERS							
I_{off}		V_{CC} = 0, BIAS V_{CC} = 0	V_I or V_O = 0 to 5.5 V			±10	µA
I_{BHL}(3)	3A port	V_{CC} = 3.15 V	V_I = 0.8 V	75			µA
I_{BHH}(4)	3A port	V_{CC} = 3.15 V	V_I = 2 V	–75			µA
I_{BHLO}(5)	3A port	V_{CC} = 3.45 V	V_I = 0 to V_{CC}	500			µA
I_{BHHO}(6)	3A port	V_{CC} = 3.45 V	V_I = 0 to V_{CC}	–500			µA
$I_{OZ(PU/PD)}$(7)		V_{CC} ≤ 1.3 V, V_O = 0.5 V to V_{CC}, V_I = GND or V_{CC}, $\overline{OE}$ = Don't care				±10	µA
I_{CC}		V_{CC} = 3.45 V, I_O = 0, V_I = V_{CC} or GND	Outputs high			30	mA
			Outputs low			30	
			Outputs disabled			30	

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
(2) For I/O ports, the parameters I_{OZH} and I_{OZL} include the input leakage current.
(3) The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering V_{IN} to GND, then raising it to V_{IL} max.
(4) The bus-hold circuit can source at least the minimum high sustaining current at V_{IH} min. I_{BHH} should be measured after raising V_{IN} to V_{CC}, then lowering it to V_{IH} min.
(5) An external driver must source at least I_{BHLO} to switch this node from low to high.
(6) An external driver must sink at least I_{BHHO} to switch this node from high to low.
(7) High-impedance state during power up or power down

Electrical Characteristics (continued)

over recommended operating free-air temperature range for A and B ports (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
I_{CCD}		V_{CC} = 3.45 V, I_O = 0, V_I = V_{CC} or GND, One data input switching at one-half clock frequency, 50% duty cycle	Outputs enabled		76		µA/ clock MHz/ input
			Outputs disabled		19		
ΔI_{CC}(8)		V_{CC} = 3.15 V to 3.45 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND				750	µA
C_i	1A and 2A inputs	V_I = 3.15 V or 0			2.8		pF
	Control inputs				2.6		
C_o	1Y or 2Y outputs	V_O = 3.15 V or 0			5.6		pF
C_{io}	3A port	V_{CC} = 3.3 V	V_O = 3.3 V or 0		7.9		pF
	Any B port				11	12.5	

(8) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

7.6 Live-Insertion Specifications

over recommended operating free-air temperature range for B port

PARAMETER	TEST CONDITIONS			MIN	TYP(1)	MAX	UNIT
I_{CC} (BIAS V_{CC})	V_{CC} = 0 to 3.15 V,	BIAS V_{CC} = 3.15 V to 3.45 V,	$I_{O(DC)}$ = 0			5	mA
	V_{CC} = 3.15 V to 3.45 V(2),	BIAS V_{CC} = 3.15 V to 3.45 V,	$I_{O(DC)}$ = 0			10	µA
V_O	V_{CC} = 0,	BIAS V_{CC} = 3.15 V to 3.45 V		1.3	1.5	1.7	V
I_O	V_{CC} = 0	V_O = 0,	BIAS V_{CC} = 3.15 V	–20		–100	µA
		V_O = 3 V,	BIAS V_{CC} = 3.15 V	20		100	

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C
(2) V_{CC} – 0.5 V < BIAS V_{CC}

7.7 Timing Requirements for UBT Transceiver (I Version)

over recommended operating conditions (unless otherwise noted) (see Figure 7 and Figure 8); T_A = –40°C to 85°C

				MIN	MAX	UNIT
f_{clock}	Clock frequency				120	MHz
t_w	Pulse duration	LE high		2.5		ns
		CLK high or low		3		
t_{su}	Setup time	3A before CLK↑	Data high	2.1		ns
			Data low	2.2		
		3A before LE↓	CLK high	2		
			CLK low	2		
		3B before CLK↑	Data high	2.5		
			Data low	2.7		
		3B before LE↓	CLK high	2		
			CLK low	2		
t_h	Hold time	3A after CLK↑	Data high	0		ns
			Data low	0		
		3A after LE↓	CLK high	1		
			CLK low	1		
		3B after CLK↑	Data high	0		
			Data low	0		
		3B after LE↓	CLK high	1		
			CLK low	1		

7.8 Switching Characteristics for Bus Transceiver Function (I Version)

over recommended operating conditions (unless otherwise noted) (see Figure 7 and Figure 8); T_A = –40°C to 85°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	UNIT
t_{PLH}	1A or 2A	1B or 2B	4.5		9.2	ns
t_{PHL}			4.2		7.8	
t_{PLH}	1A or 2A	1Y or 2Y	6.2		14.5	ns
t_{PHL}			6.1		13	
t_{PZH}	OEAB	1B or 2B	3.6		8.1	ns
t_{PZL}			3.4		7.8	
t_{PHZ}	OEAB	1B or 2B	3.3		9.7	ns
t_{PLZ}			1.8		4.8	
t_r	Transition time, B port (10%–90%)			4.3		ns
t_f	Transition time, B port (90%–10%)			4.3		ns
t_{PLH}	1B or 2B	1Y or 2Y	1.6		5.6	ns
t_{PHL}			1.6		5.6	
t_{PZH}	$\overline{OEBY}$	1Y or 2Y	1.2		5.6	ns
t_{PZL}			1.8		4.9	
t_{PHZ}	$\overline{OEBY}$	1Y or 2Y	0.9		5.4	ns
t_{PLZ}			1.4		4.5	

7.9 Switching Characteristics for Bus Transceiver Function (M Version)

over recommended operating conditions (unless otherwise noted) (see Figure 7 and Figure 8); T_A = –55°C to 125°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	UNIT
t_{PLH}	1A or 2A	1B or 2B	4.5		10.8	ns
t_{PHL}			4.2		10.6	
t_{PLH}	1A or 2A	1Y or 2Y	6.2		15.7	ns
t_{PHL}			6.1		15.7	
t_{PZH}	OEAB	1B or 2B	3.6		9.8	ns
t_{PZL}			2.8		8.7	
t_{PHZ}	OEAB	1B or 2B	3.3		9.7	ns
t_{PLZ}			1.8		5.6	
t_r	Transition time, B port (10%–90%)			4.3		ns
t_f	Transition time, B port (90%–10%)			4.3		ns
t_{PLH}	1B or 2B	1Y or 2Y	1.6		6.8	ns
t_{PHL}			1.6		6.7	
t_{PZH}	$\overline{OEBY}$	1Y or 2Y	1.2		6.9	ns
t_{PZL}			1.8		6.6	
t_{PHZ}	$\overline{OEBY}$	1Y or 2Y	0.9		6.8	ns
t_{PLZ}			1.4		5.4	

7.10 Switching Characteristics for UBT Transceiver (I Version)

over recommended operating conditions (unless otherwise noted) (see Figure 7 and Figure 8); T_A = –40°C to 85°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	UNIT
f_{max}			120			MHz
t_{PLH}	3A	3B	4.8		9.5	ns
t_{PHL}			4.5		8.3	
t_{PLH}	LE	3B	5.2		10.6	ns
t_{PHL}			4.7		8.7	
t_{PLH}	CLKAB	3B	5.4		10.5	ns
t_{PHL}			4.2		8.4	
t_{PZH}	$\overline{OE}$	3B	4.2		9.3	ns
t_{PZL}			2.8		8.5	
t_{PHZ}	$\overline{OE}$	3B	4.2		9.3	ns
t_{PLZ}			2.4		5.7	
t_r	Transition time, B port (10%–90%)			4.3		ns
t_f	Transition time, B port (90%–10%)			4.3		ns
t_{PLH}	3B	3A	1.5		5.9	ns
t_{PHL}			1.7		5.9	
t_{PLH}	LE	3A	1.7		5.9	ns
t_{PHL}			1.7		5.9	
t_{PLH}	CLKBA	3A	1.1		5.5	ns
t_{PHL}			1.4		5.5	
t_{PZH}	$\overline{OE}$	3A	1.5		6.2	ns
t_{PZL}			2.1		5.5	
t_{PHZ}	$\overline{OE}$	3A	0.8		6.2	ns
t_{PLZ}			2.3		5.6	

7.11 Switching Characteristics for UBT Transceiver (M Version)

over recommended operating conditions (unless otherwise noted) (see Figure 7 and Figure 8); T_A = –55°C to 125°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	UNIT
f_{max}			120			MHz
t_{PLH}	3A	3B	4.8		11.5	ns
t_{PHL}			4.5		11.8	
t_{PLH}	LE	3B	5.2		12.9	ns
t_{PHL}			4.7		11.6	
t_{PLH}	CLKAB	3B	5.4		13.8	ns
t_{PHL}			4.2		11.9	
t_{PZH}	$\overline{OE}$	3B	4.2		11.9	ns
t_{PZL}			2.8		10.7	
t_{PHZ}	$\overline{OE}$	3B	4.2		11.9	ns
t_{PLZ}			2.4		9.1	
t_r	Transition time, B port (10%–90%)			4.3		ns
t_f	Transition time, B port (90%–10%)			4.3		ns
t_{PLH}	3B	3A	1.5		7.6	ns
t_{PHL}			1.7		7.9	
t_{PLH}	LE	3A	1.7		7.9	ns
t_{PHL}			1.7		7.9	
t_{PLH}	CLKBA	3A	1.1		5.7	ns
t_{PHL}			1.4		6.4	
t_{PZH}	$\overline{OE}$	3A	1.5		7.9	ns
t_{PZL}			2.1		7.5	
t_{PHZ}	$\overline{OE}$	3A	0.8		10.5	ns
t_{PLZ}			2.3		6.9	

7.12 Switching Characteristics for Bus Transceiver Function (I Version)

driver in slot 11, with receiver cards in all other slots (full load); over recommended operating conditions (unless otherwise noted) (see Figure 6); T_A = –40°C to 85°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP(1)	MAX	UNIT
t_{PLH}	1A or 2A	1B or 2B	5.9		8.5	ns
t_{PHL}			5.5		8.7	
t_r(2)	Transition time, B port (10%–90%)		9	8.6	11.4	ns
t_f(2)	Transition time, B port (90%–10%)		8.9	9	10.8	ns

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C. All values are derived from TI-SPICE models.
(2) All t_r and t_f times are taken at the first receiver.

7.13 Switching Characteristics for UBT (I Version)

driver in slot 11, with receiver cards in all other slots (full load); over recommended operating conditions (unless otherwise noted) (see Figure 6); T_A = –40°C to 85°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP(1)	MAX	UNIT
t_{PLH}	3A	3B	6.2		8.9	ns
t_{PHL}			5.6		9	
t_{PLH}	LE	3B	6.1		9.1	ns
t_{PHL}			5.6		9	
t_{PLH}	CLKAB	3B	6.2		9.1	ns
t_{PHL}			5.7		9	
t_r(2)	Transition time, B port (10%–90%)		9	8.6	11.4	ns
t_f(2)	Transition time, B port (90%–10%)		8.9	9	10.8	ns

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C. All values are derived from TI-SPICE models.
(2) All t_r and t_f times are taken at the first receiver.

7.14 Switching Characteristics for Bus Transceiver Function (I Version)

driver in slot 1, with one receiver in slot 21 (minimum load); over recommended operating conditions (unless otherwise noted) (see Figure 6); T_A = –40°C to 85°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP(1)	MAX	UNIT
t_{PLH}	1A or 2A	1B or 2B	5.5		7.4	ns
t_{PHL}			5.3		7.4	
t_r(2)	Transition time, B port (10%–90%)		3.9	3.4	4.4	ns
t_f(2)	Transition time, B port (90%–10%)		3.7	3.4	4.8	ns

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C. All values are derived from TI-SPICE models.
(2) All t_r and t_f times are taken at the first receiver.

7.15 Switching Characteristics for UBT (I Version)

driver in slot 1, with one receiver in slot 21 (minimum load); over recommended operating conditions (unless otherwise noted) (see Figure 6); T_A = –40°C to 85°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP(1)	MAX	UNIT
t_{PLH}	3A	3B	5.8		7.9	ns
t_{PHL}			5.5		7.7	
t_{PLH}	LE	3B	5.9		8	ns
t_{PHL}			5.5		7.8	
t_{PLH}	CLKAB	3B	5.9		8.1	ns
t_{PHL}			5.5		7.7	
t_r(2)	Transition time, B port (10%–90%)		3.9	3.4	4.4	ns
t_f(2)	Transition time, B port (90%–10%)		3.7	3.4	4.8	ns

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C. All values are derived from TI-SPICE models.
(2) All t_r and t_f times are taken at the first receiver.

7.16 Skew Characteristics for Bus Transceiver (I Version)

for specific worst-case V_{CC} and temperature within the recommended ranges of supply voltage and operating free-air temperature (see Figure 7 and Figure 8); T_A = –40°C to 85°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
$t_{sk(LH)}$	1A or 2A	1B or 2B		0.8	ns
$t_{sk(HL)}$				0.7	
$t_{sk(LH)}$	1B or 2B	1Y or 2Y		0.7	ns
$t_{sk(HL)}$				0.7	
$t_{sk(t)}$ (1)	1A or 2A	1B or 2B		3.9	ns
	1B or 2B	1Y or 2Y		1.5	
$t_{sk(pp)}$	1A or 2A	1B or 2B		3.6	ns
	1B or 2B	1Y or 2Y		1.4	

(1) $t_{sk(t)}$ – Output-to-output skew is defined as the absolute value of the difference between the actual propagation delay for all outputs of the same packaged device. The specifications are given for specific worst-case V_{CC} and temperature and apply to any outputs switching in opposite directions, both low to high (LH) and high to low (HL) [$t_{sk(t)}$].

7.17 Skew Characteristics for Bus Transceiver (M Version)

for specific worst-case V_{CC} and temperature within the recommended ranges of supply voltage and operating free-air temperature (see Figure 7 and Figure 8); T_A = –55°C to 125°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
$t_{sk(LH)}$	1A or 2A	1B or 2B		1.6	ns
$t_{sk(HL)}$				1.6	
$t_{sk(LH)}$	1B or 2B	1Y or 2Y		1.6	ns
$t_{sk(HL)}$				1.6	
$t_{sk(t)}$ (1)	1A or 2A	1B or 2B		3.9	ns
	1B or 2B	1Y or 2Y		2.5	
$t_{sk(pp)}$	1A or 2A	1B or 2B		3.6	ns
	1B or 2B	1Y or 2Y		2.4	

(1) $t_{sk(t)}$ – Output-to-output skew is defined as the absolute value of the difference between the actual propagation delay for all outputs of the same packaged device. The specifications are given for specific worst-case V_{CC} and temperature and apply to any outputs switching in opposite directions, both low to high (LH) and high to low (HL) [$t_{sk(t)}$].

7.18 Skew Characteristics for UBT (I Version)

for specific worst-case V_{CC} and temperature within the recommended ranges of supply voltage and operating free-air temperature (see Figure 7 and Figure 8); T_A = –40°C to 85°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
$t_{sk(LH)}$	3A	3B		1.4	ns
$t_{sk(HL)}$				1.1	
$t_{sk(LH)}$	CLKAB	3B		0.8	ns
$t_{sk(HL)}$				0.8	
$t_{sk(LH)}$	3B	3A		0.7	ns
$t_{sk(HL)}$				0.6	
$t_{sk(LH)}$	CLKBA	3A		0.7	ns
$t_{sk(HL)}$				0.6	
$t_{sk(t)}$ (1)	3A	3B		3.9	ns
	CLKAB	3B		3.9	
	3B	3A		1.6	
	CLKBA	3A		1.2	
$t_{sk(pp)}$	3A	3B		3.6	ns
	CLKAB	3B		3.5	
	3B	3A		1.3	
	CLKBA	3A		1.2	

(1) $t_{sk(t)}$ – Output-to-output skew is defined as the absolute value of the difference between the actual propagation delay for all outputs of the same packaged device. The specifications are given for specific worst-case V_{CC} and temperature and apply to any outputs switching in opposite directions, both low to high (LH) and high to low (HL) [$t_{sk(t)}$].

7.19 Skew Characteristics for UBT (M Version)

for specific worst-case V_{CC} and temperature within the recommended ranges of supply voltage and operating free-air temperature (see Figure 7 and Figure 8); T_A = –55°C to 125°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
$t_{sk(LH)}$	3A	3B		1.6	ns
$t_{sk(HL)}$				1.4	
$t_{sk(LH)}$	CLKAB	3B		1.3	ns
$t_{sk(HL)}$				1.3	

Skew Characteristics for UBT (M Version) (continued)

for specific worst-case V_{CC} and temperature within the recommended ranges of supply voltage and operating free-air temperature (see Figure 7 and Figure 8); T_A = –55°C to 125°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
$t_{sk(LH)}$	3B	3A		1.2	ns
$t_{sk(HL)}$				1.2	
$t_{sk(LH)}$	CLKBA	3A		1.3	ns
$t_{sk(HL)}$				1.3	
$t_{sk(t)}$ (1)	3A	3B		4.3	ns
	CLKAB	3B		3.9	
	3B	3A		2.9	
	CLKBA	3A		2.5	
$t_{sk(pp)}$	3A	3B		3.6	ns
	CLKAB	3B		3.5	
	3B	3A		1.3	
	CLKBA	3A		1.2	

(1) $t_{sk(t)}$ – Output-to-output skew is defined as the absolute value of the difference between the actual propagation delay for all outputs of the same packaged device. The specifications are given for specific worst-case V_{CC} and temperature and apply to any outputs switching in opposite directions, both low to high (LH) and high to low (HL) [$t_{sk(t)}$].

7.20 Skew Characteristics for Bus Transceiver (I Version)

driver in slot 11, with receiver cards in all other slots (full load); for specific worst-case V_{CC} and temperature within the recommended ranges of supply voltage and operating free-air temperature (see Figure 6); T_A = –40°C to 85°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP(1)	MAX	UNIT
$t_{sk(LH)}$	1A or 2A	1B or 2B			2.5	ns
$t_{sk(HL)}$					3	
$t_{sk(t)}$ (2)	1A or 2A	1B or 2B			1	ns
$t_{sk(pp)}$	1A or 2A	1B or 2B		0.5	3.4	ns

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C. All values are derived from TI-SPICE models.
(2) $t_{sk(t)}$ – Output-to-output skew is defined as the absolute value of the difference between the actual propagation delay for all outputs of the same packaged device. The specifications are given for specific worst-case V_{CC} and temperature and apply to any outputs switching in opposite directions, both low to high (LH) and high to low (HL) [$t_{sk(t)}$].

7.21 Skew Characteristics for UBT (I Version)

driver in slot 11, with receiver cards in all other slots (full load); for specific worst-case V_{CC} and temperature within the recommended ranges of supply voltage and operating free-air temperature (see Figure 6); T_A = –40°C to 85°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP(1)	MAX	UNIT
$t_{sk(LH)}$	3A	3B			2.4	ns
$t_{sk(HL)}$					3.4	
$t_{sk(LH)}$	CLKAB	3B			2.7	ns
$t_{sk(HL)}$					3.4	
$t_{sk(t)}$ (2)	3A	3B			1	ns
	CLKAB	3B			1	
$t_{sk(pp)}$	3A	3B		0.5	3.4	ns
	CLKAB	3B		0.6	3.5	

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C. All values are derived from TI-SPICE models.
(2) $t_{sk(t)}$ – Output-to-output skew is defined as the absolute value of the difference between the actual propagation delay for all outputs of the same packaged device. The specifications are given for specific worst-case V_{CC} and temperature and apply to any outputs switching in opposite directions, both low to high (LH) and high to low (HL) [$t_{sk(t)}$].

7.22 Skew Characteristics for Bus Transceiver (I Version)

driver in slot 1, with one receiver in slot 21 (minimum load); for specific worst-case V_{CC} and temperature within the recommended ranges of supply voltage and operating free-air temperature (see Figure 6); T_A = –40°C to 85°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP(1)	MAX	UNIT
$t_{sk(LH)}$	1A or 2A	1B or 2B			1.7	ns
$t_{sk(HL)}$					2.1	
$t_{sk(t)}$ (2)	1A or 2A	1B or 2B			1	ns
$t_{sk(pp)}$	1A or 2A	1B or 2B		0.2	2.1	ns

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C. All values are derived from TI-SPICE models.
(2) $t_{sk(t)}$ – Output-to-output skew is defined as the absolute value of the difference between the actual propagation delay for all outputs of the same packaged device. The specifications are given for specific worst-case V_{CC} and temperature and apply to any outputs switching in opposite directions, both low to high (LH) and high to low (HL) [$t_{sk(t)}$].

7.23 Skew Characteristics for UBT (I Version)

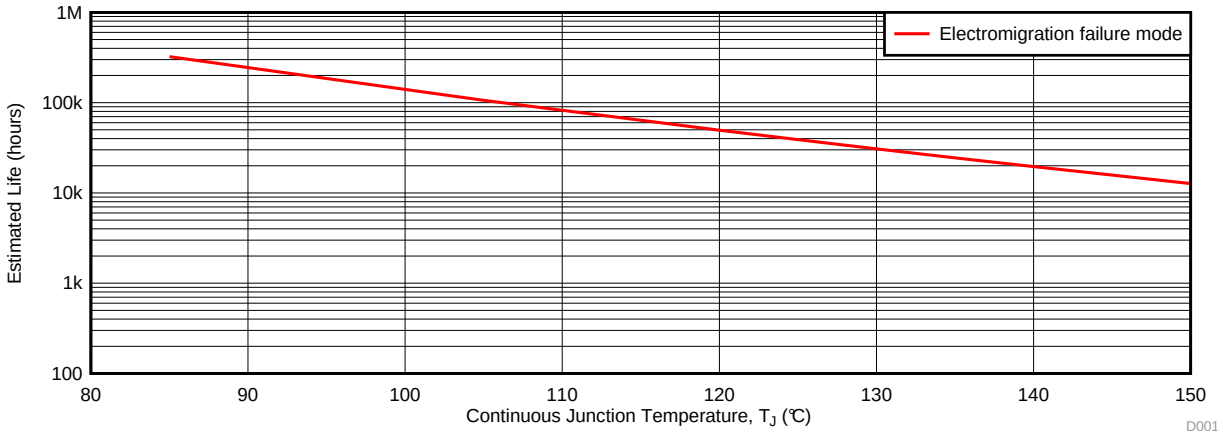
driver in slot 1, with one receiver in slot 21 (minimum load); for specific worst-case V_{CC} and temperature within the recommended ranges of supply voltage and operating free-air temperature (see Figure 6); T_A = –40°C to 85°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP(1)	MAX	UNIT
$t_{sk(LH)}$	3A	3B			2	ns
$t_{sk(HL)}$					2.3	
$t_{sk(LH)}$	CLKAB	3B			2.1	ns
$t_{sk(HL)}$					2.4	
$t_{sk(t)}$ (2)	3A	3B			1	ns
	CLKAB	3B			1	
$t_{sk(pp)}$	3A	3B		0.2	2.5	ns
	CLKAB	3B		0.2	2.9	

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C. All values are derived from TI-SPICE models.
(2) $t_{sk(t)}$ – Output-to-output skew is defined as the absolute value of the difference between the actual propagation delay for all outputs of the same packaged device. The specifications are given for specific worst-case V_{CC} and temperature and apply to any outputs switching in opposite directions, both low to high (LH) and high to low (HL) [$t_{sk(t)}$].

7.24 Maximum Data Transfer Rates

DATE	TOPOLOGY	PROTOCOL	DATA (BITS PER CYCLE)	DATA TRANSFERS PER CLOCK CYCLE	PER SYSTEM (MBps)	FREQUENCY (MHz)	
						BACKPLANE	CLOCK
1981	VMEbus IEEE-1014	BLT	32	1	40	10	10
1989	VME64	MBLT	64	1	80	10	10
1995	VME64x	2eVME	64	2	160	10	20
1997	VME64x	2eSST	64	2-No Ack	160 to 320	10 to 20	20 to 40
1999	VME320	2eSST	64	2-No Ack	320 to 1000	20 to 62.5	40 to 125



(1) See data sheet for absolute maximum and minimum recommended operating conditions.
(2) Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).
(3) Enhanced plastic product disclaimer applies.

Figure 1. SN74VMEH22501A-EP Derating Chart

7.25 Typical Characteristics

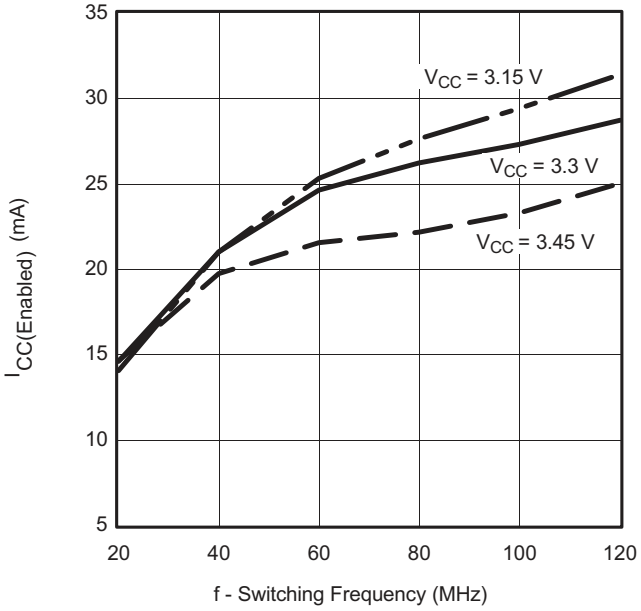


Figure 2. Supply Current vs Frequency A to B

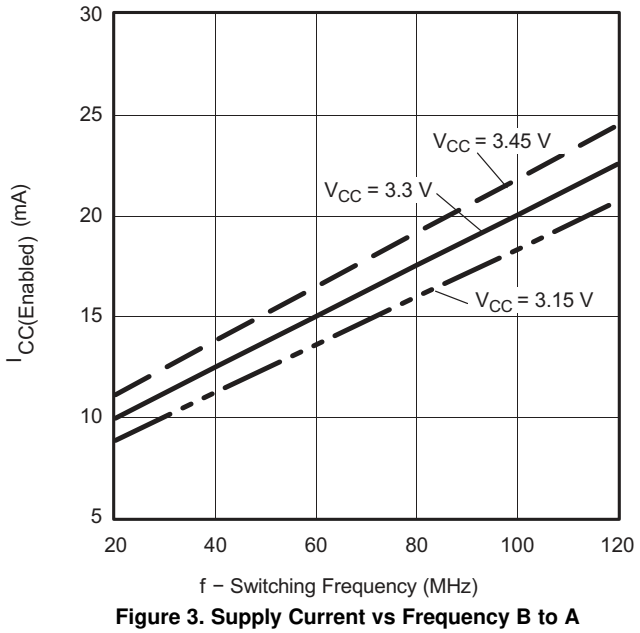


Figure 3. Supply Current vs Frequency B to A

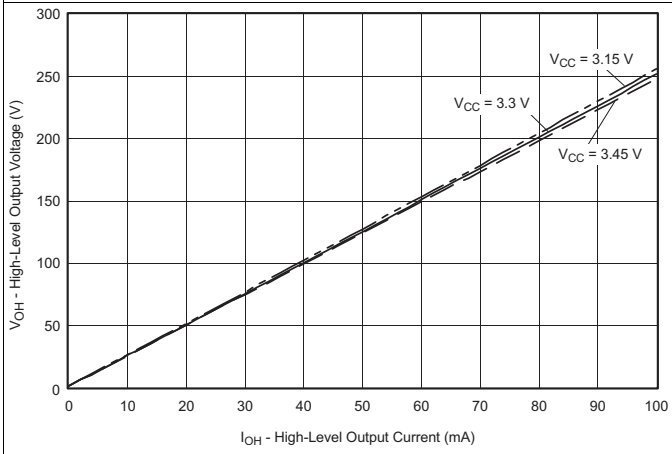


Figure 4. High-Level Output Voltage vs High-Level Output Current, V_{OL} vs I_{OL}

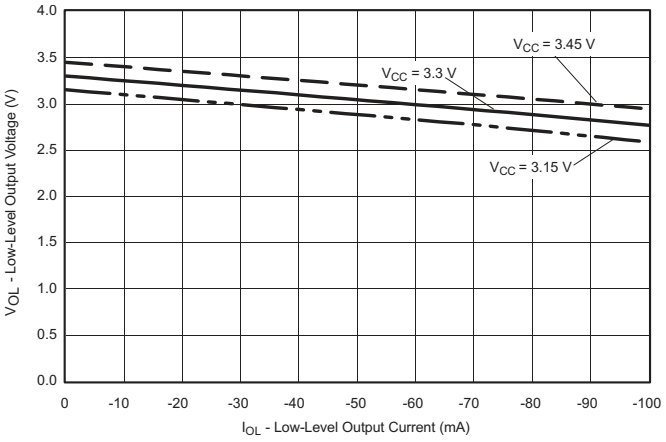
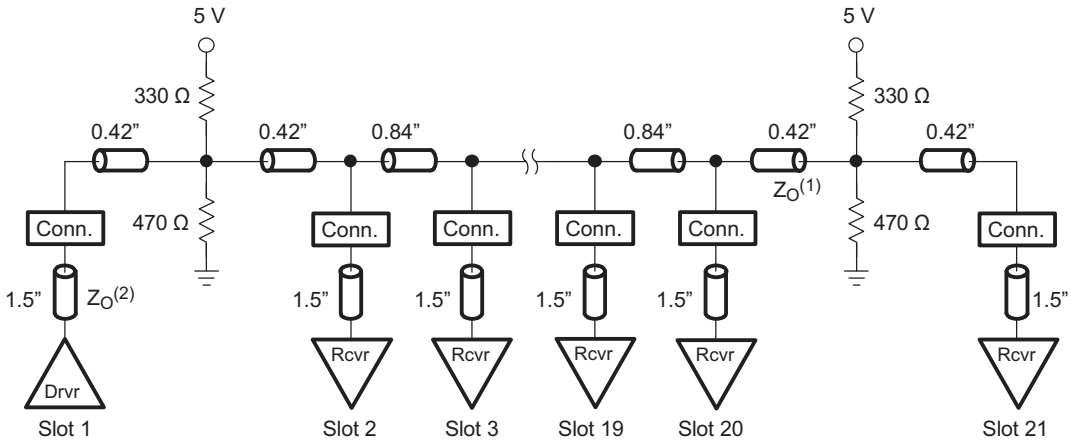


Figure 5. Low-Level Output Voltage vs Low-Level Output Current, V_{OH} vs I_{OH}

8 Parameter Measurement Information

8.1 Distributed-Load Backplane Switching Characteristics

The switching characteristics tables show the switching characteristics of the device into the lumped load shown in this section (see Figure 7 and Figure 8). All logic devices currently are tested into this type of load. However, the designer's backplane application probably is a distributed load. For this reason, this device has been designed for optimum performance in the VME64x backplane as shown in Figure 6.

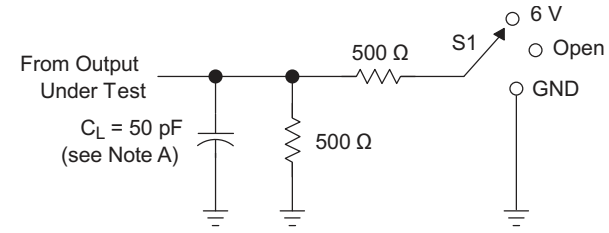


1. Unloaded backplane trace natural impedance (Z_O) is 45 Ω. 45 Ω to 60 Ω is allowed, with 50 Ω being ideal.
2. Card stub natural impedance (Z_O) is 60 Ω.

Figure 6. VME64x Backplane

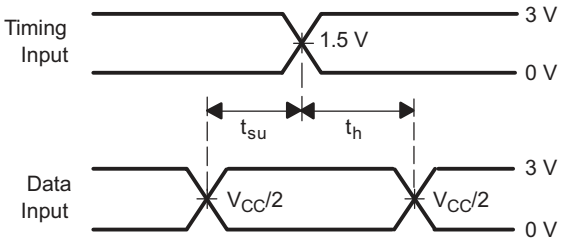
The following switching characteristics tables derived from TI-SPICE models show the switching characteristics of the device into the backplane under full and minimum loading conditions, to help the designer better understand the performance of the VME device in this typical backplane.

Distributed-Load Backplane Switching Characteristics (continued)

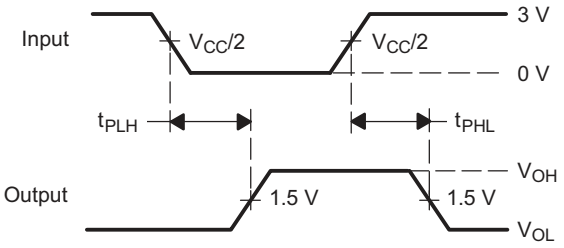


LOAD CIRCUIT

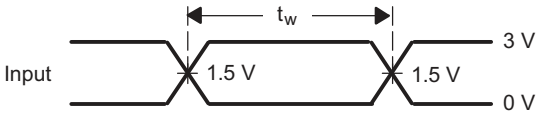
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND
B-to-A Skew	Open



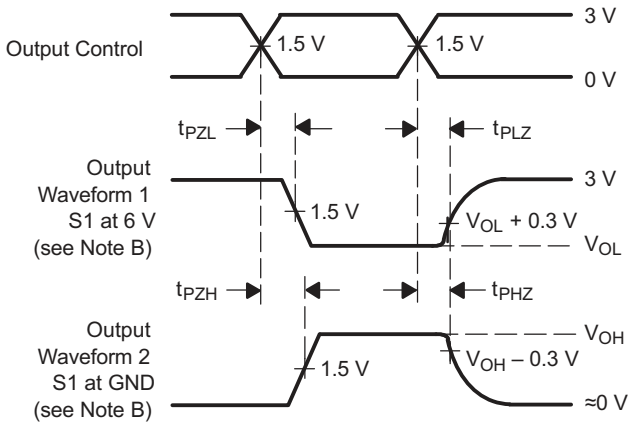
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

A. C_L includes probe and jig capacitance.

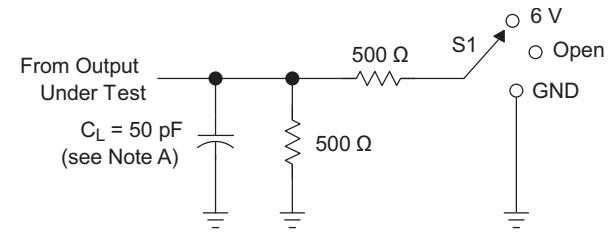
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR ≈ 10 MHz, Z_O = 50 Ω, t_r ≈ 2 ns, t_f ≈ 2 ns.

D. The outputs are measured one at a time, with one transition per measurement.

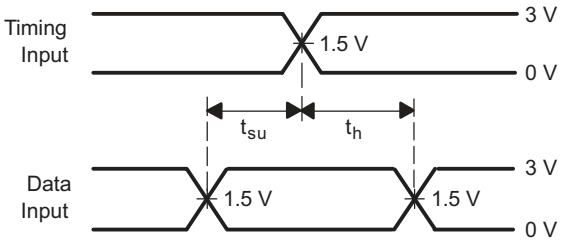
Figure 7. A Port Load Circuit and Voltage Waveforms

Distributed-Load Backplane Switching Characteristics (continued)

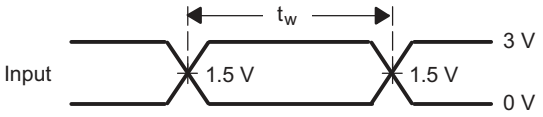


LOAD CIRCUIT

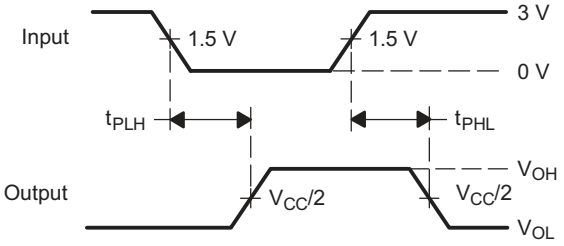
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND
A-to-B Skew	Open



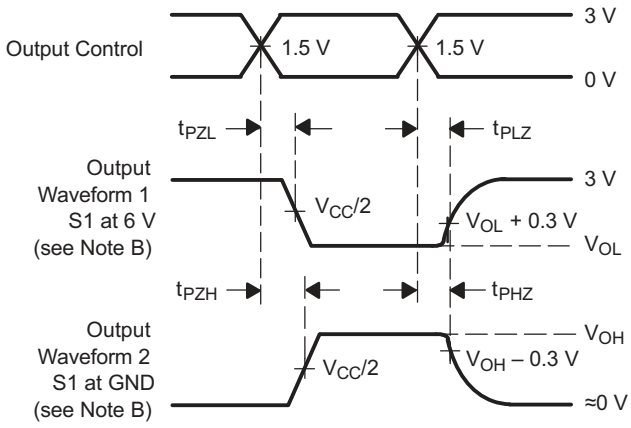
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR ≈ 10 MHz, Z_O = 50 Ω, t_r ≈ 2 ns, t_f ≈ 2 ns.

D. The outputs are measured one at a time, with one transition per measurement.

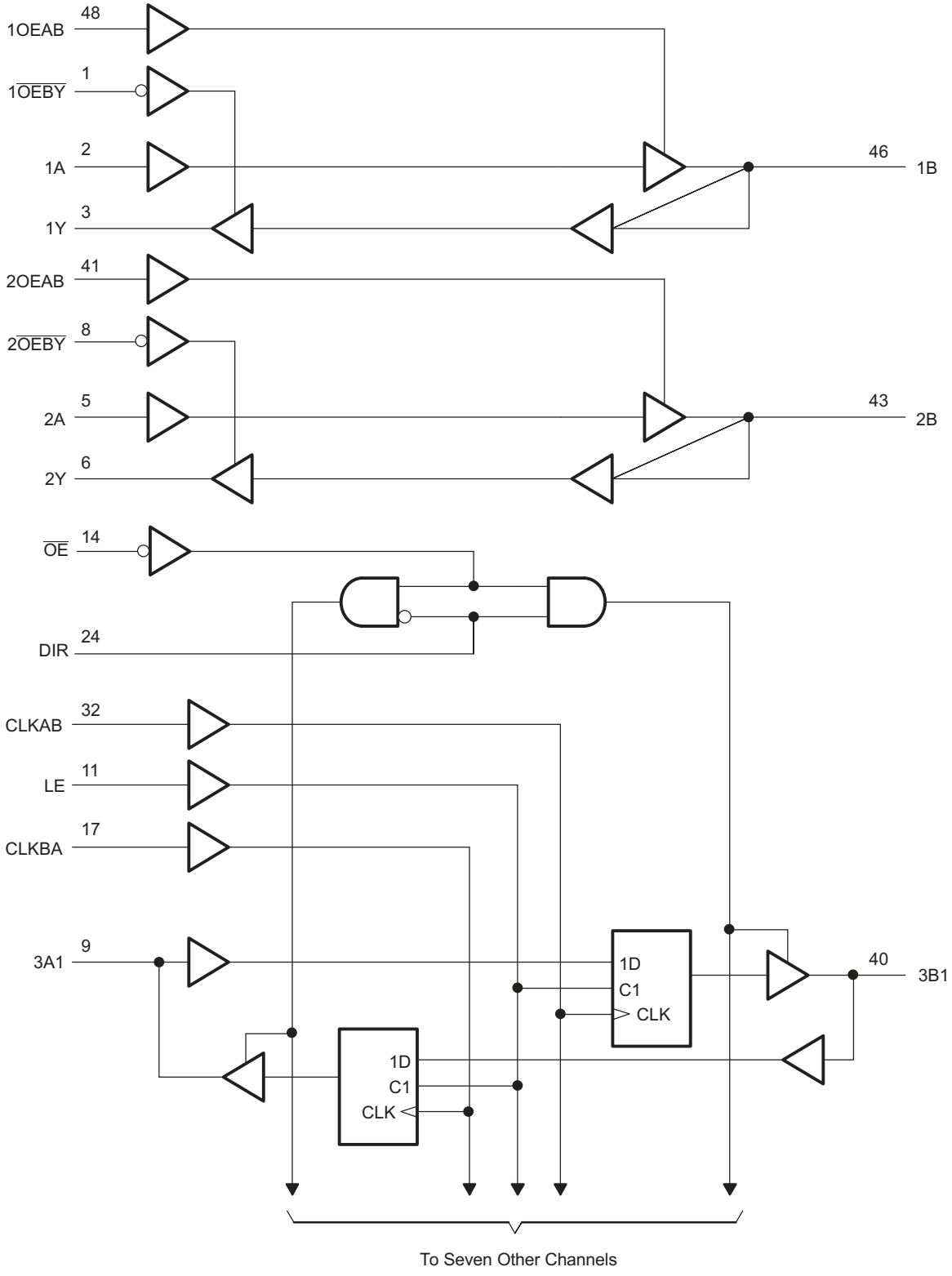
Figure 8. B Port Load Circuit and Voltage Waveforms

9 Detailed Description

9.1 Overview

The SN74VMEH22501A-EP device is a high-drive (–48/64 mA), 8-bit UBT transceiver containing D-type latches and D-type flip-flops for data-path operation in transparent, latched, or flip-flop modes. Data transmission is true logic. The SN74VMEH22501A-EP device is uniquely partitioned as 8-bit UBT transceivers with two integrated 1-bit three-wire bus transceivers.

9.2 Functional Block Diagram



Pin numbers shown are for the DGG and DGV packages.

Figure 9. Logic Diagram (Positive Logic)

9.3 Feature Description

9.3.1 Functional Description for Two 1-Bit Bus Transceivers

The OEAB inputs control the activity of the 1B or 2B port. When OEAB is high, the B-port outputs are active. When OEAB is low, the B-port outputs are disabled.

Separate 1A and 2A inputs and 1Y and 2Y outputs provide a feedback path for control and diagnostics monitoring. The $\overline{OEBY}$ inputs control the 1Y or 2Y outputs. When $\overline{OEBY}$ is low, the Y outputs are active. When $\overline{OEBY}$ is high, the Y outputs are disabled.

The $\overline{OEBY}$ and OEAB inputs can be tied together to form a simple direction control where an input high yields A data to B bus and an input low yields B data to Y bus.

Table 1. 1-Bit Bus Transceiver Function Table

INPUTS		OUTPUT	MODE
OEAB	$\overline{OEBY}$		
L	H	Z	Isolation
H	H	A data to B bus	True driver
L	L	B data to Y bus	
H	L	A data to B bus, B data to Y bus	True driver with feedback path

9.3.2 Functional Description for 8-Bit UBT Transceiver

The 3A and 3B data flow in each direction is controlled by the $\overline{OE}$ and direction-control (DIR) inputs. When $\overline{OE}$ is low, all 3A- or 3B-port outputs are active. When $\overline{OE}$ is high, all 3A- or 3B-port outputs are in the high-impedance state.

Table 2. Function Table

INPUTS		OUTPUT
$\overline{OE}$	DIR	
H	X	Z
L	H	3A data to 3B bus
L	L	3B data to 3A bus

The UBT transceiver functions are controlled by latch-enable (LE) and clock (CLKAB and CLKBA) inputs. For 3A-to-3B data flow, the UBT operates in the transparent mode when LE is high. When LE is low, the 3A data is latched if CLKAB is held at a high or low logic level. If LE is low, the 3A data is stored in the latch/flip-flop on the low-to-high transition of CLKAB.

The UBT transceiver data flow for 3B to 3A is similar to that of 3A to 3B, but uses CLKBA.

Table 3. UBT Transceiver Function Table(1)

INPUTS				OUTPUT 3B	MODE
$\overline{OE}$	LE	CLKAB	3A		
H	X	X	X	Z	Isolation
L	L	H	X	B_0(2)	Latched storage of 3A data
L	L	L	X	B_0(3)	
L	H	X	L	L	True transparent
L	H	X	H	H	
L	L	↑	L	L	Clocked storage of 3A data
L	L	↑	H	H	

(1) 3A-to-3B data flow is shown; 3B-to-3A data flow is similar, but uses CLKBA.
(2) Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LE went low.
(3) Output level before the indicated steady-state input conditions were established.

The UBT transceiver can replace any of the functions as shown in Table 4.

Table 4. SN74VMEH22501A-EP UBT Transceiver Replacement Functions(1)

FUNCTION	8 BIT
Transceiver	'245, '623, '645
Buffer/driver	'241, '244, '541
Latched transceiver	'543
Latch	'373, '573
Registered transceiver	'646, '652
Flip-flop	'374, '574

(1) SN74VMEH22501A-EP UBT transceiver replaces all above functions

9.3.3 VMEbus Summary

In 1981, the VMEbus was introduced as a backplane bus architecture for industrial and commercial applications. The data-transfer protocols used to define the VMEbus came from the Motorola® VERSA bus architecture that owed its heritage to the then recently introduced Motorola 68000 microprocessor. The VMEbus, when introduced, defined two basic data-transfer operations: single-cycle transfers consisting of an address and a data transfer, and a block transfer (BLT) consisting of an address and a sequence of data transfers. These transfers were asynchronous, using a master-slave handshake. The master puts address and data on the bus and waits for an acknowledgment. The selected slave either reads or writes data to or from the bus, then provides a data-acknowledge (DTACK*) signal. The VMEbus system data throughput was 40 MBps. Previous to the VMEbus, it was not uncommon for the backplane buses to require elaborate calculations to determine loading and drive current for interface design. This approach made designs difficult and caused compatibility problems among manufacturers. To make interface design easier and to ensure compatibility, the developers of the VMEbus architecture defined specific delays based on a 21-slot terminated backplane and mandated the use of certain high-current TTL drivers, receivers, and transceivers.

In 1989, multiplexing block transfer (MBLT) effectively increased the number of bits from 32 to 64, thereby doubling the transfer rate. In 1995, the number of handshake edges was reduced from four to two in the double-edge transfer (2eVME) protocol, doubling the data rate again. In 1997, the VMEbus International Trade Association (VITA) established a task group to specify a synchronous protocol to increase data-transfer rates to 320 MBps, or more. The unreleased specification, VITA 1.5 [double-edge source synchronous transfer (2eSST)], is based on the asynchronous 2eVME protocol. It does not wait for acknowledgment of the data by the receiver and requires incident-wave switching. Sustained data rates of 1 GBps, more than ten times faster than traditional VME64 backplanes, are possible by taking advantage of 2eSST and the 21-slot VME320 star-configuration backplane. The VME320 backplane approximates a lumped load, allowing substantially higher-frequency operation over the VME64x distributed-load backplane. Traditional VME64 backplanes with no changes theoretically can sustain 320 MBps.

From BLT to 2eSST – A Look at the Evolution of VMEbus Protocols by John Rynearson, Technical Director, VITA, provides additional information on VMEbus and can be obtained at www.vita.com.

9.4 Device Functional Modes

9.4.1 True Driver With Feedback Path Mode (1-Bit Transceiver)

When OEAB is high and $\overline{\text{OEABY}}$is s low, the 1-bit transceiver will act as true driver with a feedback path through the Y port for control and diagnostic monitoring.

9.4.2 Direction Control Model (1-Bit Transceiver)

The two 1 bit transceiver can act as a true driver when $\overline{\text{OEBY}}$ and OEAB are tied together.

1. Input high:data move from A port to B bus
2. Input low: data move from B port to Y bus

9.4.3 Direction Control for 8 Bit UBT

The UBT data flow is controlled by DIR pin. DIR set as high, it will be 3A-3B data flow and if DIR set as low, it will be 3B-3A dataflow. When LE is high, the UBT is in transparent mode and all inputs will be translated to the output.

9.4.4 Latch Storage and Clock Storage

When LE is low and CLK at high or low level, data is latched. During latch state, the output level is per the previous state. When the CLK transitions from low to high, the latched data will be output.

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

Target applications for VME backplanes include industrial controls, telecommunications, simulation, high-energy physics, office automation, and instrumentation systems.

10.2 Typical Application

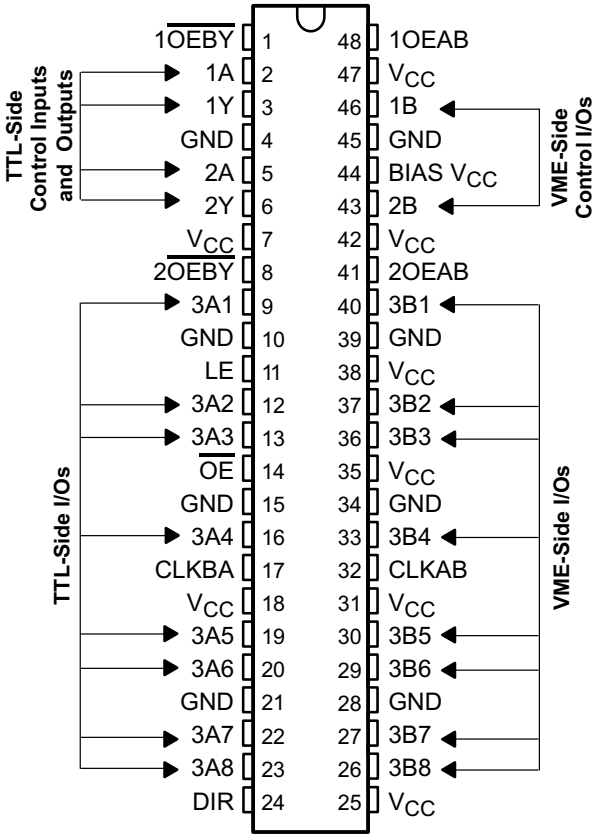


Figure 10. Application Schematic

10.2.1 Design Requirements

The SN74VMEH22501-EP is a combination of 8-bit universal bus transceivers (UBT) and two-bit transceivers, with split LVTTL ports for control and diagnostic monitoring purposes. For the UBTs, 3B1 to 3B8 are the VME-side I/O ports and 3A1 to 3A8 are the LVTTL-side I/O ports. For the two split LVTTL-port transceivers, 1A, 2A are the LVTTL-side input ports, 1Y, 2Y are the LVTTL-side output ports, and 1B, 2B are the VME-side I/O ports (see Figure 5). The UBTs allow transparent, latched, and flip-flop modes of data transfer. It operates at 3.3-V VCC, but can accept 5.5-V input signals at both VME and LVTTL ports. The LVTTL 3A ports and Y outputs have 26-Ω series resistors to reduce the line mismatch on the daughter-card LVTTL side. With the help of Ioff, power-up 3-state, and precharge (BIAS VCC) features, the SN74VMEH22501-EP supports live insertion.

Typical Application (continued)

The VME-side input port has tightly controlled input-switching thresholds of ½ VCC ±50 mV for increased noise immunity. In the VMEbus, this input threshold is a clear advantage over the normal TTL or LVTTL type inputs, where $V_{IH(min)}$ is 2.0 V and $V_{IL(max)}$ is 0.8 V. Because the input threshold follows the VCC, data transfer is more immune to the fluctuation of supply voltage, as opposed the ABTE family, where the input threshold is fixed at 1.5 V ±100 mV. To optimize performance, the SN74VMEH22501-EP has been designed into a distributed VME backplane. The OEC™ circuitry, for output edge-rate control, helps reduce reflections as well as electromagnetic interference. The OEC circuitry and high ac drive strength are instrumental in achieving the goal of incident-wave switching. The VME port can source and sink very-high transient currents, which effectively helps to overdrive the reflection on the backplane during transition.

10.2.2 Detailed Design Procedure

By simulating the performance of the device using the VME64x backplane (see Figure 6), the maximum peak current in or out of the B-port output, as the devices switch from one logic state to another, was found to be equivalent to driving the lumped load shown in Figure 11.

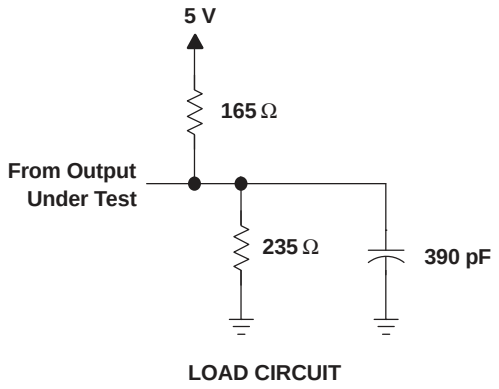


Figure 11. Equivalent AC Peak Output-Current Lumped Load

In general, the rise- and fall-time distribution is shown in Figure 12. Because VME devices were designed for use into distributed loads like the VME64x backplane (B/P), there are significant differences between low-to-high (LH) and high-to-low (HL) values in the lumped load shown in the PMI (see Figure 7 and Figure 8).

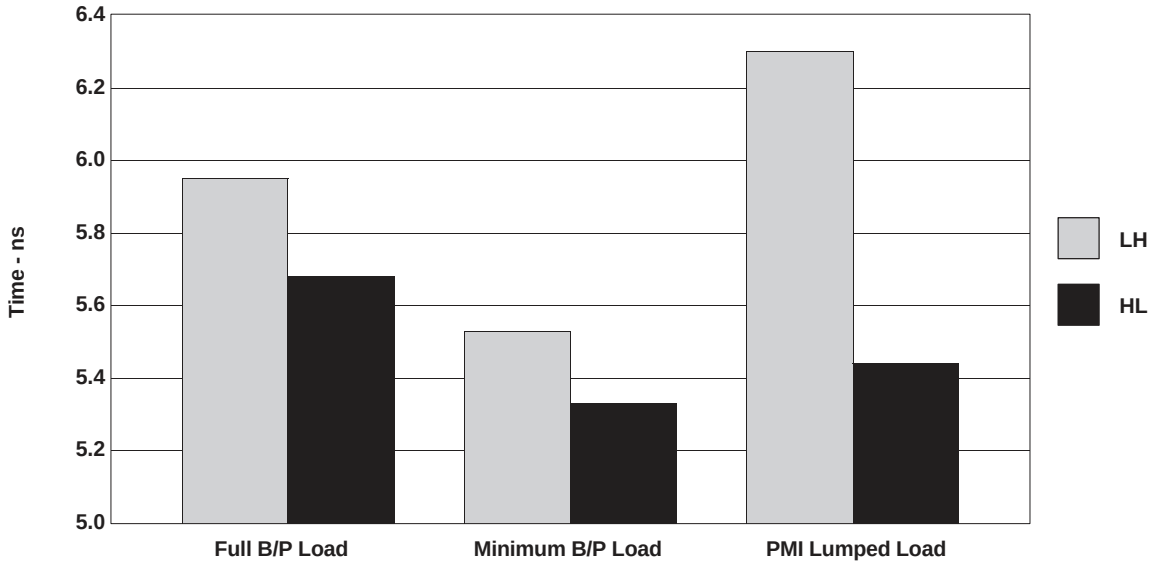


Figure 12. Propagation Delay of VMEH22501 Across Different Loads

Typical Application (continued)

10.2.3 Application Curves

Characterization-laboratory data in Figure 13 and Figure 14 show the absolute ac peak output current, with different supply voltages, as the devices change output logic state. A typical nominal process is shown to demonstrate the devices' peak ac output drive capability.

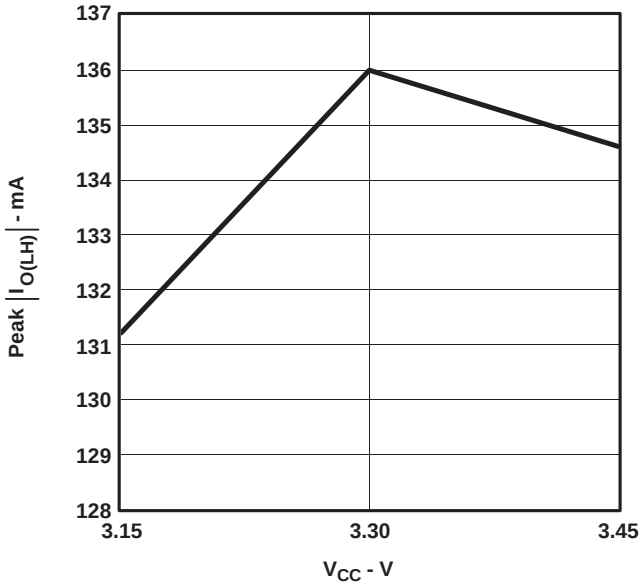


Figure 13. Peak | $I_{O(LH)}$ | vs V_{CC}

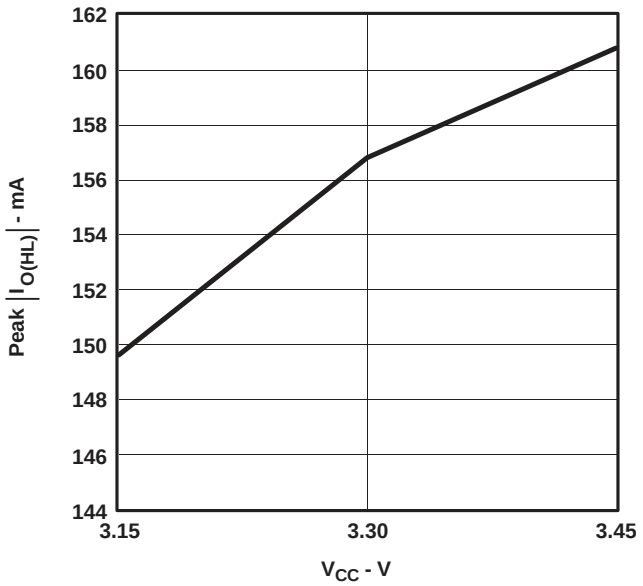


Figure 14. Peak | $I_{O(HL)}$ | vs V_{CC}

11 Power Supply Recommendations

Place 0.1-µF bypass capacitors close to the power supply pins to reduce errors coupling in from noisy or high impedance power supplies.

12 Layout

12.1 Layout Guidelines

The stub length from the VMEH22501 to the connector should be as short as possible. To reduce system skew, stub lengths should be matched for all the data and control bits. Populating both sides of the daughter card may help optimize the stub lengths.

The 5-row connector and the 3-row connector specifications correspond completely. All the data and control lines have the same pin positions in these two connectors. This allows easy migration from a 3-row connector to a 5-row connector. If a 5-row connector is used instead of a 3-row connector, some bypass capacitors between the supply pins and GND of the external rows (at the back of the connector) will help reduce some ground-bounce noise.

TI recommends to use multiple bypass capacitors to stabilize the supply line. To reduce high-frequency noise, TI recommends a small capacitor (0.1 µF, or less) for every two VCC pins on the VME side of the VMEH22501. The capacitors should be as close as possible to the VCC pins. An additional large capacitor close to the chip helps maintain the dc level of the power-supply line.

If live insertion is required, TI recommends a specific power-up sequence to use the full live-insertion capability of the VMEH22501. The power-up sequence should be GND, BIAS VCC, OE pin, I/O ports, then VCC.

12.2 Layout Example

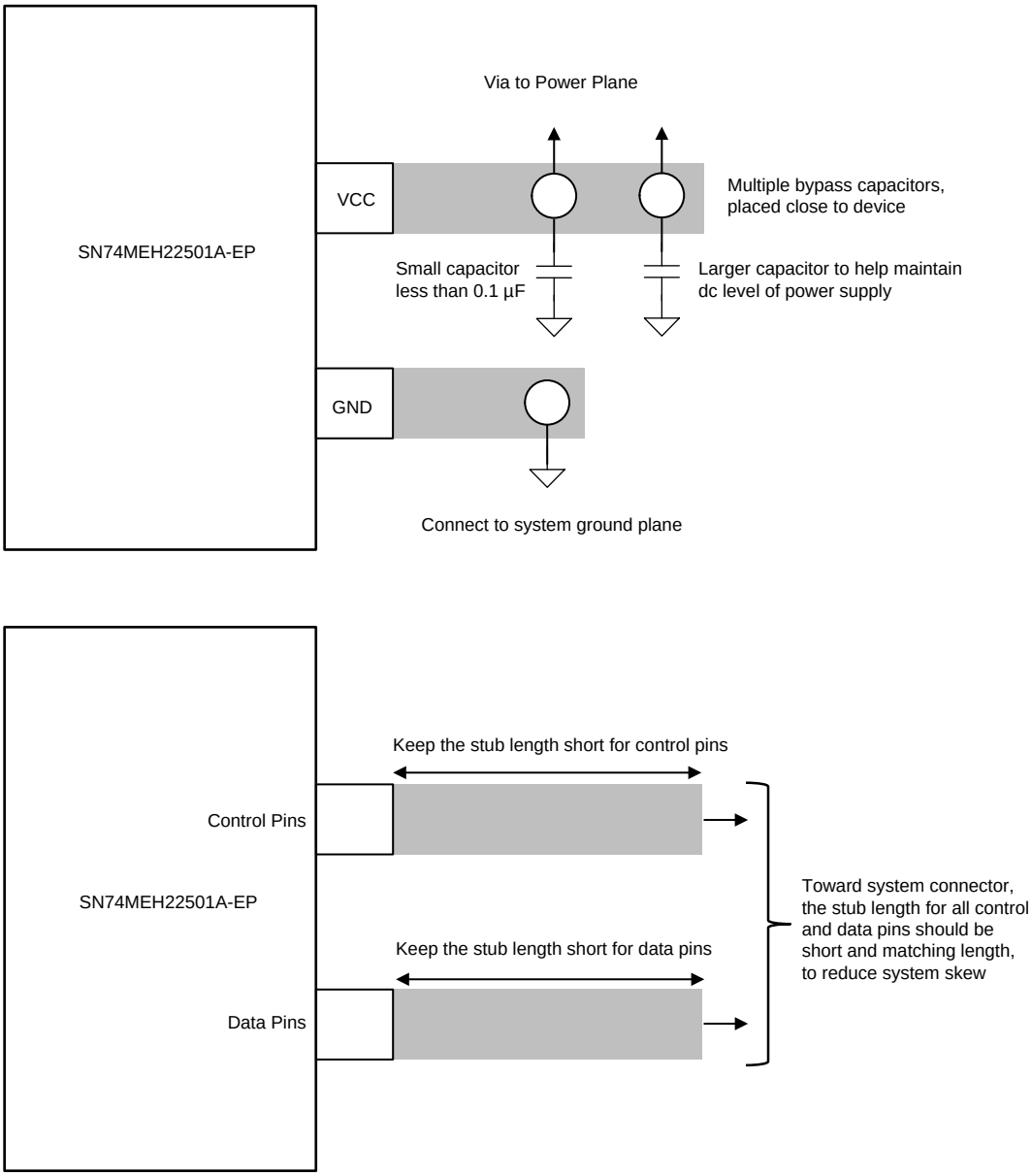


Figure 15. Layout Recommendation

13 Device and Documentation Support

13.1 Device Support

13.1.1 Third-Party Products Disclaimer

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13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 5. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74VMEH22501A-EP	Click here	Click here	Click here	Click here	Click here
SN74VMEH22501AM-EP	Click here	Click here	Click here	Click here	Click here

13.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.4 Trademarks

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Motorola is a registered trademark of Motorola, Inc.
OEC is a trademark of OEC AG.
All other trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CVMEH22501AIDGGREP	ACTIVE	TSSOP	DGG	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VMEH22501EP	Samples
CVMEH22501AIDGVREP	ACTIVE	TVSOP	DGV	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VK501AEP	Samples
CVMEH22501AMDGGREP	ACTIVE	TSSOP	DGG	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	VMEH22501MEP	Samples
V62/05606-01XE	ACTIVE	TSSOP	DGG	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VMEH22501EP	Samples
V62/05606-01YE	ACTIVE	TVSOP	DGV	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VK501AEP	Samples
V62/05606-02XE	ACTIVE	TSSOP	DGG	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	VMEH22501MEP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN74VMEH22501A-EP :

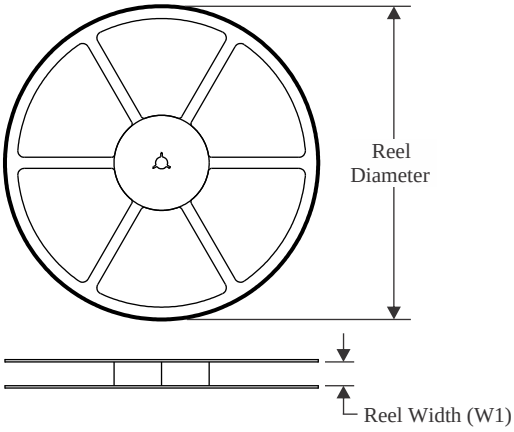
- Catalog: SN74VMEH22501A

NOTE: Qualified Version Definitions:

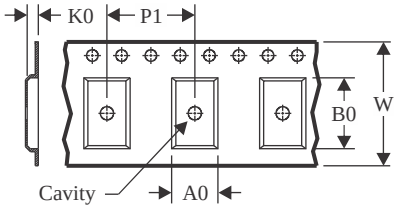
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

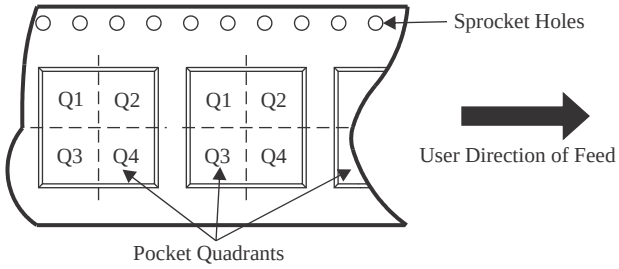


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

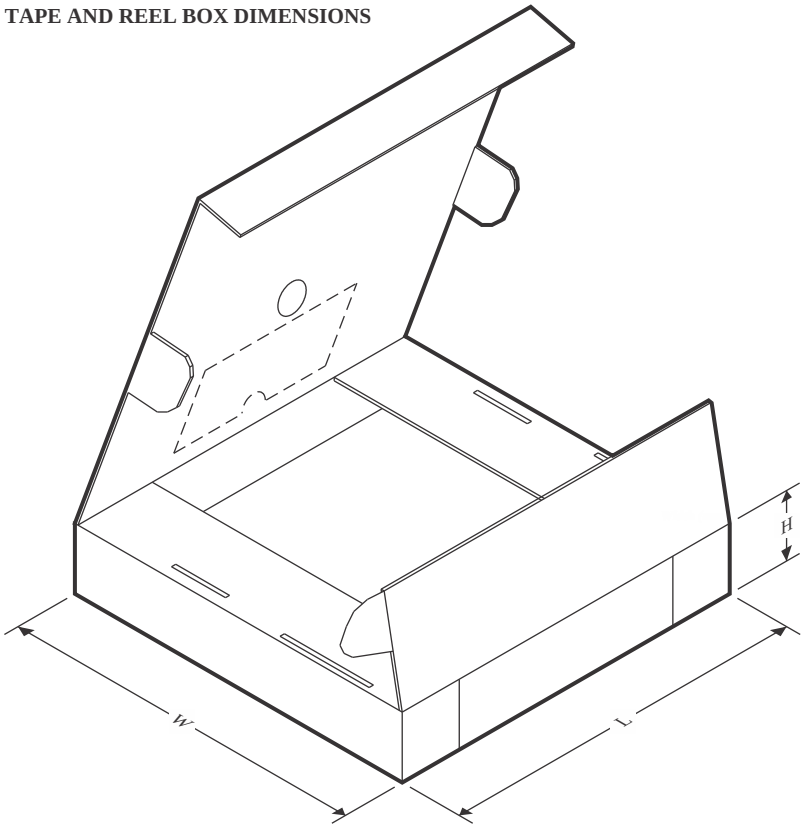
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CVMEH22501AIDGGREP	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
CVMEH22501AIDGVREP	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1
CVMEH22501AMDGGREP	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

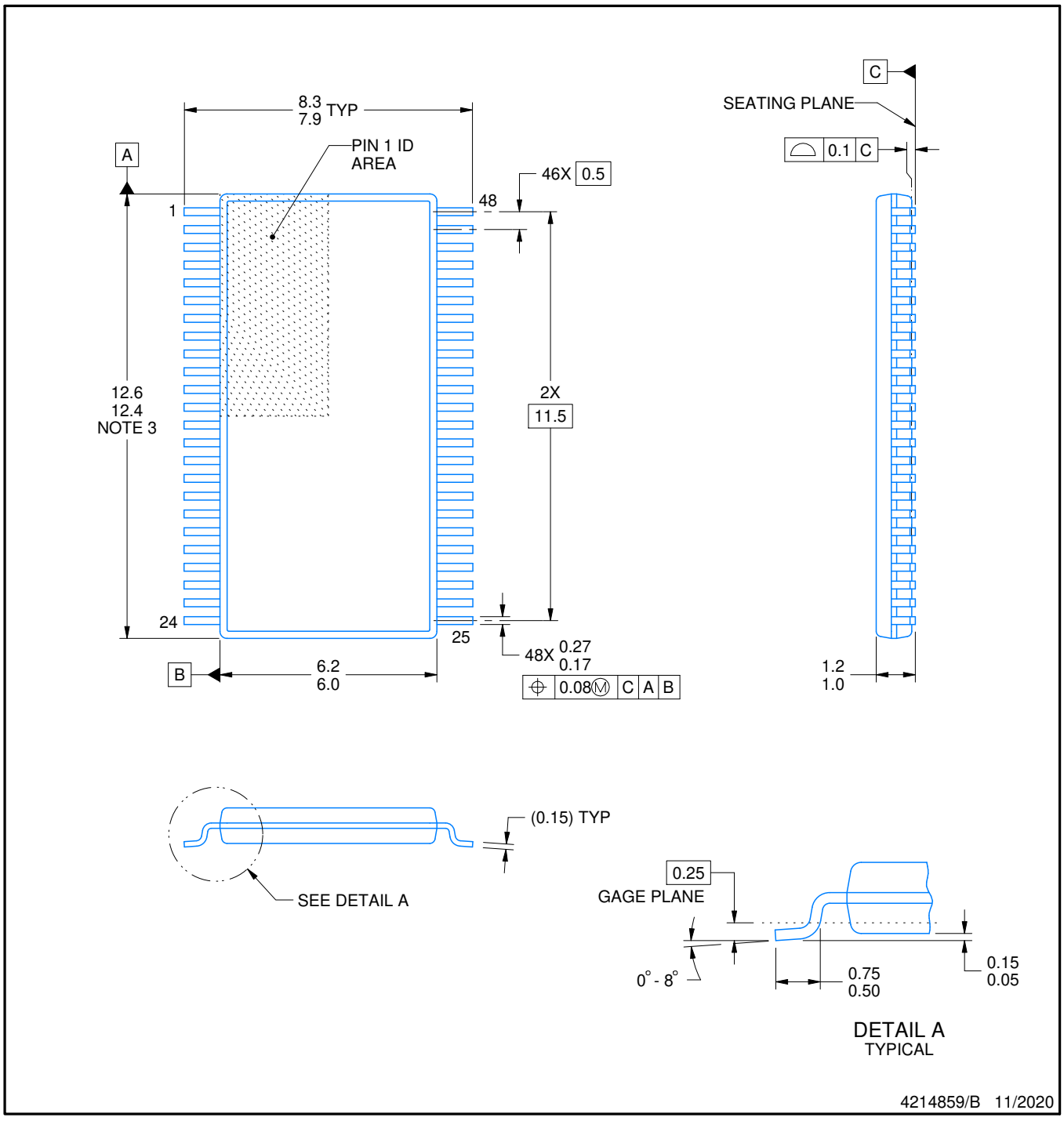
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CVMEH22501AIDGGREP	TSSOP	DGG	48	2000	356.0	356.0	41.0
CVMEH22501AIDGVREP	TVSOP	DGV	48	2000	356.0	356.0	35.0
CVMEH22501AMDGGREP	TSSOP	DGG	48	2000	356.0	356.0	41.0

PACKAGE OUTLINE

DGG0048A

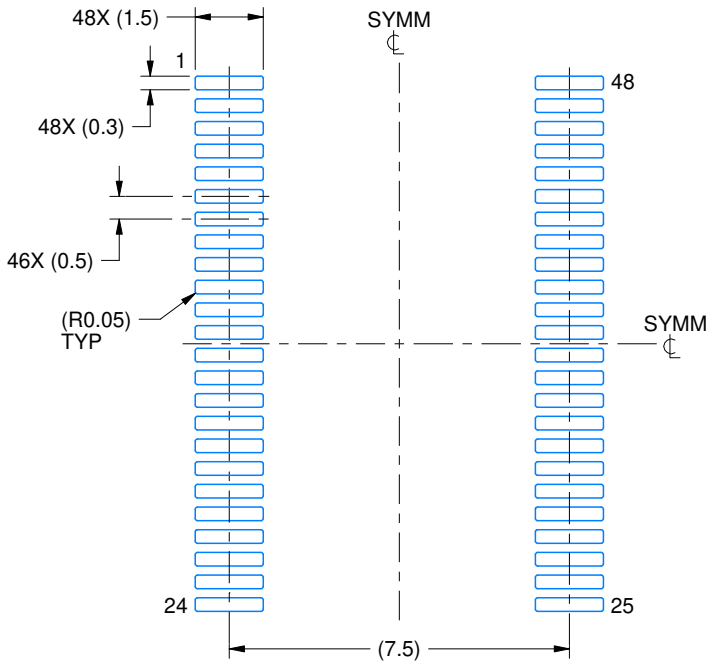
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

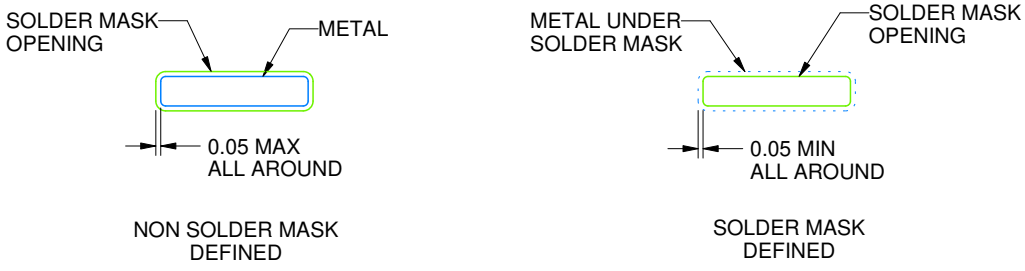


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
SCALE:6X

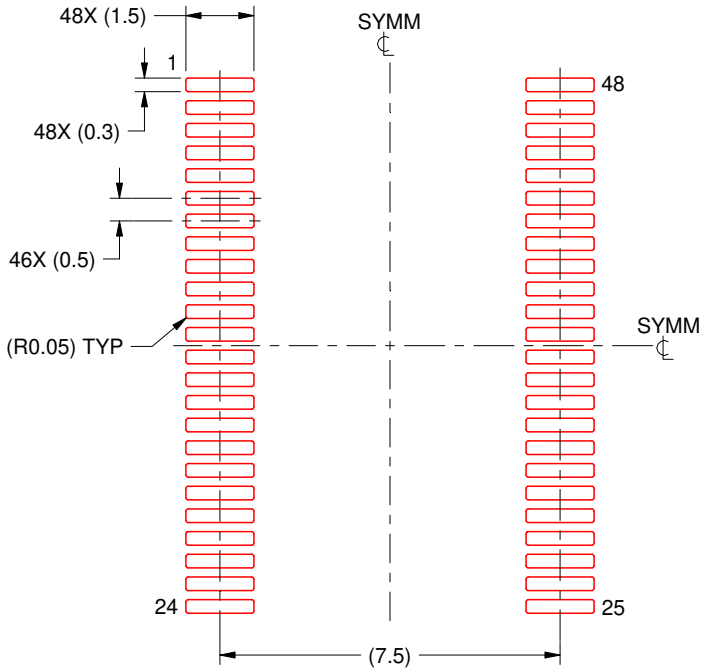


SOLDER MASK DETAILS

4214859/B 11/2020

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4214859/B 11/2020

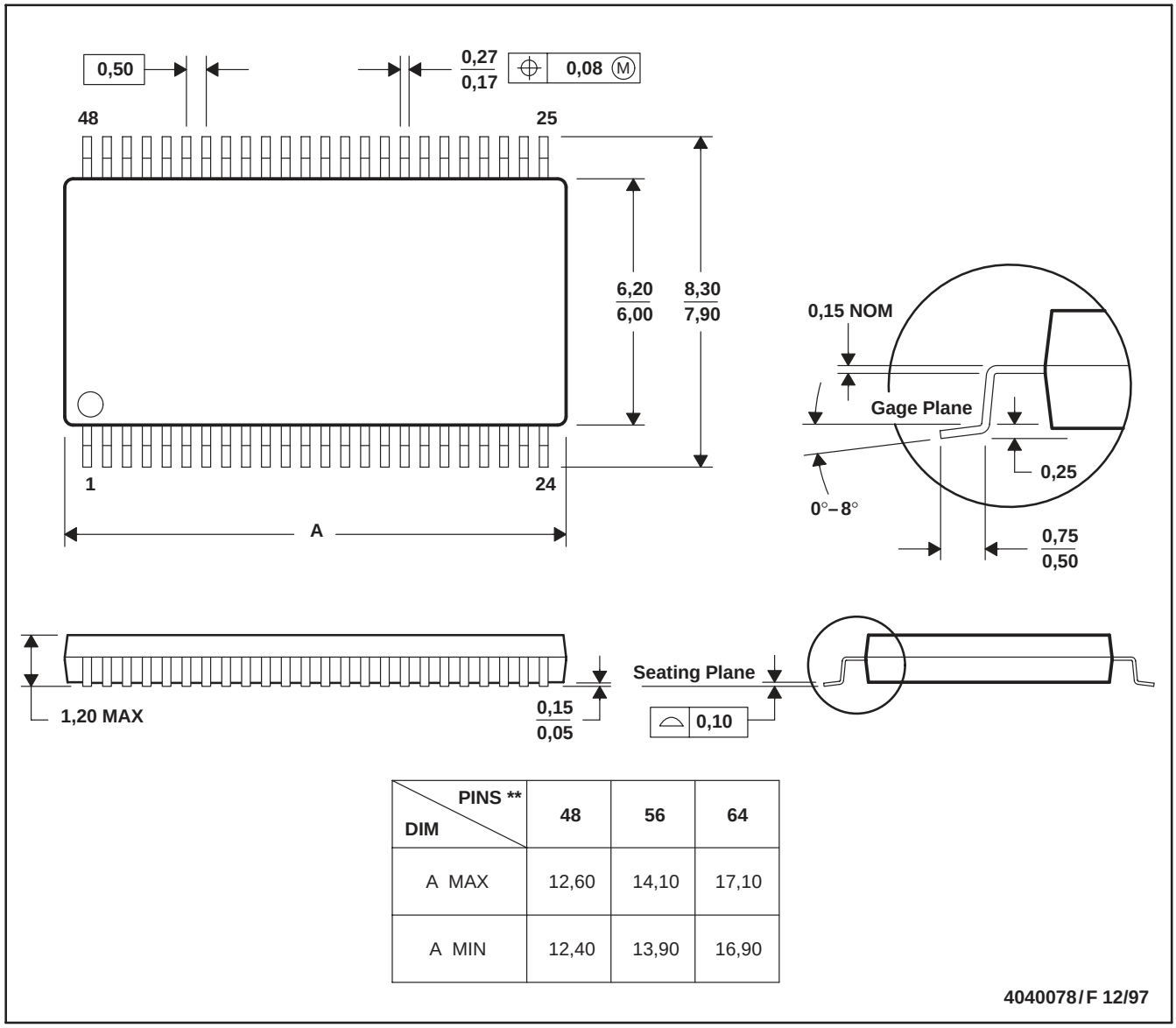
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

MTSS003D – JANUARY 1995 – REVISED JANUARY 1998

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265