

MM74HCT05 Hex Inverter (Open Drain)

Features

- Open drain for wire-NOR function
- LS-TTL pinout and threshold compatible
- Fanout of 10 LS-TTL loads
- Typical propagation delays:
 - t_{PZL} (with 1k Ω resistor) 10ns
 - t_{PLZ} (with 1k Ω resistor) 8ns

General Description

The MM74HCT05 is a logic function fabricated by using advanced silicon-gate CMOS technology, which provides the inherent benefits of CMOS—low quiescent power and wide power supply range. The device is also input and output characteristic and pinout compatible with standard DM74LS logic families. The MM74HCT05 open drain Hex Inverter requires the addition of an external resistor to perform a wire-NOR function.

All inputs are protected from static discharge damage by internal diodes to V_{CC} and ground.

MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Ordering Information

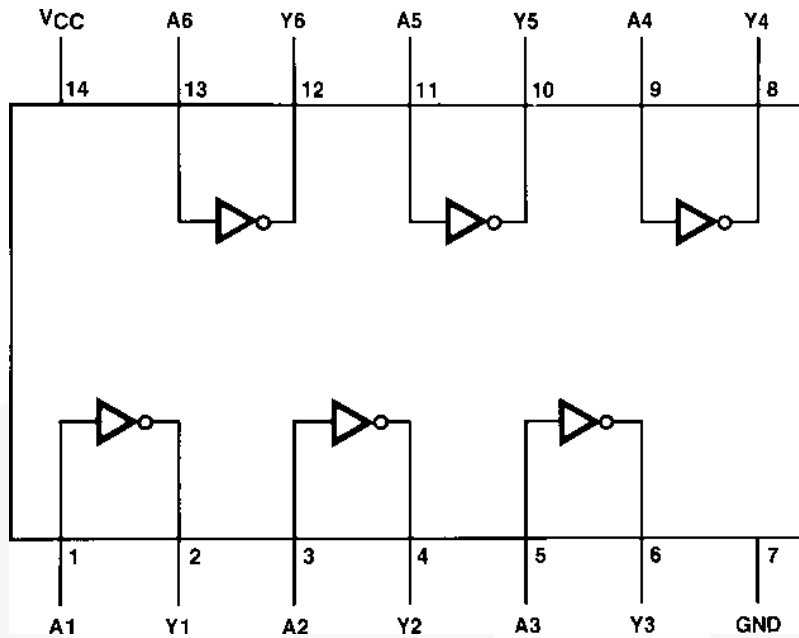
| Order Number | Package Number | Package Description |
|--------------|----------------|--|
| MM74HCT05M | M14A | 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow |
| MM74HCT05SJ | M14D | 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| MM74HCT05MTC | MTC14 | 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |
| MM74HCT05N | N14A | 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.



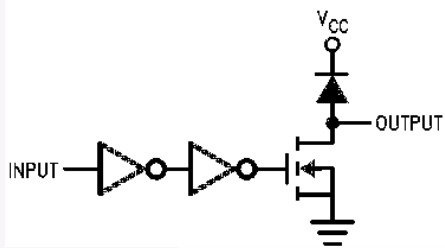
All packages are lead free per JEDEC: J-STD-020B standard.

Connection Diagram

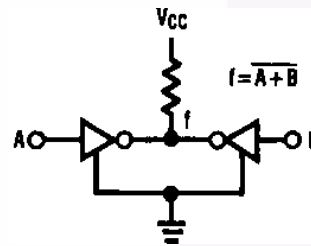


Top View

Logic Diagram



Typical Application



Absolute Maximum Ratings⁽¹⁾

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol | Parameter | Rating |
|------------------|---|-----------------------|
| V_{CC} | Supply Voltage | -0.5 to +7.0V |
| V_{IN} | DC Input Voltage | -1.5 to $V_{CC}+1.5V$ |
| V_{OUT} | DC Output Voltage | -0.5 to $V_{CC}+0.5V$ |
| I_{IK}, I_{OK} | Clamp Diode Current | $\pm 20mA$ |
| I_{OUT} | DC Output Current, per pin | $\pm 25mA$ |
| I_{CC} | DC V_{CC} or GND Current, per pin | $\pm 50mA$ |
| T_{STG} | Storage Temperature Range | -65°C to +150°C |
| P_D | Power Dissipation Note 2 | 600mW |
| | S.O. Package only | 500mW |
| T_L | Lead Temperature (Soldering 10 seconds) | 260°C |

Notes:

1. Unless otherwise specified all voltages are referenced to ground.
2. Power Dissipation temperature derating — plastic “N” package: -12mW/°C from 65°C to 85°C.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

| Symbol | Parameter | Min. | Max. | Units |
|------------|-----------------------------|------|----------|-------|
| V_{CC} | Supply Voltage | 4.5 | 5.5 | V |
| V_{IN} | DC Input Voltage | 0 | V_{CC} | V |
| V_{OUT} | DC Output Voltage | 0 | 5.5 | V |
| T_A | Operating Temperature Range | -40 | +85 | °C |
| t_r, t_f | Input Rise or Fall Times | | 500 | ns |

DC Electrical Characteristics $V_{CC} = 5V \pm 10\%$ unless otherwise specified)

| Symbol | Parameter | Conditions | $T_A = 25^\circ\text{C}$ | | Units | |
|-----------|---|---|--------------------------|-------------------|---------------|---------------|
| | | | Typ. | Guaranteed Limits | | |
| V_{IH} | Minimum HIGH Level Input Voltage | | | 2.0 | V | |
| V_{IL} | Maximum LOW Level Input Voltage | | | 0.8 | V | |
| V_{OL} | Maximum LOW Level Voltage | $V_{IN} = V_{IH}, I_{OUT} = 20\mu\text{A}$ | 0 | 0.1 | V | |
| | | $V_{IN} = V_{IH}, I_{OUT} = 4.0\text{mA}, V_{CC} = 4.5\text{V}$ | 0.2 | 0.26 | 0.33 | |
| | | $V_{IN} = V_{IH}, I_{OUT} = 4.8\text{mA}, V_{CC} = 5.5\text{V}$ | 0.2 | 0.26 | 0.33 | |
| I_{IN} | Maximum Input Current | $V_{IN} = V_{CC}$ or GND, V_{IH} or V_{IL} | | ± 0.1 | μA | |
| I_{LKG} | Maximum HIGH Level Output Leakage Current | $V_{IN} = V_{IH}$ or $V_{IL},$ $V_{OUT} = V_{CC}$ | | 0.5 | μA | |
| I_{CC} | Maximum Quiescent Supply Current | $V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0\mu\text{A}$ | | 2.0 | μA | |
| | | $V_{IN} = 2.4\text{V}$ or $0.5\text{V}^{(3)}$ | | 0.3 | 0.4 | mA |
| I_{OHZ} | Off State Current | $V_{CC} = 4.5\text{V} - 5.5\text{V}, V_O = 5.5\text{V}$ | | | 10 | μA |

Note:3. This is measured per input with all other inputs held at V_{CC} or ground.**AC Electrical Characteristics** $V_{CC} = 5V, T_A = 25^\circ\text{C}, C_L = 15\text{pF}, t_r = t_f = 6\text{ns}$ unless otherwise noted.

| Symbol | Parameter | Conditions | Typ. | Guaranteed Limit | Units |
|-----------|---------------------------|-------------------------|------|------------------|-------|
| t_{PZL} | Maximum Propagation Delay | $R_L = 1\text{k}\Omega$ | 8 | 15 | ns |
| t_{PLZ} | Maximum Propagation Delay | $R_L = 1\text{k}\Omega$ | 9 | 16 | ns |

AC Electrical Characteristics $V_{CC} = 5V, \pm 10\%, C_L = 50\text{pF}, t_r = t_f = 6\text{ns}$ unless otherwise specified.

| Symbol | Parameter | Conditions | $T_A = 25^\circ\text{C}$ | | Units |
|-----------|-------------------------------|------------------------------------|--------------------------|-------------------|-------|
| | | | Typ. | Guaranteed Limits | |
| t_{PZL} | Maximum Propagation Delay | $R_L = 1\text{k}\Omega$ | 10 | 22 | ns |
| t_{PLZ} | Maximum Propagation Delay | $R_L = 1\text{k}\Omega$ | 12 | 20 | ns |
| t_{THL} | Maximum Output Fall Time | | 10 | 15 | ns |
| C_{PD} | Power Dissipation Capacitance | (per gate), $R_L = \infty, ^{(4)}$ | | 20 | pF |
| C_{IN} | Maximum Input Capacitance | | | 5 | pF |

Note:4. C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Physical Dimensions

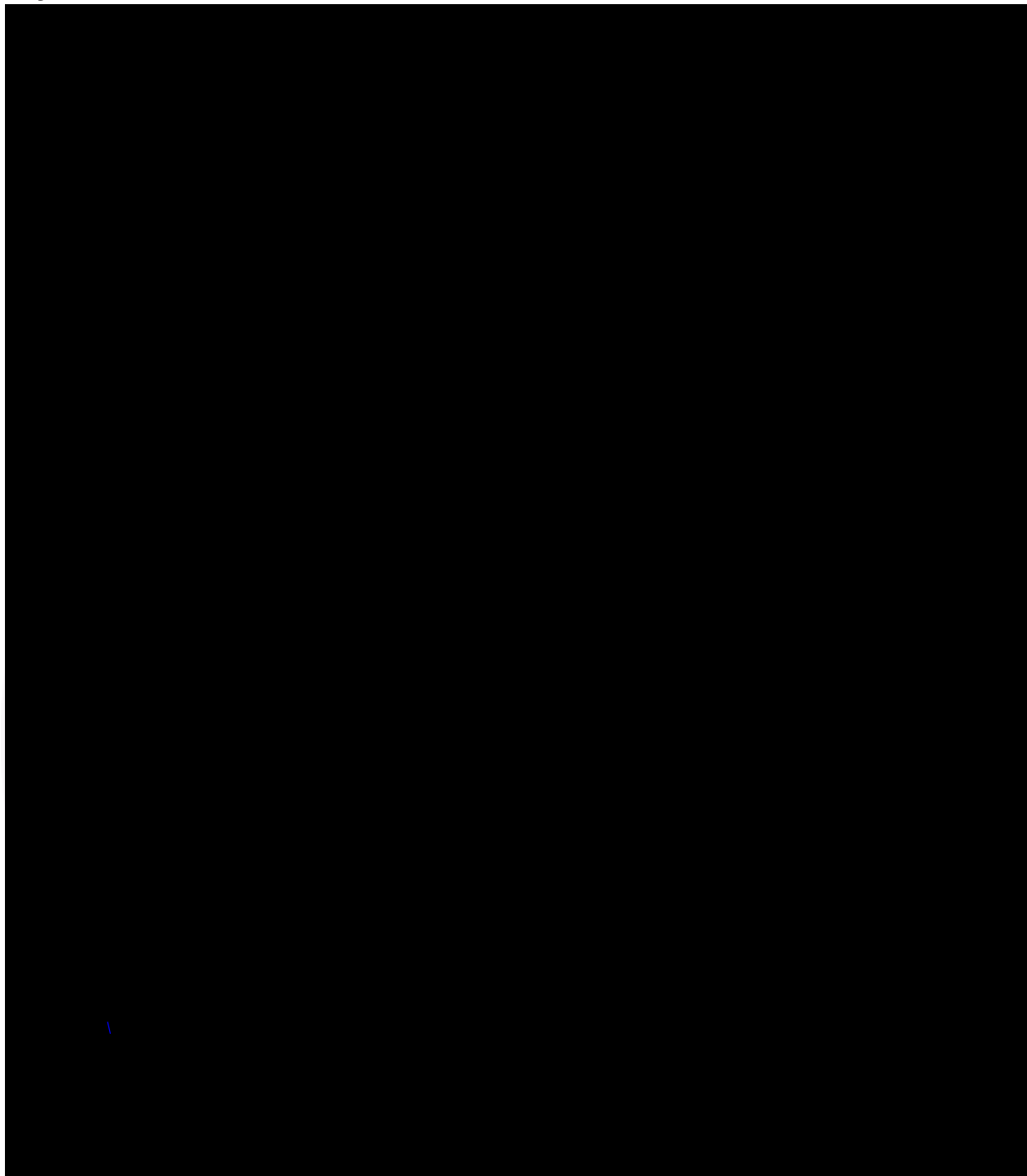
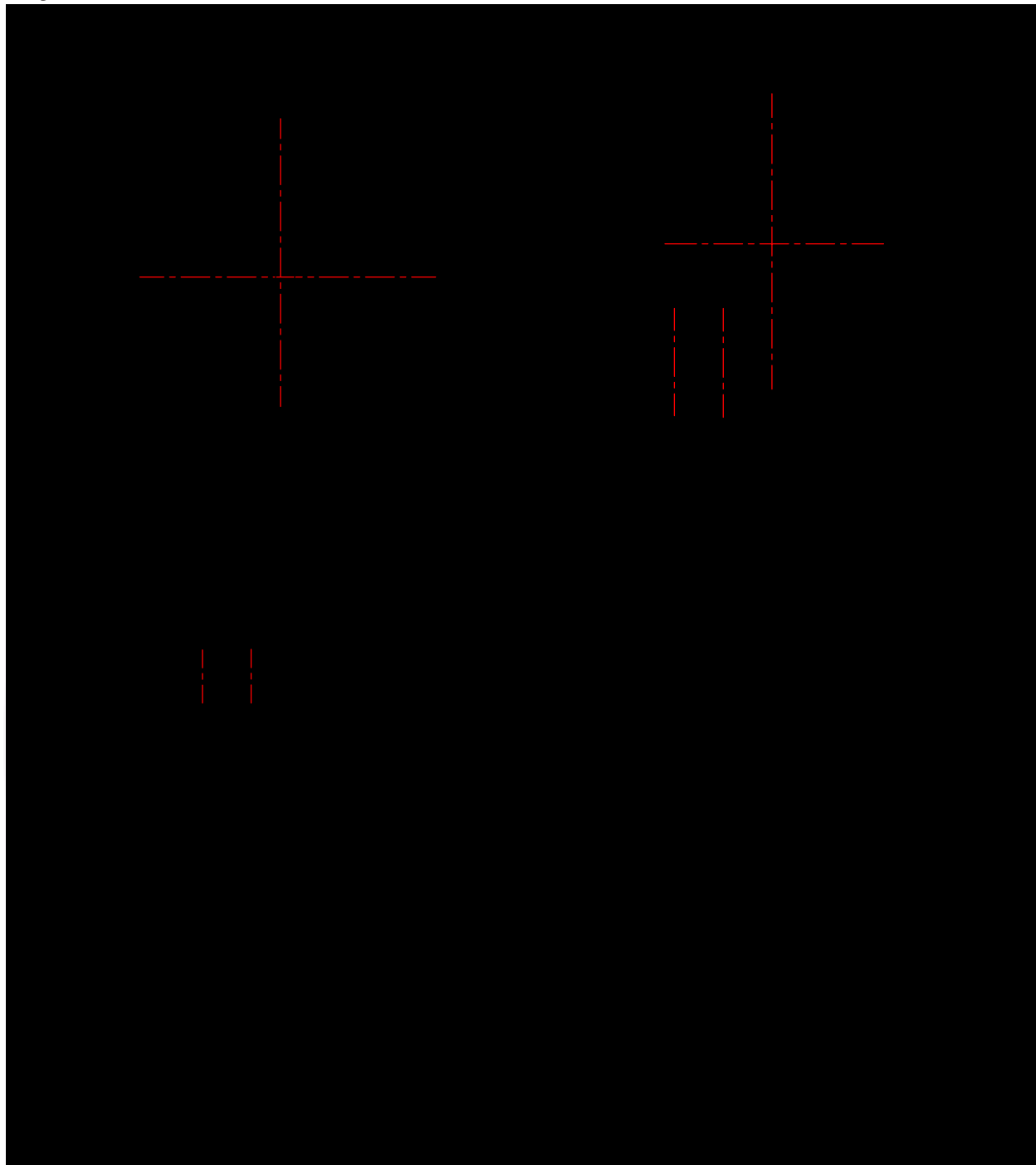


Figure 1. 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow

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Physical Dimensions (Continued)**Figure 2. 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide**

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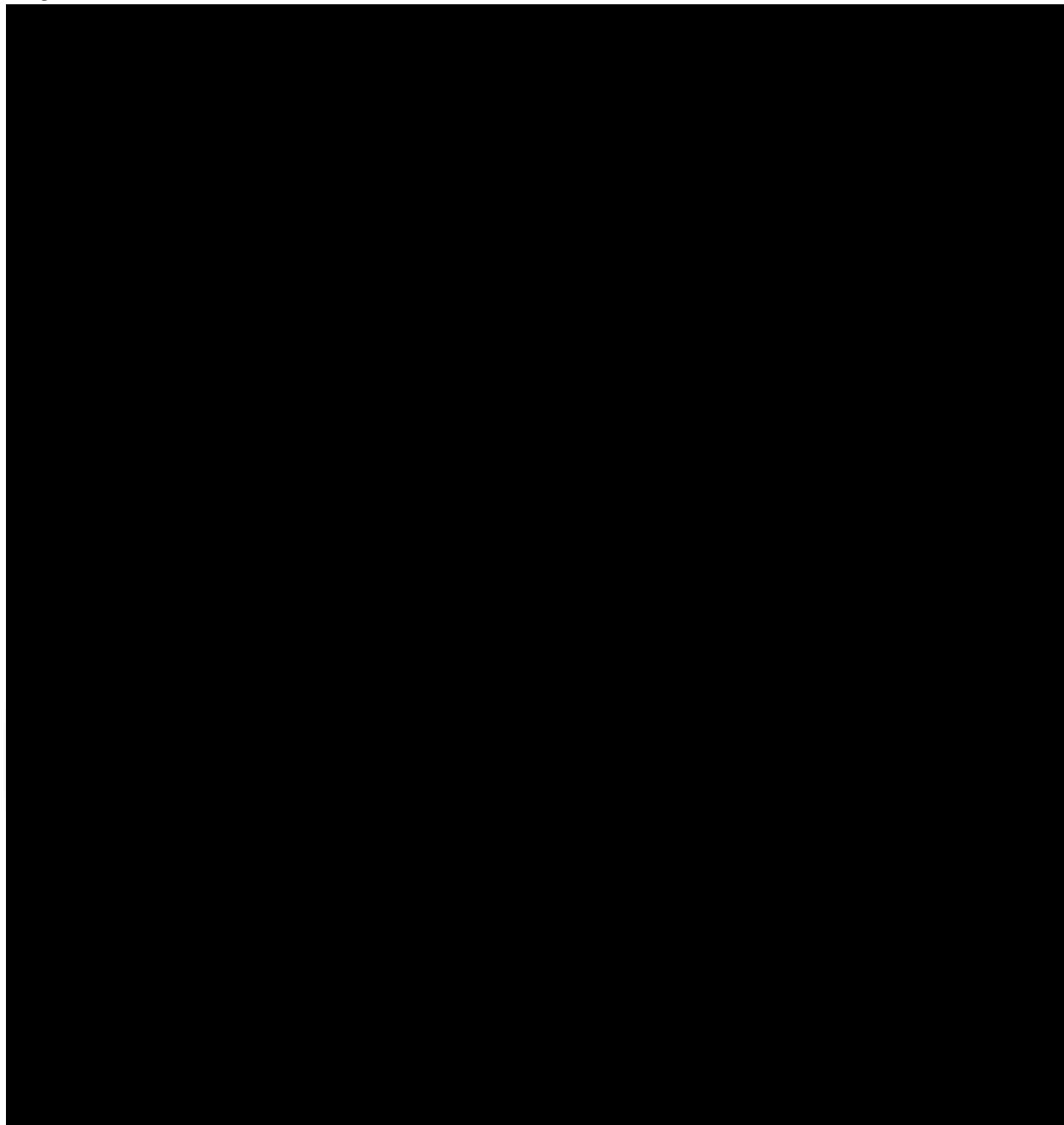
Physical Dimensions (Continued)

Figure 3. 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

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Physical Dimensions (Continued)

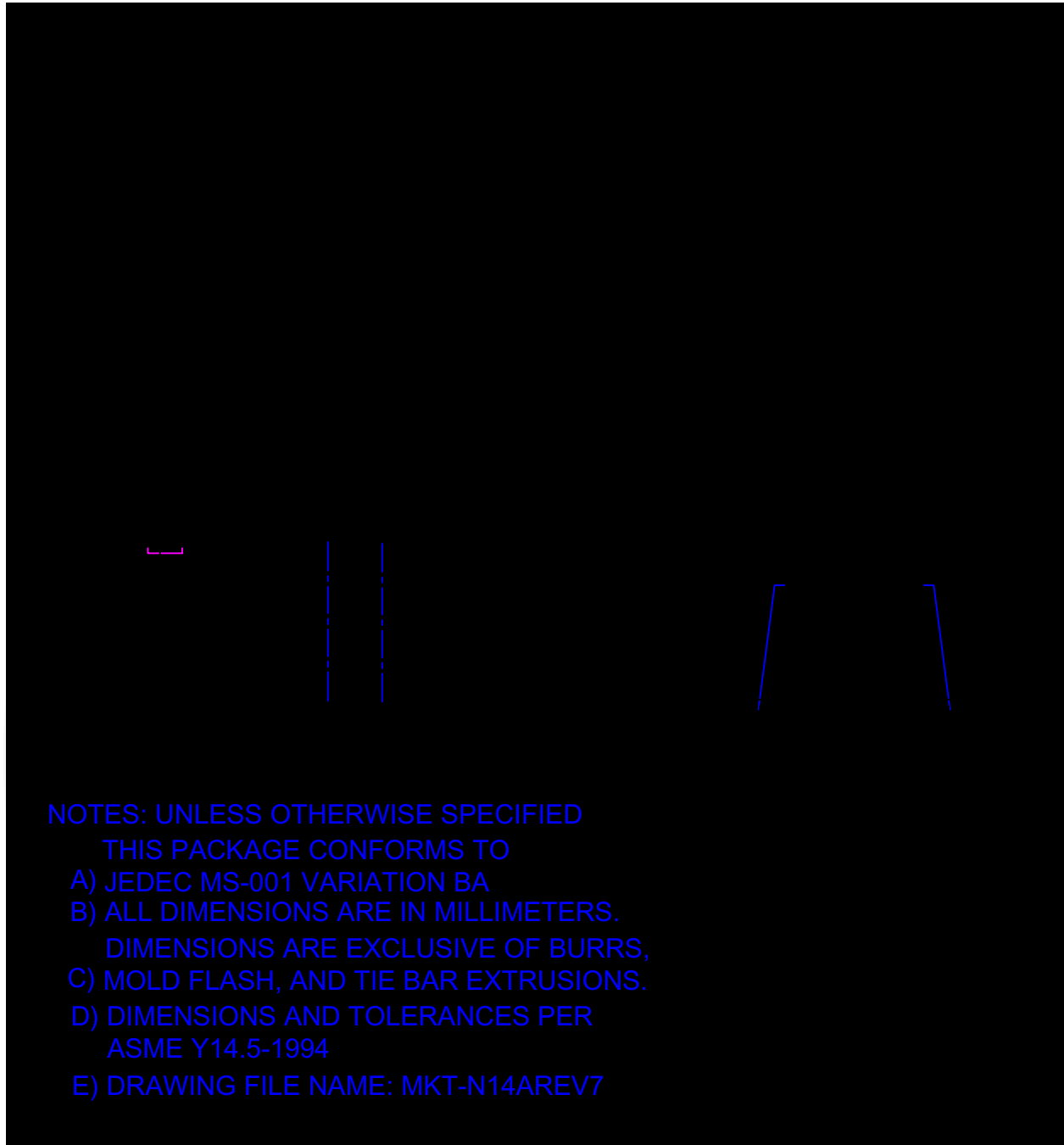


Figure 4. 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide



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