User's Guide

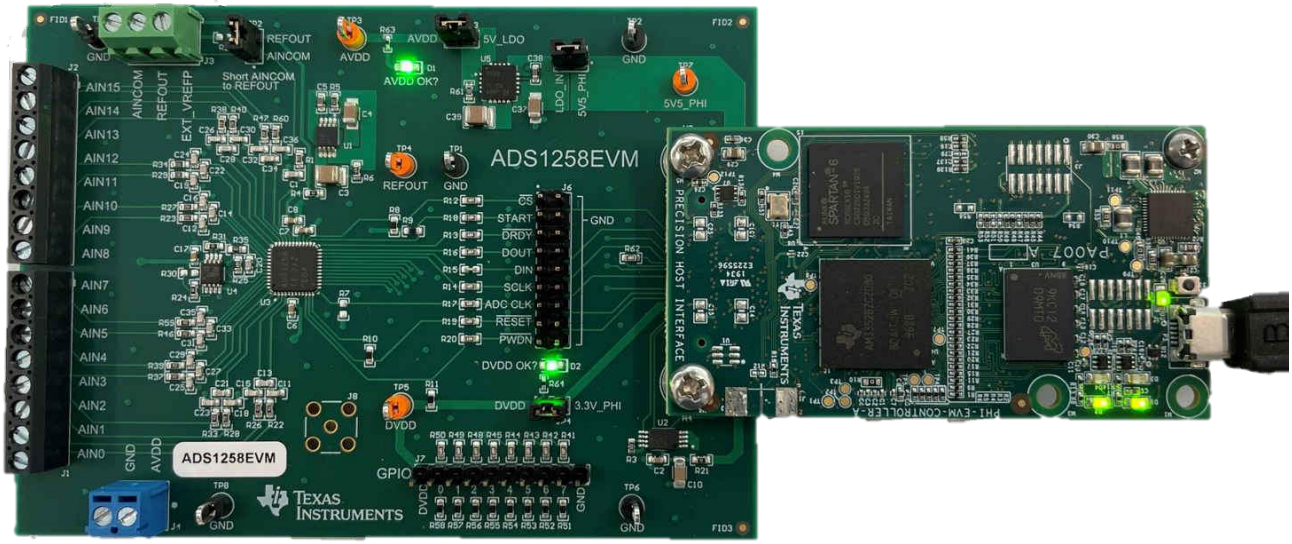
ADS1258EVM-PDK Evaluation Module

ABSTRACT

This user's guide describes the characteristics, operation, and use of the ADS1258 evaluation module (EVM). This EVM is an evaluation platform for the ADS1258, a 24-bit, 125-kSPS, 16-channel (multiplexed), delta-sigma (ΔΣ) analog-to-digital converter (ADC). The ADS1258 offers excellent noise performance, fast sampling speeds, a programmable channel sequencer, and access to the multiplexer output for efficient signal conditioning. The ADS1258EVM eases the evaluation of the device with hardware, software, and computer connectivity through the universal serial bus (USB) interface. This user's guide includes complete circuit descriptions, schematic diagrams, and a bill of materials. Throughout this document, the abbreviation *EVM* and the term *evaluation module* are synonymous with the ADS1258EVM.

Note

The ADS1258EVM and software can also support the 16-bit ADS1158 device. However, the user must manually remove the ADS1258 and install the ADS1158. See Section 8.3 for the location of the ADS1258 on the EVM. The ADS1158 is not discussed further in this document.



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1 ADS1258EVM Overview

The ADS1258EVM is a platform for evaluating the performance of the ADS1258, a 24-bit, 125-kSPS, 16-channel (multiplexed), ΔΣ ADC. The evaluation kit includes the ADS1258EVM and the precision host interface (PHI) controller board that enables the accompanying computer software to communicate with the ADC over USB for data capture and analysis. The ADS1258EVM includes the ADS1258 ADC as well as the high-performance peripheral analog circuits necessary to extract the best performance from the ADC. The PHI board primarily serves three functions:

- Provides a communication interface from the EVM to the computer through a USB port
- Provides the digital input and output signals necessary to communicate with the ADS1258
- Supplies power to all active circuitry on the ADS1258EVM board

1.1 ADS1258EVM Kit

The ADS1258 evaluation kit includes the following features:

- Hardware and software required for diagnostic testing as well as accurate performance evaluation of the ADS1258 ADC.
- USB powered: No external power supply is required.
- PHI controller that provides a convenient communication interface to the ADS1258 ADC over USB 2.0 (or higher) for power delivery as well as digital input and output.
- Microsoft® Windows® 8, and Windows 10 operating systems.
- Easy-to-use evaluation software for 64-bit Windows operating systems.
- The software suite includes graphical tools for data capture, histogram analysis, and spectral analysis. This suite also has a provision for exporting data to a text file for post-processing.

Figure 1-1 shows system connections for the EVM.

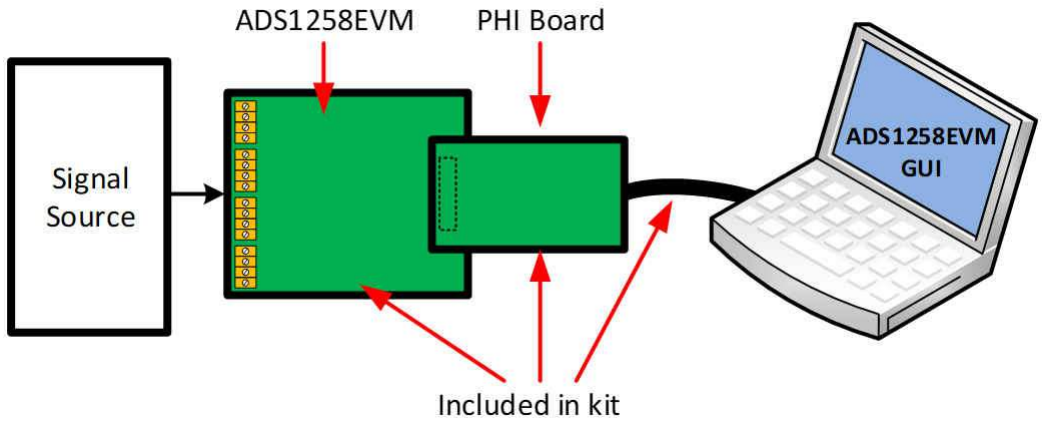

Figure 1-1. System Connection for Evaluation

1.2 ADS1258EVM

The ADS1258EVM includes the following features and configuration options:

- An OPA2320 precision amplifier buffer between the multiplexer output and ADC input, or bypass external circuitry
- Low-noise, low-drift, 2.5-V REF6025 as the default reference source, or use an external reference source
- A 16-MHz clock signal provided by the PHI controller, or use an external clock source
- Eight general-purpose input-output (GPIO) pins brought out to a dedicated header
- Ultra-low noise TPS7A4700 low-dropout (LDO) linear regulator supplies 5-V ADC analog voltage (AVDD), or use an external voltage supply
- 3.3-V ADC digital voltage (DVDD) supplied by PHI controller, or use external voltage supply
- Test points for power, GND, reference, and all digital signals to and from the PHI controller

2 Getting Started With the ADS1258EVM

The following list of instructions provides an overview to quickly get the ADS1258EVM set up and operational. The subsequent sections in this document expand on each step to explain in detail the available features on the EVM and the corresponding GUI. Links are provided to navigate from this quick-start guide to the appropriate section at each applicable step.

1. Remove the ADS1258EVM, PHI board, and USB cable from the ADS1258EVM-PDK box.
2. If necessary, connect the PHI board to the ADS1258EVM (see Figure 7-1).
3. Configure the ADS1258EVM:
   a. Power supplies (see Section 5).
   b. Clocking (see Section 3.4, if applicable).
   c. Voltage reference (see Section 3.5, if applicable)
4. Connect the micro-USB-to-USB cable from the PHI directly to a USB port on the computer. Do not connect the cable to the computer through a USB hub.
5. Open the latest version of the ADS1258EVM GUI on the connected computer.
   a. First-time users must download the latest version of the EVM GUI installer from the *Tools and Software* folder of the ADS1258EVM and run the GUI installer to install the EVM GUI software on the host computer.
6. Connect the analog input (see Section 3.1) to the input terminal blocks (J1-J2).
7. Capture and analyze data (see Section 7.2) using the GUI.

3 Analog Interface

The ADS1258EVM is designed for convenient interfacing with analog input signals. This section covers the details of the front-end circuit, including jumper configurations for different input test signals and board connectors for signal sources.

3.1 Analog Input Options

The ADS1258EVM allows for up to 16 single-ended inputs or eight differential inputs, as well as combinations of single-ended and differential inputs. As shown in Figure 3-1, connect analog input signals to terminal blocks J1 and J2 on the EVM.

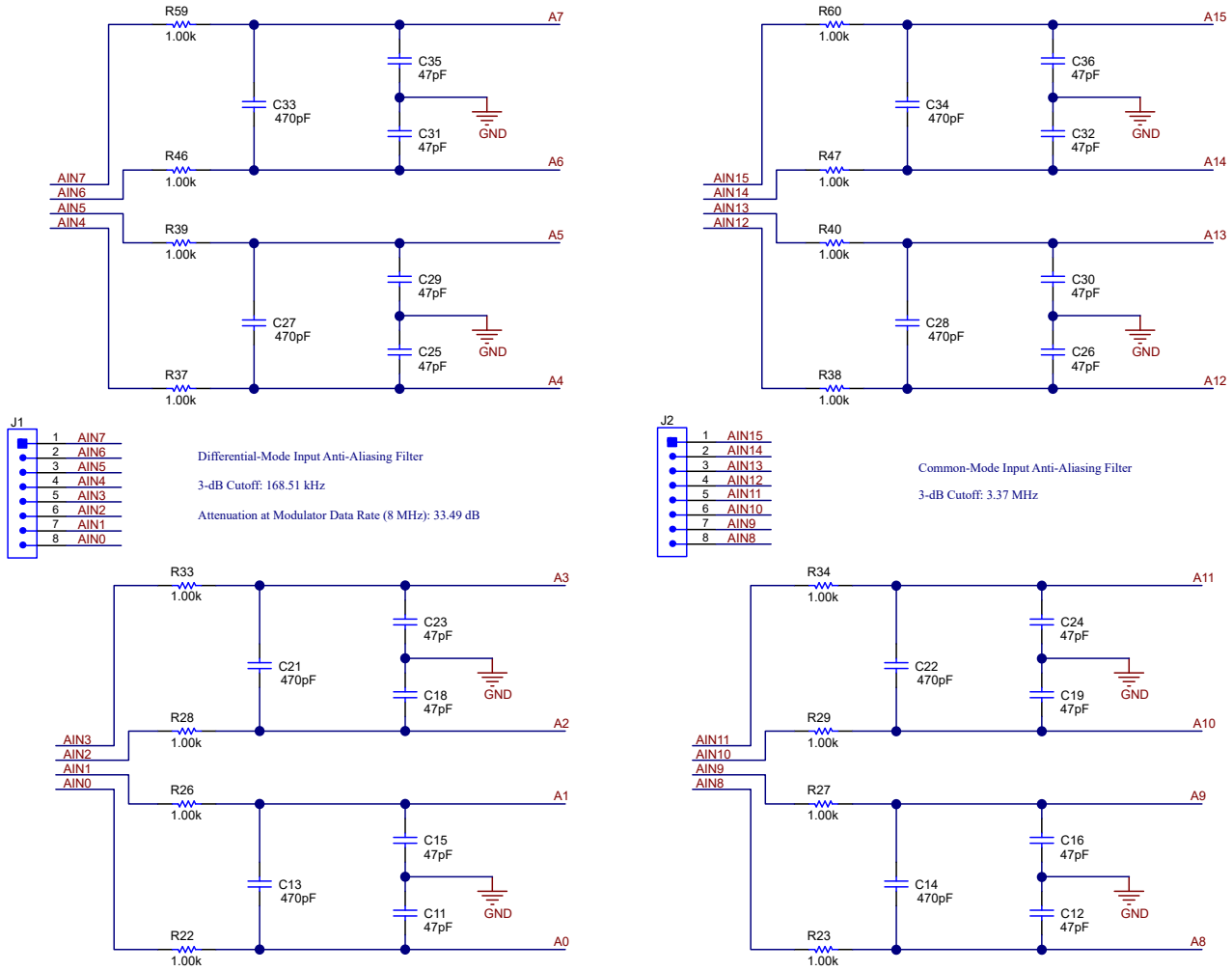

Figure 3-1. ADS1258EVM Analog Input Channels and Filtering

Each analog input signal passes through a set of low-pass filters to prevent aliasing. The differential filters have a 3-dB cutoff of 168.5 kHz, resulting in 33.49 dB of attenuation at the 8-MHz modulator frequency. As an example, Figure 3-1 shows that capacitor C13 and resistors R22 and R26 create the differential filter between analog inputs AIN0 and AIN1. The common-mode filters have a 3-dB cutoff of 3.37 MHz. As an example, Figure 3-1 shows that capacitor C11 and resistor R22 create the common-mode filter for analog input AIN0. Precision 5% C0G or NPO-type capacitors and 0.1% resistors are used in the analog signal chain to reduce measurement error.

Use adjacent input pins when measuring differential input signals to benefit from differential filtering and to achieve best performance. For example, AIN0 and AIN1 are set up for differential signaling because C13 connects these two inputs. Conversely, do not use AIN1 and AIN2 as a differential pair because there is no capacitor connecting these two inputs.

3.2 ADC Connections and Decoupling

Figure 3-2 shows all ADC connections. Each power-supply and reference connection have a 100-nF decoupling capacitor. Place these capacitors as close as possible to the ADC pins and make sure each component has a low-impedance connection to the GND plane.

Each digital pin of the ADC has a 49.9-Ω series resistor. These resistors smooth the edges of the digital signals so that the signals have minimal overshoot and ringing. A resistor is most important on the serial clock (SCLK) trace because the SCLK signal can toggle as quickly as 8 MHz. Resistors on the other pins are not strictly required, though these components can be included in the final design to improve digital signal integrity.

Pullup resistors R8, R9, R10, and R11 prevent $\overline{CS}$, START, $\overline{RESET}$, and $\overline{PWDN}$, respectively, from floating when not driven. The differential voltage across test points TP4 and ground is the reference voltage used by the ADC.

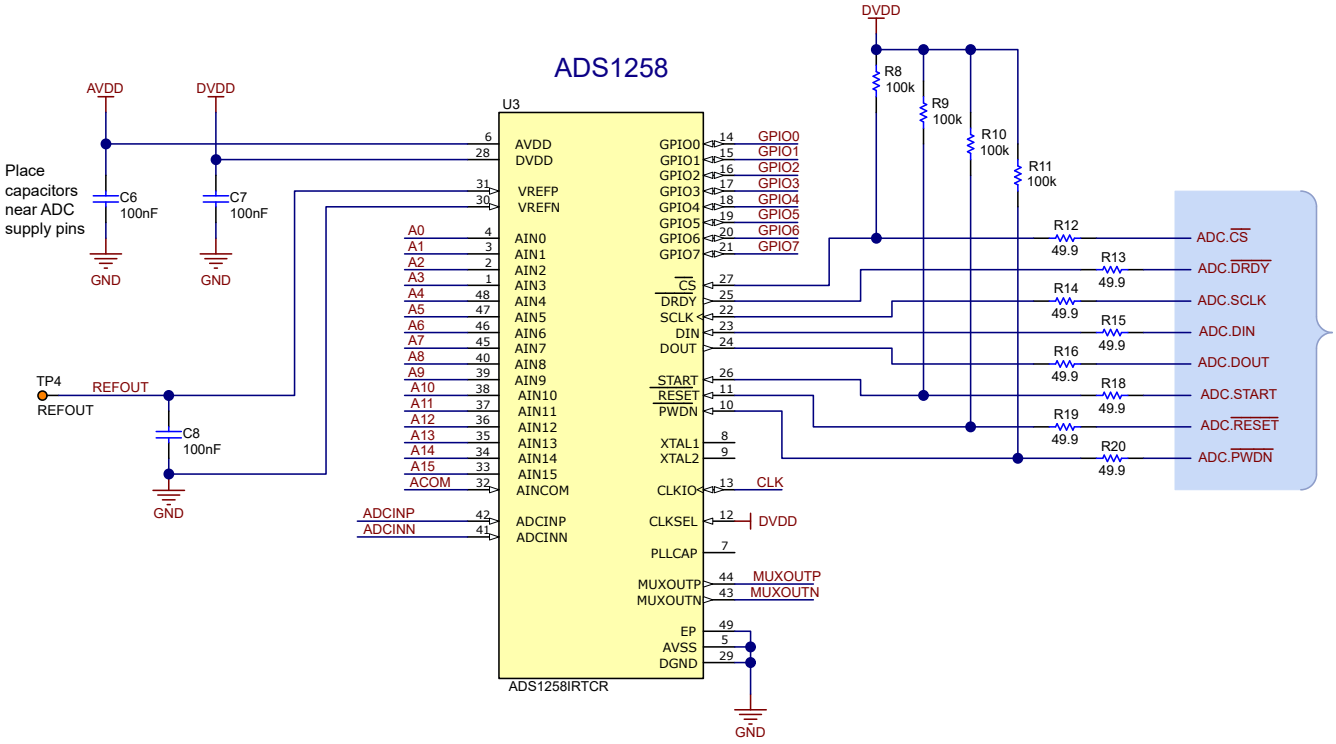

Figure 3-2. ADS1258EVM ADC Power-Supply Decoupling and Analog and Digital Connections

3.3 Configurable Multiplexer Loop

The ADS1258 multiplexer has optional differential output connections (MUXOUTx) that enable a single signal-conditioning circuit to be used for all analog inputs. The default signal conditioning circuit is a differential unity-gain buffer (OPA2320) between each MUXOUTx and ADCINx pin. A low-pass filter is connected to the output of the buffer. As shown in Figure 3-3, capacitor C20 is used to bypass the ADC sampling currents and resistors R25 and R35 are used to isolate the op-amp outputs from the filter capacitor.

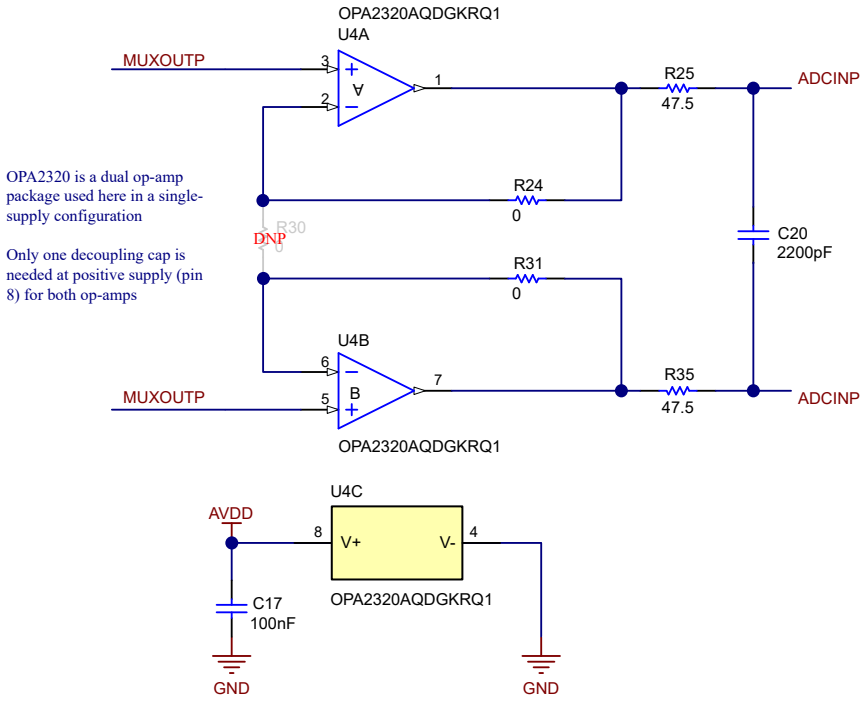

Figure 3-3. ADS1258EVM Configurable Multiplexer Loop With a Signal-Conditioning Circuit

The signal-conditioning circuit shown in Figure 3-3 can also be configured into a differential-input, differential-output gain stage by changing resistors R24, R30, and R31 as per Equation 1.

$$G = 1 + 2 \times (R24) / R30 \quad (1)$$

Importantly, Equation 1 assumes that R31 = R24.

As an example, replacing R24 and R31 with 10-kΩ resistors and R30 with a 2.2-kΩ resistor creates a gain of 10 V/V between the MUXOUTx and ADCINx pins. Choose R24, R30, and R31 to be size 0603 resistors with a tolerance ≤0.1% to maintain system accuracy.

Enable the multiplexer loop by setting BYPAS = 1 in the CONFIG0 register. To bypass the multiplexer loop, set BYPAS = 0. One important caveat to the multiplexer bypass option is that the signal-conditioning circuit is only disconnected from the ADCINx pins. In other words, the signal-conditioning circuit is still connected to the MUXOUTx pins regardless of the state of the BYPAS bit.

3.3.1 Measuring Single-Ended Inputs Using a Pseudo-Differential Configuration

Both the buffer or gain stage configuration can be used to directly measure true differential input signals. Measuring single-ended inputs requires additional consideration because the OPA2320 is powered by a unipolar, 5-V supply. Additionally, the OPA2320 requires up to 45 mV of headroom between the output voltage and either supply (V+ or V–). These two limitations restrict the ability of the default amplifier circuit shown in Figure 3-3 to measure single-ended signals referenced to ground. Instead, the amplifier negative input (MUXOUTN) must be level-shifted to a mid-supply voltage. This type of measurement is referred to as pseudo-differential, or a measurement with respect to some fixed voltage above ground.

Implement a pseudo-differential measurement on the ADS1258EVM by shorting the 2.5-V REFOUT voltage to the appropriate channel. In Auto-Scan mode, use jumper JP2 to short REFOUT to AINCOM because AINCOM

is used as the negative channel for all single-ended measurements. In Fixed-Channel mode, short REFOUT to whichever analog input is selected as AINN in the MUXSCH register. This short can be applied externally using terminal block J3. Figure 3-4 shows both JP2 and J3.

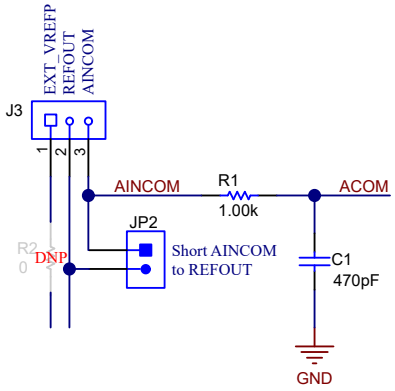

Figure 3-4. Shorting AINCOM to REFOUT

A pseudo-differential measurement only sets the voltage on the MUXOUTN pin to be within the amplifier output voltage limits. The user must also make sure that the voltage applied to the ADCINP pin is within this same range. To measure signals that are outside of the amplifier output voltage limitations, consider bypassing the external multiplexer loop as described in Section 3.3.

3.4 Clocking

The ADS1258 requires a high-frequency system clock to oversample the inputs and provide digital data at the output data rate. By default, a 16-MHz system clock is provided by the PHI controller board. The PHI also generates the SCLK signal from the same clock domain, which improves overall ADC performance.

An external clock can also be used with the ADS1258EVM, though this setup requires altering the EVM components. First, install SMA connector J8, then remove termination resistor R17 and install this component at R7. Figure 3-5 shows the external clocking circuit. See the ADS1258 data sheet for information about the allowable clock frequency range.

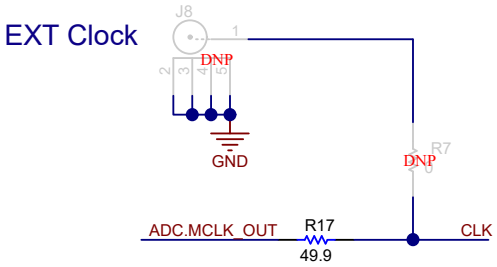

Figure 3-5. ADS1258EVM Clock Circuit

3.5 Voltage Reference

The ADS1258EVM requires a precision reference voltage to accurately convert the analog inputs to digital outputs. Figure 3-6 shows the EVM voltage reference circuitry.

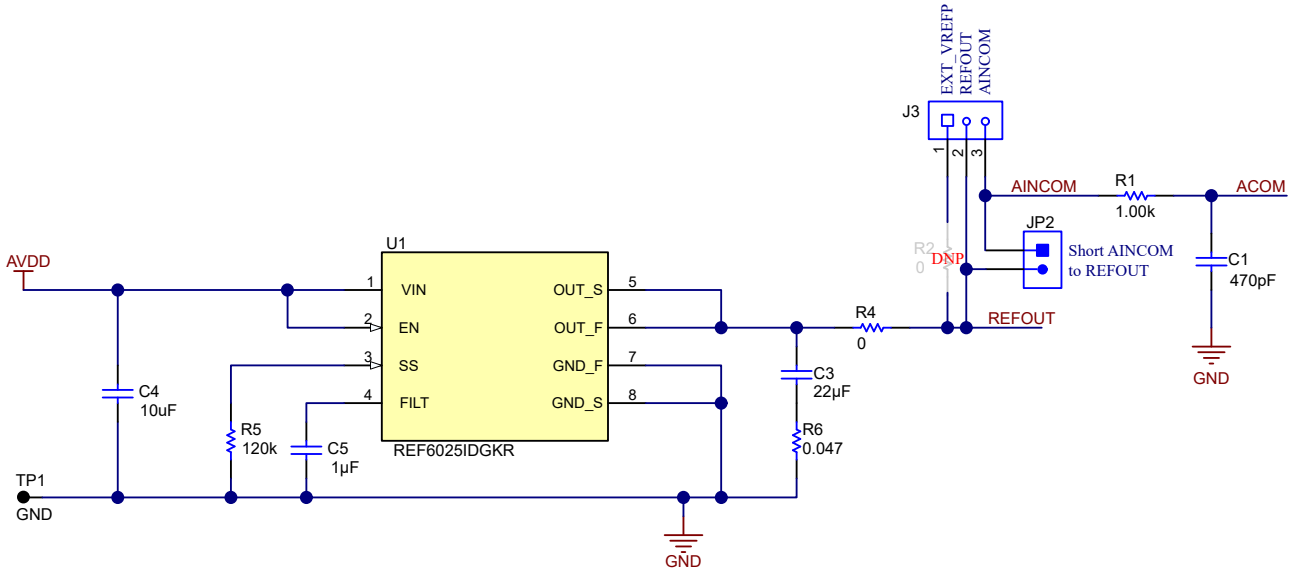

Figure 3-6. ADS1258EVM Voltage Reference Circuit

The EVM includes two options to provide a reference voltage to the ADC. The first option is an installed component: the low-noise, low-drift, buffered-output REF6025. This discrete voltage reference outputs a voltage of 2.5 V to the ADC reference pins (REFOUT and ground). Additionally, the REF6025 output voltage is also connected to the J3 terminal block as REFOUT.

The second voltage reference option on the EVM is to use an external voltage source. An external component can be useful if a reference voltage other than 2.5 V is required. Configure the EVM for an external voltage reference by moving the 0-Ω resistor at R4 to R2. Then connect EXT_VREFP on J3 to the external reference output voltage, and connect the external reference ground to the EVM ground. REFOUT on J3 is shorted to EXT_VREFP to make sure that the reference voltage can still be used to bias external circuitry. See the ADS1258 data sheet for information about the allowable voltage range on the VREFx pins.

4 Digital Interface

As noted in Section 1, the EVM interfaces with the PHI and communicates with the host over USB. Figure 4-1 shows how the PHI communicates with two devices on the EVM: the ADS1258 using the serial peripheral interface (SPI) and the EEPROM using the inter-integrated circuit (I^2C) interface. The EEPROM comes preprogrammed with the information required to configure and initialize the ADS1258EVM. When the hardware is initialized, no further communication with the EEPROM is necessary and this device can be ignored by the user.

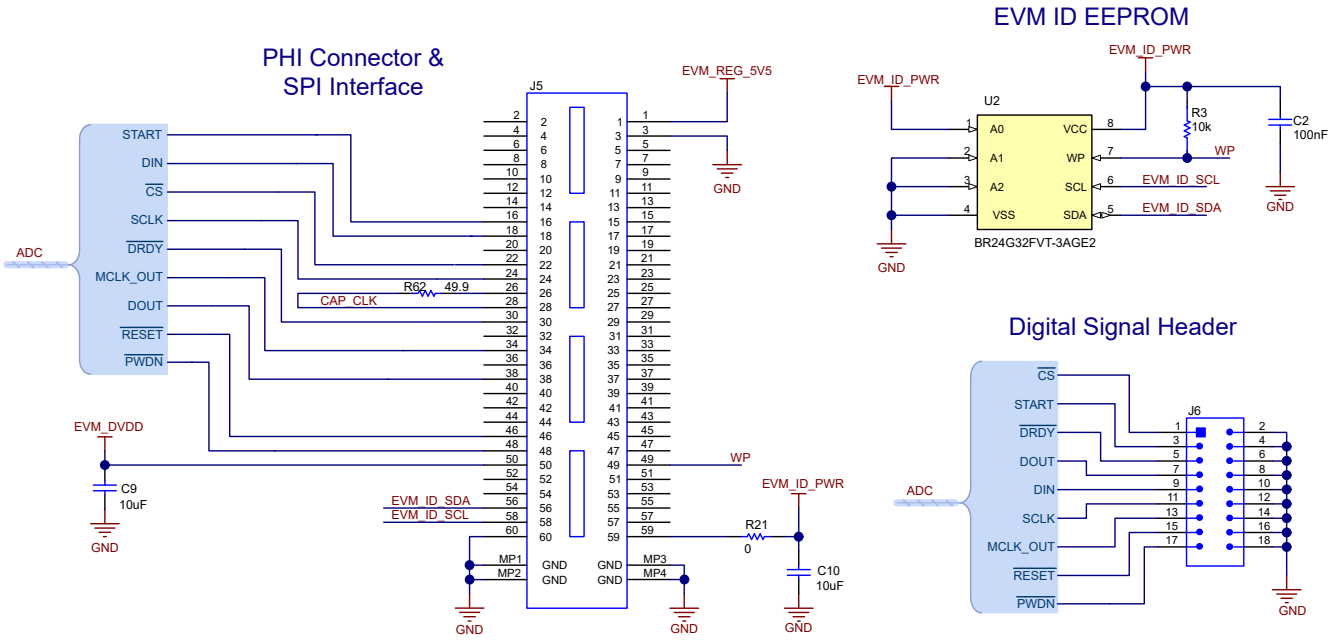

Figure 4-1. ADS1258EVM Digital Interface Connections (SPI and I^2C)

The ADS1258 communicates with the PHI using an SPI interface in mode 00 (CPOL = 0, CPHA = 0). Header J6 in Figure 4-1 provides test points for all digital signals to and from the PHI controller. The test points can be connected to a logic analyzer for convenient visualization of the digital signals. These test points can also be used to communicate with the ADS1258EVM using an external controller.

4.1 GPIO

The ADS1258 has eight dedicated GPIO pins. The EVM connects a 100-kΩ pulldown resistor to each GPIO pin. These resistors prevent the pin voltage from floating because the default ADC settings configure each GPIO as an input. Additionally, 49.9-Ω resistors are placed in series with each GPIO pin to limit current flow into the ADC. All eight GPIO pins are terminated at header J7 for easy connection to external circuitry if desired. Figure 4-2 shows the GPIO circuitry.

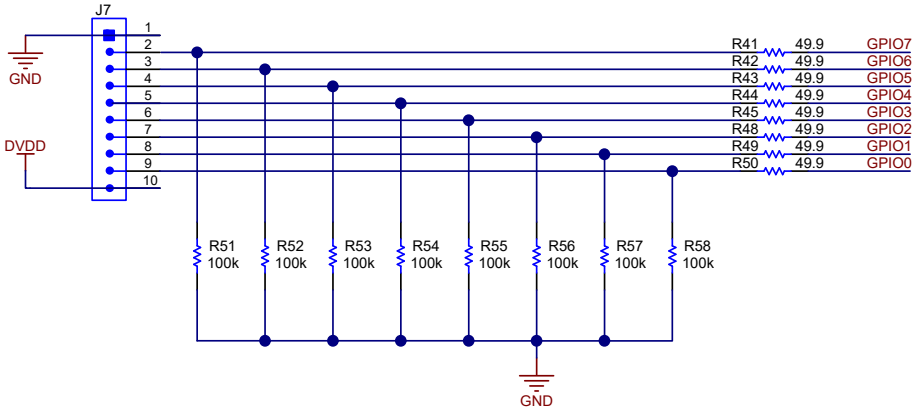

Figure 4-2. ADS1258EVM GPIO Circuit and Header

5 Power Supplies

The default ADC power-supply voltages (DVDD and AVDD) are generated by the PHI controller using power from the USB. The PHI provides 3.3-V and 5.5-V power rails. The 3.3-V power rail directly supplies the ADC DVDD voltage. The 5.5-V power rail is supplied to the input of the TPS7A4700, a low-noise, configurable-output LDO, to supply AVDD. The LDO output voltage depends on the internal reference voltage (V_{LDO_REF}) of 1.4 V and the pin connections. Grounding any LDO pin between pins 4 through pin 12 adds that pin voltage to V_{LDO_REF} and increases the LDO output voltage, LDO_{VOUT}. Figure 5-1 shows that the ADS1258EVM grounds pins 6 and 10 (3P2V and 0P4V, respectively) to set LDO_{VOUT} equal to 5 V.

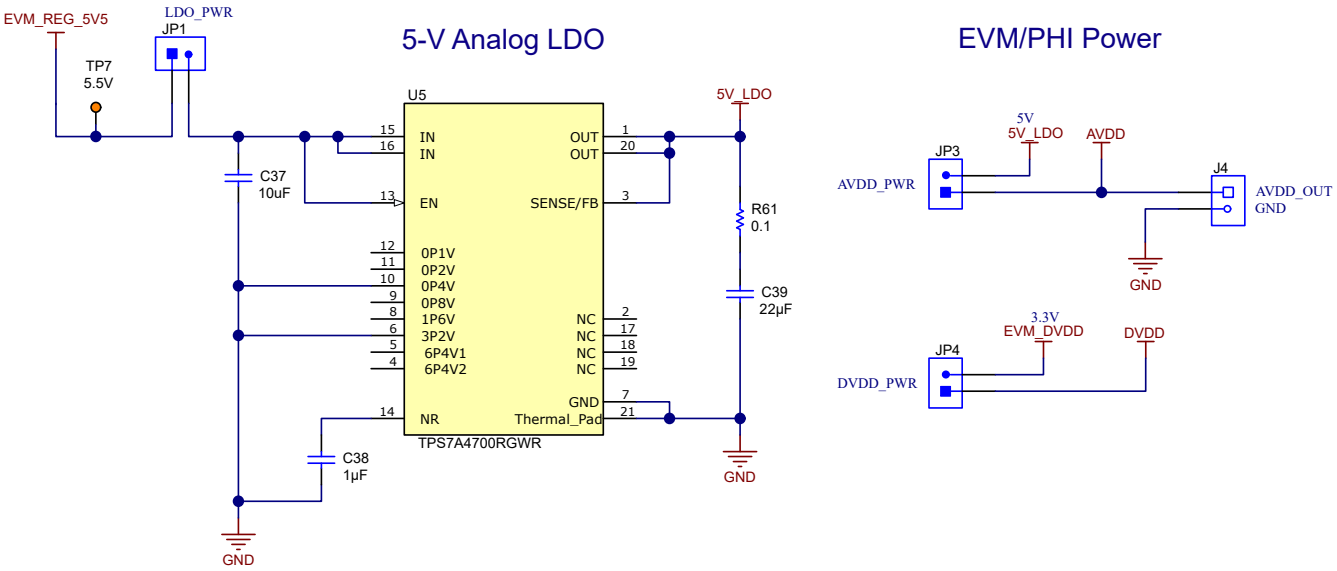

Figure 5-1. ADS1258EVM LDO Circuit and External Power Source Connections

Figure 5-1 shows that the 5V_LDO output is used for the AVDD connections across the EVM. Additionally, the user can measure the AVDD current by connecting an ammeter between pins 1 and 2 of JP3 or the DVDD current by connecting an ammeter between pins 1 and 2 of JP4.

External power sources can also be provided for each supply voltage:

- LDO: Remove the shunt on JP1 and connect external power to JP1:2
- AVDD: Remove the shunt on JP3 and connect external power to JP3:1
- DVDD: Remove the shunt on JP4 and connect external power to JP4:1

When using either internal or external power supplies, LEDs D1 and D2 indicate if power is connected to AVDD and DVDD, respectively. These LEDs do not necessarily indicate if AVDD is 5 V or if DVDD s 3.3 V. Check the AVDD voltage using test point TP3 and check the DVDD voltage using test point TP5. Figure 5-2 shows the portion of the ADS1258EVM schematic that includes the LEDs and test points.

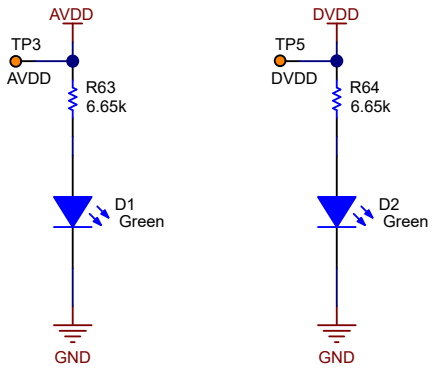

Figure 5-2. ADS1258EVM AVDD and DVDD Indicator LEDs

6 Software Installation

Download the latest version of the EVM GUI installer from the *Tools and Software* folder of the ADS1258EVM and run the GUI installer to install the EVM GUI software on the computer.

CAUTION

Manually disable any antivirus software running on the computer before downloading the EVM GUI installer onto the local hard disk. Depending on the antivirus settings, an error message may appear or the *installer.exe* file may be deleted.

As shown in Figure 6-1, accept the license agreements and follow the on-screen instructions to complete the installation.

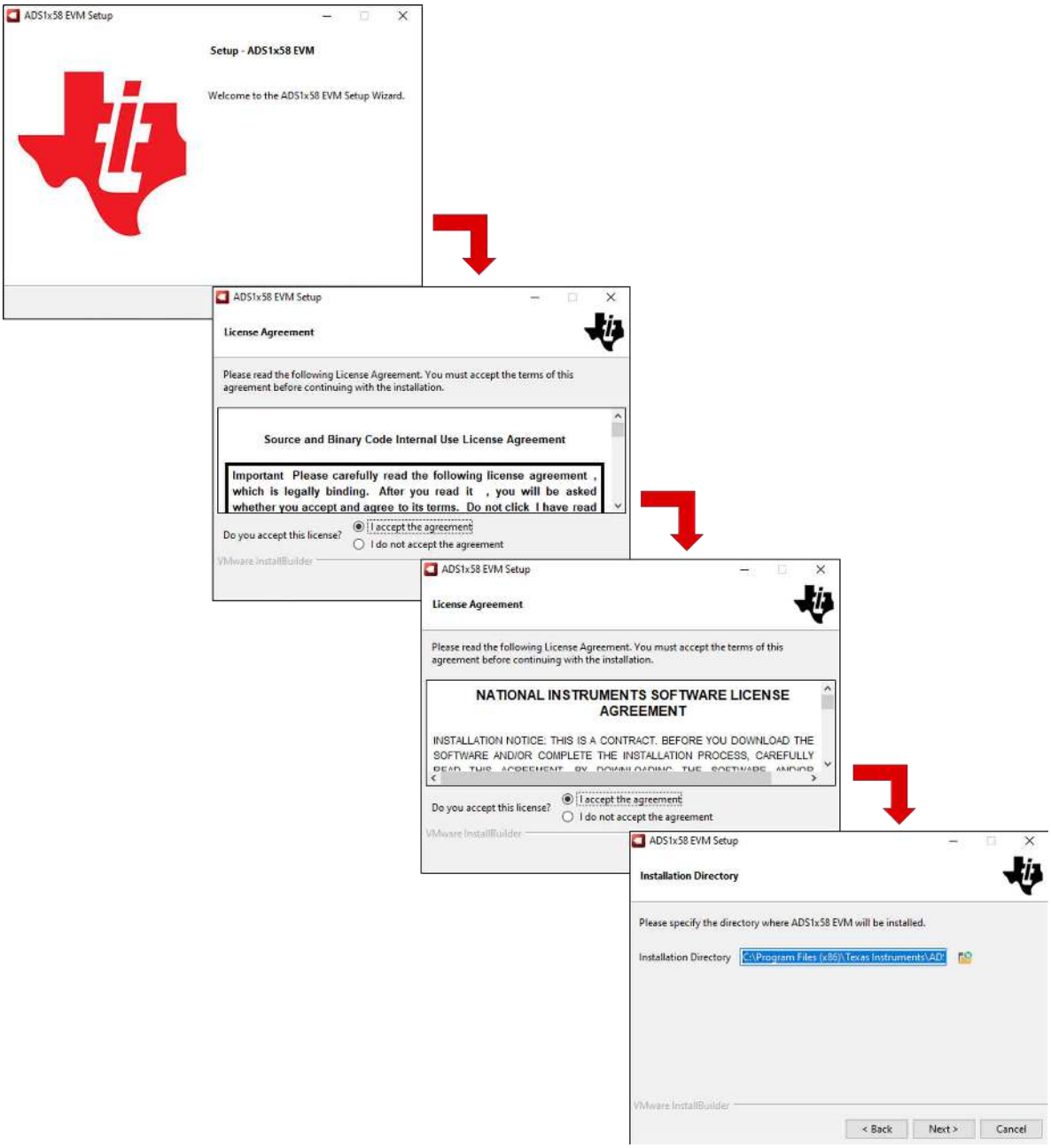

Figure 6-1. Software Installation and Prompts

As a part of the ADS1258EVM GUI installation, a prompt with a *Device Driver Installation*, as shown in Figure 6-2, appears on the screen. Click *Next* to proceed.

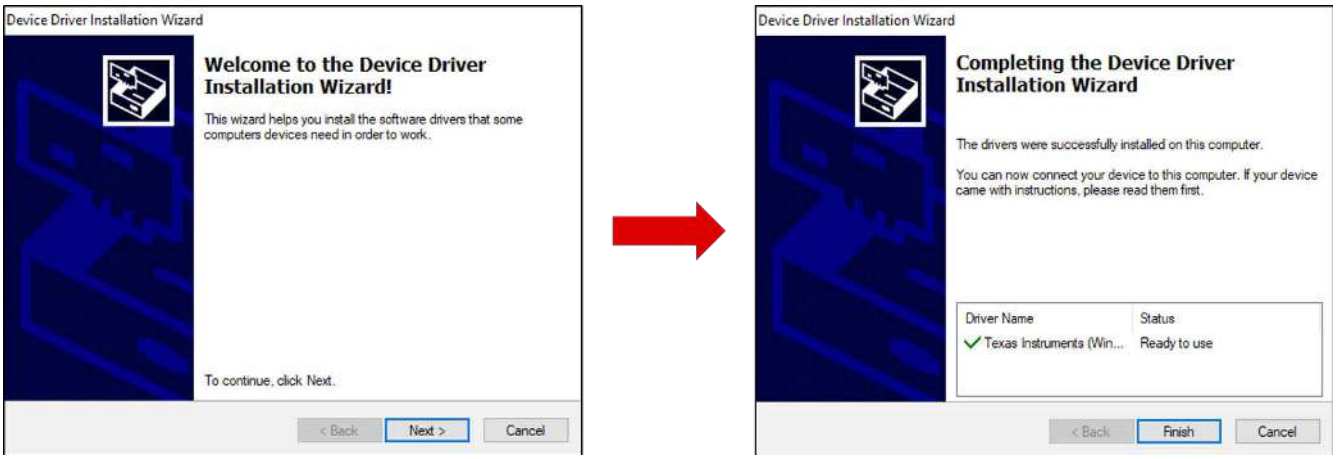

Figure 6-2. Device Driver Installation and Prompts

The ADS1258EVM requires the LabVIEW™ run-time engine and can prompt for the installation of this software, as shown in Figure 6-3, if not already installed.

Figure 6-3. LabVIEW Run-Time Engine Installation

7 EVM Operation and GUI

7.1 Connecting the Hardware

Connect the EVM as shown in Figure 7-1 after installing the software:

1. Physically connect P2 of the PHI to J5 of the ADS1258EVM. Install the screws to make a robust connection.
2. Connect the USB cable from the computer to the PHI:
   a. LED D5 on the PHI lights up, indicating that the PHI is powered up.
   b. LEDs D1 and D2 on the PHI start blinking to indicate that the PHI is booted up and communicating with the PC. Figure 7-1 shows the resulting LED indicators.
3. Start the software GUI as shown in Figure 7-2. The LEDs blink slowly as the FPGA firmware is loaded on the PHI. This loading takes a few seconds and then the AVDD and DVDD power supplies turn on, as indicated by LEDs D1 and D2 on the ADS1258EVM.
4. Connect the input signal using terminal blocks J1 and J2. The input range is 0 V to 5 V with the multiplexer loop bypassed. See Section 3.3 for the input range limitations when the multiplexer loop is enabled.

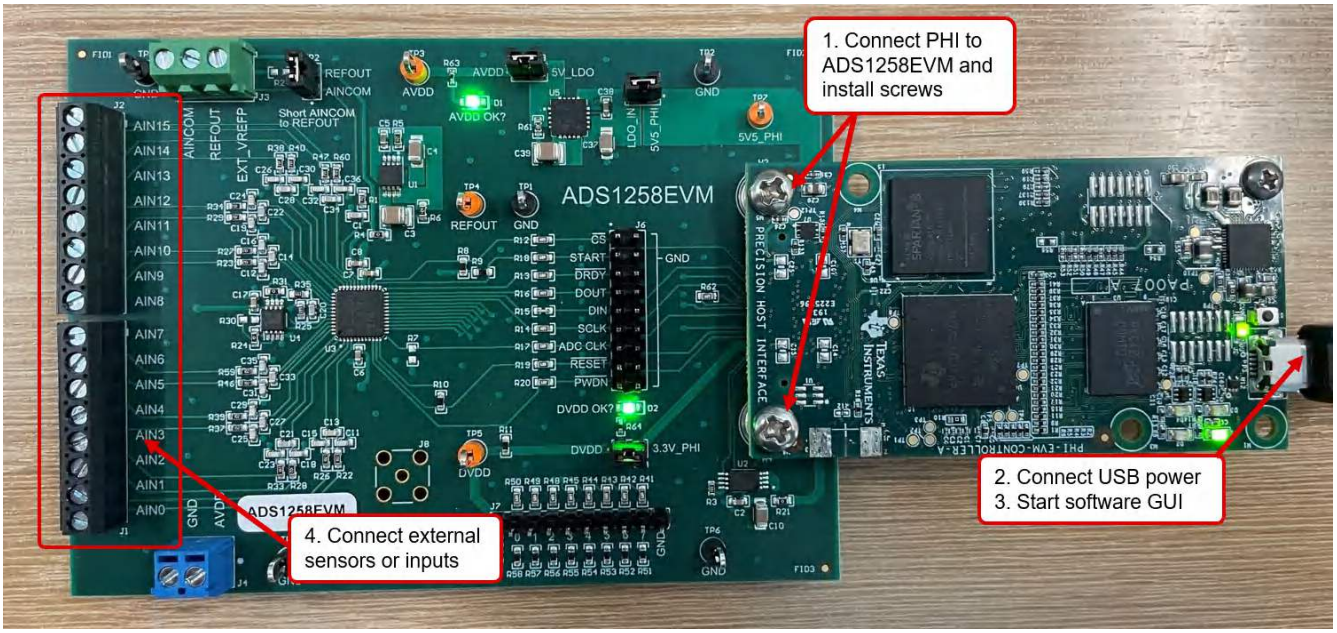

Figure 7-1. ADS1258EVM Hardware Connections

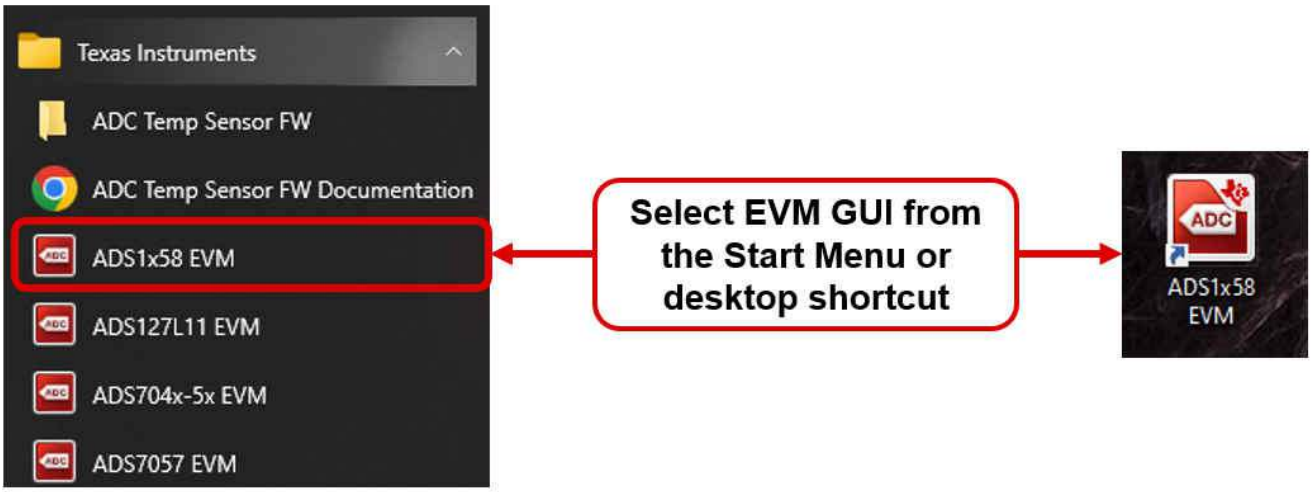

Figure 7-2. Launch the EVM GUI Software

7.2 EVM GUI Global Settings for ADC Control

Figure 7-3 shows that the EVM global controls are located on the left side of the GUI. These controls include the sampling mode, data rate, MUXOUT connection, switch time delay, channel selection, number of samples, and others. The *Pages* control in the upper-left corner allows access to the other pages in the GUI. Figure 7-3 also shows the available ADC register settings. The registers can be used to configure the ADC data rate, channel sequencer, or integrated features. Change the register settings by clicking on each bit, typing a value directly into the *Value* column, or by selecting from the drop-down menus in the *Field View* control.

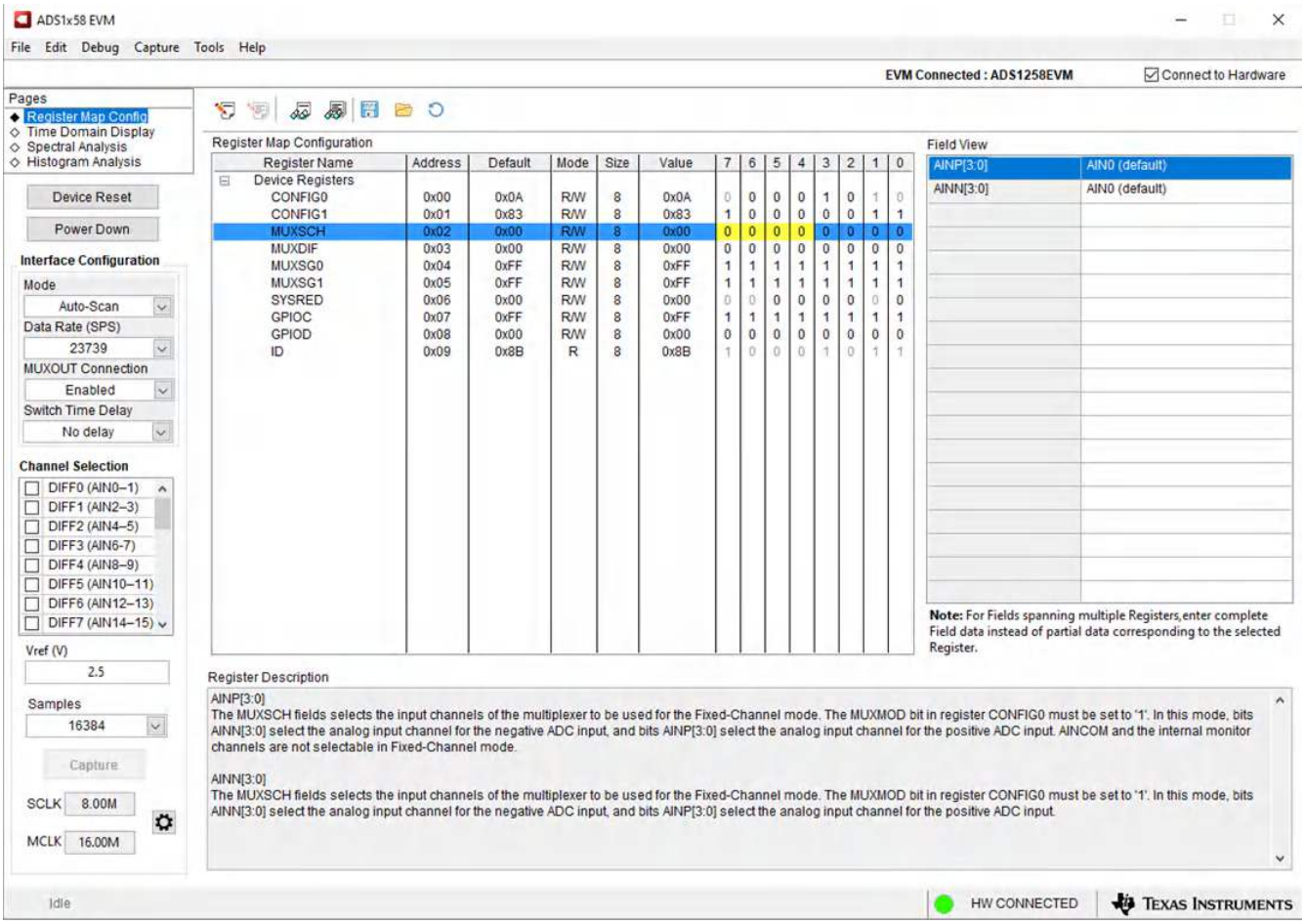

Figure 7-3. ADS1258EVM GUI Global Settings for ADC Control Page

7.3 Time-Domain Display

The time-domain display tool allows visualization of the ADC response to a given input signal. This tool is useful for studying the behavior of and debugging any gross problems with the ADC or drive circuits. Trigger a data capture of the selected number of samples from the ADS1258EVM by using the *Capture* button in Figure 7-4. The captured data are subject to the current interface mode settings. The time-domain plot has *Samples* on the x-axis and by default shows the corresponding *Codes* on the y-axis relative to the specified reference voltage. The y-axis units can also be changed to *Voltage/Temp/Gain* using the *Unit* control in the bottom right. The *Temp* and *Gain* units are only used with the Temp and Gain channel selections, respectively.

The *Measurements* control on the bottom of Figure 7-4 calculates the code range, the mean code, and the code standard deviation. Switching pages to any of the *Analysis* tools described in the subsequent sections causes calculations to be performed on the same set of data.

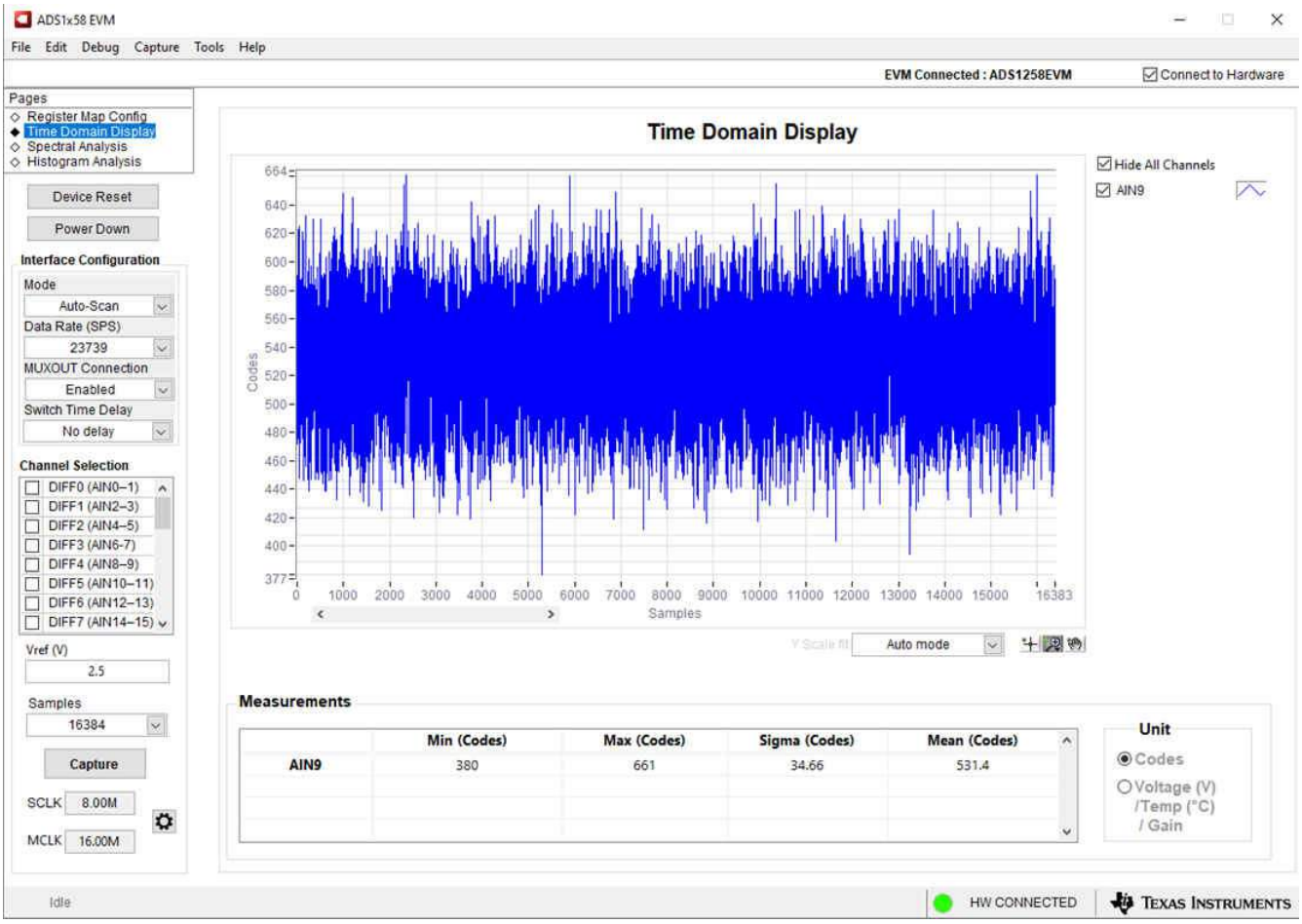

Figure 7-4. ADS1258EVM GUI Time Domain Display Page

7.4 Frequency-Domain Display

Figure 7-5 shows the spectral analysis tool that evaluates the dynamic performance (SNR, THD, SFDR, SINAD, and ENOB) of the ADS1258. This dynamic performance is calculated by single-tone sinusoidal signal FFT analysis using the 7-term Blackman-Harris window setting. The FFT tool includes windowing options that are required to mitigate the effects of non-coherent sampling (this discussion is beyond the scope of this document). The 7-term Blackman-Harris window is the default option and has sufficient dynamic range to resolve the frequency components of a 24-bit ADC. The *None* option corresponds to not using a window (or using a rectangular window) and is not recommended.

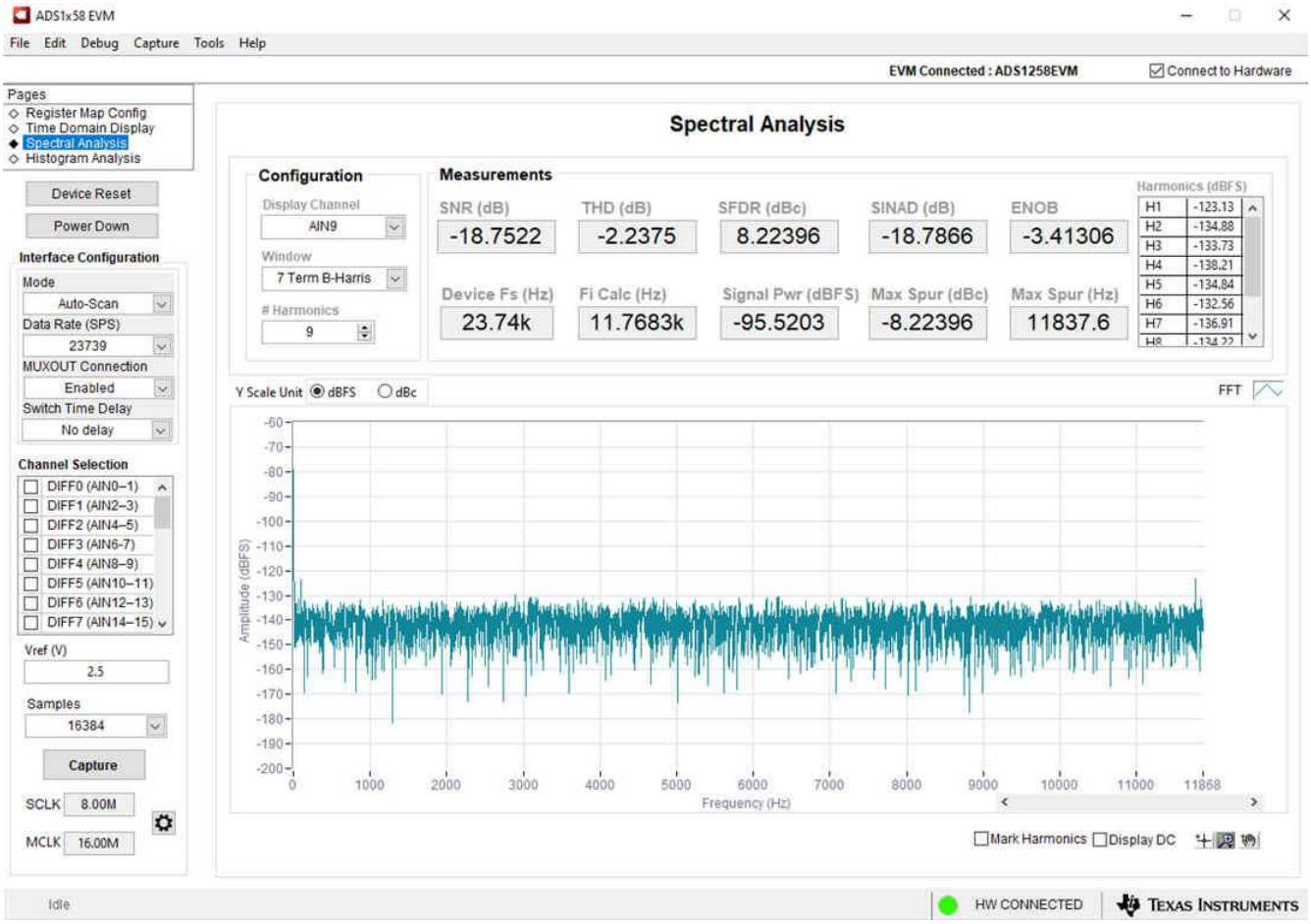

Figure 7-5. ADS1258EVM GUI Frequency Domain Display Page

7.5 Histogram Display

Noise degrades ADC resolution and the histogram tool shown in Figure 7-6 can be used to estimate effective resolution. Effective resolution is a metric describing the ADC resolution loss resulting from noise generated by the various sources connected to the ADC when measuring a dc signal. The cumulative effect of noise coupling to the ADC output from sources such as the input drive circuits, the reference drive circuit, the ADC power supply, and the ADC is reflected in the standard deviation of the ADC output code histogram that is obtained by performing multiple conversions of a dc input applied to a given channel.

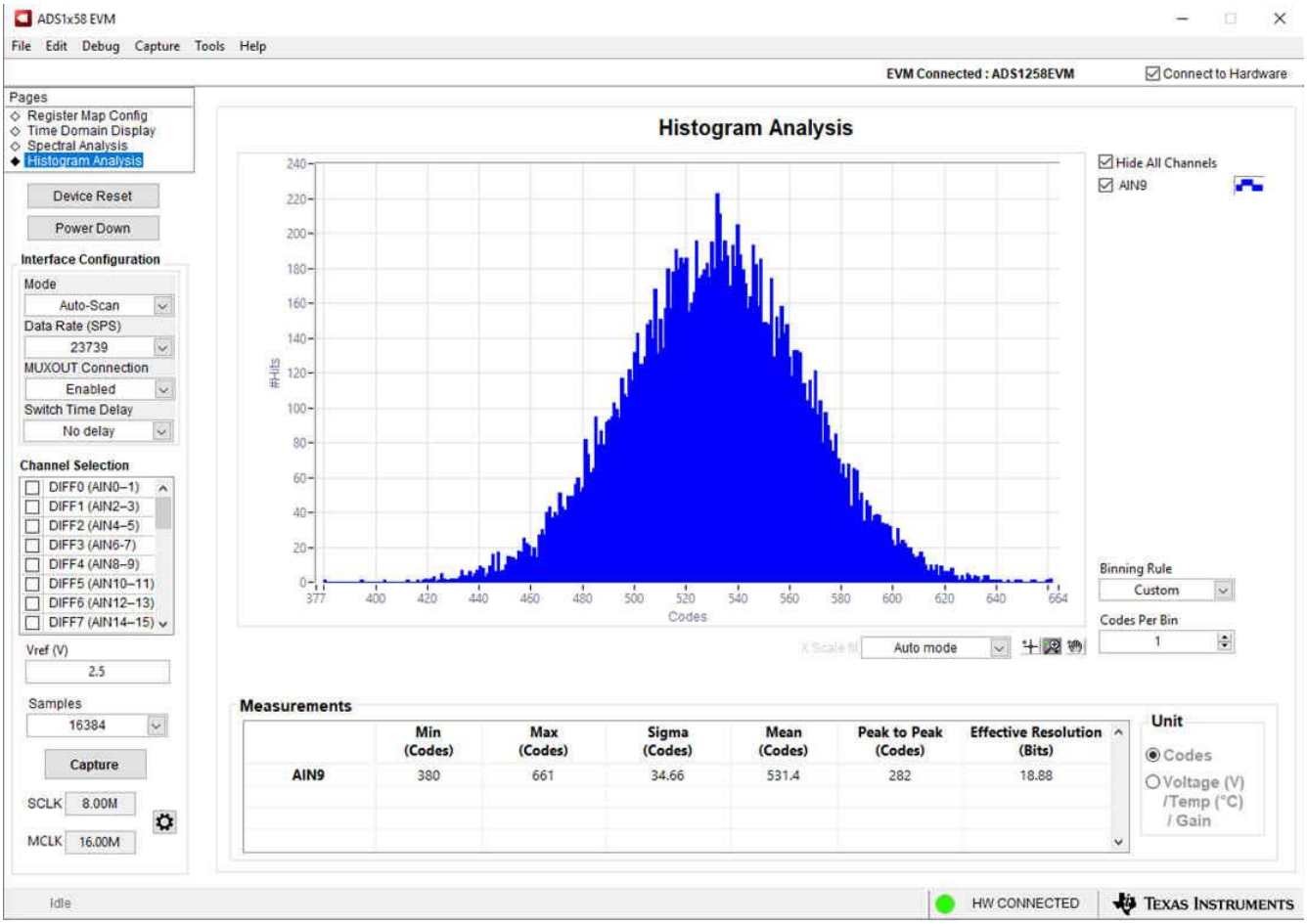

Figure 7-6. ADS1258EVM GUI Histogram Display Page

8 Bill of Materials, Layout, and Schematics

8.1 Bill of Materials

Table 8-1 lists the bill of materials (BOM) for the ADS1258EVM.

Table 8-1. Bill of Materials

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
C1, C13, C14, C21, C22, C27, C28, C33, C34	9	470 pF	CAP, CERM, 470 pF, 50 V, +/- 5%, C0G/NP0, 0603	0603	06035A471JAT2A	AVX
C2, C6, C7, C8, C17	5	0.1 uF	CAP, CERM, 0.1 uF, 25 V, +/- 5%, X7R, 0603	0603	C0603C104J3RACTU	Kemet
C3, C39	2	22 uF	CAP, CERM, 22 µF, 25 V,+/- 10%, X7R, 1210	1210	CL32B226KAJNFNE	Samsung Electro-Mechanics
C4, C9, C10, C37	4	10 uF	CAP, CERM, 10 uF, 25 V, +/- 10%, X7R, 1206_190	1206_190	C1206C106K3RACTU	Kemet
C5, C38	2	1 uF	CAP, CERM, 1 µF, 16 V,+/- 10%, X7R, AEC-Q200 Grade 1, 0603	0603	CGA3E1X7R1C105K080AC	TDK
C11, C12, C15, C16, C18, C19, C23, C24, C25, C26, C29, C30, C31, C32, C35, C36	16	47 pF	CAP, CERM, 47 pF, 50 V, +/- 5%, C0G/NP0, 0603	0603	C0603C470J5GACTU	Kemet
C20	1	2200 pF	CAP, CERM, 2200 pF, 50 V, +/- 5%, C0G/NP0, 0603	0603	GRM1885C1H222JA01D	MuRata
D1, D2	2	Green	LED, Green, SMD	LED_0805	APT2012LZGCK	Kingbright
H1, H2	2		Machine Screw Pan PHILLIPS M3		RM3X4MM 2701	APM HEXSEAL
H3, H4	2		ROUND STANDOFF M3 STEEL 5MM	ROUND STANDOFF M3 STEEL 5MM	9774050360R	Wurth Elektronik
H5, H6, H7, H8	4		Bumpon, Cylindrical, 0.312 X 0.200, Black	Black Bumpon	SJ61A1	3M
J1, J2	2		Terminal Block, 3.5mm, 8-Pos, TH	Terminal Block, 3.5mm, 8-Pos, TH	ED555/8DS	On-Shore Technology
J3	1		Terminal Block, 3.5mm, 3x1, Tin, TH	Terminal Block, 3.5mm, 3x1, Tin, TH	691214110003	Wurth Elektronik
J4	1		Terminal Block, 2x1, 3.5mm, TH	2x1 Terminal Block	OSTTE020161	On-Shore Technology
J5	1		Header(Shrouded), 19.7mil, 30x2, Gold, SMT	Header (Shrouded), 19.7mil, 30x2, SMT	QTH-030-01-L-D-A	Samtec
J6	1		Header, 100mil, 9x2, Gold, TH	9x2 Header	TSW-109-07-G-D	Samtec
J7	1		Header, 100mil, 10x1, Gold, TH	10x1 Header	TSW-110-07-G-S	Samtec

Table 8-1. Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
JP1, JP2, JP3, JP4	4		Header, 100mil, 2x1, Gold, TH	2x1 Header	TSW-102-07-G-S	Samtec
R1, R22, R23, R26, R27, R28, R29, R33, R34, R37, R38, R39, R40, R46, R47, R59, R60	17	1.00 k	RES, 1.00 k, 0.1%, 0.1 W, 0603	0603	RT0603BRD071KL	Yageo America
R3	1	10 k	Res Thin Film 0603 10K Ohm 0.1% 1/10W ±10ppm/°C Molded SMD SMD Punched Carrier T/R	0603	ERA-3ARB103V	Panasonic
R4, R21, R24, R31	4	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	ERJ-3GEY0R00V	Panasonic
R5	1	120 k	RES, 120 k, 0.1%, 0.1 W, 0603	0603	RG1608P-124-B-T5	Susumu Co Ltd
R6	1	0.047	RES, 0.047, 1%, 0.1 W, AEC-Q200 Grade 1, 0603	0603	ERJ-L03KF47MV	Panasonic
R8, R9, R10, R11, R51, R52, R53, R54, R55, R56, R57, R58	12	100 k	RES, 100 k, 0.5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW0603100KDHEAP	Vishay-Dale
R12, R13, R14, R15, R16, R17, R18, R19, R20, R41, R42, R43, R44, R45, R48, R49, R50, R62	18	49.9	RES, 49.9, 0.5%, 0.1 W, 0603	0603	RT0603DRE0749R9L	Yageo America
R25, R35	2	47.5	RES, 47.5, 0.1%, 0.1 W, 0603	0603	RT0603BRD0747R5L	Yageo America
R61	1	0.1	RES, 0.1, 1%, 0.1 W, AEC-Q200 Grade 1, 0603	0603	ERJ-L03KF10CV	Panasonic
R63, R64	2	6.65 k	RES, 6.65 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04026K65FKED	Vishay-Dale
SH-J1, SH-J2, SH-J3, SH-J4	4	1x2	Shunt, 100mil, Flash Gold, Black	Closed Top 100mil Shunt	SPC02SYAN	Sullins Connector Solutions
TP1, TP2, TP6, TP8, TP9	5		Test Point, Multipurpose, Black, TH	Black Multipurpose Testpoint	5011	Keystone Electronics
TP3, TP4, TP5, TP7	4		Test Point, Multipurpose, Orange, TH	Orange Multipurpose Testpoint	5013	Keystone Electronics

Table 8-1. Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
U1	1		5ppm/C High-Precision Voltage Reference with Integrated High-Bandwidth Buffer, DGK0008A (VSSOP-8)	DGK0008A	REF6025IDGKR	Texas Instruments
U2	1		I2C BUS EEPROM (2-Wire), TSSOP-B8	TSSOP-8	BR24G32FVT-3AGE2	Rohm
U3	1		24 Bit Analog to Digital Converter 8, 16 Input 1 Sigma-Delta 48-VQFN (7x7)	VQFN48	ADS1258IRTCR	Texas Instruments
U4	1		Automotive Qualified Precision, Zero-Crossover, 20MHz, 0.9pA Ib, RRIO, CMOS Operational Amplifier, DGK0008A (VSSOP-8)	DGK0008A	OPA2320AQDGKRQ1	Texas Instruments
U5	1		36-V, 1-A, 4.17-µVRMS, RF low-dropout (LDO) voltage regulator 20-VQFN -40 to 125	VQFN20	TPS7A4700RGWR	Texas Instruments
J8	0		SMA Straight Jack, Gold, 50 Ohm, TH	SMA Straight Jack, TH	901-144-8RFX	Amphenol RF
R2, R7, R30	0	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	ERJ-3GEY0R00V	Panasonic

8.2 EVM PCB Layout

Figure 8-1 shows the EVM printed circuit board (PCB) layout for the ADS1258EVM.

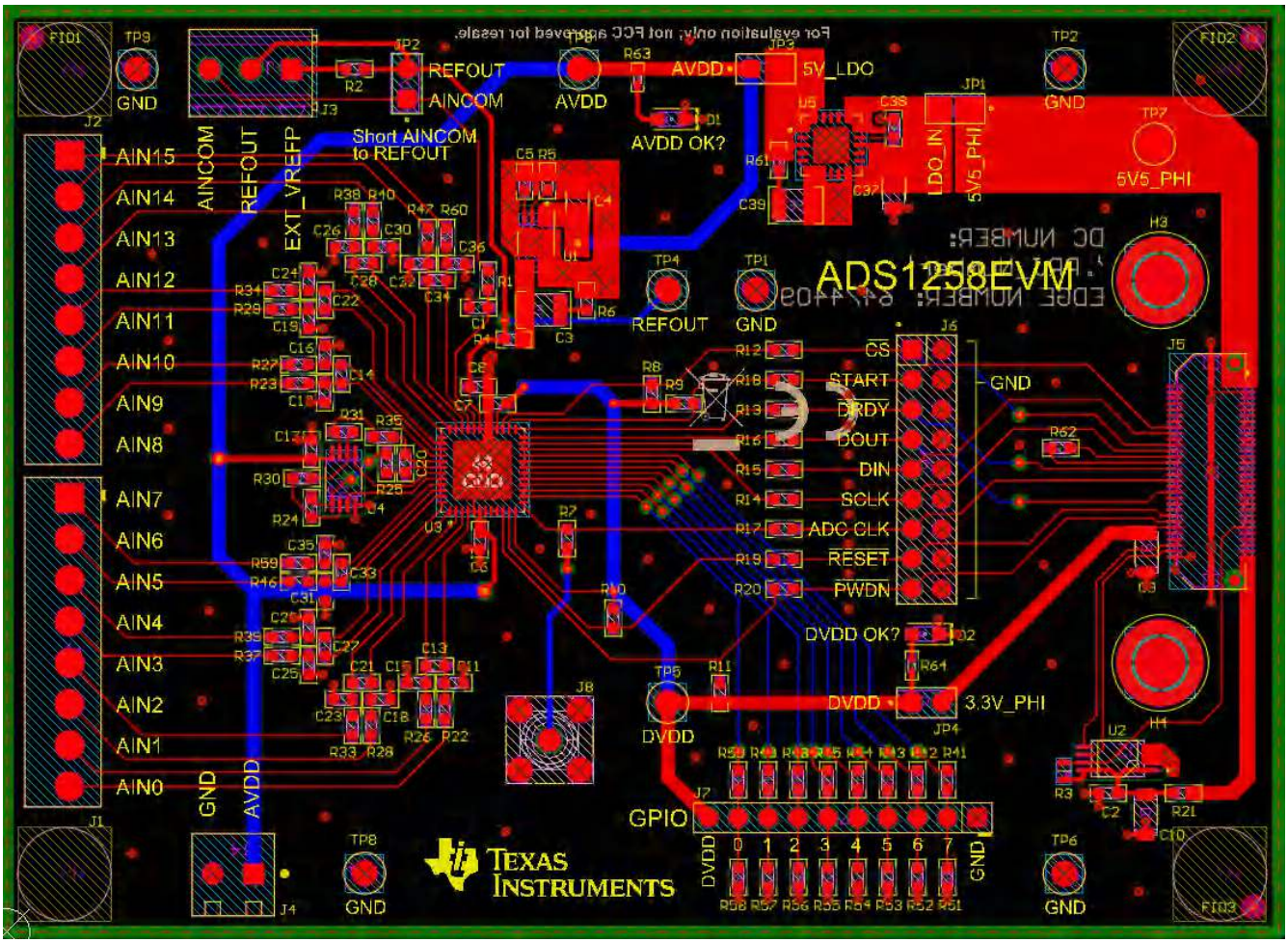

Figure 8-1. ADS1258EVM PCB Layout

8.3 Schematics

This section provides the schematics for the ADS1258EVM.

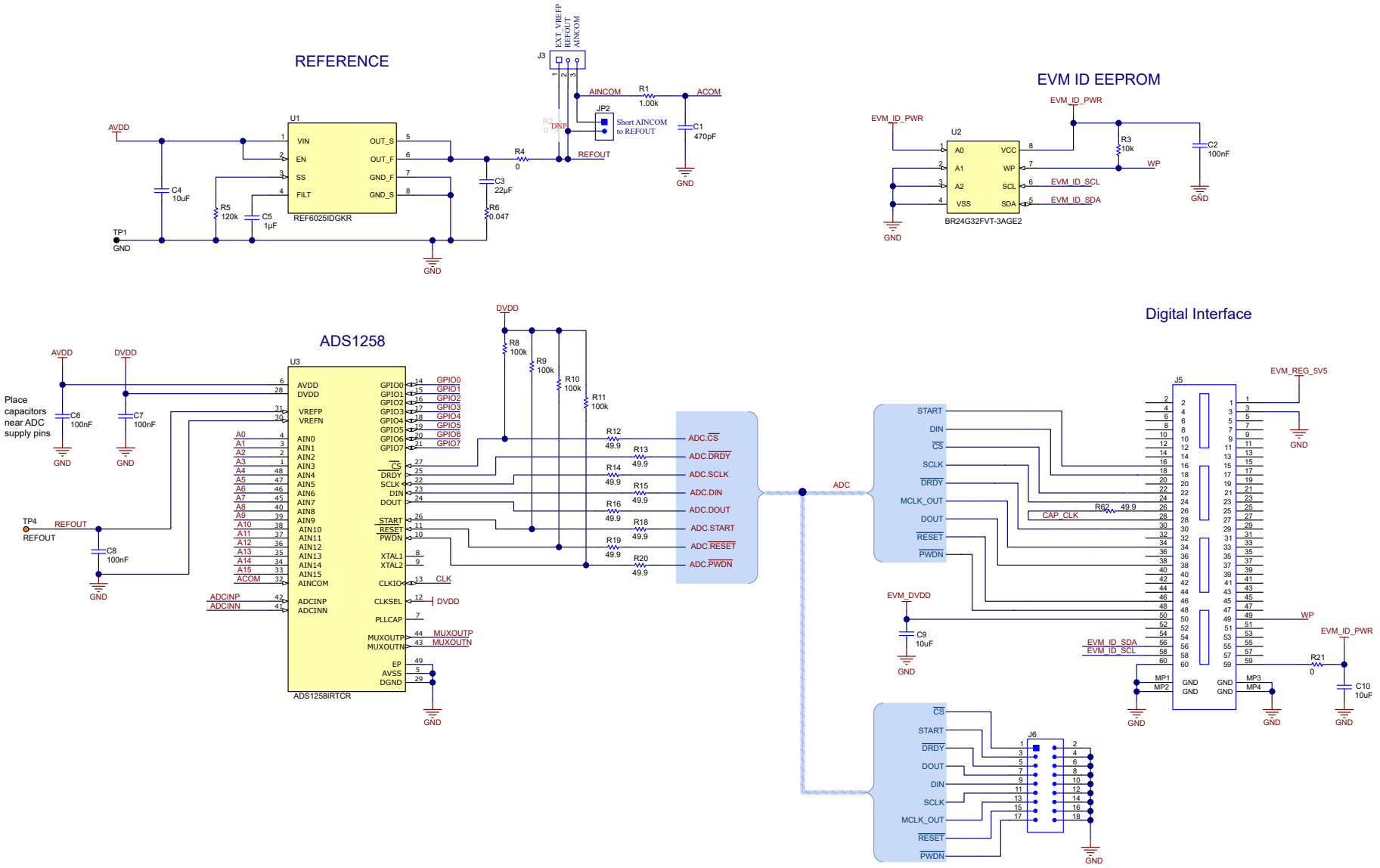

Figure 8-2. ADS1258EVM ADC, Voltage Reference, EEPROM, and Digital Interface Circuits

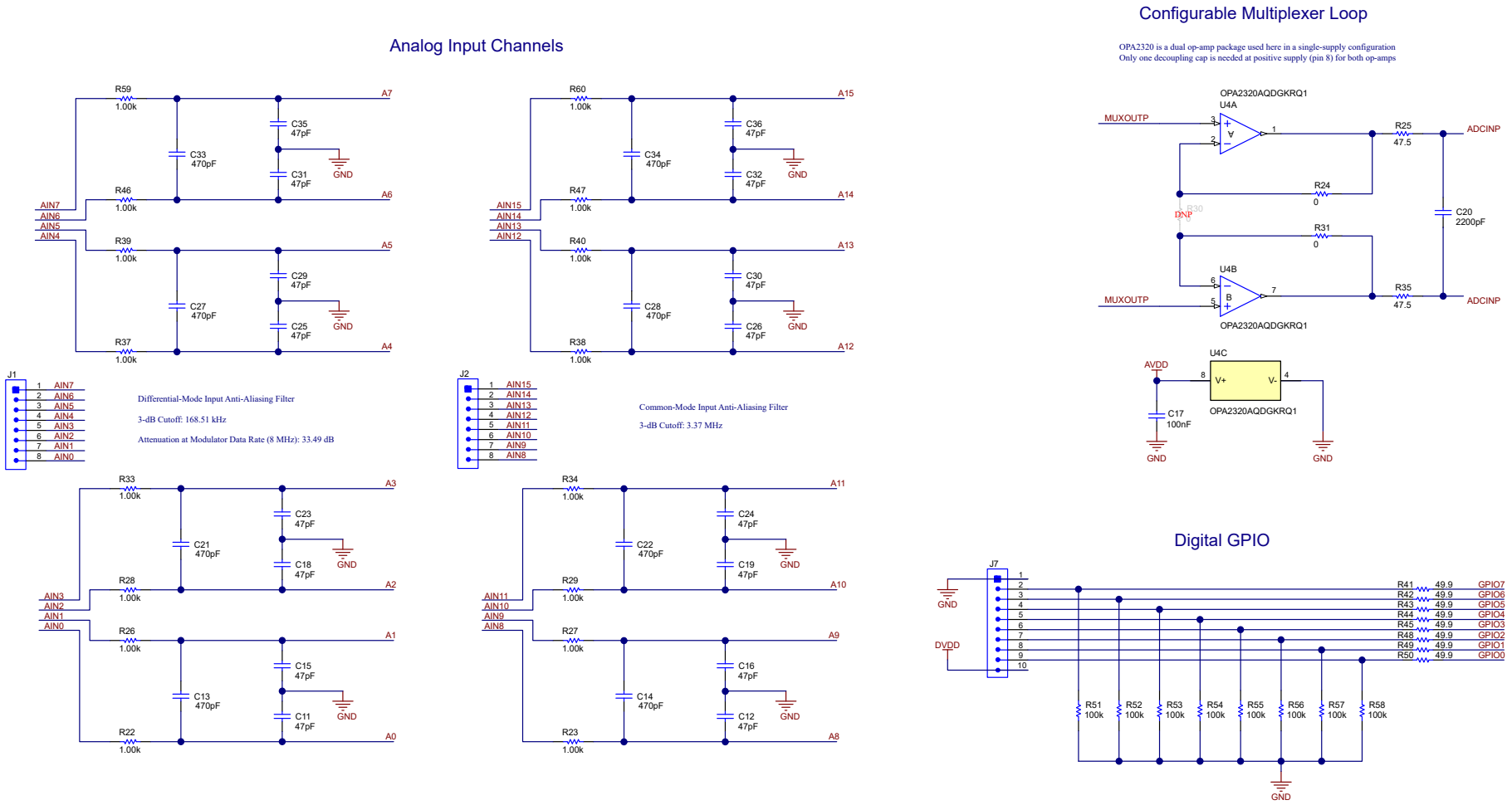

Figure 8-3. ADS1258EVM Analog Input, Multiplexer Loop, and GPIO Circuits

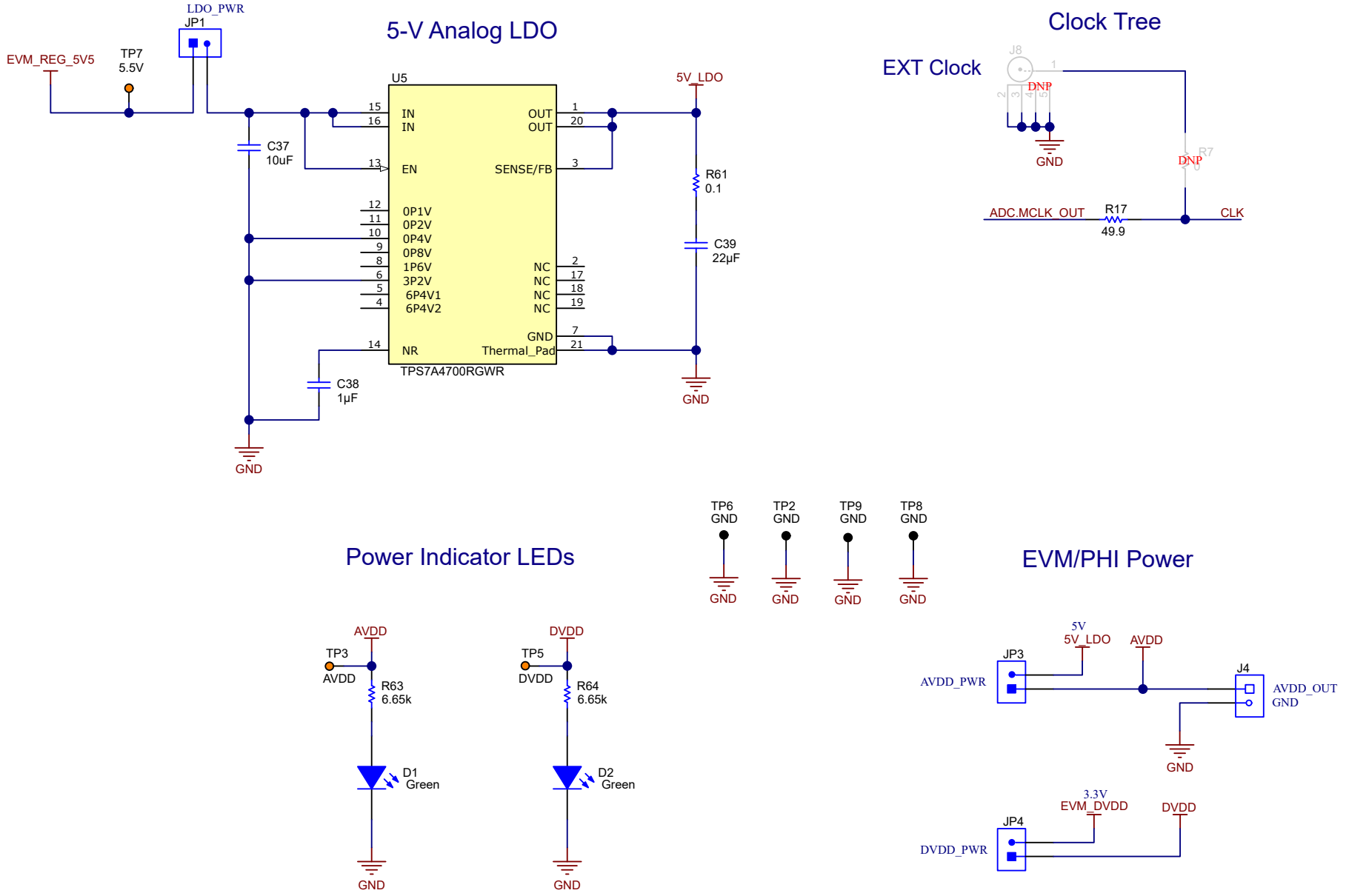

Figure 8-4. ADS1258EVM Power and Clock Circuits

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (May 2016) to Revision E (June 2023)	Page
• Changed entire document to reflect changes made in EVM moving to a new platform	3

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1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】 開発キットの中には技術基準適合証明を受けていないものがあります。 技術適合証明を受けていないもののご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

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3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

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3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

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8. *Limitations on Damages and Liability:*

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   8.2 *Specific Limitations.* IN NO EVENT SHALL TI'S AGGREGATE LIABILITY FROM ANY USE OF AN EVM PROVIDED HEREUNDER, INCLUDING FROM ANY WARRANTY, INDEMITY OR OTHER OBLIGATION ARISING OUT OF OR IN CONNECTION WITH THESE TERMS, , EXCEED THE TOTAL AMOUNT PAID TO TI BY USER FOR THE PARTICULAR EVM(S) AT ISSUE DURING THE PRIOR TWELVE (12) MONTHS WITH RESPECT TO WHICH LOSSES OR DAMAGES ARE CLAIMED. THE EXISTENCE OF MORE THAN ONE CLAIM SHALL NOT ENLARGE OR EXTEND THIS LIMIT.

9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

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