

# Am2917A

Quad Three-State Bus Transceiver with Interface Logic

## DISTINCTIVE CHARACTERISTICS

- Quad high-speed LSI bus-transceiver
- D-type driver register with tri-state bus driver output can sink 48mA at 0.5V max.
- Internal 4-bit odd parity checker/generator
- Receiver has output latch for pipeline operation
- Three-state receiver outputs sink 12mA
- 3.5V minimum output high voltage for direct interface to MOS microprocessors

## GENERAL DESCRIPTION

The Am2917A is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops. The flip-flop outputs are connected to four three-state bus drivers. Each bus driver is internally connected to the input of a receiver. The four receiver outputs drive four D-type latches, that feature three-state outputs. The device also contains a four-bit odd parity checker/generator.

This LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The three-state bus output can sink up to 48mA at 0.5V maximum. The bus enable input ( $\overline{BE}$ ) is used to force the driver outputs to the high-impedance state. When  $\overline{BE}$  is HIGH, the driver is disabled.

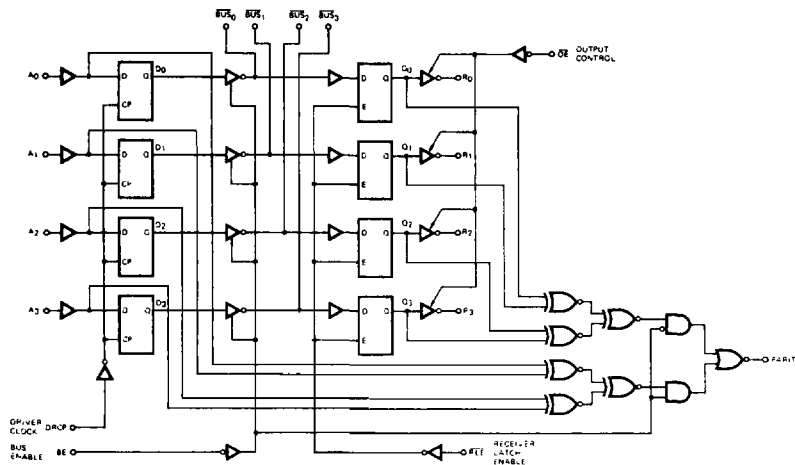
The input register consists of four D-type flip-flops with a buffered common clock. The buffered common clock (DRCP) enters the  $A_i$  data into this driver register on the LOW-to-HIGH transition.

Data from the A input is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver

output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ( $\overline{RLE}$ ) input. When the  $\overline{RLE}$  input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted and  $\overline{OE}$  LOW). When the  $\overline{RLE}$  input is HIGH, the latch will close and retain the present data regardless of the bus input. The four latches have three-state outputs and are controlled by a buffered common three-state control ( $\overline{OE}$ ) input. When  $\overline{OE}$  is HIGH, the receiver outputs are in the high-impedance state.

The Am2917A features a built-in four-bit odd parity checker/generator. The bus enable input ( $\overline{BE}$ ) controls whether the parity output is in the generate or check mode. When the bus enable is LOW (driver enabled), odd parity is generated based on the A field data input to the driver register. When  $\overline{BE}$  is HIGH, the parity output is determined by the four latch outputs of the receiver. Thus, if the driver is enabled, parity is generated and if the driver is in the high-impedance state, the BUS parity is checked.

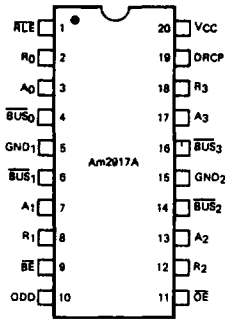
## BLOCK DIAGRAM



BD001890

### CONNECTION DIAGRAM Top View

D-20-1

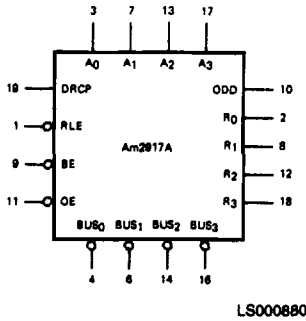


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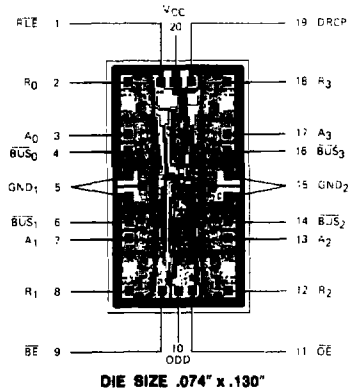
Note: Pin 1 is marked for orientation

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### LOGIC SYMBOL

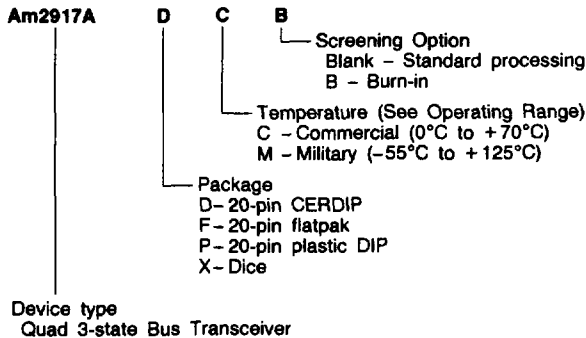


### METALLIZATION AND PAD LAYOUT



### ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).



Valid Combinations	
Am2917A	PC DC, DCB, DM, DMB FM, FMB XC, XM

**Valid Combinations**  
Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

## PIN DESCRIPTION

Pin No.	Name	I/O	Description
3, 7 13, 17	A <sub>0</sub> , A <sub>1</sub> , A <sub>2</sub> , A <sub>3</sub>	I	The four driver register inputs.
19	DRCP	I	Driver Clock Pulse. Clock pulse for the driver register.
9	BE	I	Bus Enable. When the Bus Enable is HIGH, the four drivers are in the high impedance state.
4, 6, 14, 16	BUS <sub>0</sub> , BUS <sub>1</sub> , BUS <sub>2</sub> , BUS <sub>3</sub>	I/O	The four driver outputs and receiver inputs (data is inverted).
2, 6, 12, 18	R <sub>0</sub> , R <sub>1</sub> , R <sub>2</sub> , R <sub>3</sub>	O	The four receiver outputs. Data from the bus is inverted while data from the A inputs is non-inverted.
1	RLE	I	Receiver Latch Enable. When RLE is LOW, data on the BUS inputs is passed through the receiver latches. When RLE is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.
10	ODD	O	Odd parity output. Generates parity with the driver enabled, checks parity with the driver in the high-impedance state.
11	OE	I	Output Enable. When the OE input is HIGH, the four three-state receiver outputs are in the high-impedance state.

## FUNCTION TABLE

INPUTS					INTERNAL TO DEVICE		BUS	OUTPUT	FUNCTION
A <sub>i</sub>	DRCP	BE	RLE	OE	D <sub>i</sub>	Q <sub>i</sub>	BUS <sub>i</sub>	R <sub>i</sub>	
X	X	H	X	X	X	X	Z	X	Driver output disable
X	X	X	X	H	X	X	X	Z	Receiver output disable
X	X	H	L	L	X	L	L	H	Driver output disable and receive data via Bus input
X	X	H	L	L	X	H	H	L	Driver output disable and receive data via Bus input
X	X	X	H	X	X	NC	X	X	Latch received data
L	↑	X	X	X	L	X	X	X	Load driver register
H	↑	X	X	X	H	X	X	X	Load driver register
X	L	X	X	X	NC	X	X	X	No driver clock restrictions
X	H	X	X	X	NC	X	X	X	No driver clock restrictions
X	X	L	X	X	L	X	H	X	Drive Bus
X	X	L	X	X	H	X	L	X	Drive Bus

H = HIGH

L = LOW

Z = HIGH Impedance

NC = No change

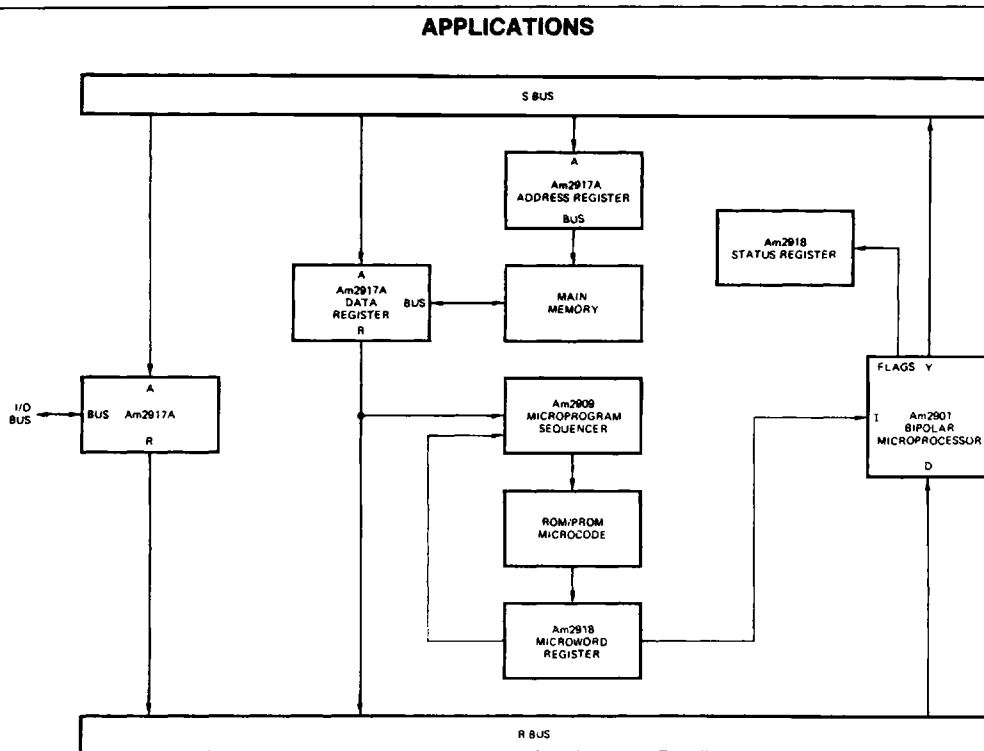
X = Don't care

↑ = LOW to HIGH transition

i = 0, 1, 2, 3

## PARITY OUTPUT FUNCTION TABLE

BE	ODD PARITY OUTPUT
L	ODD = A <sub>0</sub> ⊕ A <sub>1</sub> ⊕ A <sub>2</sub> ⊕ A <sub>3</sub>
H	ODD = Q <sub>0</sub> ⊕ Q <sub>1</sub> ⊕ Q <sub>2</sub> ⊕ Q <sub>3</sub>



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The Am2917A can be used as an I/O Bus Transceiver and Main Memory I/O Transceiver in high-speed Microprocessor Systems.

**ABSOLUTE MAXIMUM RATINGS**

Storage Temperature .....	-65°C to +150°C
Ambient Temperature Under Bias .....	-55°C to +125°C
Supply Voltage to Ground Potential Continuous .....	-0.5V to +7.0V
DC Voltage Applied to Outputs For High Output State .....	-0.5V to +V <sub>CC</sub> max.
DC Input Voltage .....	-0.5V to +7.0V
DC Output Current, Into Bus .....	100mA
DC Output Current, Into Outputs (Except Bus) .....	30mA
DC Input Current .....	-30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

**OPERATING RANGES**

Commercial (C) Devices	Temperature .....	0°C to +70°C
	Supply Voltage .....	+4.75V to +5.25V
Military (M) Devices	Temperature .....	-55°C to +125°C
	Supply Voltage .....	+4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

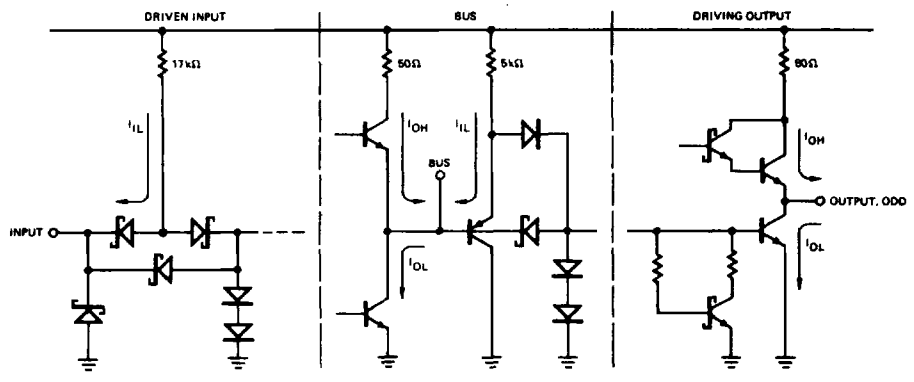
**DC CHARACTERISTICS** over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)	Min	Typ (Note 1)	Max	Units	
V <sub>OH</sub>	Receiver Output HIGH Voltage	V <sub>CC</sub> = MIN V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> MIL: I <sub>OH</sub> = -1.0mA	2.4	3.4		Volts	
		COM'L: I <sub>OH</sub> = -2.6mA	2.4	3.4			
		V <sub>CC</sub> = 5.0V, I <sub>OH</sub> = -100μA	3.5				
V <sub>OH</sub>	Parity Output HIGH Voltage	V <sub>CC</sub> = MIN, I <sub>OH</sub> = -660μA V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> MIL	2.5	3.4		Volts	
		COM'L	2.7	3.4			
V <sub>OL</sub>	Output LOW Voltage (Except Bus)	V <sub>CC</sub> = MIN V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub>	I <sub>OL</sub> = 4.0mA	0.27	0.4	Volts	
			I <sub>OL</sub> = 8.0mA		0.32		0.45
			I <sub>OL</sub> = 12mA		0.37		0.5
V <sub>IH</sub>	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs	2.0			Volts	
V <sub>IL</sub>	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs	MIL		0.7	Volts	
			COM'L		0.8		
V <sub>I</sub>	Input Clamp Voltage (Except Bus)	V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18mA			-1.2	Volts	
I <sub>IL</sub>	Input LOW Current (Except Bus)	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4V	BE, PLE		-0.72	mA	
			All other inputs		-0.36		
I <sub>IH</sub>	Input HIGH Current (Except Bus)	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7V			20	μA	
I <sub>I</sub>	Input HIGH Current (Except Bus)	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0V			100	μA	
I <sub>SC</sub>	Output Short Circuit Current (Except Bus)	V <sub>CC</sub> = MAX	RECEIVER	-30	-130	mA	
			PARITY	-20	-100		
I <sub>CC</sub>	Power Supply Current	V <sub>CC</sub> = MAX		63	95	mA	
I <sub>O</sub>	Off-State Output Current (Receiver Outputs)	V <sub>CC</sub> = MAX	V <sub>O</sub> = 2.4V		50	μA	
			V <sub>O</sub> = 0.4V		-50		

**BUS INPUT/OUTPUT CHARACTERISTICS** over operating temperature range

Parameters	Description	Test Conditions (Note 2)	Min	Typ	Max	Units
VOL	Bus Output LOW Voltage	VCC = MIN	IOL = 24mA		0.4	Volts
			IOL = 48mA		0.5	
VOH	Bus Output HIGH Voltage	VCC = MIN	COM'L, IOH = -20mA	2.4		Volts
			MIL, IOH = -15mA			
IO	Bus Leakage Current (High Impedance)	VCC = MAX Bus enable = 2.4V	VO = 0.4V		-200	µA
			VO = 2.4V		50	
			VO = 4.5V		100	
IOFF	Bus Leakage Current (Power OFF)	VO = 4.5V VCC = 0V			100	µA
VIH	Receiver Input HIGH Threshold	Bus enable = 2.4V	2.0			Volts
VIL	Receiver Input LOW Threshold	Bus enable = 2.4V	COM'L		0.8	Volts
			MIL		0.7	
ISC	Bus Output Short Circuit Current	VCC = MAX VO = 0V	-50	-120	-225	mA

**INPUT/OUTPUT CURRENT INTERFACE CONDITIONS**



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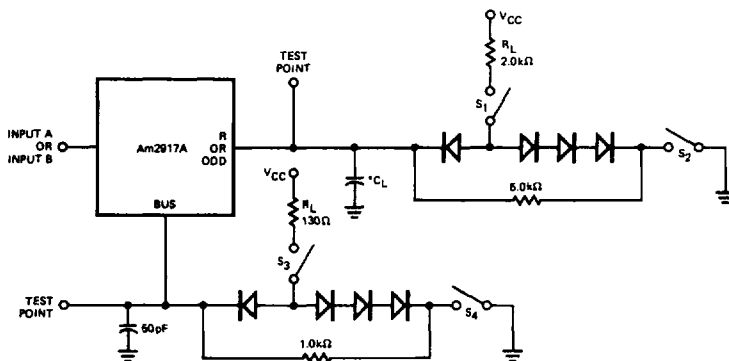
Note: Actual current flow direction shown.

**SWITCHING CHARACTERISTICS** over operating range unless otherwise specified

Parameters	Description	Test Conditions	COMMERCIAL			MILITARY			Units
			Am2917A			Am2917A			
			Min.	Typ (Note 1)	Max.	Min.	Typ (Note 1)	Max.	
t <sub>PHL</sub>	Driver Clock (DRCP) to Bus	C <sub>L</sub> (BUS) = 50 pF R <sub>L</sub> (BUS) = 130 Ω		21	32		21	36	ns
t <sub>PLH</sub>				21	32		21	36	
t <sub>ZH</sub> , t <sub>ZL</sub>	Bus Enable ( $\overline{BE}$ ) to Bus			13	23		13	26	ns
t <sub>HZ</sub> , t <sub>LZ</sub>				13	18		13	21	
t <sub>s</sub>	A Data Inputs	C <sub>L</sub> = 15 pF R <sub>L</sub> = 2.0 kΩ	12			15			ns
t <sub>h</sub>			6.0			8.0			
t <sub>PW</sub>	Clock Pulse Width (HIGH)		17			20			ns
t <sub>PLH</sub>	Bus to Receiver Output (Latch Enabled)			18	30		18	33	ns
t <sub>PHL</sub>				18	27		18	30	
t <sub>PLH</sub>	Latch Enable to Receiver Output			21	30		21	33	ns
t <sub>PHL</sub>				21	27		21	30	
t <sub>s</sub>	Bus to Latch Enable ( $\overline{LE}$ )			13			15		ns
t <sub>h</sub>				4.0			6.0		
t <sub>PLH</sub>	A Data to Odd Parity Out (Driver Enabled)			32	42		32	46	ns
t <sub>PHL</sub>				26	36		26	40	
t <sub>PLH</sub>	Bus to Odd Parity Out (Driver Inhibit)			21	32		21	36	ns
t <sub>PHL</sub>				21	32		21	36	
t <sub>PLH</sub>	Latch Enable ( $\overline{LE}$ ) to Odd Parity Output			21	32		21	36	ns
t <sub>PHL</sub>				21	32		21	36	
t <sub>ZH</sub> , t <sub>ZL</sub>	Output Control to Output		C <sub>L</sub> = 5 pF, R <sub>L</sub> = 2.0 kΩ		14	23		14	26
t <sub>HZ</sub> , t <sub>LZ</sub>				14	23		14	26	

- Notes:
1. Typical limits are at V<sub>CC</sub> = 5.0 V, 25°C ambient and maximum loading.
  2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
  3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

**SWITCHING TEST CIRCUIT**

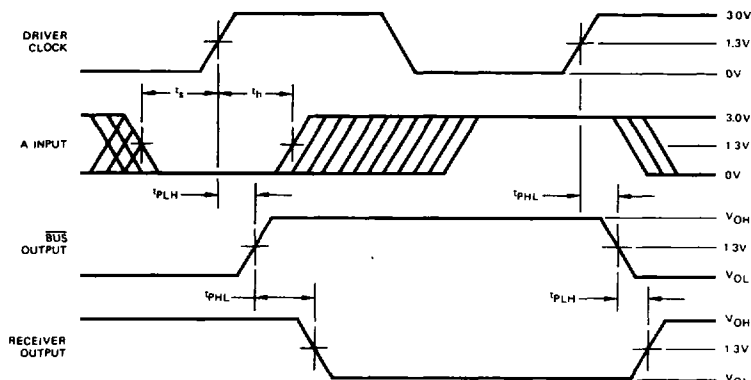


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\* $C_L = 15\text{pF}$  for  $t_{PLH}$ ,  $t_{PHL}$ ,  $t_{ZL}$ ,  $t_{ZH}$   
 $C_L = 5\text{pF}$  for  $t_{HZ}$ ,  $t_{LZ}$

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**SWITCHING WAVEFORMS**



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Note: Bus to Receiver output delay is measured by clocking data into the driver register and measuring the BUS to R combinatorial delay.