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THIS SPEC IS OBSOLETE

Spec No: 002-08407

Spec Title: CY39C031 2CH BUCK DC/DC CONVERTER + 1CH LDO WITH I2C INTERFACE AND SW FET

Replaced by: NONE

CY39C031

2ch Buck DC/DC Converter + 1ch LDO with I²C Interface and SW FET

Description

The CY39C031 contains 2ch buck DC/DC converter and 1ch LDO. It is possible to supply the main power supply line in a system by using only one chip. The current mode system is adopted for the DC/DC converter, and it is possible to use the chip inductor with the high switching frequency operation which contains internal SW FET. The CY39C031 contains the output setting resistor and the the phase compensation circuit, and contributes to reduce the number of external components and the mounting area. Also, it contains the CTL input pin which can control the ON/OFF for each CH, the Power Good signal output pin and the I²C communication interface, therefore it is easy to design the power supply sequence.

It is possible to tune in the output voltage exactly using the I²C communication and possible to correspond to the DVS/ASV system.

Features

- Operating input voltage range:2.5 V to 5.5 V (Maximum rating: 7 V)
- Output voltage setting range, Maximum output current: DD1*:1.0 V to 1.3 V (20 mV/step), 1.4 A (DC)
  DD2*:1.2 V to 1.95 V (50 mV/step), 0.6 A (DC)
  LDO:2.8 V/2.85 V/3.0 V/3.3 V, 0.25 A (DC)

  Note: Each channel has selective preset voltage (Lineup for a total of 32 kinds) .
- Soft-start time setting range: 0.9 ms to 14.3 ms (approximately 0.9 ms/step)
- Switching frequency for the DC/DC block:3 MHz (fixed)
- Communication interface: I²C (ON/OFF, Output voltage, Soft-start time setting)
- Built-in PFM/PWM auto switching mode
- Built-in function: Output setting resistor, Phase compensation circuit, Discharge resistor, Soft-start
- Each Channel Power Good output function (Open-drain)
- Protection function: Under voltage lockout protection circuit (UVLO), Over current protection circuit (OCP), Thermal shutdown protection circuit (TSD)
- Error signal output pin installed (Open-drain)
- Small package: QFN28 (4 mm × 4 mm × 0.8 mm, 0.4 mm pitch)

  *: DD1,DD2 : DC/DC converter block 1, 2

Applications

Network equipment: Wifi-tuner, Surveillance camera

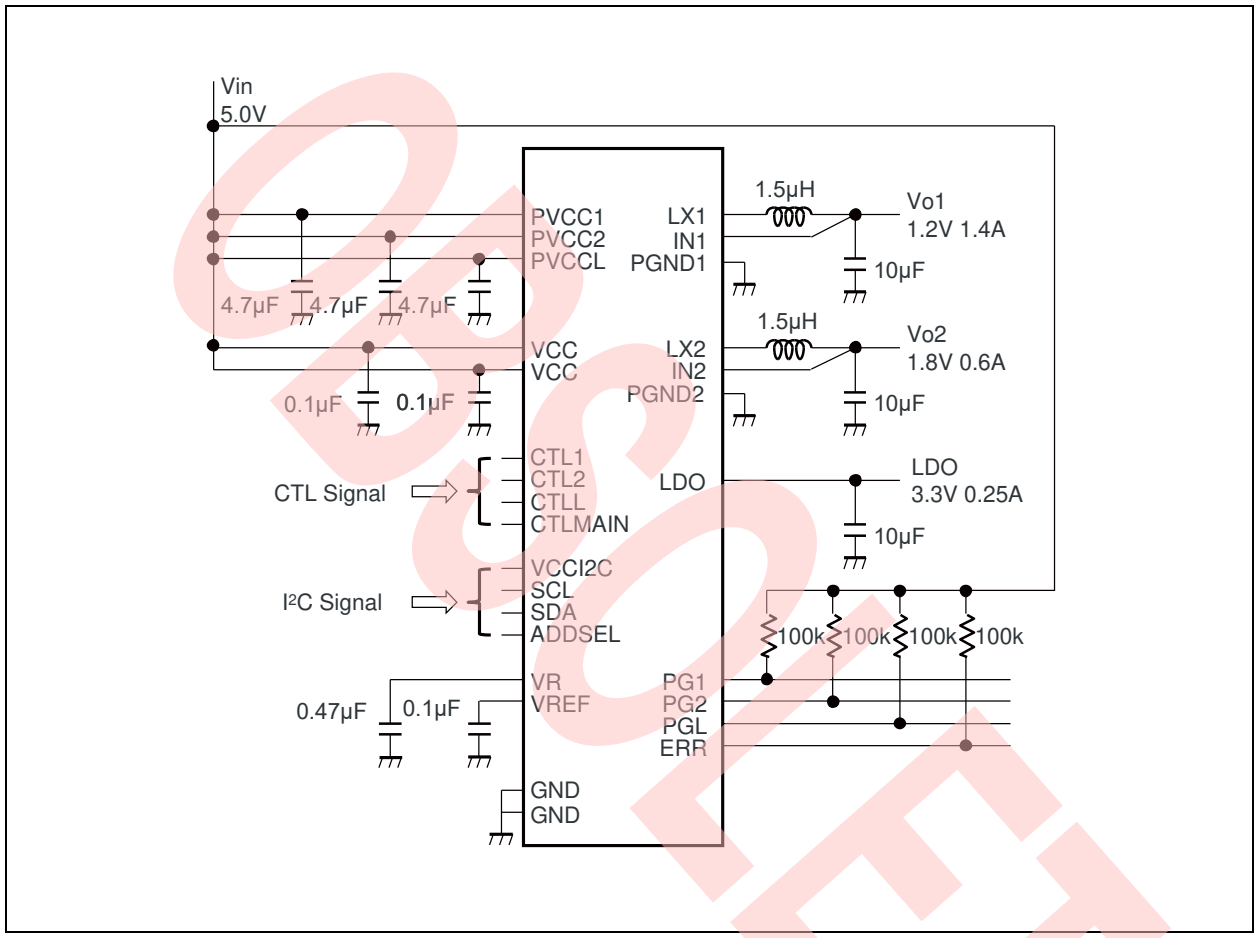
Data-storage device: HDD, SSD, Picture recording equipment

Image and voice output equipment: MFP, Printer, Scanner, Projector, Electrophone, STB

Various terminals: POS, FA, HEMS etc.

Contents

1. Application Circuit Example



2. Recommended Application Specifications

[Input Voltage Range]

Input Voltage VCC (V)		
Min	**Typ**	**Max**
2.5	3.6	5.5

[Output Specification]

(Ta=+25°C)

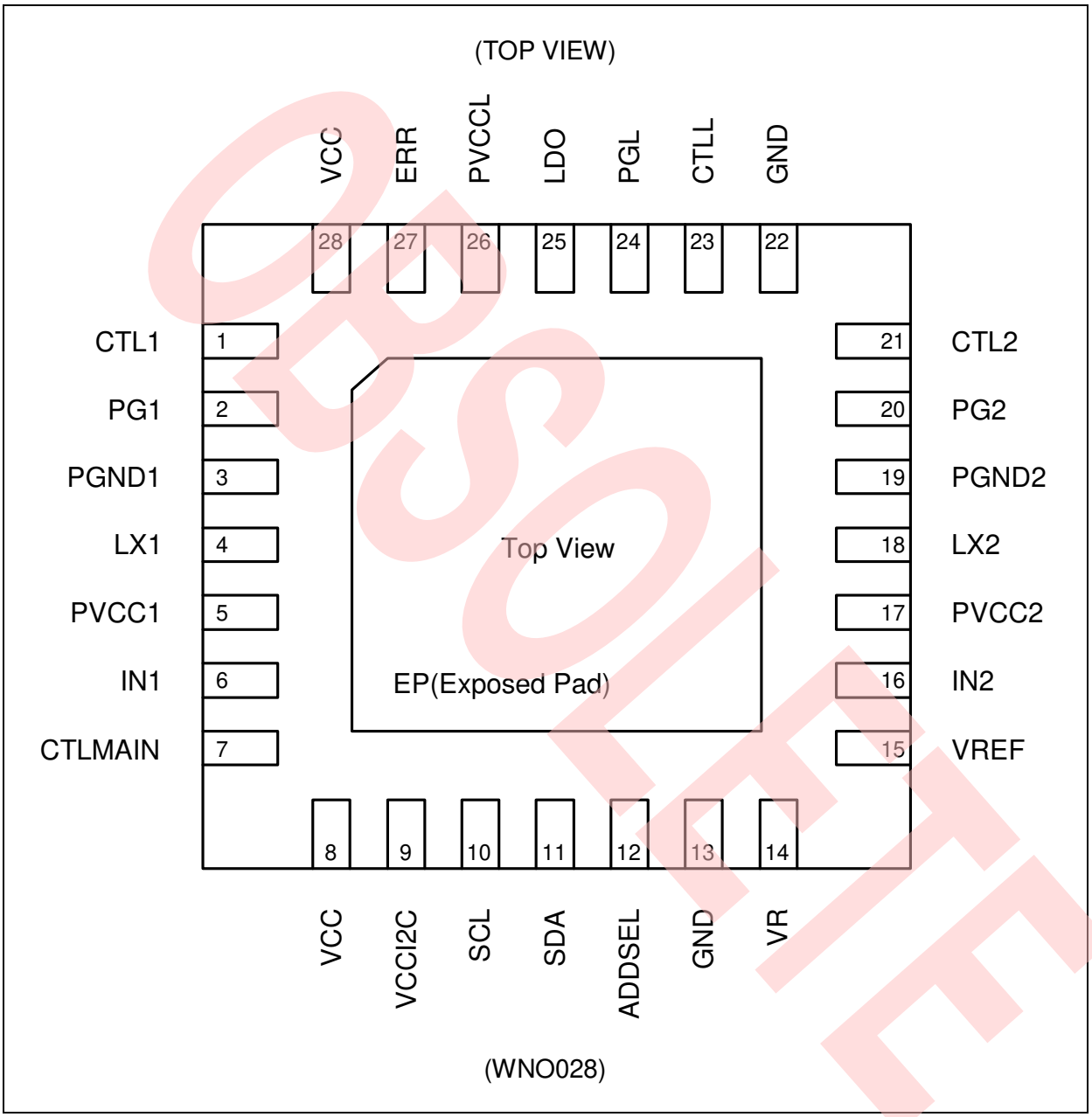
Channel	Symbol	Accuracy	Output Voltage (V)			Output Current (mA)	Limit Current (mA)	Mode	Switching Frequency (MHz)	Coil (µH)	Output Capacitance (µF)	Soft-start Time (ms)	Discharge Resistance (kΩ)	Remarks
			Min	Typ	Max	Max	Min							
DD1	Vo1	±1.2%	0.99*	1.00*	1.01*	1400	2000	Buck (synchronous rectification) C-mode	3.0	1.5	10	14.3	5	Built-in SW FET Built-in output setting resistors Operation mode switching (Fixed PWM, PFM/PWM)
			1.01	1.02	1.03							0.9*		
			1.03	1.04	1.05							1.8		
			1.05	1.06	1.07							2.7		
			1.07	1.08	1.09							3.6		
			1.09*	1.10*	1.11*							4.5		
			1.11	1.12	1.13							5.4		
			1.13	1.14	1.15							6.3		
			1.15	1.16	1.17							7.2		
			1.17	1.18	1.19							8.1		
			1.19*	1.20*	1.21*							9.0		
			1.21	1.22	1.23							9.9		
			1.23	1.24	1.25							10.8		
			1.24	1.26	1.28							11.6		
			1.26	1.28	1.30							12.5		
			1.28*	1.30*	1.32*							13.4		
DD2	Vo2	±1.2%	1.19*	1.20*	1.21*	600	900	Buck (synchronous rectification) C-mode	3.0	1.5	10	14.3	5	Built-in SW FET Built-in output setting resistors Operation mode switching (Fixed PWM, PFM/PWM)
			1.24	1.25	1.27							0.9*		
			1.28	1.30	1.32							1.8		
			1.33*	1.35*	1.37*							2.7		
			1.38	1.40	1.42							3.6		
			1.43	1.45	1.47							4.5		
			1.48*	1.50*	1.52*							5.4		
			1.53	1.55	1.57							6.3		
			1.58	1.60	1.62							7.2		
			1.63	1.65	1.67							8.1		
			1.68	1.70	1.72							9.0		
			1.73	1.75	1.77							9.9		
			1.78*	1.80*	1.82*							10.8		
			1.83	1.85	1.87							11.6		
			1.88	1.90	1.92							12.5		
			1.93	1.95	1.97							13.4		

Channel	Symbol	Accuracy	Output Voltage (V)			Output Current (mA)	Limit Current (mA)	Mode	Switching Frequency (MHz)	Coil (µH)	Output Capacitance (µF)	Soft-start Time (ms)	Discharge Resistance (kΩ)	Remarks
			Min	Typ	Max	Max	Min							
LDO	LDO	±1.8%	2.75	2.80	2.85	250	300	LDO	-	-	4.7	14.3	5	
			2.80*	2.85*	2.90*							0.9		
			2.95	3.00	3.05							1.8		
			3.24*	3.30*	3.36*							2.7*		
			-	-	-							3.6		
			-	-	-							4.5		
			-	-	-							5.4		
			-	-	-							6.3		
			-	-	-							7.2		
			-	-	-							8.1		
			-	-	-							9.0		
			-	-	-							9.9		
			-	-	-							10.8		
			-	-	-							11.6		
			-	-	-							12.5		
			-	-	-							13.4		

*: Preset value

Note: It is possible to set the output voltage and to change the soft-start time using I^2C.

3. Pin Assignment



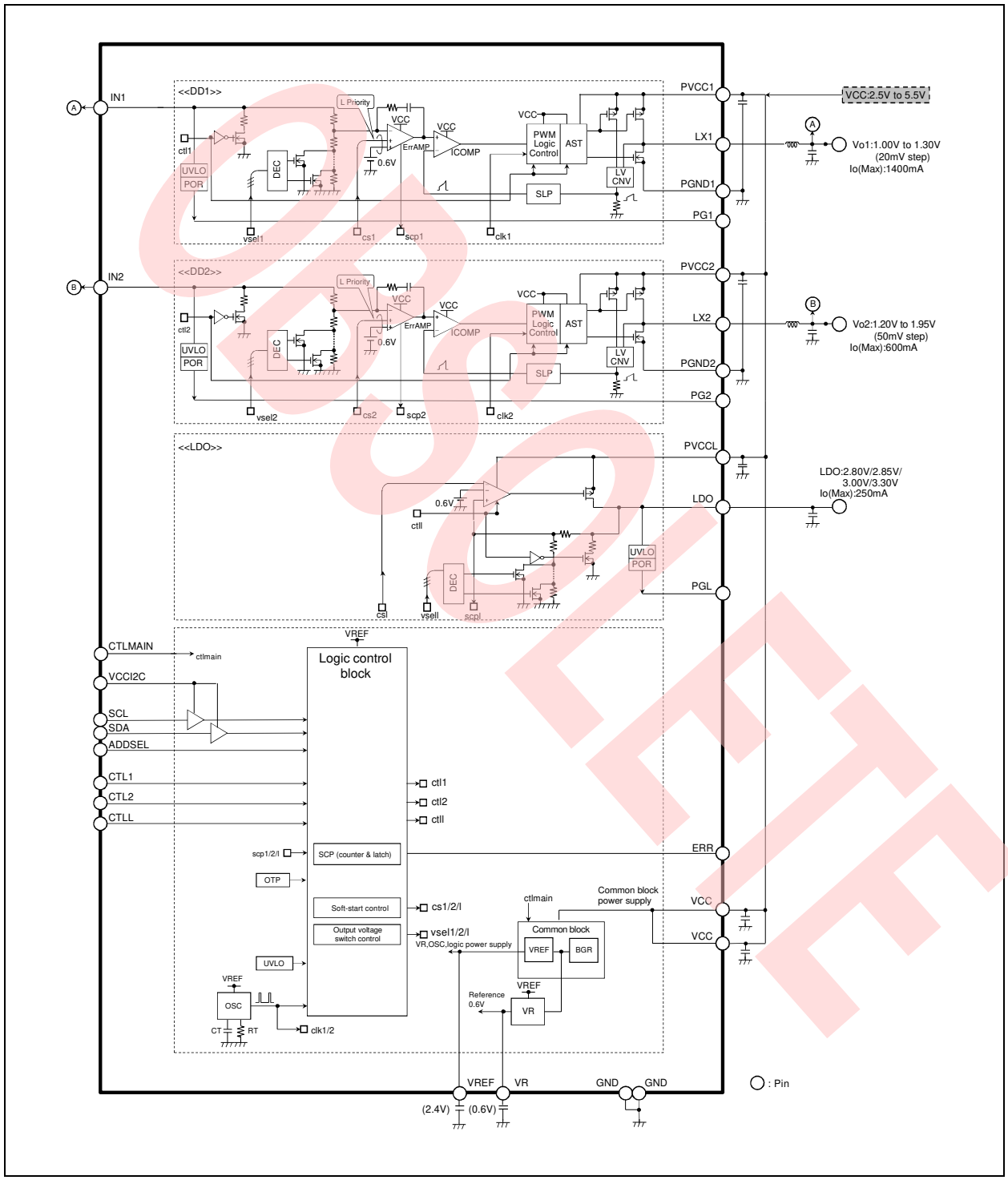
4. Pin Descriptions (PKG)

Circuit Block	Pin Name	Number of pin for PKG	Pin No	I/O	Description (PKG)	Pull-down Resistance	PAD Treatment when not using DD1	PAD Treatment when not using DD2	PAD Treatment when not using LDO	PAD Treatment when not using I²C Communication
DD1	IN1	1	6	I	DD1·Output voltage feedback pin.	-	GND connection	-	-	-
	PVCC1	1	5	-	DD1·Output block power supply pin	-	VCC connection	-	-	-
	LX1	1	4	O	DD1·Pin for inductance connection.	-	Open	-	-	-
	PG1	1	2	O	DD1·POWERGOOD output pin	-	Open	-	-	-
	PGND1	1	3	-	DD1·Output block ground pin	-	GND connection	-	-	-
DD2	IN2	1	16	I	DD2·Output voltage feedback pin.	-	-	GND connection	-	-
	PVCC2	1	17	-	DD2·Output block power supply pin	-	-	VCC connection	-	-
	LX2	1	18	O	DD2·Pin for inductance connection.	-	-	Open	-	-
	PG2	1	20	O	DD2·POWERGOOD output pin	-	-	Open	-	-
	PGND2	1	19	-	DD2·Output block ground pin	-	-	GND connection	-	-
LDO	PVCCL	1	26	-	LDO·Power supply pin	-	-	-	VCC connection	-
	LDO	1	25	O	LDO·Output pin	-	-	-	Open	-
	PGL	1	24	O	LDO·POWERGOOD output pin	-	-	-	Open	-
CTL	CTL1	1	1	I	DD1 Control pin	❍	Open	-	-	-
	CTL2	1	21	I	DD2 Control pin	❍	-	Open	-	-
	CTLL	1	23	I	LDO Control pin	❍	-	-	Open	-
	CTLMAIN	1	7	I	Control pin for common block and digital block *	❍	-	-	-	-
ERR	ERR	1	27	O	ERR signal output pin	-	-	-	-	-

Circuit Block	Pin Name	Number of pin for PKG	Pin No	I/O	Description (PKG)	Pull-down Resistance	PAD Treatment when not using DD1	PAD Treatment when not using DD2	PAD Treatment when not using LDO	PAD Treatment when not using I²C Communication
I²C	VCCI2C	1	9	-	Power supply pin for I²C.	-	-	-	-	GND connection
	SCL	1	10	I	I²C clock pin	×	-	-	-	Open
	SDA	1	11	I/O	I²C data I/O pin	×	-	-	-	Open
	ADDSEL	1	12	I	Switch pin for slave address	❍	-	-	-	Open
Common	VCC	2	8, 28	-	Control circuit block power supply pin	-	-	-	-	-
	VREF	1	15	O	Reference voltage (2.4 V) output pin	-	-	-	-	-
	VR	1	14	O	Reference voltage (0.6 V) output pin	-	-	-	-	-
	GND	2	13, 22	-	Control circuit block ground pin	-	-	-	-	-
-	GND	1	EP	-	Ground pin	-	-	-	-	-

*: When turning on DD1, DD2 and LDO, it is also necessary to set CTLMAIN to "H". See 9. Operation Mode List for the details.

5. Block Diagram



6. Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating		Unit
			Min	Max	
Power supply voltage	V_{CC}	VCC, PVCC1, PVCC2, PVCCL, VCCI2C pins	-	7	V
Input voltage	V_{CTL}	CTLMAIN, 1, 2, L pins	-	7	V
	V_{OUT}	IN1, IN2 pins	-	7	V
	Vlogic	SDA, SCL pins	-	7	V
LX voltage	V_{LX}	LX1, LX2 pins	-0.3	+7	V
Power dissipation	P_D	Ta ≤ +25°C Thermal resistor value (θj-a):(50°C/W*)	-	1720	mW
Maximum junction temperature	T_{jmax}	-	-	+125	°C
Storage temperature	T_{STG}	-	-55	+125	°C

*: When mounted on a QFN28 (WNO028) PKG, 4layers 0.8 mm thickness 117 mm × 84 mm

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

7. Recommended Operating Conditions

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
General	Power supply voltage	V_{CC}	VCC pin	2.5	3.6	5.5	V
	Reference voltage output current	I_{REF}	VREF pin	-1	-	0	mA
		I_R	VR pin	-1	-	0	µA
	Operating temperature	Ta	-	-30	+25	+85	°C
DC/DC CH	Power supply voltage	V_{CC}	VCC, PVCC1, PVCC2 pins	2.5	3.6	5.5	V
	Input voltage	V_{OUT}	IN1, IN2 pins	0	-	VCC	V
LDO CH	Power supply voltage	V_{CC}	VCC, PVCCL pins Output voltage setting: default (3.3 V)	3.5	3.6	5.5	V
CTL block	Input voltage	V_{CTL}	CTL* pin	0	-	VCC	V
Digital block (I^2C)	Power supply voltage	V_{CC}	VCCI2C pin	1.76	-	3.37	V
	Logic input voltage	Vlogic	SDA, SCL pin	0	-	VCCI2C	V

*: CTLMAIN, CTL1, CTL2, CTLL

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges. Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.
No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

8. Electrical Characteristics

Common Block

(Ta=+25°C, VCC=PVCC1, PVCC2, L=3.6V)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Reference Voltage Block [VR, VREF]	Output voltage	V_R	VR pin =0 mA	0.594	0.600	0.606	V
		V_{REF1}	VREF pin =0 mA	2.376	2.400	2.424	V
		V_{REF2}	VCC pin =2.5 V to 5.5 V	2.370	2.400	2.430	V
		V_{REF3}	VREF pin =0 mA to -1 mA	2.370	2.400	2.430	V
Under Voltage Lockout Protection Circuit Block [VCC UVLO]	Threshold voltage	V_{TH}	VCC pin = ↗	2.156	2.20	2.244	V
	Hysteresis width	V_H	-	-	0.20	-	V
Over Current Protection Circuit Block [OCP]	Timer time	t_{OCP1}	DD1, DD2, LDO Default value	0.5	1	1.5	ms
Thermal shutdown Protection Circuit Block [TSD]	Stop temperature	T_{TSDH}	-	-	150*	-	°C
Control Block (CTL) [CTL]	Input voltage	V_{IH}	CTL* pin	VCC × 0.7	-	VCC	V
		V_{IL}	CTL* pin	0	-	0.4	V
	Input current	I_{CTLH}	CTL* pin =3.6 V	2.7	3.6	5.1	µA
		I_{CTLL}	CTL* pin =0 V	-	-	1	µA
	Input pull-down resistor	R_P	CTL* pin	-	1	-	MΩ
General (DC/DC block)	Power supply current	I_{VCCS1}	CTL* pin =0 V	-	0	1.0	µA
		I_{VCCS2}	CTLMAIN=3.6 V CTL1, CTL2.L pins =0 V	-	80	120	µA
		I_{VCC}	CTLMAIN, L pins =3.6 V Only LDO operation No load	-	200	300	µA
		I_{VCC}	CTL* pin = 3.6 V all CH No load (DD operation mode: PFM/PWM mode)	-	450	680	µA
		I_{VCC}	CTL* pin = 3.6 V all CH No load (DD operation mode: Fixed PWM mode)	-	10.8	16.2	mA
		I_{VCCI2C}	CTLMAIN, L pin=3.6 V VCCI2C pin = 1.8 V	-	7.2	12.0	µA

*: These are not the rated values. Use these values as reference when planning.

DD1, DD2

(Ta=+25°C, VCC=PVCC1, PVCC2, L=3.6V)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
DC/DC Converter Block [DD1]	Output voltage	V_{OUT}	Output voltage setting: 1.2 V IOUT=-10 mA	1.186	1.20	1.214	V
	Input stability	V_{LINE}	IOUT=-10 mA, VCC=2.5 V to 5.5 V	-5	-	+5	mV
	Load stability	V_{LOAD}	IOUT=-1 mA to -1400 mA (when in Fixed PWM mode)	-10	-	-	mV
			IOUT=-1 mA to -1400 mA (when in PFM/PWM mode)	-10	-	+15	mV
	IN1 pin input impedance	R_{IN}	IN1 pin=1.5 V output voltage setting: 1.2 V	-	400	-	kΩ
	SW PMOS-Tr ON resistance	R_{PMOS}	LX1 pin=-30 mA	-	0.12*	-	Ω
	SW NMOS-Tr ON resistance	R_{NMOS}	LX1 pin= 30 mA	-	0.09*	-	Ω
	SW PMOS-Tr leak current	I_{LEAK}	LX1 pin=0 V	-1	-	-	µA
	SW NMOS-Tr leak current	I_{LEAK}	LX1 pin=3.6 V	-	-	1	µA
	Overcurrent protection value	I_{LIMIT}	L=1.5 µH	2000	-	-	mA
	PFM/PWM reshuffling electric current	I_{PFM}	L=1.5 µH	-	40*	-	mA
	Discharge resistor	R_{DIS}	-	-	5	-	kΩ
	Soft-start time	t_{SS}	Preset value	0.8	0.9	1.0	ms
	Switching frequency	f_{OSC}	-	2.7	3.0	3.3	MHz
DC/DC Converter Block [DD2]	Output voltage	V_{OUT}	Output voltage setting: 1.8 V IOUT=-10 mA	1.778	1.80	1.822	V
	Input stability	V_{LINE}	IOUT=-10mA VCC=2.5 V to 5.5 V	-5	-	+5	mV
	Load stability	V_{LOAD}	IOUT=-1 mA to -600mA (when in Fixed PWM mode)	-10	-	-	mV
			IOUT=-1 mA to -600mA (when in PFM/PWM mode)	-10	-	+20	mV
	IN2 pin input impedance	R_{IN}	IN2 pin =2.0 V Output voltage setting: 1.8 V	-	300	-	kΩ
	SW PMOS-Tr ON resistance	R_{PMOS}	LX2 pin =-30 mA	-	0.16*	-	Ω
	SW NMOS-Tr ON resistance	R_{NMOS}	LX2 pin = 30 mA	-	0.14*	-	Ω
	SW PMOS-Tr leak current	I_{LEAK}	LX2 pin =0 V	-1	-	-	µA
	SW NMOS-Tr leak current	I_{LEAK}	LX2 pin =3.6 V	-	-	1	µA
	Overcurrent protection value	I_{LIMIT}	L=1.5 µH	900	-	-	mA
	PFM/PWM reshuffling electric current	I_{PFM}	L=1.5 µH	-	70*	-	mA
	Discharge resistor	R_{DIS}	-	-	5	-	kΩ
	Soft-start time	t_{SS}	Preset value	0.8	0.9	1.0	ms
	Switching frequency	f_{OSC}	-	2.7	3.0	3.3	MHz

*: These are not the rated values. Use these values as reference when planning.

LDO

(Ta=+25°C, VCC=PVCC1, PVCC2, L=3.6V)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
LDO Block [LDO]	Output voltage	V_{OUT}	Output voltage setting : 3.3 V IOUT=-10 mA	3.241	3.300	3.359	V
	I/O voltage difference	V_{DIF}	IOUT=-10 mA	-	-	0.20	V
	Input stability	V_{LINE}	IOUT=-10 mA, VCC=3.5 V to 5.5 V	-5	-	+5	mV
	Load stability	V_{LOAD}	IOUT=-1mA to -150 mA	-30	-20	-	mV
	Ripple remove ratio	RR	PVCCL=0.2 Vrms, f=10 Hz, IOUT=-150 mA	35	75	-	dB
			PVCCL=0.2 Vrms, f=10 kHz, IOUT=-150 mA	15	50	-	dB
	Overcurrent protection value	I_{LIMIT}	Vout×0.9	300	-	-	mA
	Control macro consumption current	I_{PVCCLS}	At stand-by	-	0	1	µA
		I_{PVCCL}	IOUT=0 mA	-	80	105	µA
	Discharge resistor	R_{DIS}	-	-	5	-	kΩ
	Soft-start time	t_{SS}	Preset value	2.4	2.7	3.0	ms

Digital Block

(Ta=+25°C, VCC=PVCC1, PVCC2, L=3.6V)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
POWER-GOOD Block [Power Good]	Output voltage	V_{OL}	PG1, PG2, L pins I_{OL}=1mA	-	-	0.4	V
	Output current	I_{OL}	PG1, PG2, L pins	1	-	-	mA
	Low-voltage detection	V_{th}	IN1, IN2, LDO pins = ↓	-	Vo × 0.75*	-	V
	Power-on detection voltage	V_{th}	IN1, IN2, LDO pins = ↑	-	Vo × 0.85*	-	V
Error Block [ERR]	Output voltage	V_{OL}	ERR pin I_{OL} = 1 mA	-	-	0.4	V
	Output current	I_{OL}	ERR pin	1	-	-	mA
I^2C Block [I^2C]	Input voltage	V_{IH}	SCL, SDA pins VCCI2C=3.3 V	VCCI2C × 0.7	-	VCCI2C	V
		V_{IL}	SCL, SDA pins VCCI2C=3.3 V	0	-	VCCI2C × 0.3	V
	Input current	I_{IH}	SCL, SDA pins VCCI2C=3.3 V	-	-	10	µA
		I_{IL}	SCL, SDA pins VCCI2C=3.3 V	-10	-	-	µA
	Output voltage	V_{OL}	SDA pin I_{OL} =3 mA	-	-	0.4	V
	Output current	I_{OL}	SDA pin	3	-	-	mA
	Input pull-down resistor	R_P	ADDSEL pin	-	1	-	MΩ

*: These are not the rated values. Use these values as reference when planning.

9. Operation Mode List

	Mode	Stand-by	Stand-by 2	General	ERR detection
CTL Signal	CTLMAIN (External)	L	H	H	H
	CTL1 (External / I²C)	L	L	H/L	X
	CTL2 (External / I²C)	L	L	H/L	X
	CTLL (External / I²C)	L	L	H/L	X
Operation Block	General	OFF	ON	ON	ON
	Digital Block	OFF	ON	ON	ON
	OSC, VR Block	OFF	OFF	ON*2	OFF
	DD1	OFF	OFF	ON/OFF	OFF
	DD2	OFF	OFF	ON/OFF	OFF
	LDO	OFF	OFF	ON/OFF	OFF
I²C Communication	I²C communication	Disabled	Enabled	Enabled	Enabled
Protection Operating	Thermal shutdown Protection (TSD)	Not available	Not available	Available	*1
	Over Current Protection (OCP)	Not available	Not available	Available	*1

*1:This is the state after detection of ERR. It is possible to release the ERR detection mode by turning the power supply on again or turning CTLMAIN on again.

*2:When only LDO is operating, the OSC block stops (OFF) after LDO activation. Also, the VR block keeps operating (ON) after LDO activation.

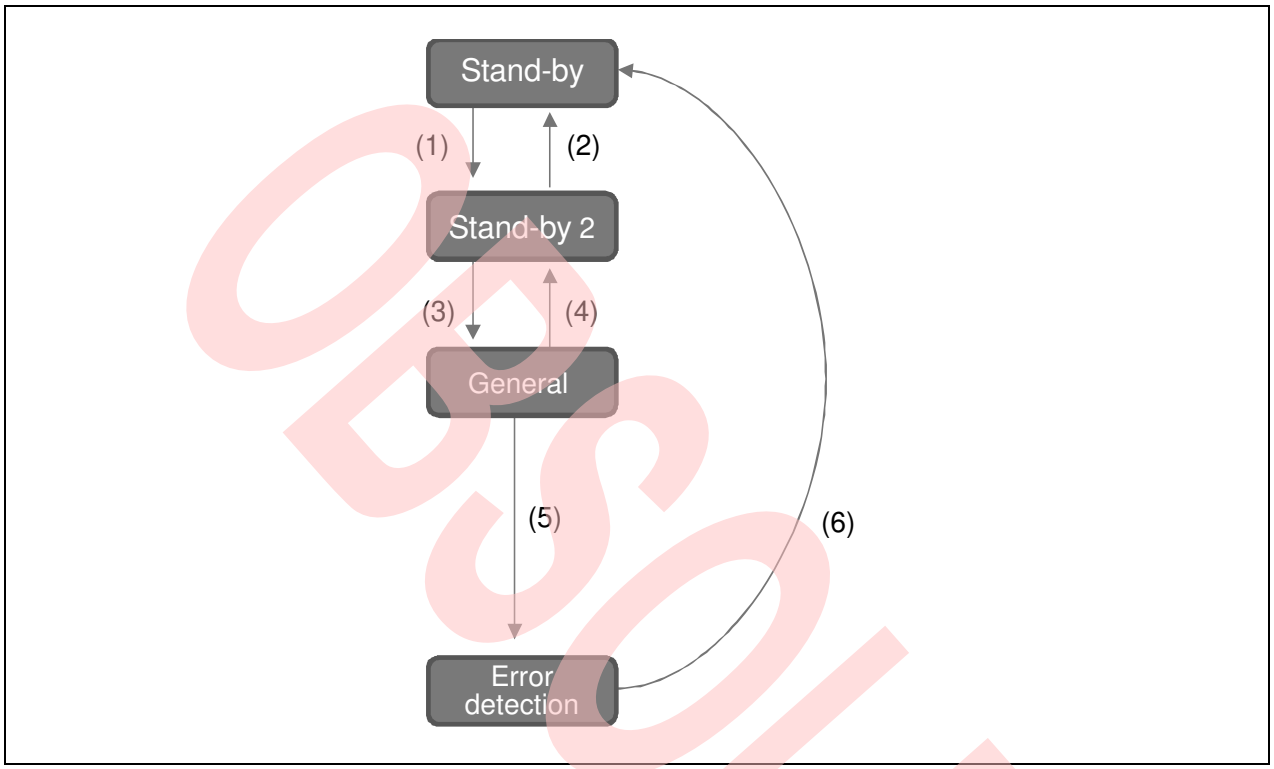
Priority of the external pin/I²C communication for CTL1, CTL2 and L

CTLMAIN (External Pin)	CTL* (External Pin)	CTL* (I²C Communication)	Relevant CH
H	H	H	Unavailable
H	H	L	ON
H	L	H	ON
H	L	L	OFF
L	X	Communication disabled	OFF

*:The I²C communication is enabled after the common block and digital block activation setting the external CTLMAIN pin to "H".

- When executing the ON/OFF control for DD1, DD2 and LDO using the external pin, don't execute the ON/OFF control using I²C. Aside from the ON/OFF control, it is possible to control everything else using I²C.
- When executing the ON/OFF control for DD1, DD2 and LDO using I²C, input "L" to the CTL* pin (the pin is open or in the GND connection condition).

10. State Transition Diagram



(1)External CTLMAIN pin "H"

(2)External CTLMAIN pin "L"

(3)External CTL pin "H" / I²C communication "relevant CH_ON"

(4)External CTL pin "L" / I²C communication "relevant CH_OFF"

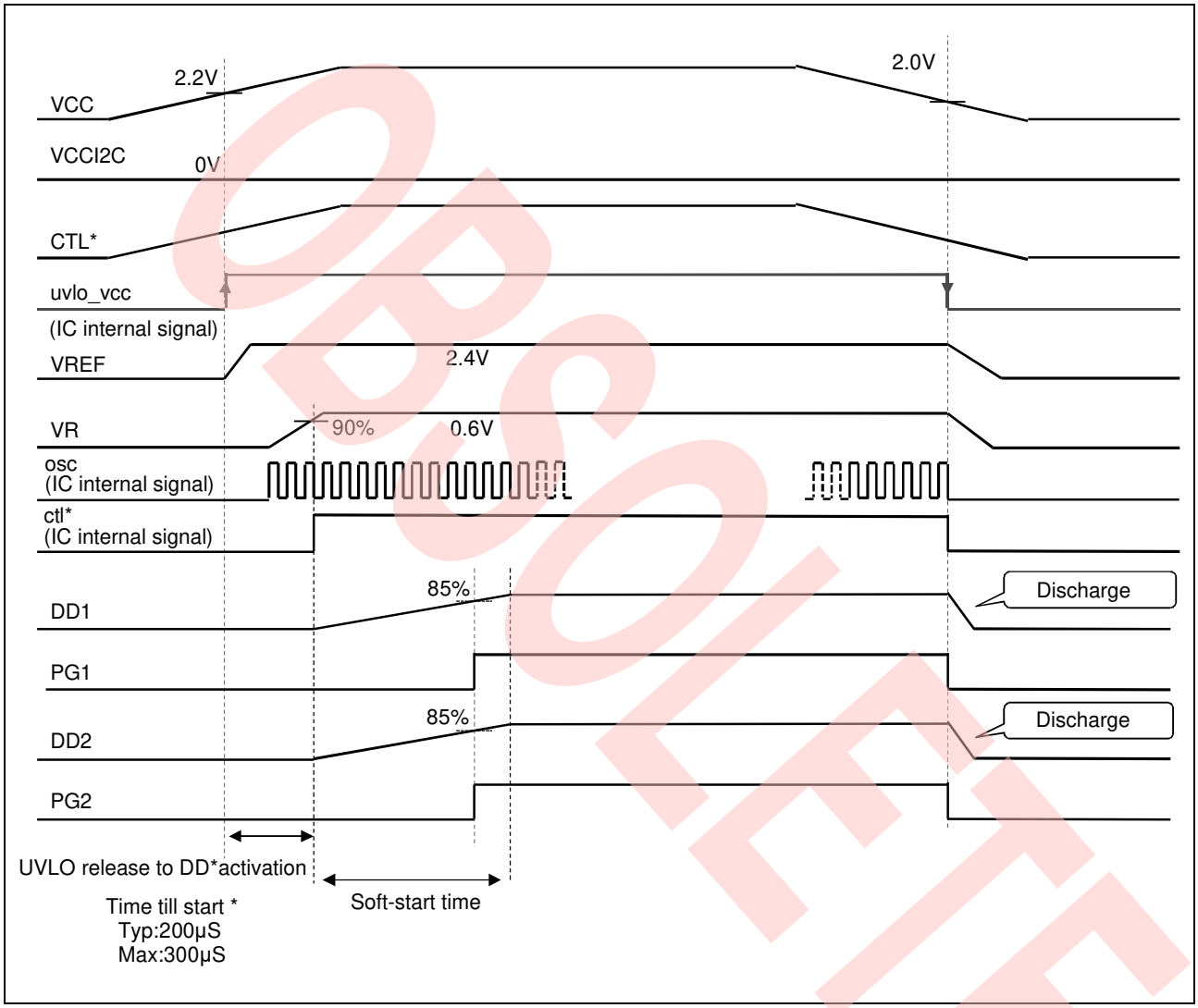
(5)Error detection (OCP, OCP_1ms continuation)

(6)Turning on the power supply again (equal to or less than uvlo_vcc reset voltage) or setting CTLMAIN to "L"

Notes:

- When executing the ON/OFF control for DD1, DD2 and LDO using the external pin, don't execute the ON/OFF control using I²C. Aside from the ON/OFF control, it is possible to control everything else using I²C.
- When executing the ON/OFF control for DD1, DD2 and LDO using I²C, input "L" to the CTL* pin (the pin is open or in the GND connection condition).

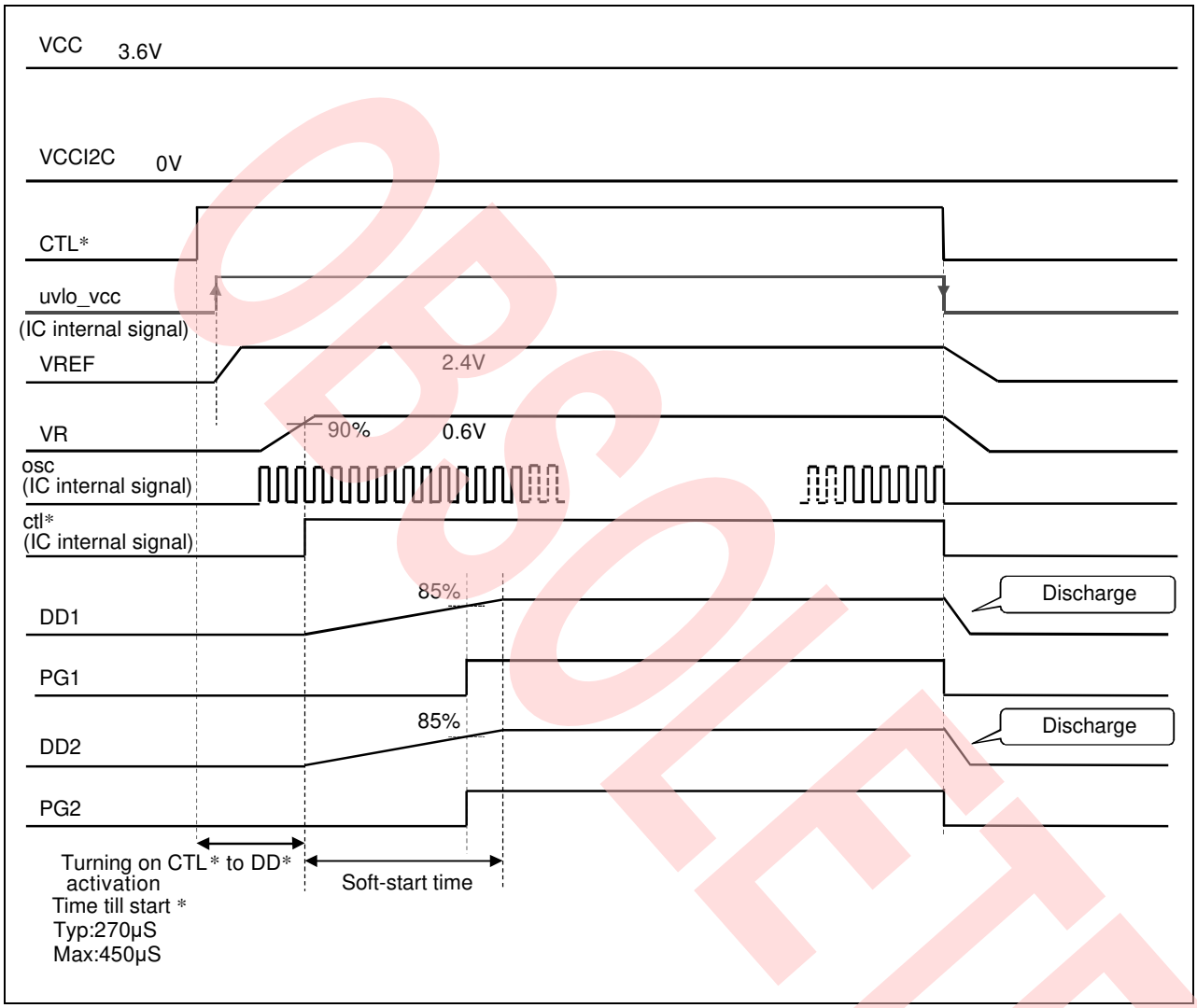
11. Turning On and Off Sequence (Turning On CTL*:CTL1, CTL2, CTLMAIN=VCC Simultaneously)



*: VREF and VR activations depend on the VREF pin capacitance and VR pin capacitance. Time in the sequence figure above is applied for the following condition.

- VREF pin capacitance : 0.1 µF
- VR pin capacitance : 0.47 µF

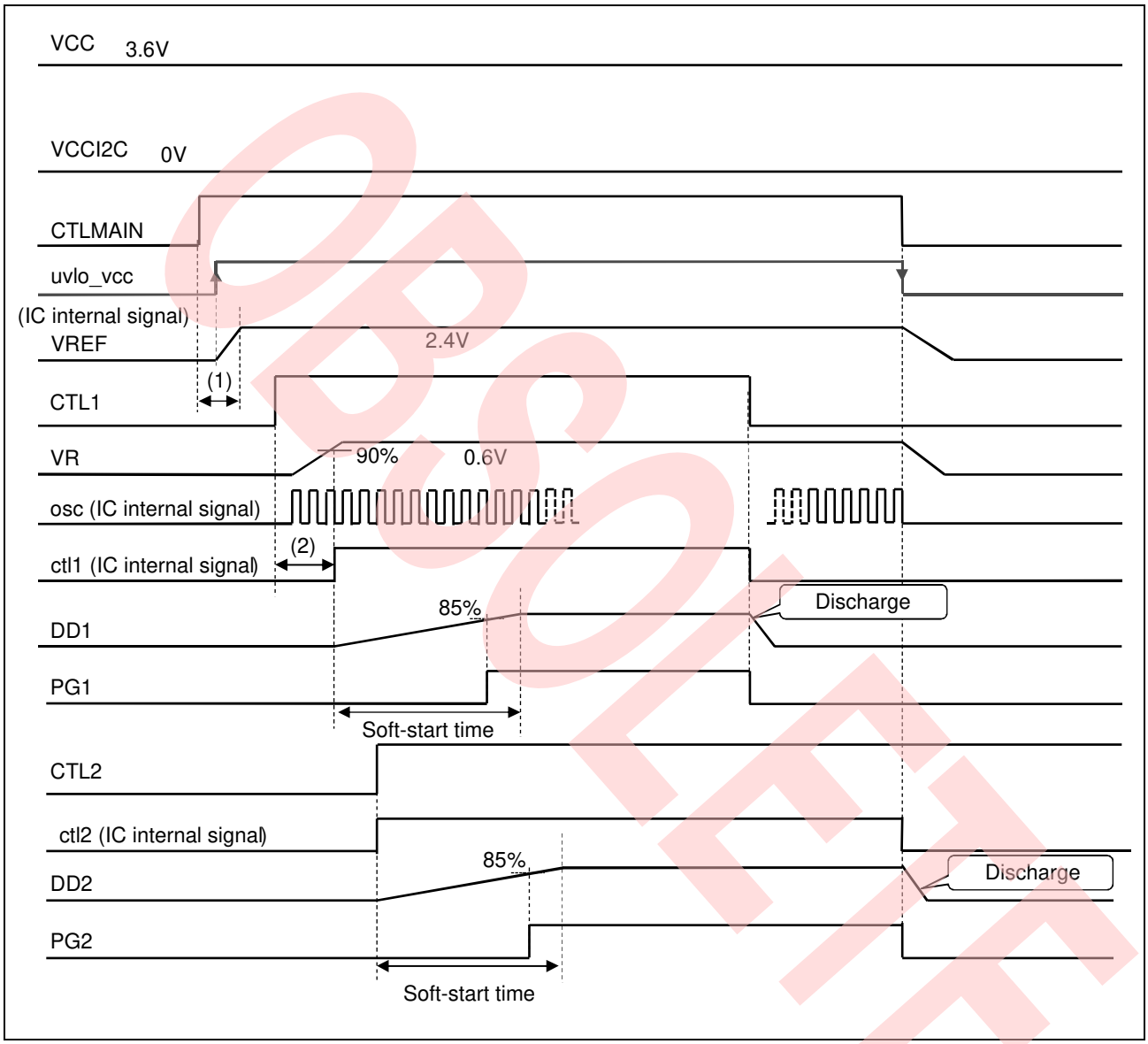
12. CTL* Turning On and Off Sequence 1 (VCC→CTL*: CTL1, CTL2, CTLMAIN)



*: VREF and VR activations depend on the VREF pin capacitance and VR pin capacitance. Time in the sequence figure above is applied for the following condition.

- VREF pin capacitance : 0.1 µF
- VR pin capacitance : 0.47 µF

13. CTL* Turning On and Off Sequence 2(VCC→CTLMAIN→CTL1→CTL2)



(1) Time from turning on CTLMAIN to VREF activation completion (=communication enabled)*
Typ: 130 µs, Max: 200 µs

(2) Time from turning on CTL1 to ctll (IC internal signal) "H"
Typ: 150 µs, Max: 250 µs

*: VREF and VR activations depend on the VREF pin capacitance and VR pin capacitance.
Time in the sequence figure above is applied for the following condition.

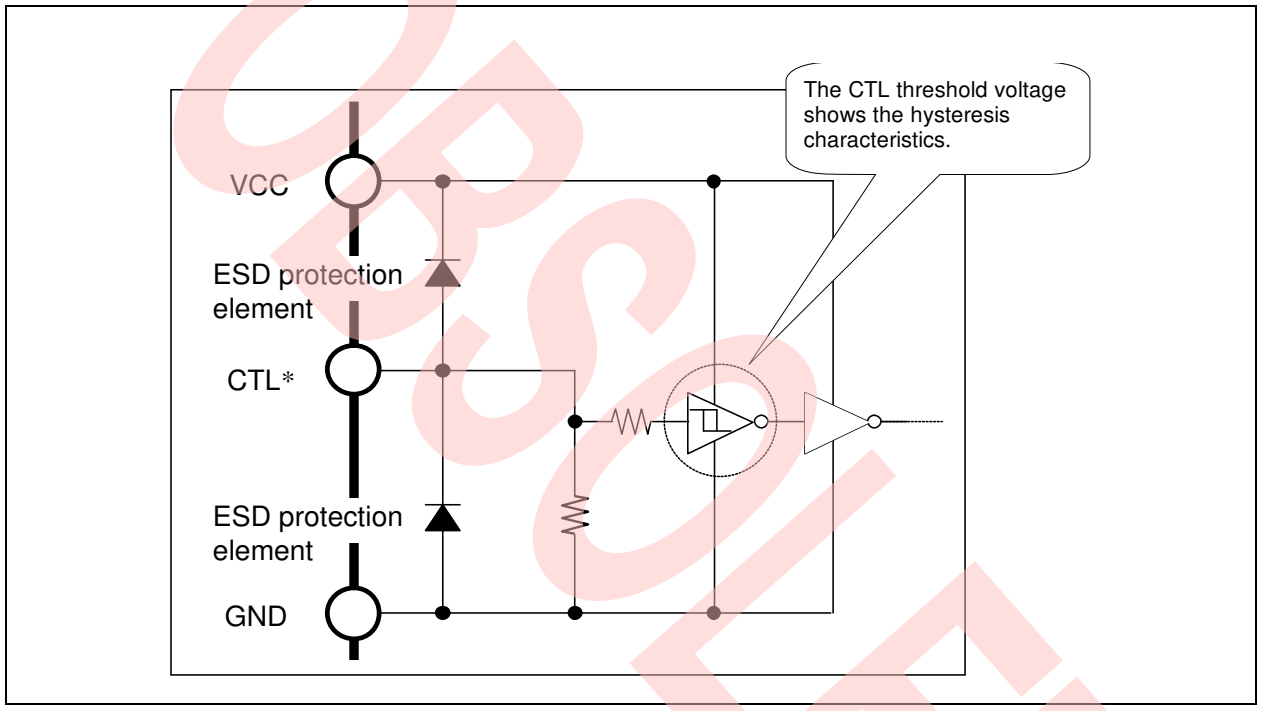
- VREF pin capacitance : 0.1 µF
- VR pin capacitance : 0.47 µF

14. CTL* Pin Threshold Voltage

The input circuit structure for the CTL* pin is the schmitt trigger style, and the threshold voltage shows the hysteresis characteristics when CTL* OFF → ON and ON → OFF. (See "･CTL* pin equivalent circuit diagram" below.)

Also, the threshold voltage level depends on the VCC pin voltage.
Moreover, make sure to input either the "H" level (>"VCC×0.7"V) or "L" level (<0.4 V) to the CTL* pin when in use.

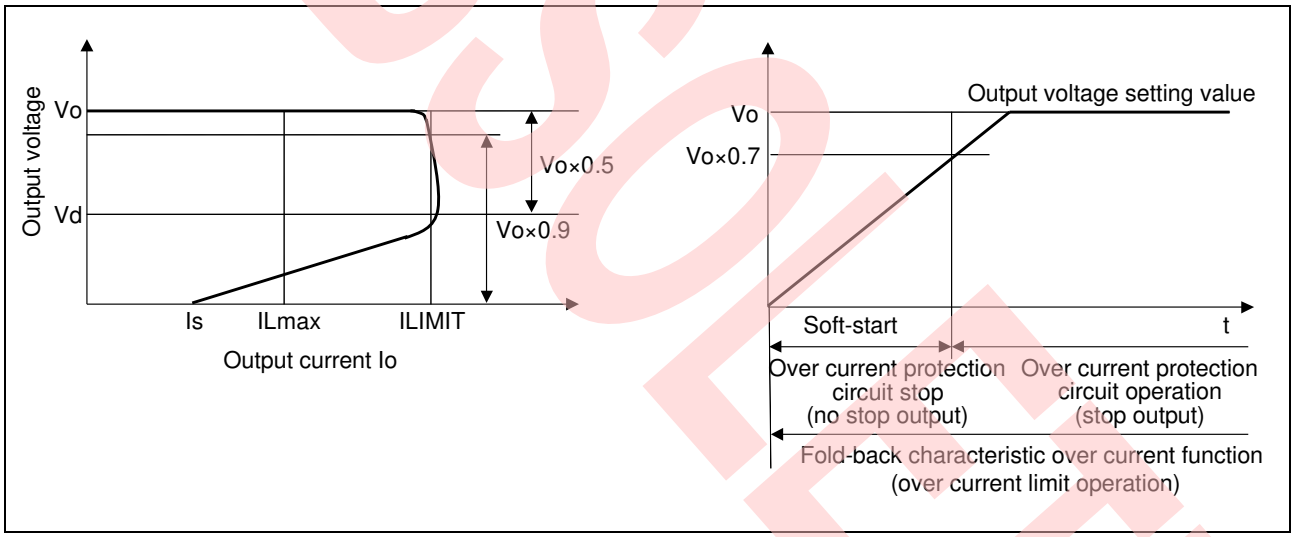
CTL* pin equivalent circuit diagram



15. Protection Operation Sequence

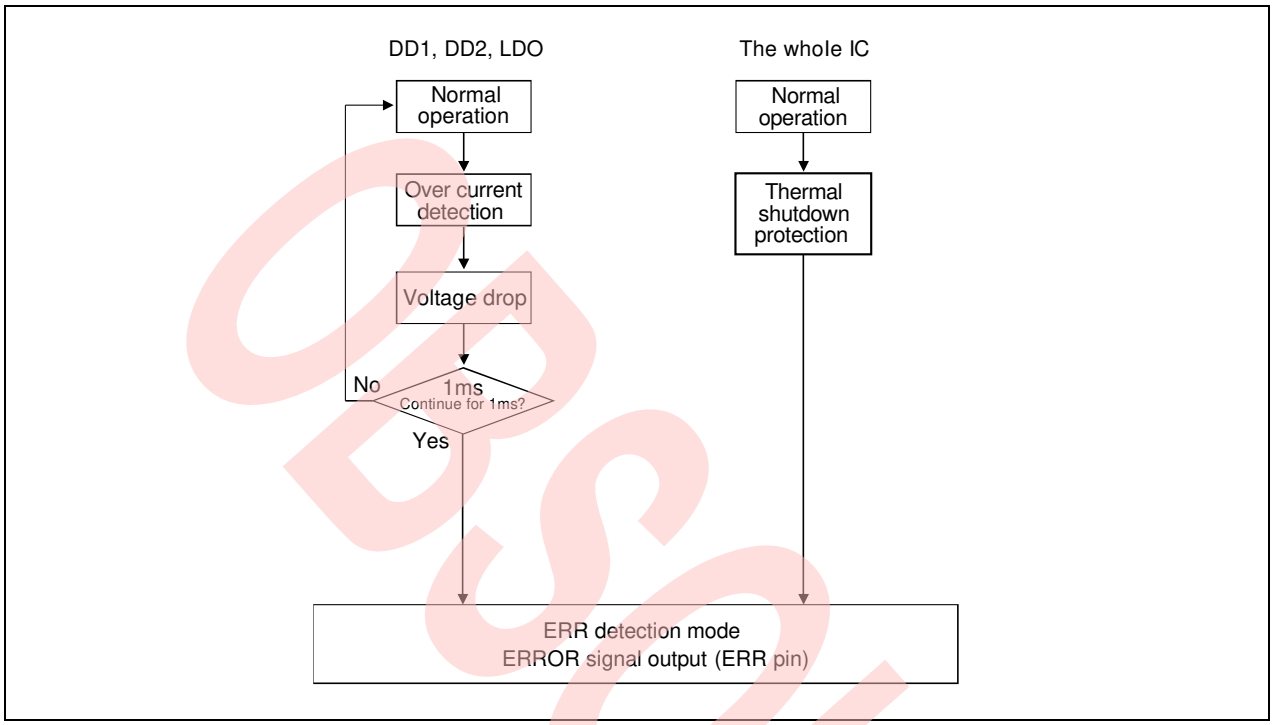
DD Channel
The DD channel monitors the FET current peak value at any time during the operation. When the DD output becomes the over current state, the output voltage is decreased. Afterward, the timer operation is performed and the output stops after about 1ms progress.

LDO Channel
It contains the fold-back type over current protection circuit in order to prevent destroy because of the over load and the output over current. It limits the output current and the output voltage from the peak around the over current protection value for LDO (ILIMIT) to the over current current (Is).
At this time, if the output voltage Vo gets lower than the detection voltage Vd (Vd: Vo×0.5), the timer operation starts and the output stops after about 1ms progress. Moreover, because the over current protection circuit does not operate at the soft-start (0 V to Vo × 0.7), neither the output stops nor the error signal outputs. However, the fold-back type over current protection characteristic functions. The following shows the fold-back type over current protection characteristic.



Thermal Shutdown Protection
If the temperature at the junction part reaches +150 °C, the thermal shutdown protection circuit turns all channels off.

Error Detection Sequence



ERR Detection Mode Release

It is necessary to turn the power supply on again, or to turn CTLMAIN on again to release the ERR detection mode.

16. Operation Condition, Stop Circuit and Release Condition for Protection Circuit

Channel	Operation Whilst Under Protection	Over Voltage Protection (OCP)	Under Voltage Lockout Protection (UVLO)	Thermal Shutdown Protection (TSD)
DD1, DD2	Discharge	Operating condition: After about 1ms progress in the over current condition Process during protection operation: DD1, DD2, LDO stop Recovery condition: (1) Power supply reasserted (2) CTLMAIN reasserted	Operating condition: Input voltage drop Process during protection operation: DD1, DD2, LDO stop Recovery condition: Input voltage rise UVLO operates only when CTLMAIN is "H" (normal operation).	Operating condition: Chip temperature increment Process during protection operation: DD1, DD2, LDO stop Recovery condition: (1) Power supply reasserted (2) CTLMAIN reasserted Only when CTLMAIN is in the "H" state and one of CTL1, CTL2 or L is in the "H" state, TSD will operate.
LDO	Discharge	Operating condition: After about 1ms progress in the over current condition Process during protection operation: DD1, DD2, LDO stop Recovery condition: (1) Power supply re-asserted (2) CTLMAIN reasserted		
ERR output (ERRpin)	-	"L" output when detecting OCP at CH of DD1, DD2, or LDO	No change	"L" output when detecting TSD

Thermal shutdown protection (TSD) operation during over current protection timer operation

When the thermal shutdown protection (TSD) operated during the over current protection (OCP) timer operation, the thermal shutdown protection has priority.

Operation when releasing under voltage lockout protection (UVLO)

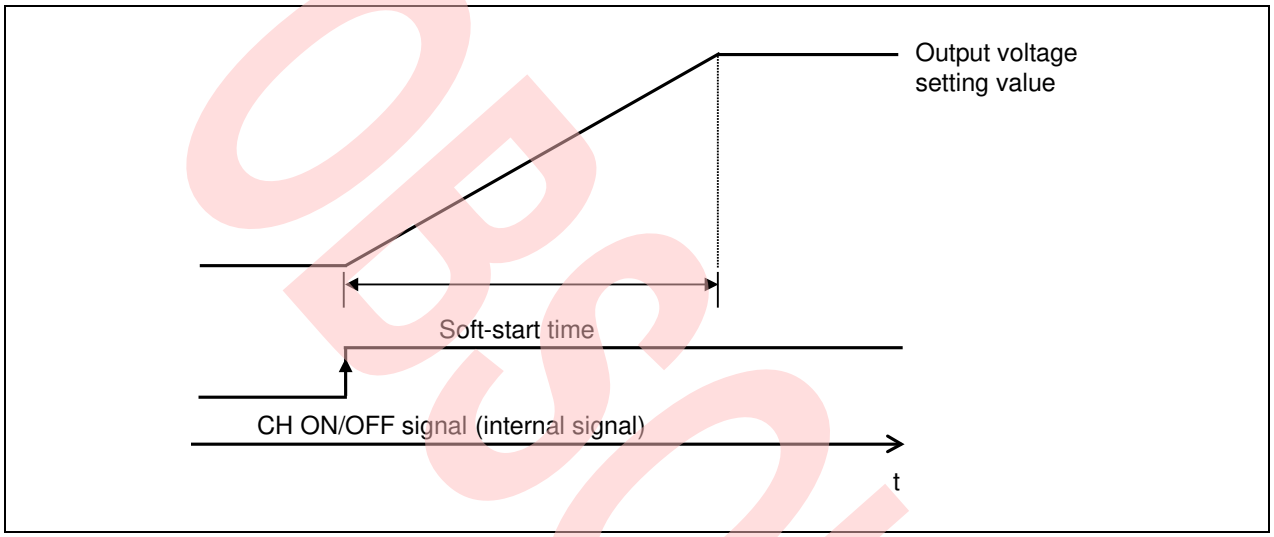
DD1, DD2 and LDO: Activation following the condition for CTL* pin

17. DD Soft-Start Operation

The soft-start operation for DD1, DD2 and LDO is enabled in order to prevent the rush current during the DD activation. The soft-start time can be controlled by I^2C.

Soft-start control: enabled to set at DD1, DD2 and LDO

DD, LDO Soft-start



18. Discharge Operation

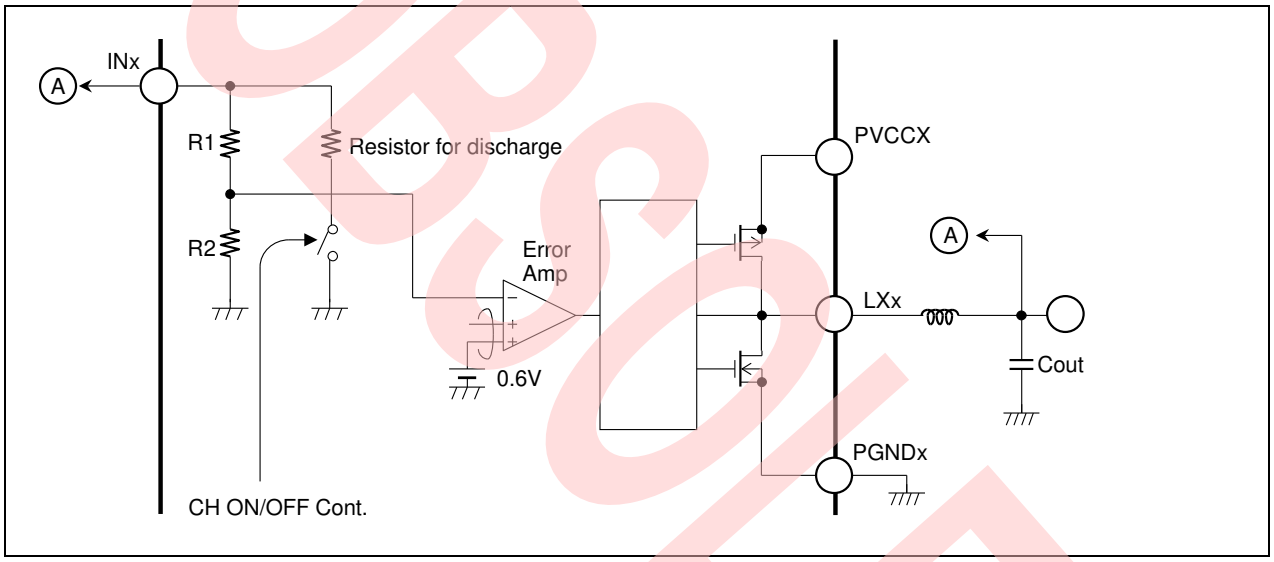
DD Channel

When executing the DD OFF operation at the CH ON/OFF signal, the DC/DC smooth capacitance charged for each output voltage is discharged using resistor for discharge which is set in the IC and the output voltage is decreased gradually. However, the discharge time changes depending on the DC/DC converter load current. The discharge time is calculated by the following equation.

Discharge time (time till the output becomes 10% without load)

toff(s) ≈ 2.3 × R_{DIS} × Cout(F)

Note: See the table in ELECTRICAL CHARACTERISTICS for the discharge resistor value.



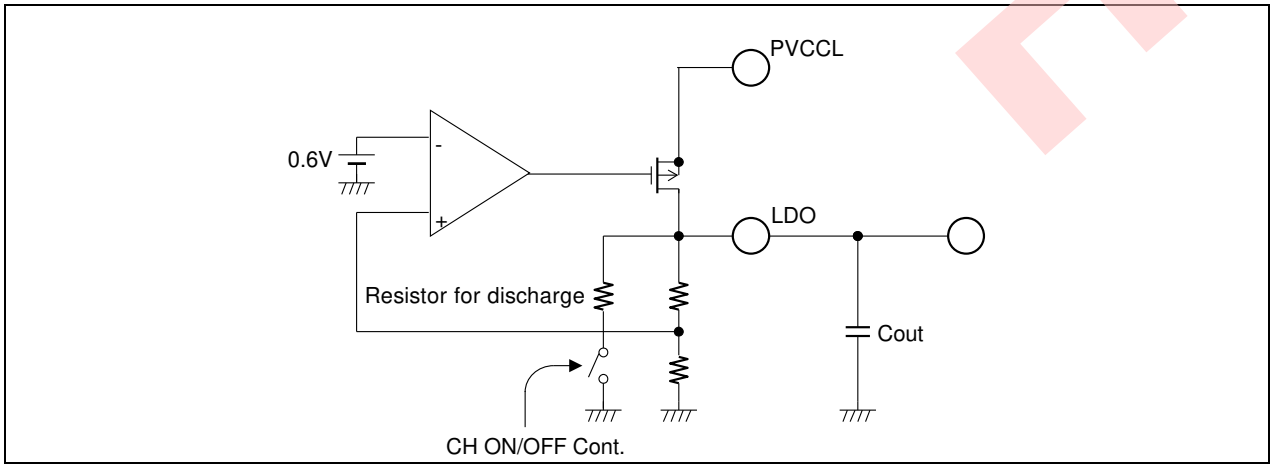
LDO Channel

When executing the LD OFF operation at the CH ON/OFF signal, the output capacitance charged for the output voltage is discharged using resistor for discharge which is set in the IC and the output voltage is decreased gradually. However, the discharge time changes depending on the output load current. The discharge time is calculated by the following equation.

Discharge time (time till the output becomes 10 % without load).

toff(s) ≈ 2.3 × R_{DIS}× Cout(F)

Note: See the table in ELECTRICAL CHARACTERISTICS for the discharge resistor value.



19. PG1/PG2/PGL PIN and ERR PIN

The following pins for each CH POWER GOOD output are prepared.

PG1

It is the pin for DD1 POWER GOOD output.
When the output voltage exceeds 85 % of the setting value at the DD1 ON mode, "H" is output.
Also, when the output voltage becomes equal to or lower than 75 % of the setting value after the "H" output, "L" is output.
"L" is output at the DD1 OFF mode.

PG2

It is the pin for DD2 POWER GOOD output.
When the output voltage exceeds 85% of the setting value at the DD2 ON mode, "H" is output.
Also, when the output voltage becomes equal to or lower than 75% of the setting value after the "H" output, "L" is output.
"L" is output at the DD2 OFF mode.

PGL

It is the pin for LDO POWER GOOD output.
When the output voltage exceeds 85 % of the setting value at the LDO ON mode, "H" is output.
Also, when the output voltage becomes equal to or lower than 75 % of the setting value after the "H" output, "L" is output.
"L" is output at the LDO OFF mode.

The following pin for the error state output is prepared.

ERR Pin

It is the pin for the error state output. "L" is output during the error detection mode.
The ERR detection mode is released by turning on the power supply or CTLMAIN again.

20. I²C Interface

1. Structure of I²C Interface

The I²C interface executes the data communication in 1 byte (8-bit) units using two signal lines (bus), a SCL (serial clock line) and a SDA (serial data line).

This bus is connected to multiple devices;

master: device to generate the clock signal and to control the data transfer (CPU and so on)

slave: device that an address is specified by a master.

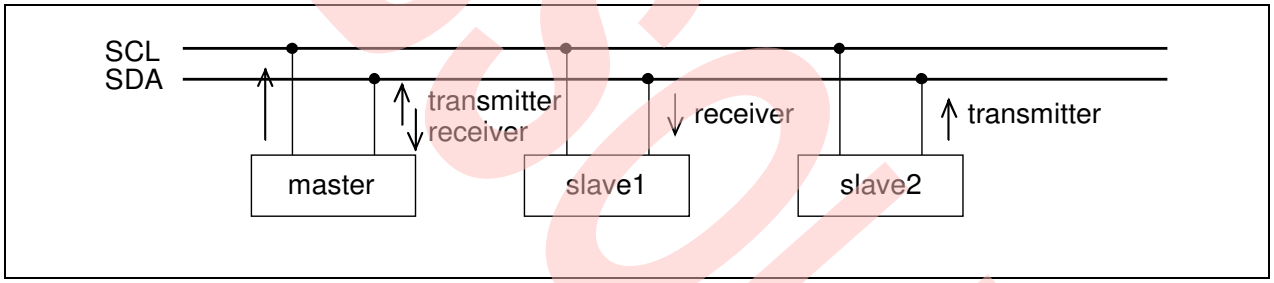
This IC is set as the slave and has no function to be the master.

Each device is defined due to the communication direction as described below.

transmitter: device to send data to bus

receiver: device to receive data from bus

The IC has the function both transmitter and receiver.



The IC defines the followings;

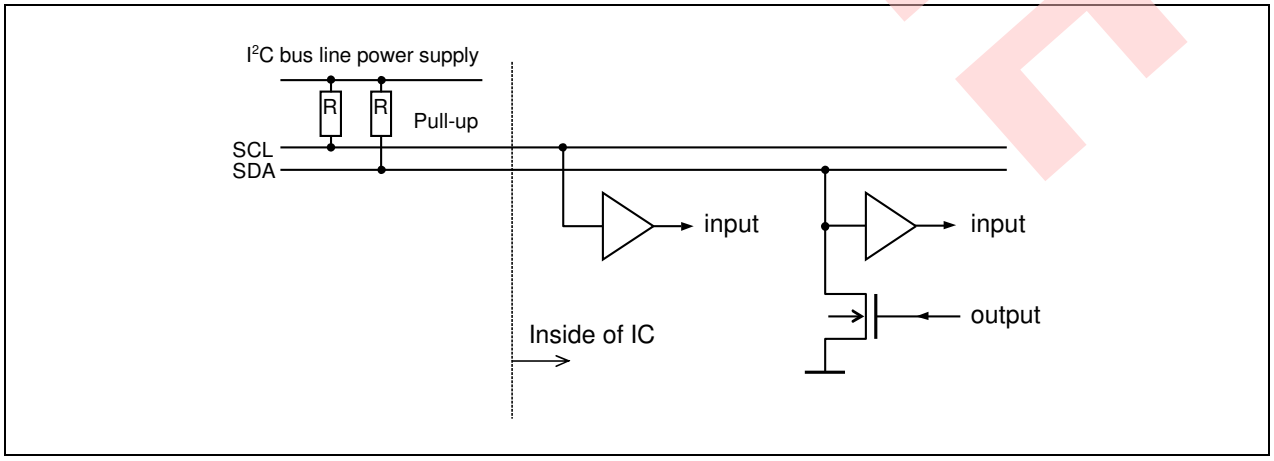
Write: data is transmitted from master and the IC receives data

Read: The IC transmits data and master receives data.

2. Definition of Signal Lines

SCL and SDA are connected to the power supply by the pull-up resistor.
The output circuit is the open Drain output.
When a bus is not used (waiting state), the open "H" is set changing the open Drain to the OFF state.

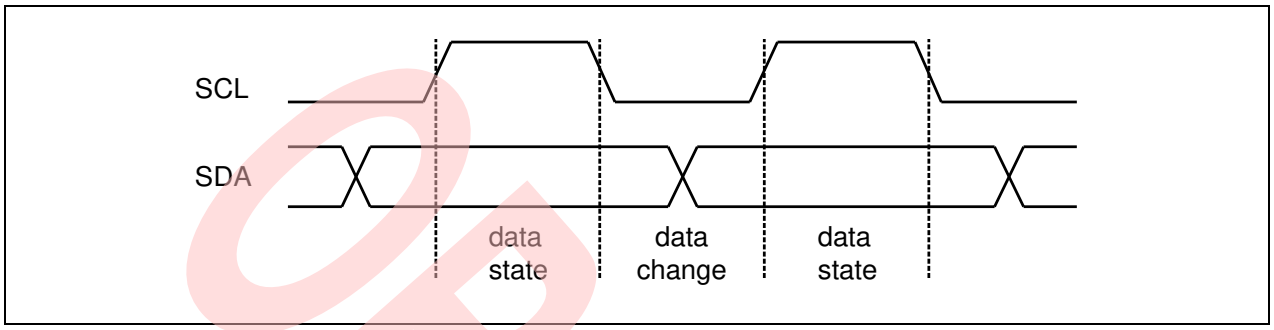
Note: SCL and SDA pins adopt a different ESD protection system from standard I²C specification because of ESD enhancement (see 2.3 I/O CIRCUIT TYPE).
When the power supply is in the bus line, don't shut off the power supply for an IC (VCCI2C).



3. Validity of Data

Data has the following characteristics;

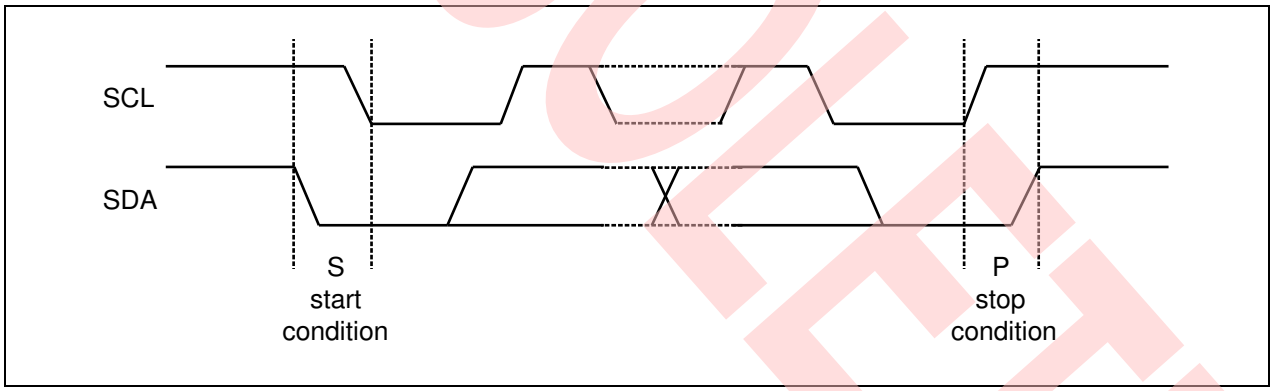
change when SCL is the "L" level
valid if the state is kept while SCL is the "H" level.



Moreover, the SDA signal change means the start or stop condition when SCL is the "H" level.

4. Definition of Start and Stop Condition

The start and stop conditions are output from the master and shows start and stop of communications to the slave.
Start: SDA changes from "H" to "L" when SCL is "H".
Stop: SDA changes from "L" to "H" when SCL is "H".

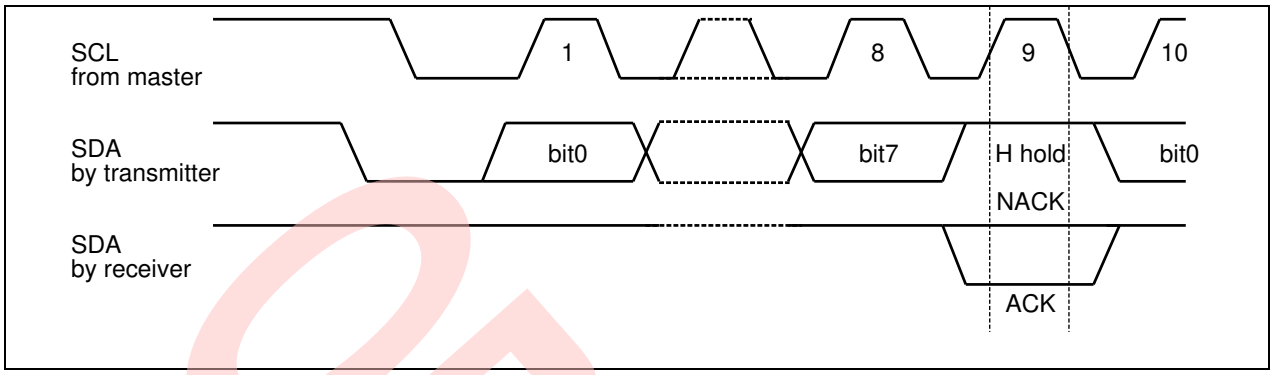


5. ACK Signal

This is a signal to confirm the data reception during communication.
The receiver replies the ACK signal to show the data reception to a transmitter every time 1 byte (8-bit) of data is received. The ACK signal is sent in 9clk after sending data 8-bit matching to the SCL signal that the master generates.

- A transmitter keeps SDA output "open H" in SCL9clk.
- A receiver informs the data reception situation to a transmitter outputting the followings in SCL 9 clk ;
  when data was received : SDA output "L" (ACK)
  when no data was received : SDA output "open H" (NACK)

However, if the master is changed to the receiver, ACK is not replied after the last data reception because the bus keeps open stopping the data transmission to the slave transmitter. In this case, the slave transmitter opens the bus (open H) and is set to the stop condition reception waiting state from the master.

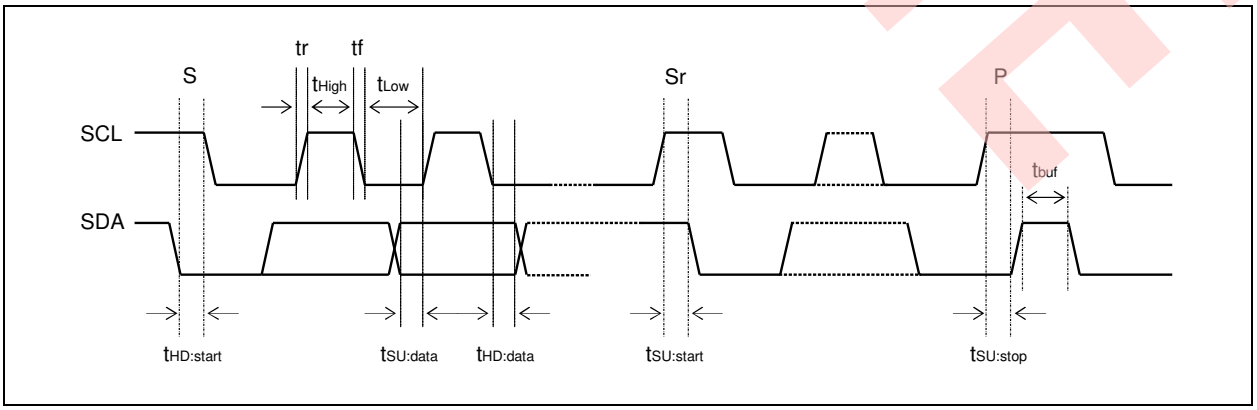


6. I²C Interface Input Timing

(within recommended operating conditions)

Parameter	Symbol	Value				Unit
		SCL=100 kHz		SCL=400 kHz		
		Min	Max	Min	Max	
SCL clock frequency	fSCL	-	100	-	400	kHz
Start condition hold time	$t_{HD:start}$	4.0	-	0.6	-	µs
Restart condition setup time	$t_{SU:start}$	4.7	-	0.6	-	µs
Stop condition setup time	$t_{SU:stop}$	4.0	-	0.6	-	µs
Stop to Start bus open time	t_{buf}	4.7	-	1.3	-	µs
SCL "L" time	t_{Low}	4.7	-	1.3	-	µs
SCL "H" time	t_{High}	4.0	-	0.6	-	µs
SCL/SDA rising time	t_r	-	1.0	-	0.3	µs
SCL/SDA falling time	t_f	-	0.3	-	0.3	µs
Data hold time	$t_{HD:data}$	0.0	-	0.0	-	µs
Data setup time	$t_{SU:data}$	0.25	-	0.10	-	µs
SCL/SDA capacitor load	C_b	-	400	-	400	pF

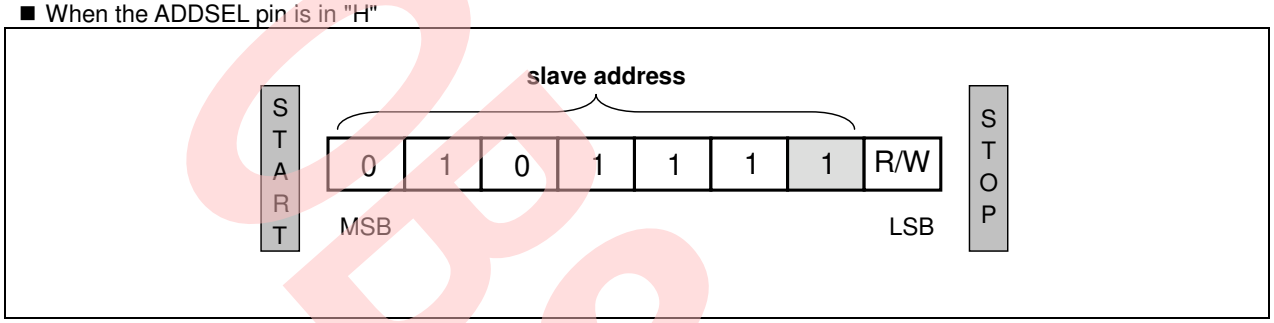
- VIH/VIL level reference
- Conform to I²C bus specifications



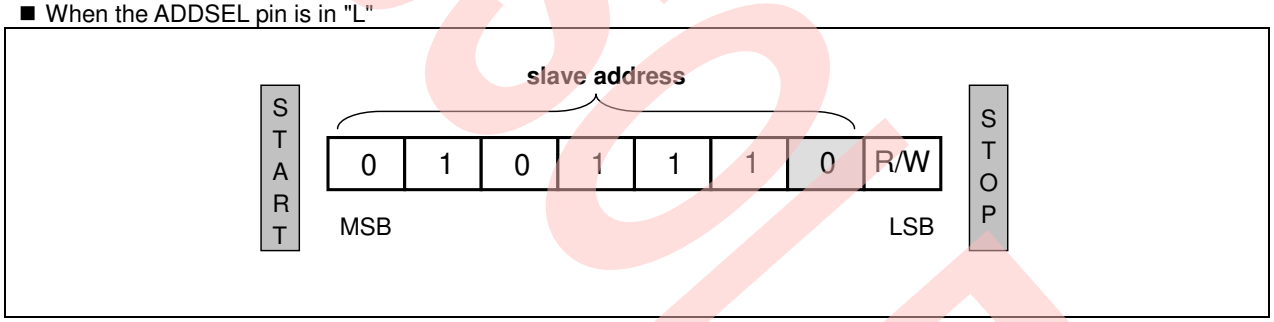
7. Slave Address

This is a slave address when communicating with the I²C interface.
The slave address of this IC is set by the first seven bits as shown below.
The seventh bit follows the ADDSEL pin and "0"/"1" are variable.
The eighth bit is called the least significant bit (LSB) and determines the message direction. The bit "0" shows that information will be written from the master to the slave.
The bit "1" shows that the master reads information from the slave.
This does not support the general call address.

■ When the ADDSEL pin is in "H"



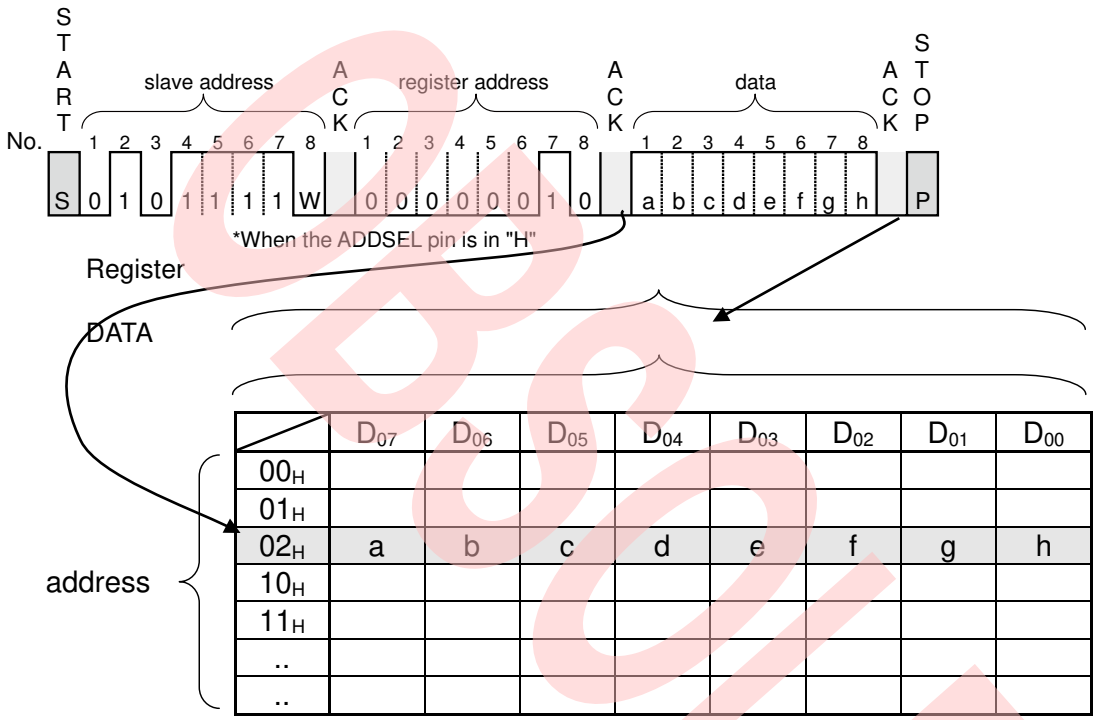
■ When the ADDSEL pin is in "L"



8. Bit Structure of Data on I²C Interface

(1) Writing data to register and reading data

The data line is sent/received in the order from the most significant bit (MSB) to the least significant bit (LSB).



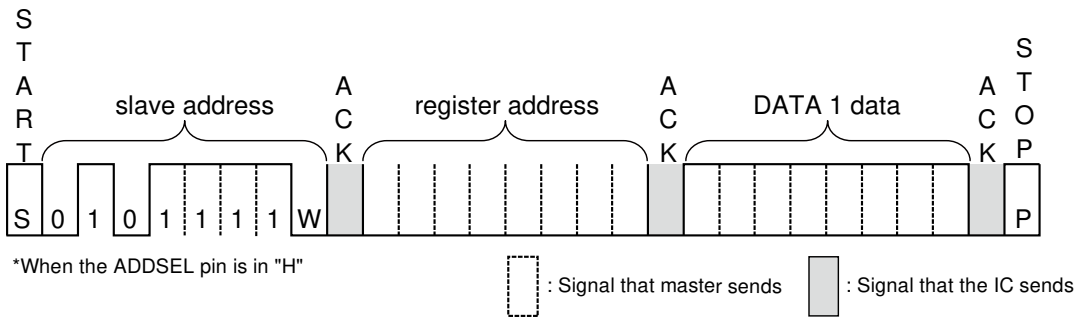
Output the "stop" condition after sending the Write data.

(2) I²C Interface Data Format

I²C Communication

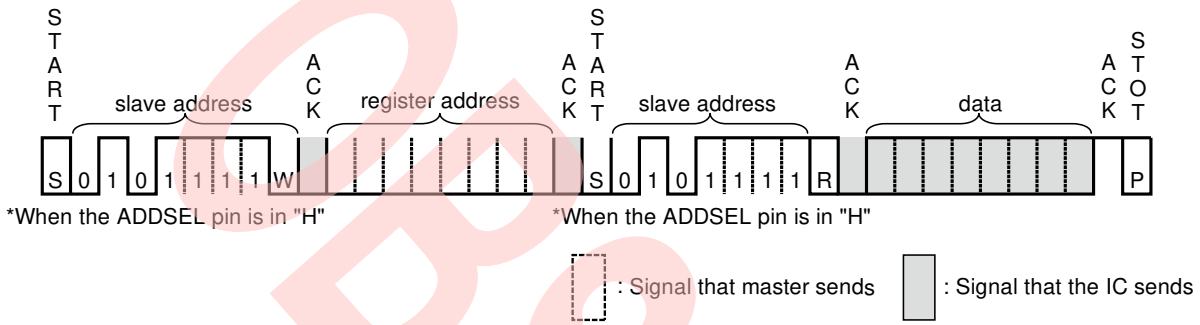
1. When a different slave address comes, non-matching ID is informed by not replying ACK after receiving the slave address.
2. All registers write to internal registers in the ACK signal after receiving the 8-bit data of each setting.
3. If a non-existing register address is specified, data is not written to a register.
4. Output the "stop" condition after sending the write data.

< During write (W)>



Write is allowed per one address. (sequential writing is not allowed.)
Send register address and data as one unit.

< During read (R) >



Read is allowed per one address. Be sure to perform read by specifying the register addresses.
(sequential reading is not allowed.)

21. Structure of I²C Interface and Data

Register Map

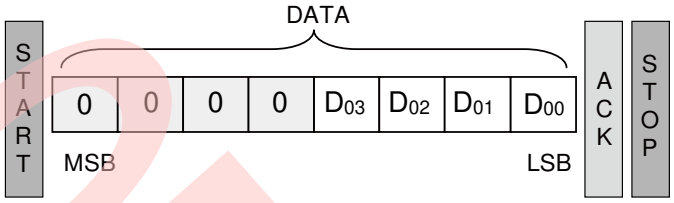
	Address	DATA								Writing Timing	Remarks
		d07	d06	d05	d04	d03	d02	d01	d00	Default	
Output voltage	00_H	X	X	X	X	D03	D02	D01	D00	00_H* 05_H* $0A_H$* $0F_H$*	ACK	DD1 output voltage setting
	01_H	X	X	X	X	D03	D02	D01	D00	00_H* 03_H* 06_H* $0C_H$*	ACK	DD2 output voltage setting
	02_H	X	X	X	X	X	X	D01	D00	03_H	ACK	LDO output voltage setting
Soft start	10_H	X	X	X	X	D03	D02	D01	D00	01_H	ACK	DD1 soft-start time setting
	11_H	X	X	X	X	D03	D02	D01	D00	01_H*/ 03_H*	ACK	DD2 soft-start time setting
	12_H	X	X	X	X	D03	D02	D01	D00	03_H	ACK	LDO soft-start time setting
DD operation mode	20_H	X	X	X	X	X	X	D01	D00	00_H	ACK	DD1, DD2 operation mode setting "0": Fixed PWM mode, "1": PFM/PWM mode
ON/OFF	30_H	X	X	X	X	X	D02	D01	D00	00_H	ACK	DD1, DD2, LDO output ON/OFF setting "0":Output OFF/ "1":Output ON
For test	FX_H	-	-	-	-	-	-	-	-	-	-	Disabled

*: The value depends on the preset value.

- Because the "X" block in the register map has no register, "0" is returned when in reading.
- The address FX_H is used for tests. It is normally disabled.
  Don't read/write to the FX_H address.

(1) DD1 and DD2 output voltage control

1. Addresses 00_H, 01_H are allocated as registers for the DC/DC output voltage control.
2. The DC/DC output voltage control is controlled by writing data to addresses 00_H, 01_H.



address 00_H : For DD1 output voltage setting
address 01_H : For DD2 output voltage setting
D_{03} to D_{00}: Set the output voltage

DD1 output voltage setting table

DATA	Output Voltage
00_H	1.00*
01_H	1.02
02_H	1.04
03_H	1.06
04_H	1.08
05_H	1.10*
06_H	1.12
07_H	1.14
08_H	1.16
09_H	1.18
$0A_H$*	1.20*
$0B_H$	1.22
$0C_H$	1.24
$0D_H$	1.26
$0E_H$	1.28
$0F_H$	1.30*

[V]

DD2 output voltage setting table

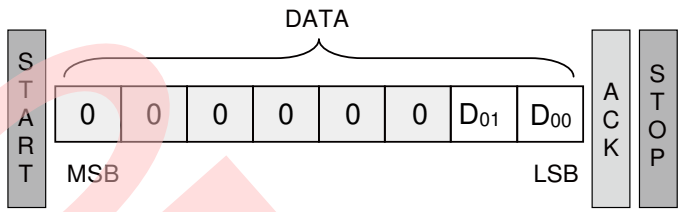
DATA	Output Voltage
00_H	1.20*
01_H	1.25
02_H	1.30
03_H	1.35*
04_H	1.40
05_H	1.45
06_H	1.50*
07_H	1.55
08_H	1.60
09_H	1.65
$0A_H$	1.70
$0B_H$	1.75
$0C_H$*	1.80*
$0D_H$	1.85
$0E_H$	1.90
$0F_H$	1.95

[V]

*: The selectable output voltage setting as preset value.

(2) LDO output voltage control

1. Address 02_H is allocated as a register for the LDO output voltage control.
2. The LDO output voltage control is controlled by writing data to addresse 02_H.



address 02_H: For LDO output voltage setting
D_{01} to D_{00}: Set the output voltage

LDO output voltage setting table

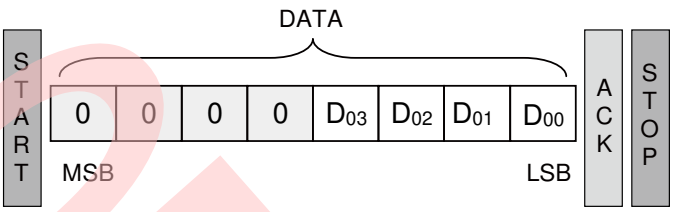
DATA	Output Voltage
00_H	2.80
01_H	2.85*
02_H	3.00
03_H*	3.30*

[V]

*: The selectable output voltage using the preset value changing products

(3) Soft start time

1. Address 10_H to 12_H are allocated as registers for the soft start time control.
2. The soft start time control is controlled by writing data to addresses 10_H to 12_H.



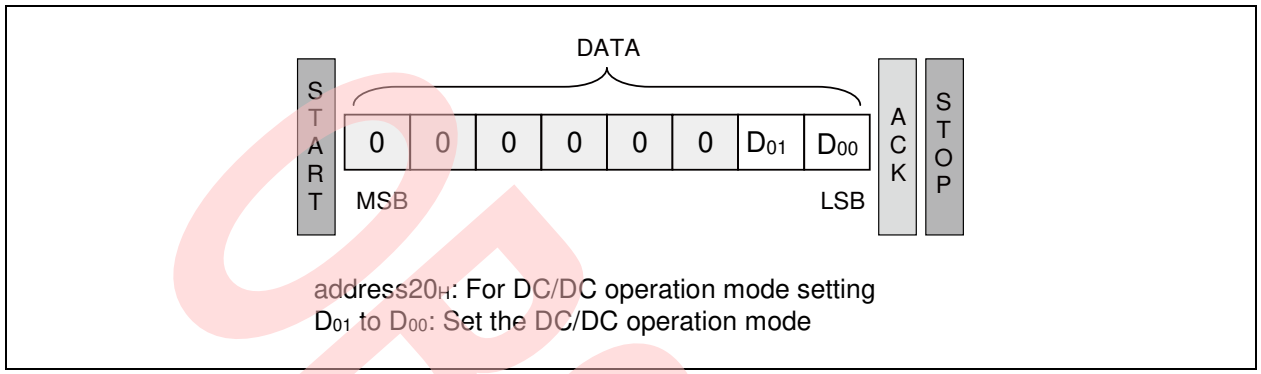
address10_H: For DD1 soft start time setting
address11_H: For DD2 soft start time setting
address12_H: For LDO soft start time setting
D_{03} to D_{00}: Set the soft start time

Soft start time setting table

DATA1	Soft Start Time	Default Setting
00_H	14.3ms	
01_H	0.9ms	DD1, DD2
02_H	1.8ms	
03_H	2.7ms	LDO
04_H	3.6ms	
05_H	4.5ms	
06_H	5.4ms	
07_H	6.3ms	
08_H	7.2ms	
09_H	8.1ms	
$0A_H$	9.0ms	
$0B_H$	9.9ms	
$0C_H$	10.8ms	
$0D_H$	11.6ms	
$0E_H$	12.5ms	
$0F_H$	13.4ms	

(4) DC/DC operation mode

1. Address 20_H is allocated as a register for the DC/DC operation mode control.
2. The DC/DC operation mode is controlled by writing data to address 20_H.

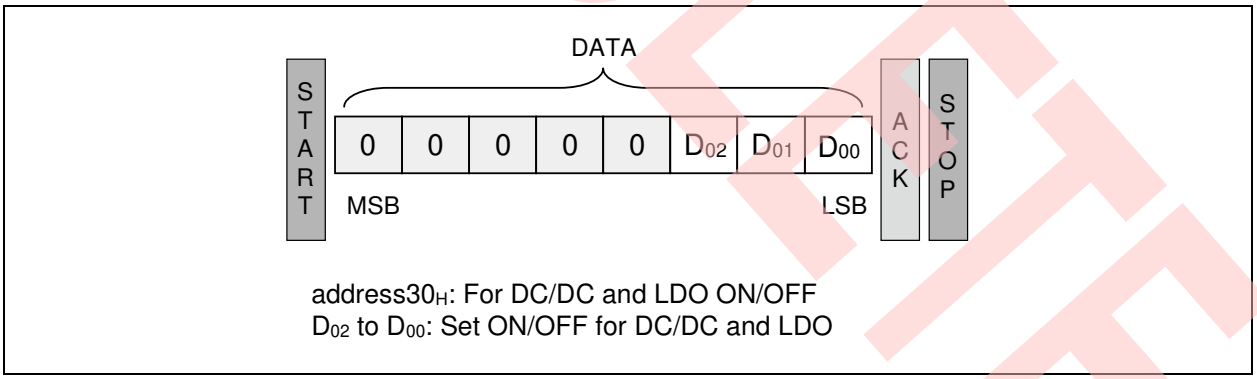


Address	Bit	Value	Description	Value	Description
20_H	D00	0*	DD1 Fixed PWM*	1	DD1 PFM/PWM
20_H	D01	0*	DD2 Fixed PWM*	1	DD2 PFM/PWM

*: It is a preset value.

(5) ON/OFF for DC/DC and LDO

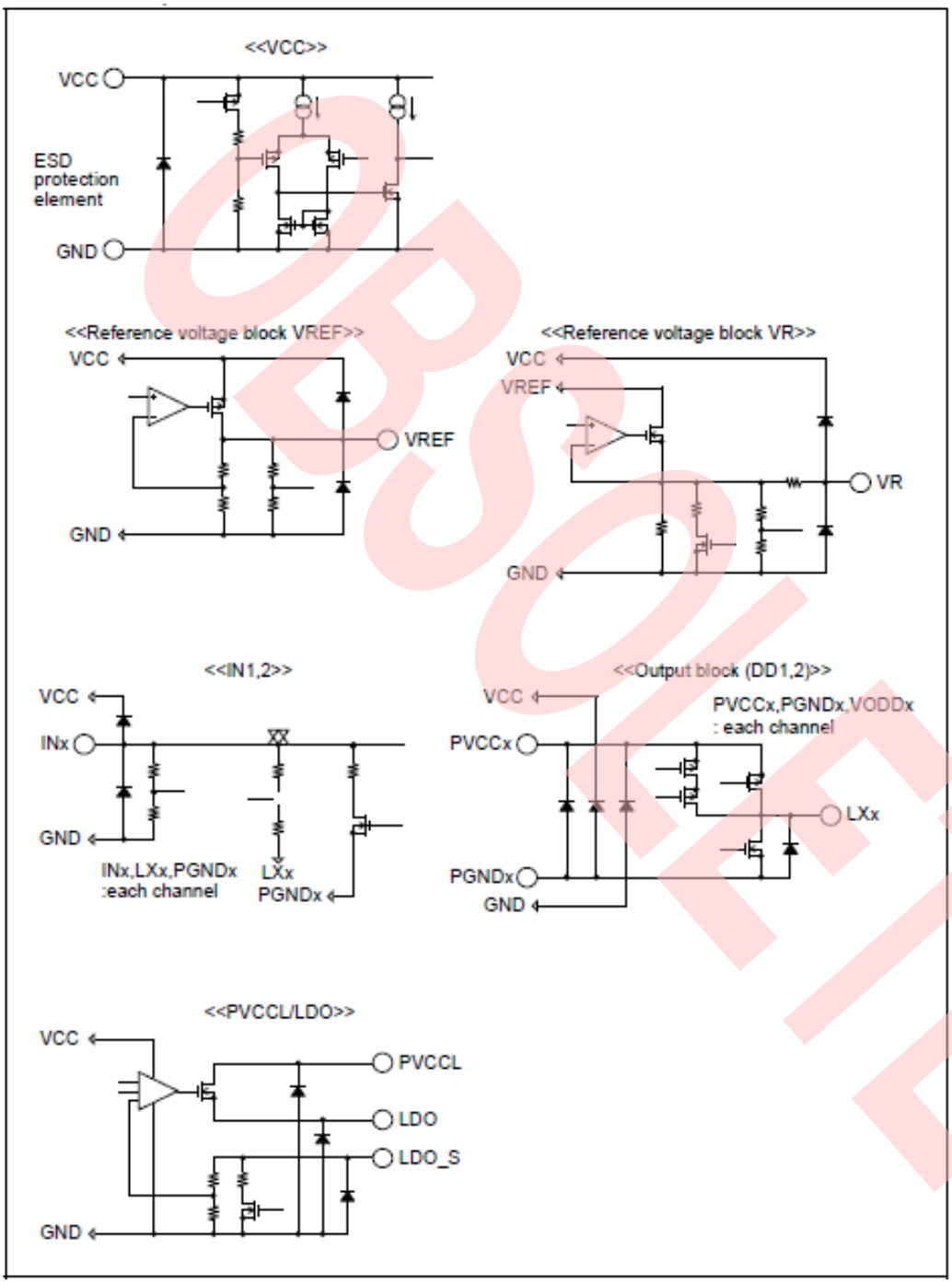
1. Address 30_H is allocated as a register for the DC/DC and LDO ON/OFF.
2. The DC/DC and LDO ON/OFF is controlled by writing data to address 30_H.



Address	Bit	Value	Description	Value	Description
30_H	D00	0*	DD1 output OFF*	1	DD1 output ON
30_H	D01	0*	DD2 output OFF*	1	DD2 output ON
30_H	D02	0*	LDO output OFF*	1	LDO output ON

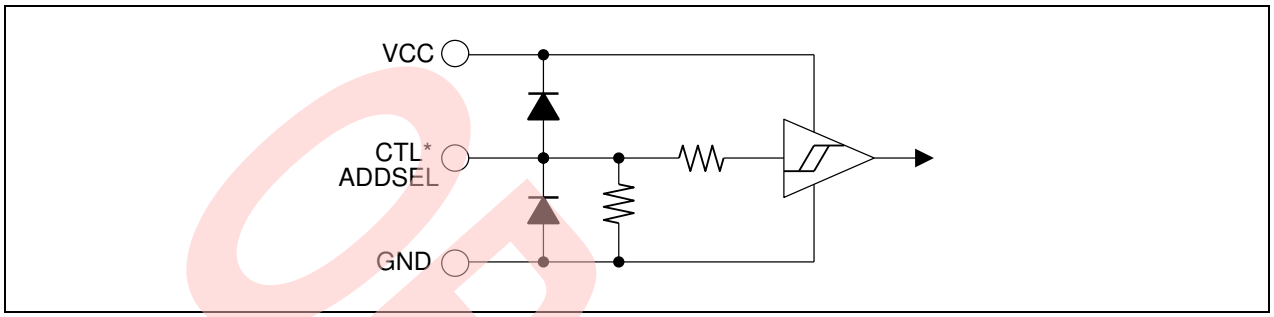
*: It is a preset value.

22. I/O Pin Equivalent Circuit Diagram

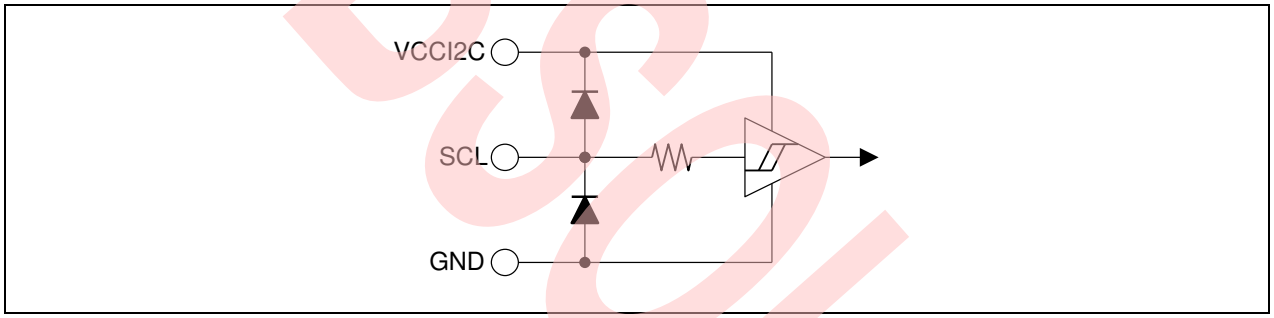


23. I/O Circuit Type

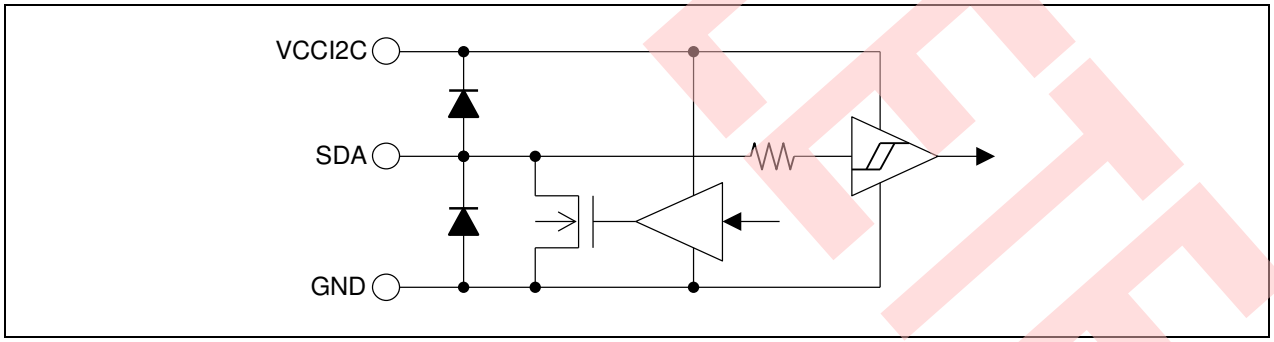
CTLMAIN/CTL1/CTL2/CTLL/ADDSEL pins



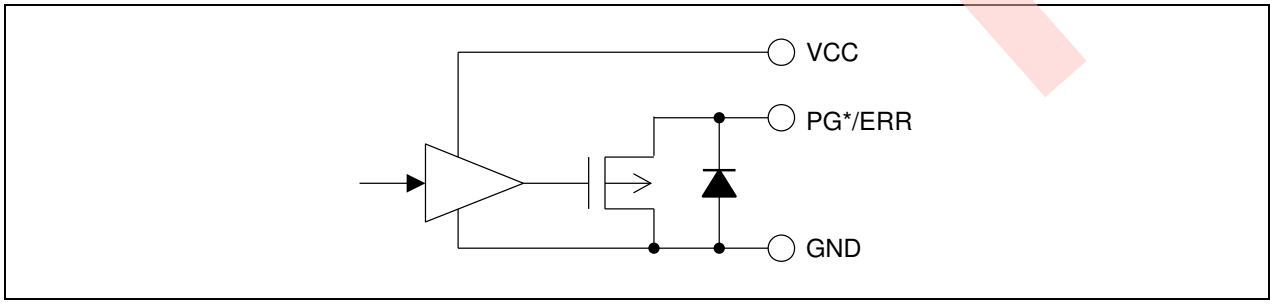
SCL pin



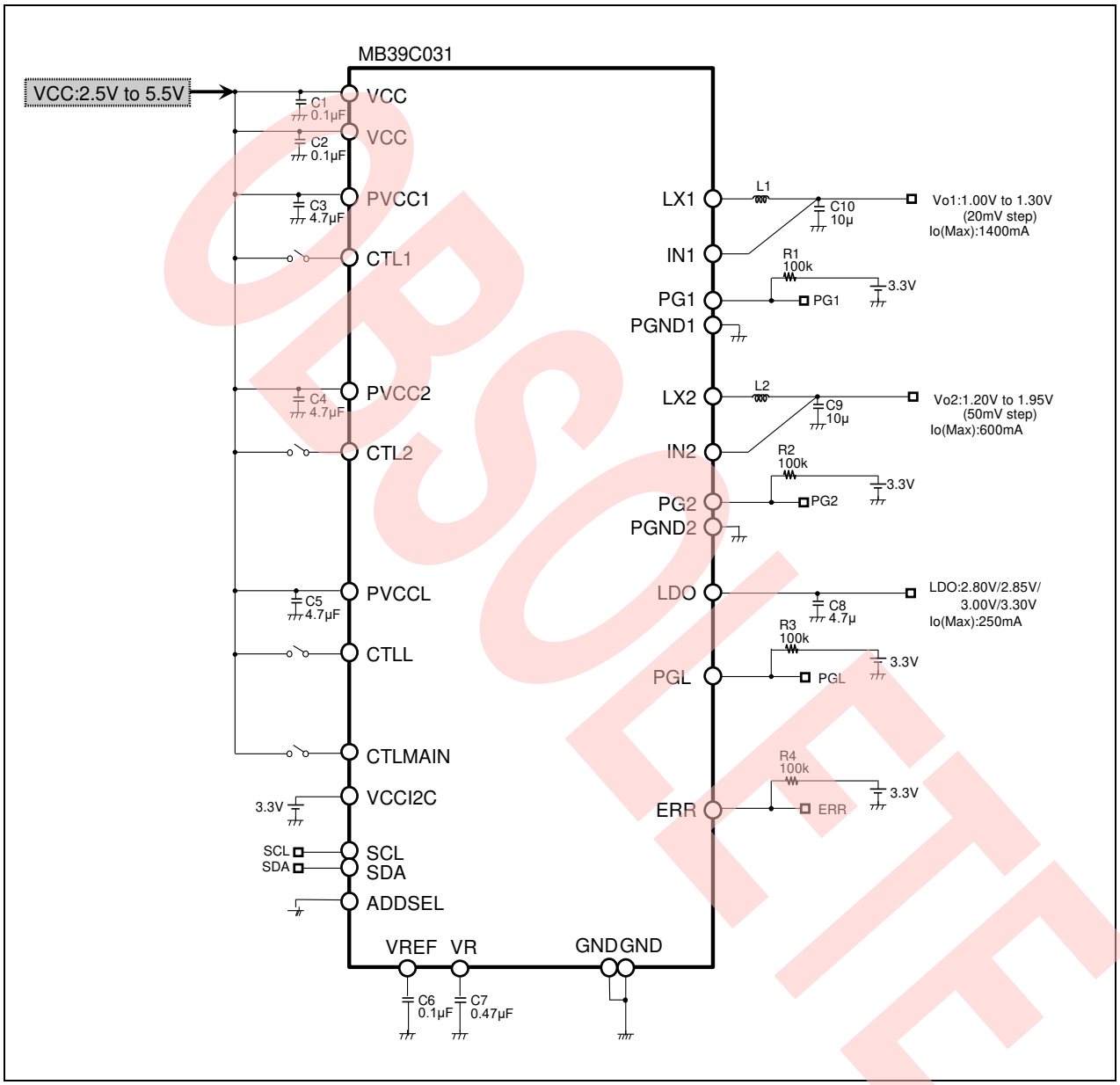
SDA pin



PG1/PG2/PGL/ERR pins



24. Typical Operation Characteristic Measurement Circuit



Part List

Symbol (Circuit Diagram Notation)	Parts	Part Number	Specifications	Vendor
L1	Metal alloy inductor	1299AS-H-1R5N	1.5 µH	TOKO
L2	Metal alloy inductor	1299AS-H-1R5N	1.5 µH	TOKO
C1	Ceramic Capacitor	C1608X5R1H104K	0.1 µF	TDK
C2	Ceramic Capacitor	C1608X5R1H104K	0.1 µF	TDK
C3	Ceramic Capacitor	C1608X5R1V475K	4.7 µF	TDK
C4	Ceramic Capacitor	C1608X5R1V475K	4.7 µF	TDK
C5	Ceramic Capacitor	C1608X5R1V475K	4.7 µF	TDK
C6	Ceramic Capacitor	C1608X5R1H104K	0.1 µF	TDK
C7	Ceramic Capacitor	C1608X5R1H474K	0.47 µF	TDK
C8	Ceramic Capacitor	C1608X5R1V475K	4.7 µF	TDK
C9	Ceramic Capacitor	C1608X5R1A106K	10 µF	TDK
C10	Ceramic Capacitor	C1608X5R1A106K	10 µF	TDK
R1	Resistor	RR0816P-104-D	100 kΩ	SSM
R2	Resistor	RR0816P-104-D	100 kΩ	SSM
R3	Resistor	RR0816P-104-D	100 kΩ	SSM
R4	Resistor	RR0816P-104-D	100 kΩ	SSM

TOKO: TOKO, INC.

TDK: TDK Corporation

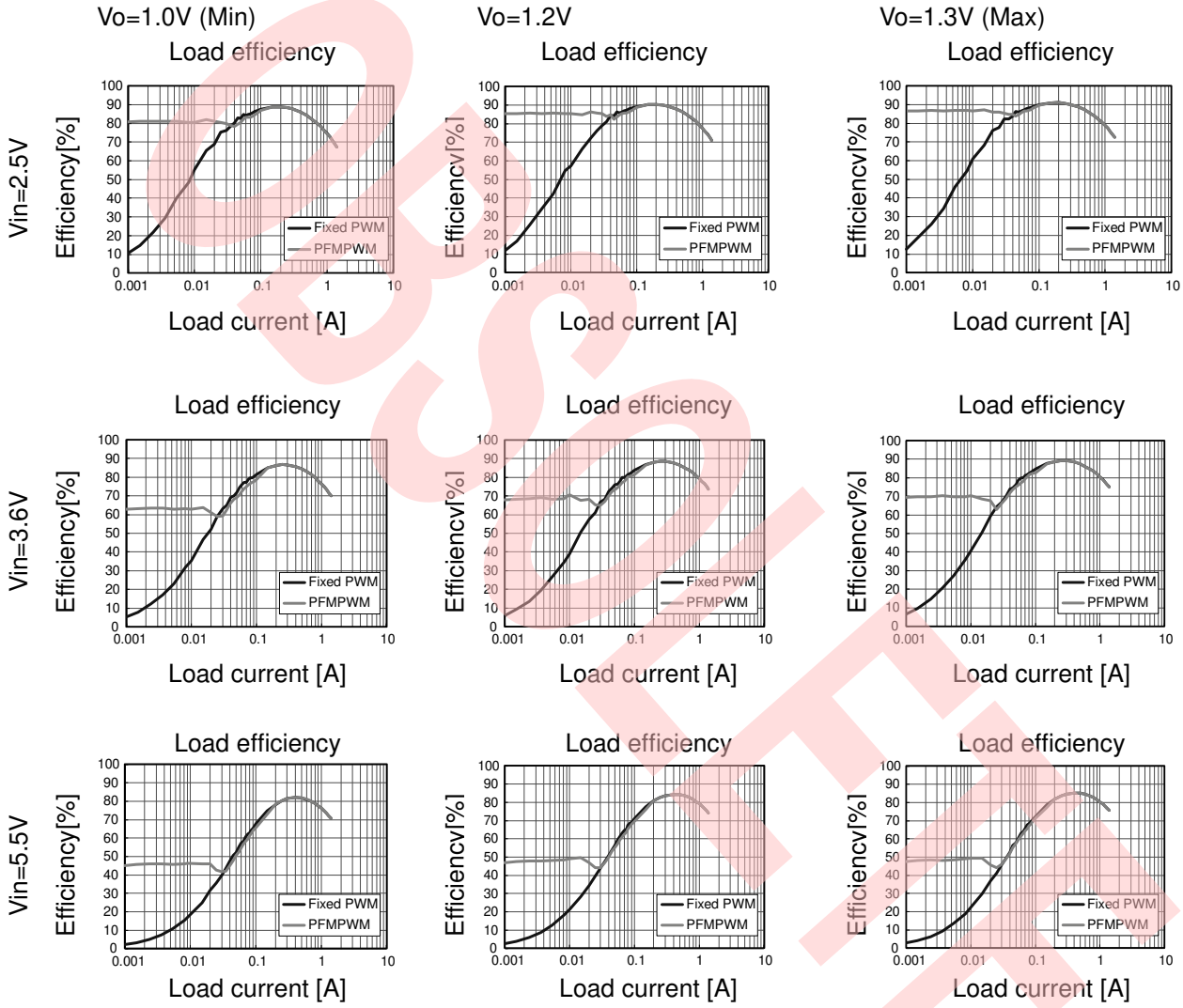
SSM: SUSUMU CO., LTD.

Note: The list above is recommended parts.

25. Reference Data

■ DC/DC Load Efficiency Characteristics

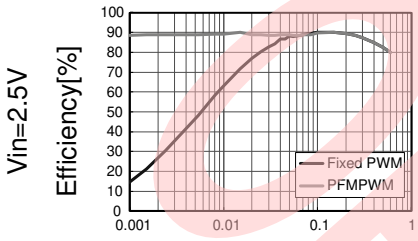
• DD1

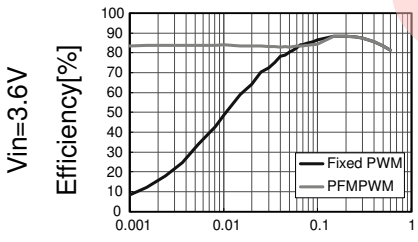


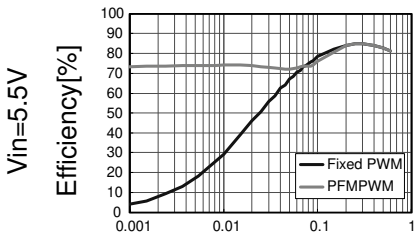
• DD2

Vo=1.2V (Min)

Load efficiency

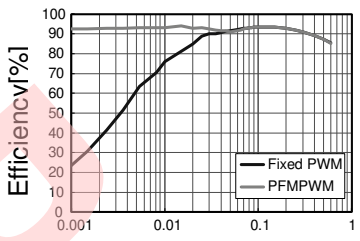




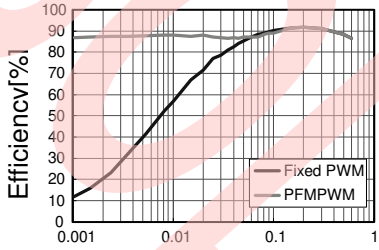


Vo=1.8V

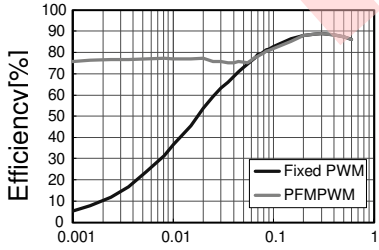
Load efficiency



Load efficiency

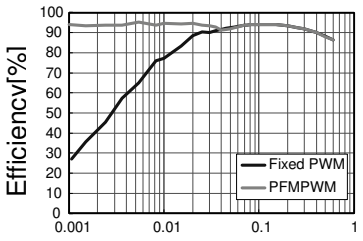


Load efficiency

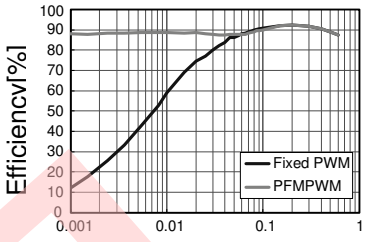


Vo=1.95V (Max)

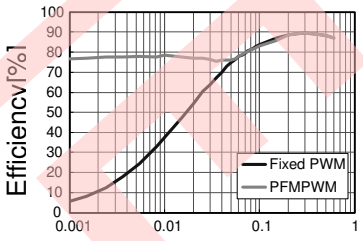
Load efficiency



Load efficiency



Load efficiency

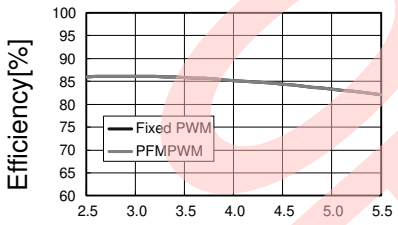


■ DC/DC Line Efficiency Characteristics

• DD1

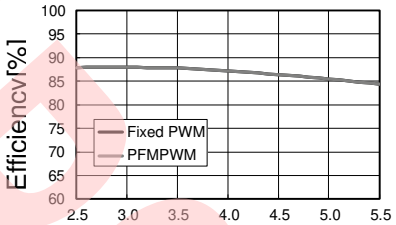
Vo=1.0V (Min)

Line efficiency characteristics (Io=400mA)



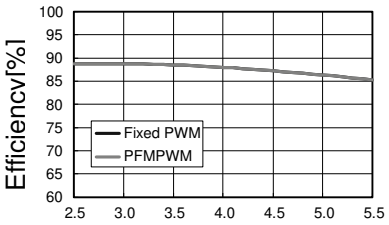
Vo=1.2V

Line efficiency characteristics (Io=400mA)



Vo=1.3V (Max)

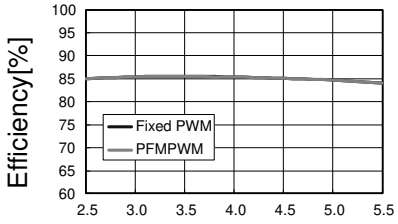
Line efficiency characteristics (Io=400mA)



• DD2

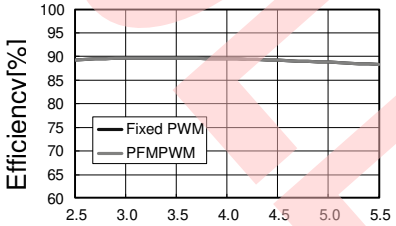
Vo=1.2V (Min)

Line efficiency characteristics (Io=400mA)



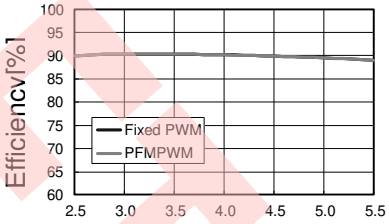
Vo=1.8V

Line efficiency characteristics (Io=400mA)



Vo=1.95V (Max)

Line efficiency characteristics (Io=400mA)

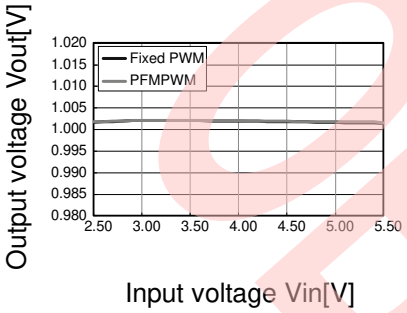


■ DC/DC Line Regulation Characteristics

• DD1

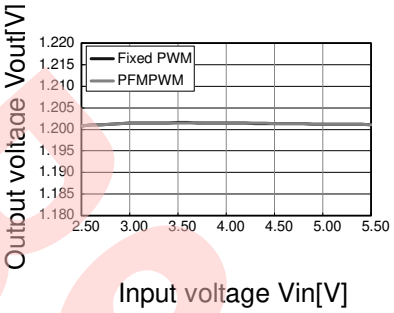
Vo=1.0V (Min)

Line regulation
(Io=400mA)



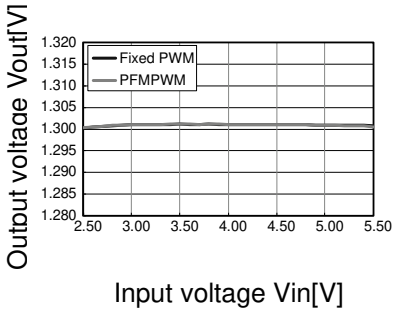
Vo=1.2V

Line regulation
(Io=400mA)



Vo=1.3V (Max)

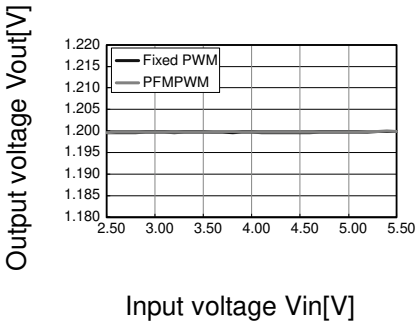
Line regulation
(Io=400mA)



• DD2

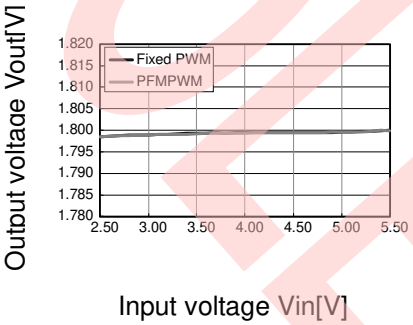
Vo=1.2V (Min)

Line regulation
(Io=400mA)



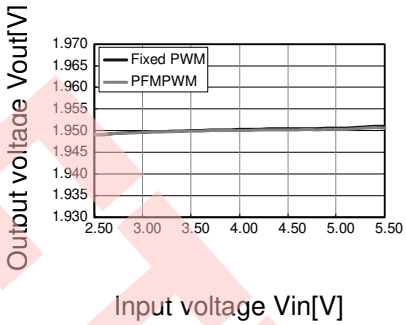
Vo=1.8V

Line regulation
(Io=400mA)



Vo=1.95V (Max)

Line regulation
(Io=400mA)

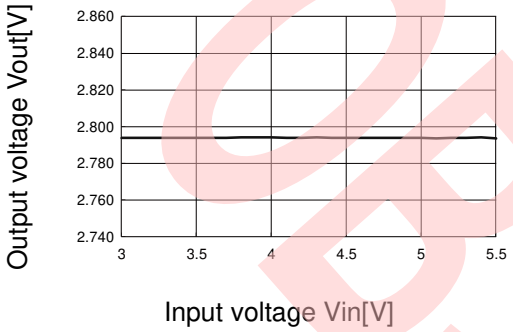


■ LDO Line Regulation Characteristics

• LDO

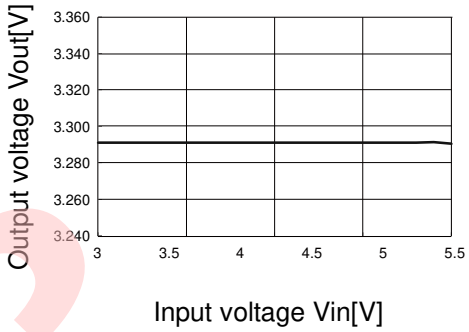
Vo=2.8V (Min)

Line regulation
(Io=50mA)



Vo=3.3V (Max)

Line regulation
(Io=50mA)



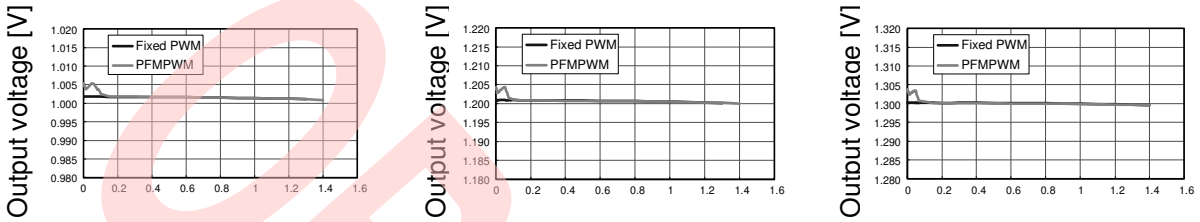
■ DC/DC Load Regulation Characteristics

• DD1

Vo=1.0V (Min) | Vo=1.2V | Vo=1.3V (Max)

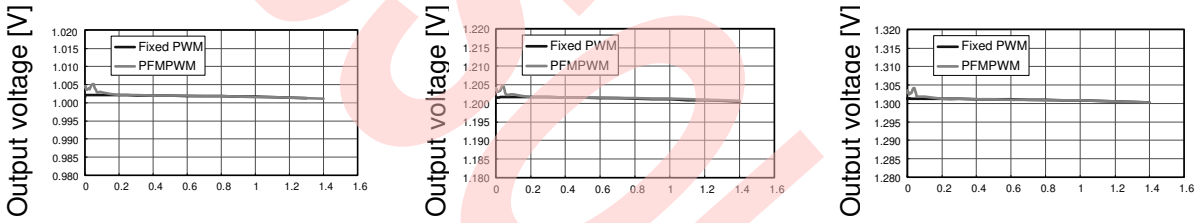
Load regulation

Vin=2.5V



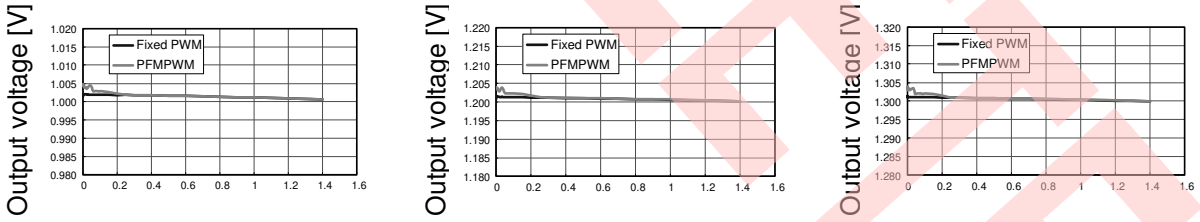
Load regulation

Vin=3.6V



Load regulation

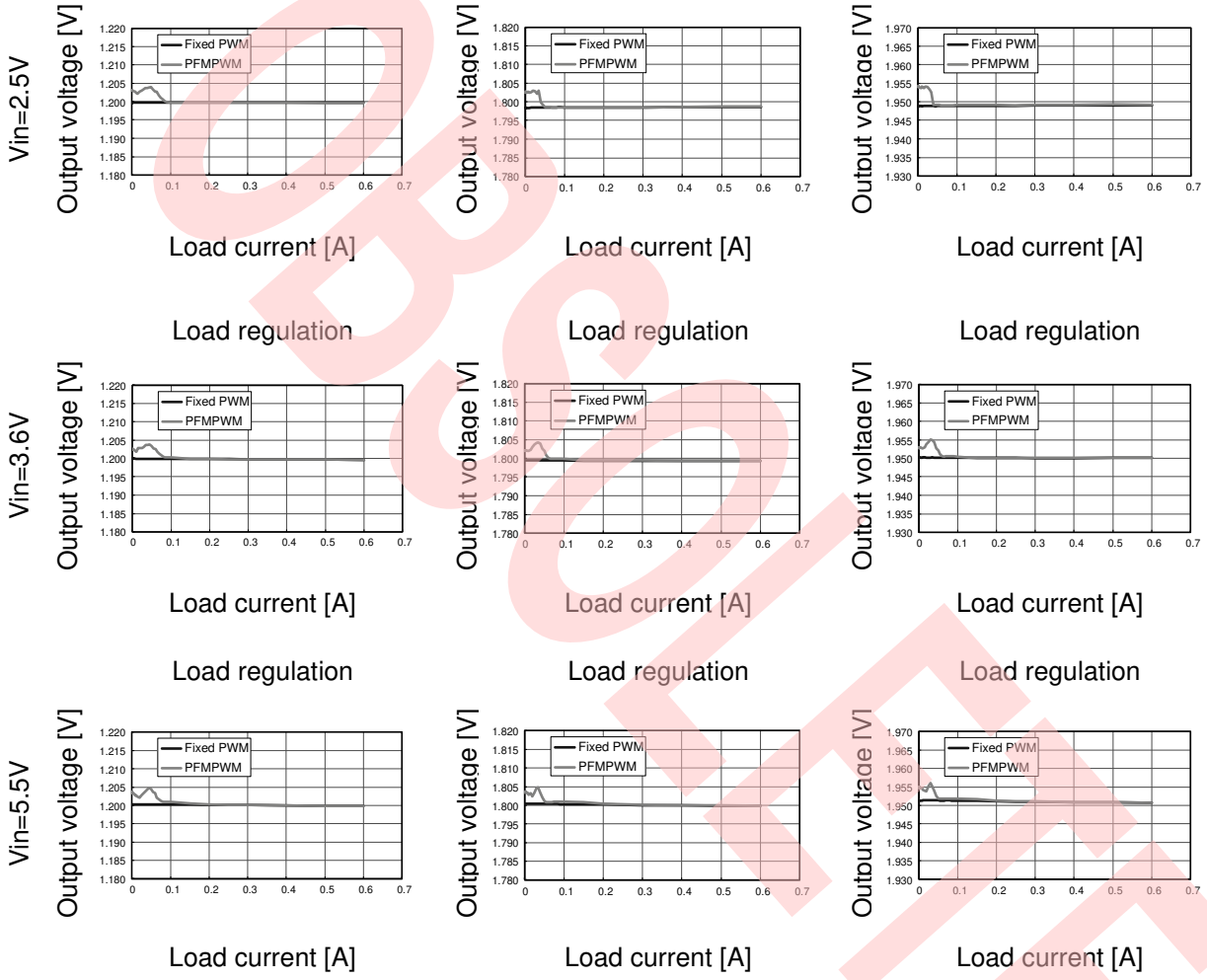
Vin=5.5V



• DD2

Vo=1.2V (Min) | Vo=1.8V | Vo=1.95V (Max)

Load regulation

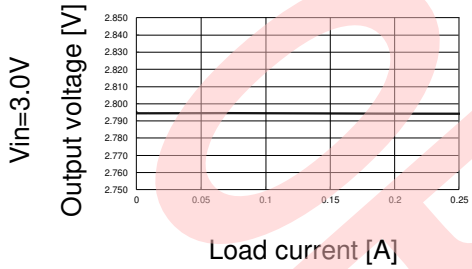


■ LDO Load Regulation Characteristics

• LDO

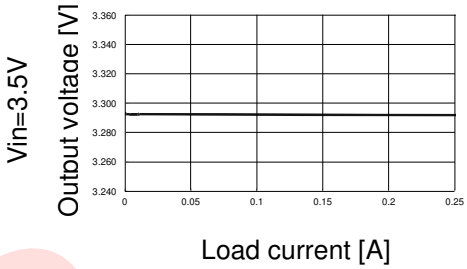
Vo=2.8V (Min)

Load regulation

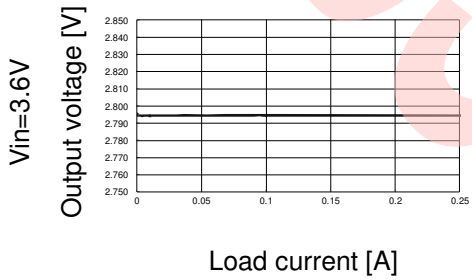


Vo=3.3V (Max)

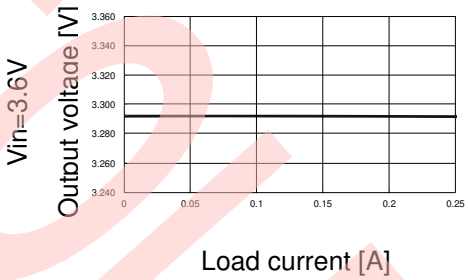
Load regulation



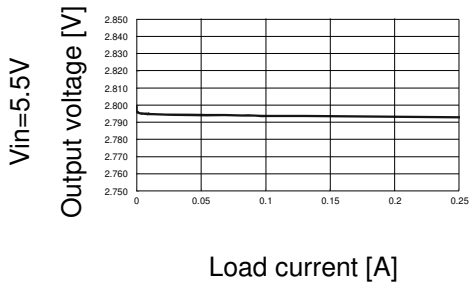
Load regulation



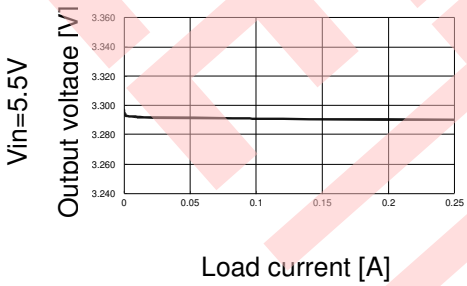
Load regulation



Load regulation



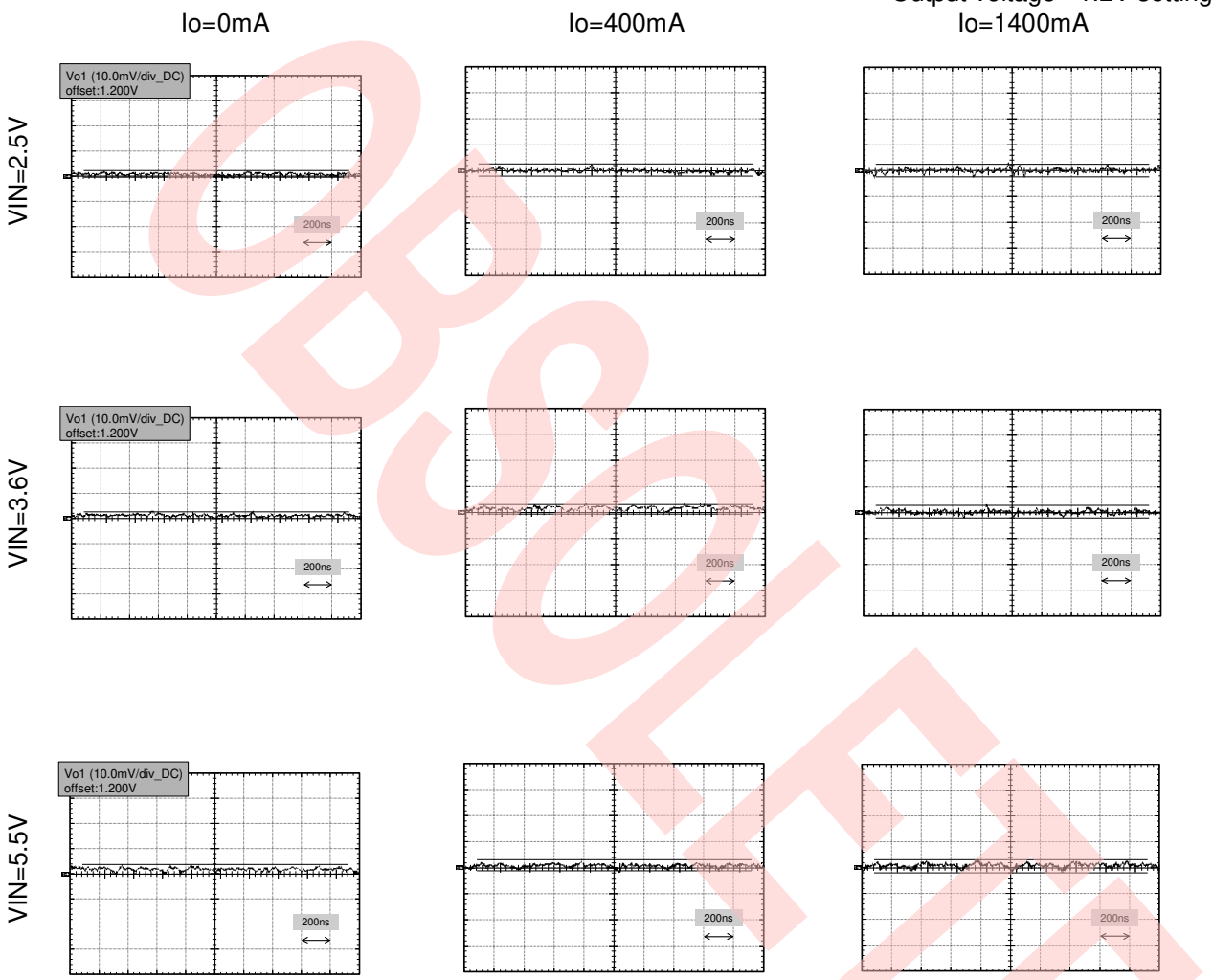
Load regulation



■ DC/DC Output Ripple Waveform

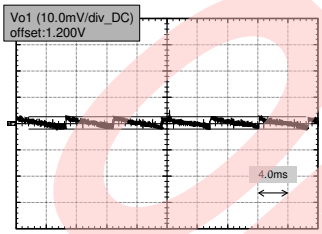
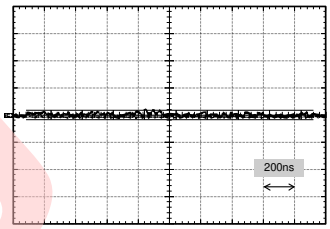
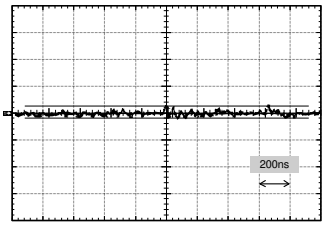
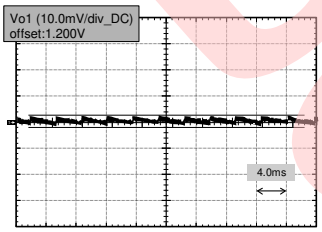
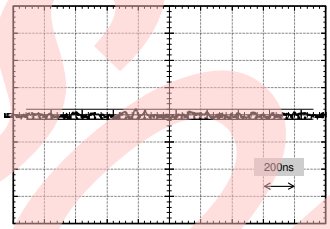
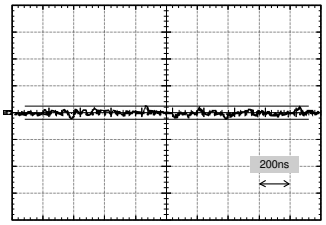
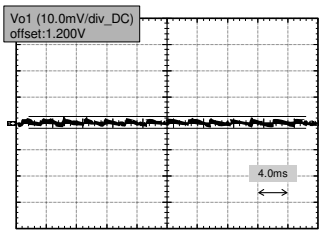
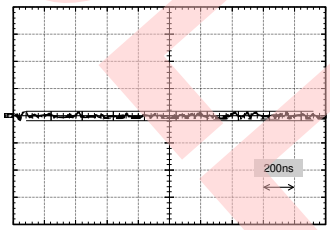
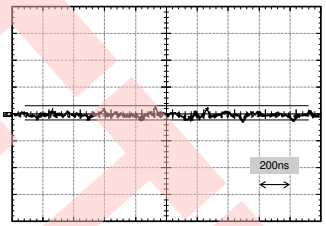
• DD1 (Fixed PWM mode)

Output voltage =1.2V setting



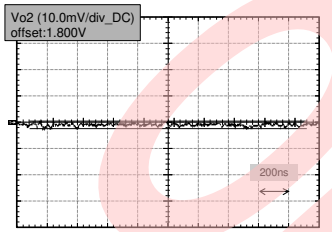
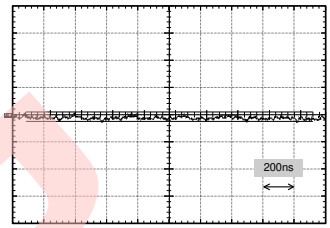
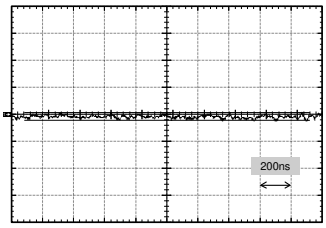
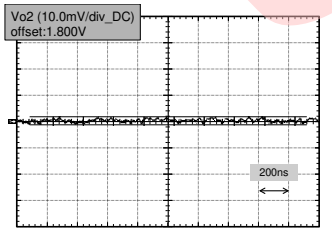
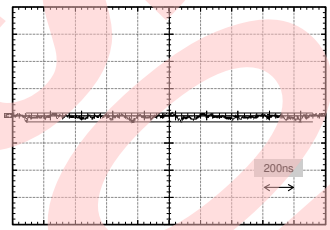
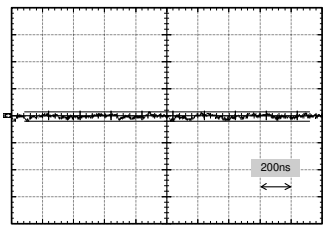
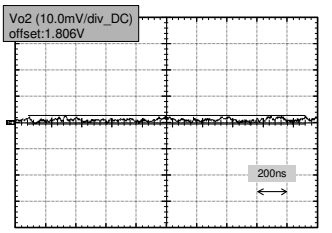
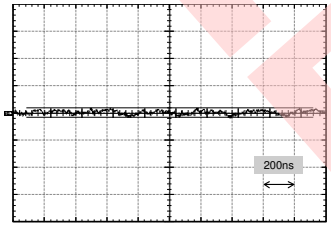
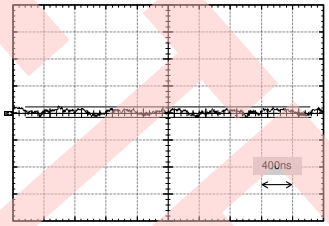
• DD1 (PFM/PWM mode)

Output voltage =1.2V setting

	Io=0mA	Io=400mA	Io=1400mA
VIN=2.5V			
VIN=3.6V			
VIN=5.5V			

• DD2 (Fixed PWM mode)

Output voltage =1.8V setting

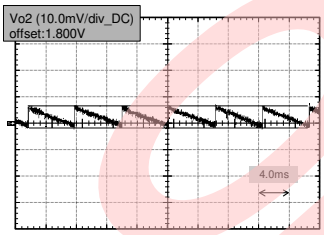
	Io=0mA	Io=400mA	Io=600mA
VIN=2.5V			
VIN=3.6V			
VIN=5.5V			

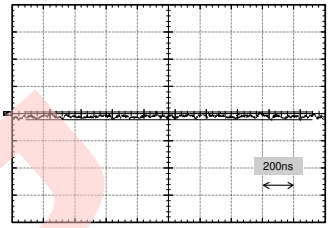
• DD2 (PFM/PWM mode)

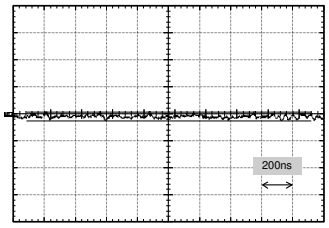
Output voltage =1.8V setting

Io=0mA | Io=400mA | Io=600mA

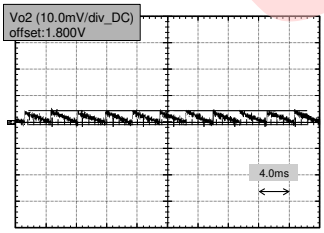
VIN=2.5V

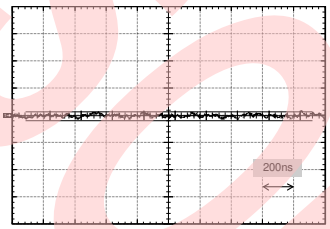


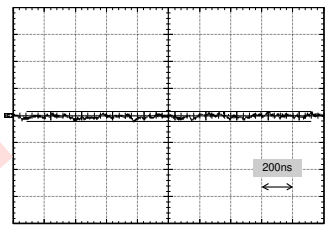




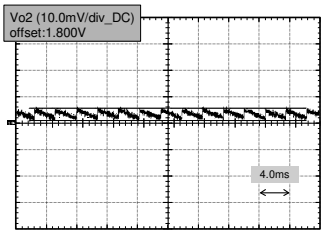
VIN=3.6V

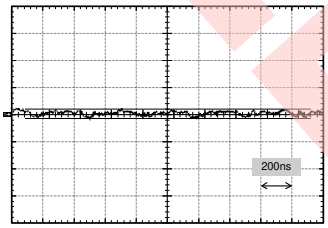


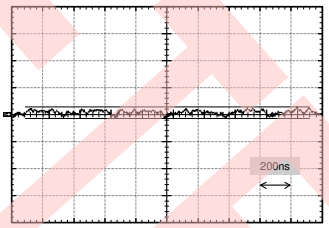




VIN=5.5V





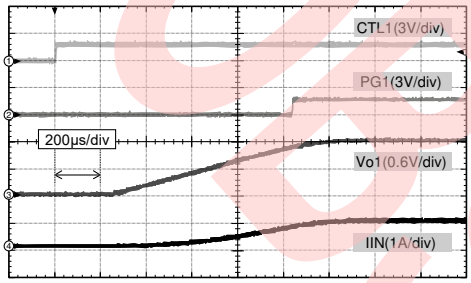


■ **DD1 Startup/shutdown Waveform**

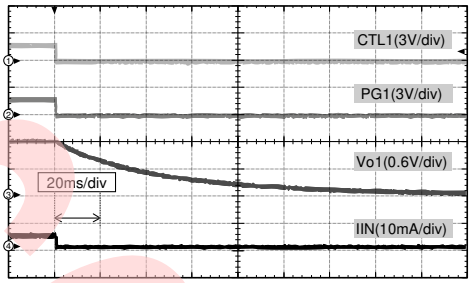
Output voltage =1.2V setting
Soft-start setting=0.9ms
Fixed PWM mode
Control using the external pin (CTL1)

VCC = 2.5V

Io=1400mA

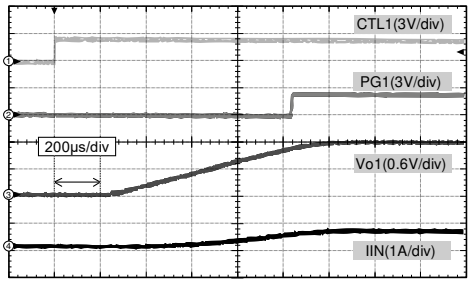


Io=0mA

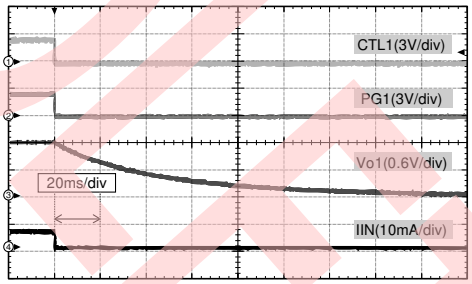


VCC = 3.6V

Io=1400mA

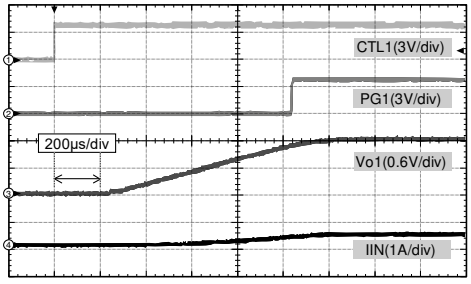


Io=0mA

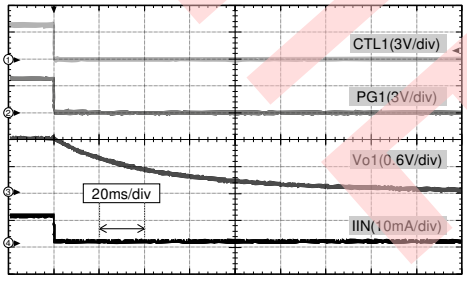


VCC = 5.5V

Io=1400mA



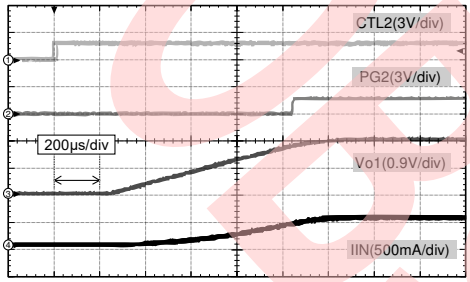
Io=0mA



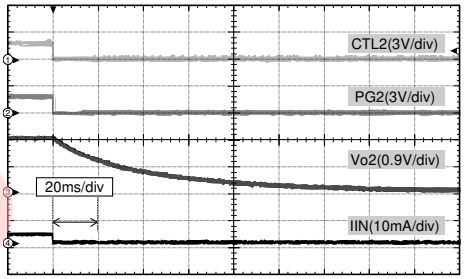
■ **DD2 Startup/shutdown Waveform**

Output voltage =1.8V setting
Soft-start setting=0.9ms
Fixed PWM mode
Control using the external pin (CTL2)

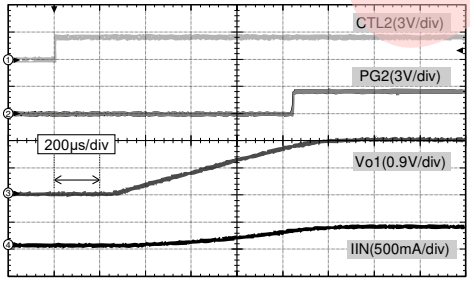
VCC = 2.5V
Io=600mA



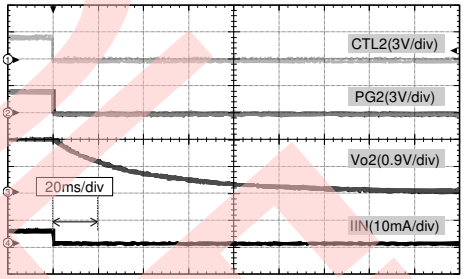
Io=0mA



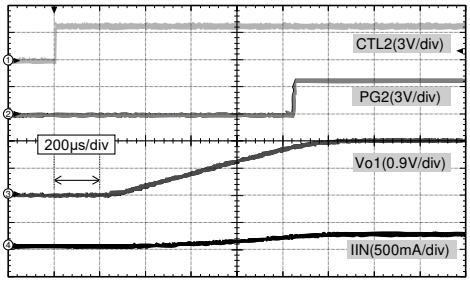
VCC = 3.6V
Io=600mA



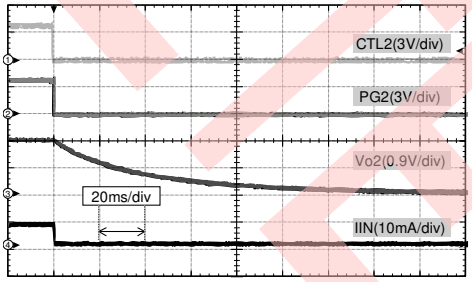
Io=0mA



VCC = 5.5V
Io=600mA



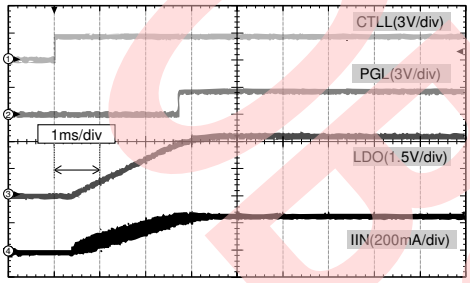
Io=0mA



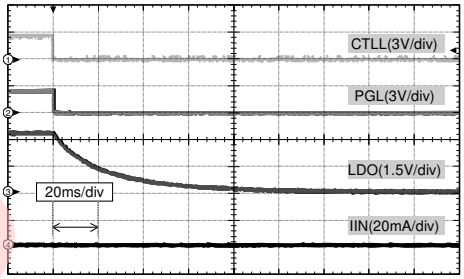
■ **LDO Startup/shutdown Waveform**

Output voltage =3.3V setting
Soft-start setting=2.7ms
Control using the external pin (CTLL)

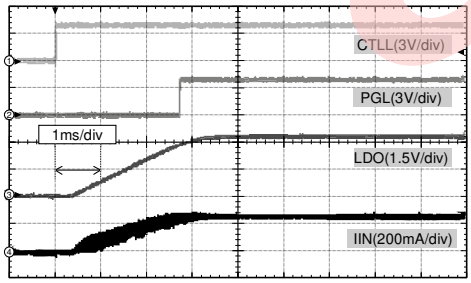
VCC = 3.6V
Io=250mA



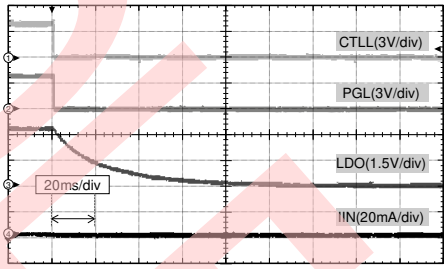
Io=0mA



VCC = 5.5V
Io=250mA



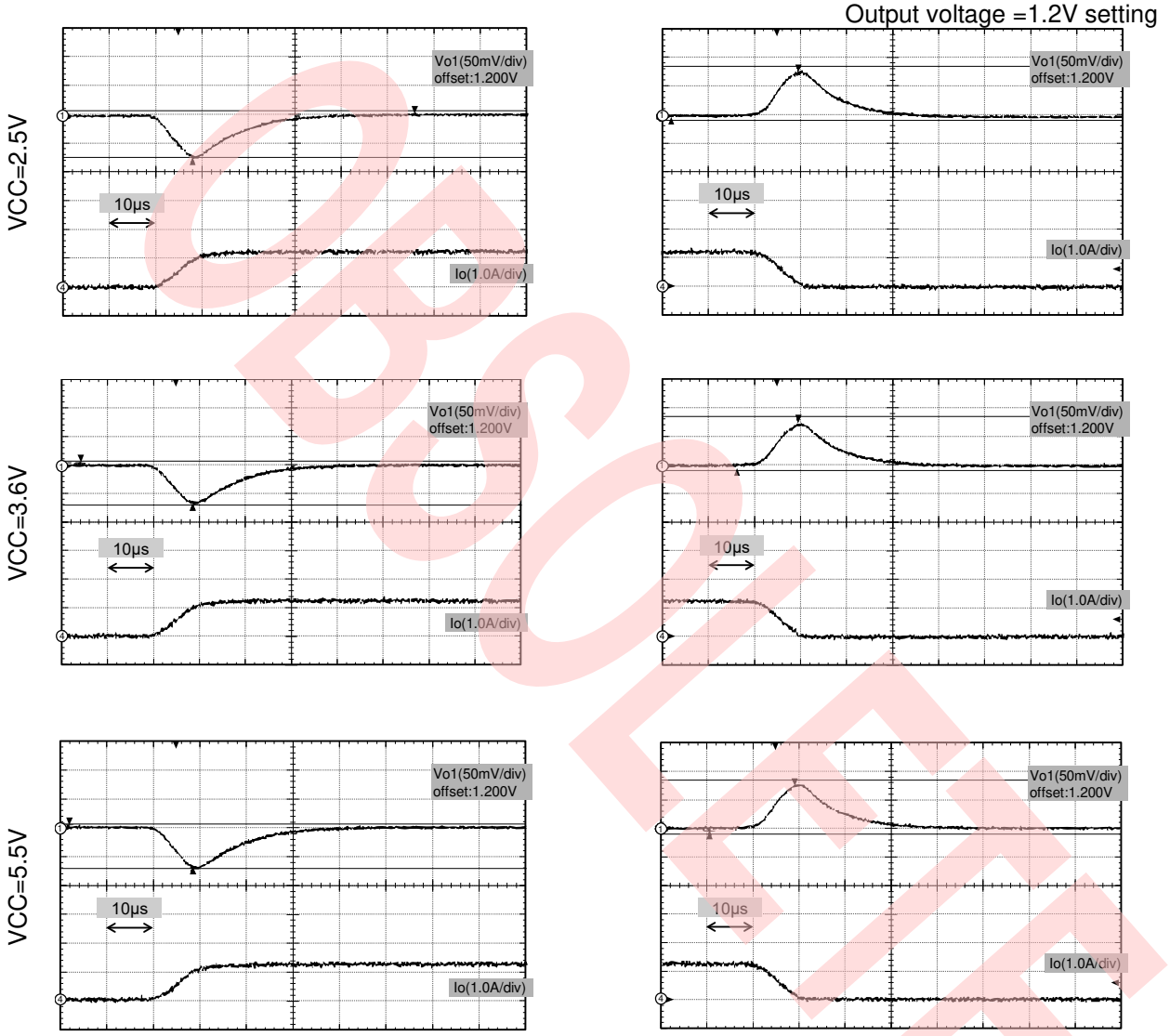
Io=0mA



■ DC/DC Sudden Load Change Characteristics

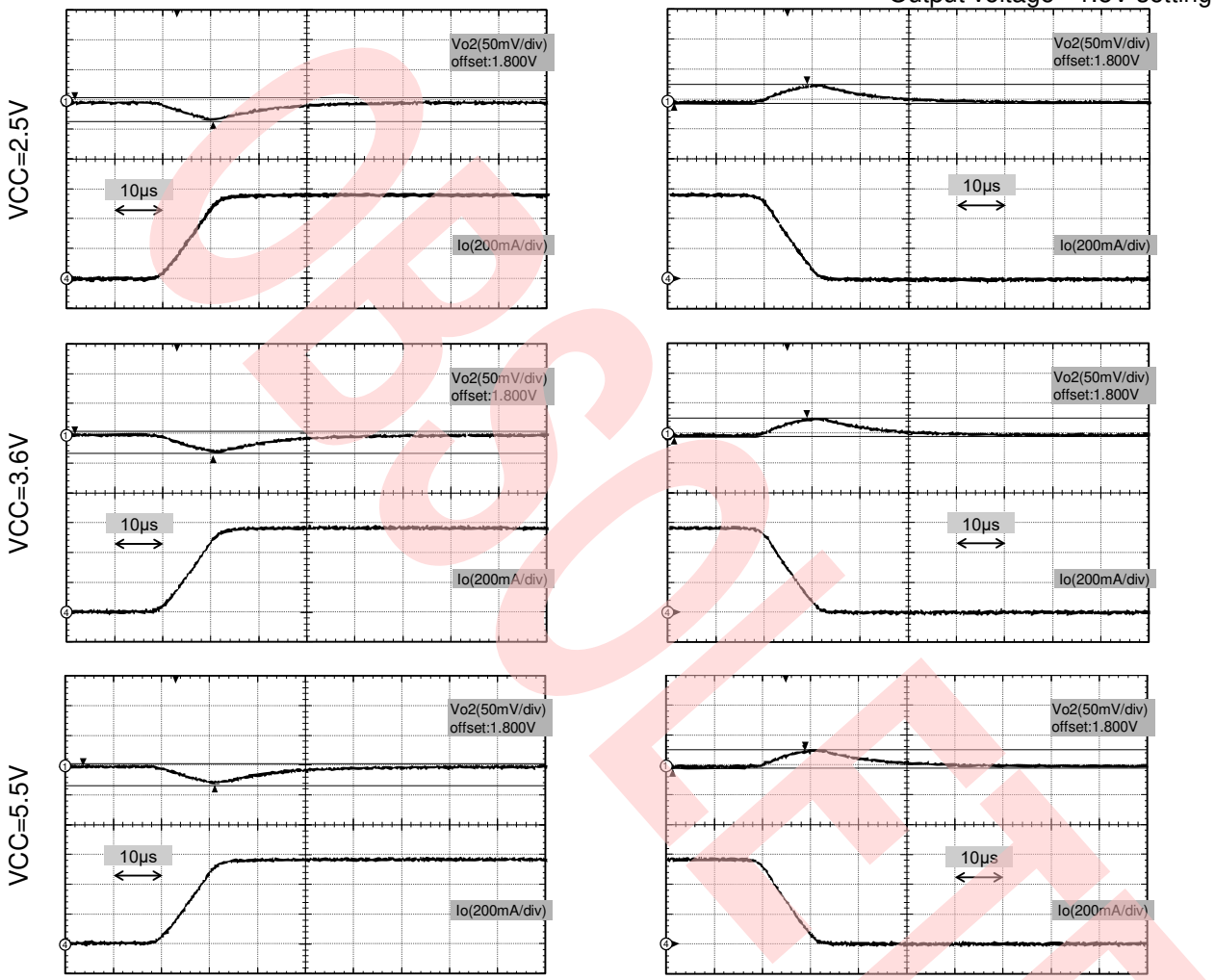
• DD1(Fixed PWM mode) 0mA↔1400mA/10µs

Output voltage =1.2V setting



• DD2 (Fixed PWM mode) 0mA↔600mA/10µs

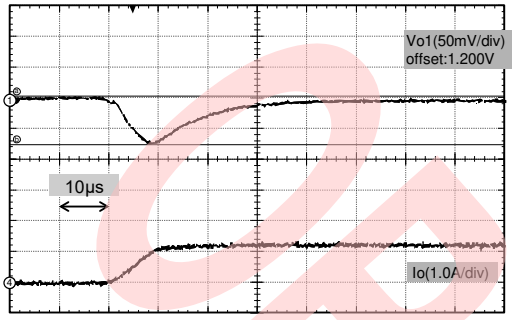
Output voltage =1.8V setting

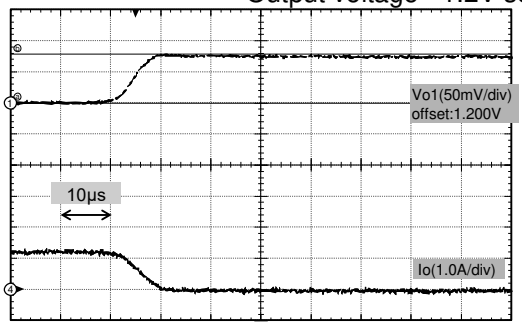


• DD1 (PFM/PWM mode) 0mA⇔1400mA/10µs

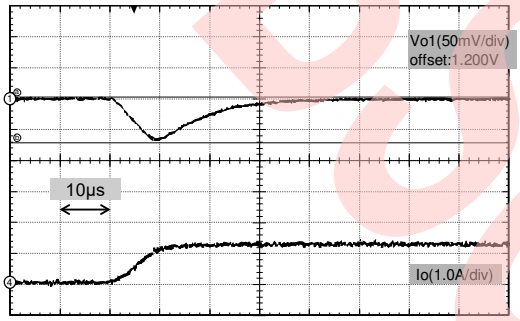
Output voltage =1.2V setting

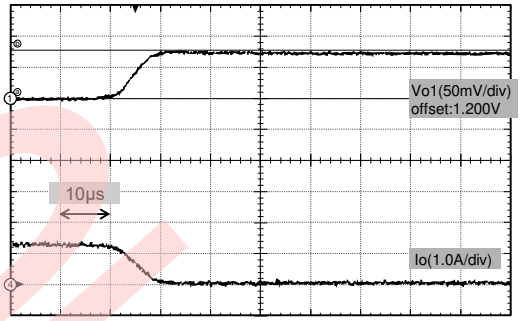
VCC=2.5V



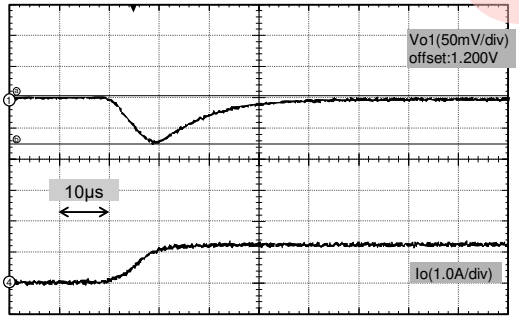


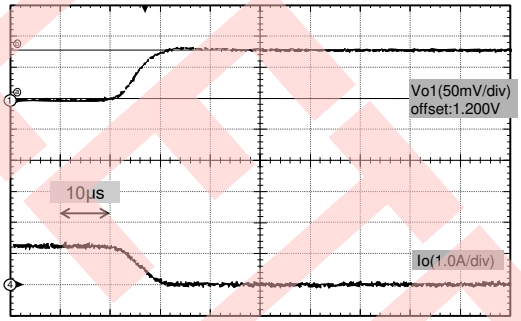
VCC=3.6V





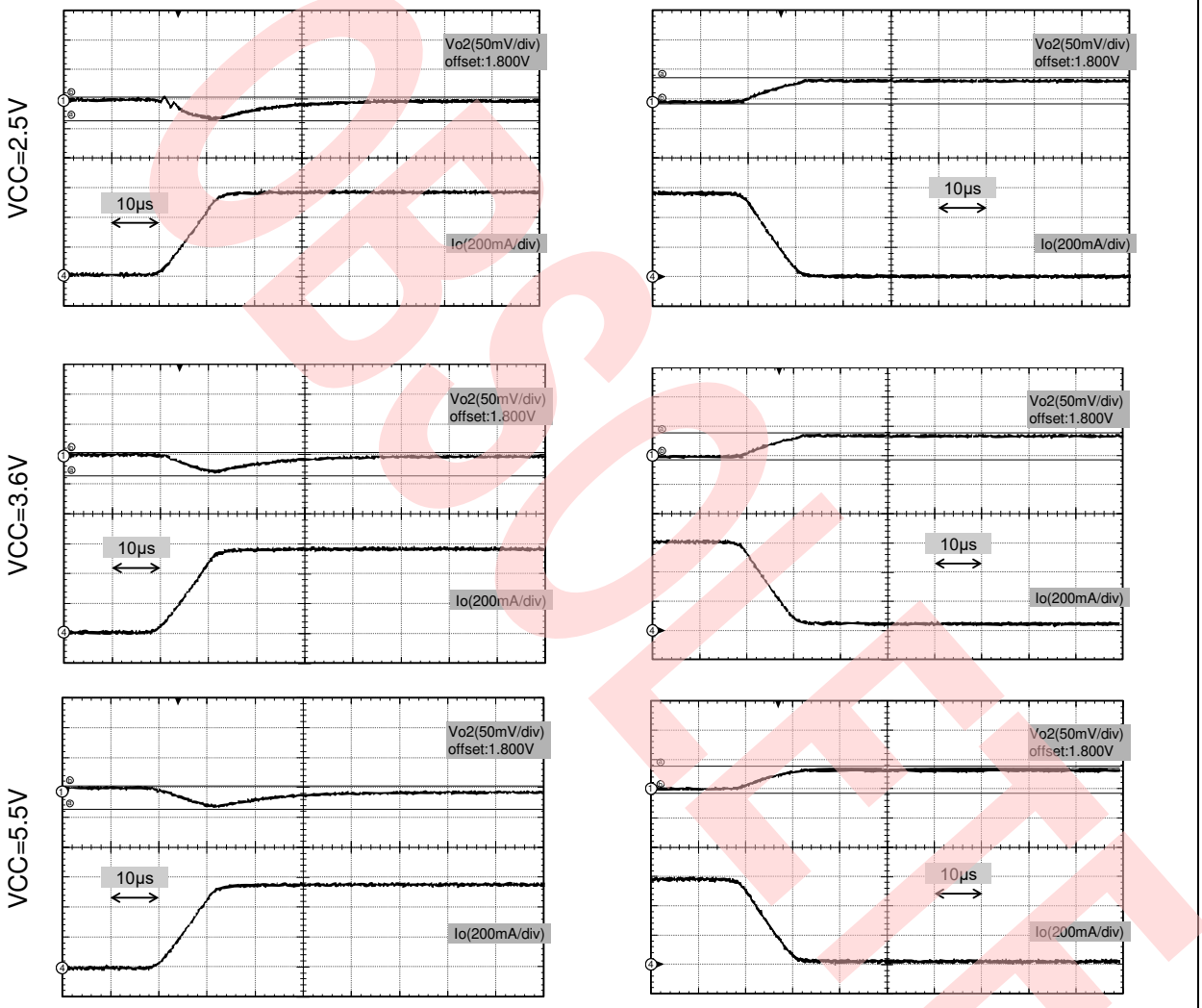
VCC=5.5V





• DD2 (PFM/PWM mode) 0mA⇔600mA/10µs

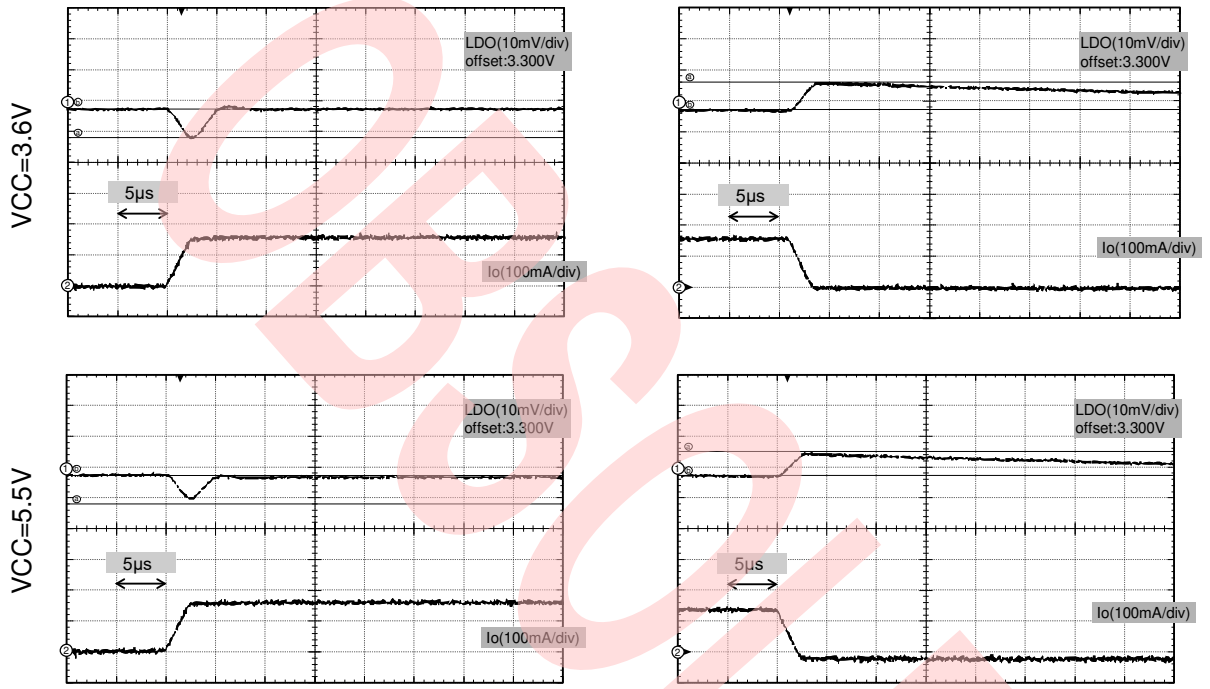
Output voltage =1.8V setting



■ LDO Sudden Load Change Characteristics

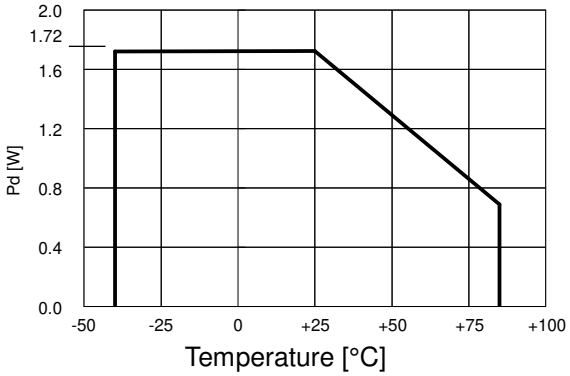
• LDO 0mA↔150mA/2µs

Output voltage = 3.3V setting



■ Power Dissipation

Power dissipation vs.
Operation ambient temperature



26. Usage Precaution

1. Do not configure the IC over the maximum ratings.

   If the IC is used over the maximum ratings, the LSI may be permanently damaged.

   It is preferable for the device to be normally operated within the recommended usage conditions. Usage outside of these conditions can have a bad effect on the reliability of the LSI.

2. Use the devices within recommended operating conditions.

   The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device.
   All of the device's electrical characteristics are warranted when the device is operated within these ranges.
   Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.
   No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

3. Printed circuit board ground lines should be set up with consideration for common impedance.

4. Take appropriate measures against static electricity.

- Containers for semiconductor materials should have anti-static protection or be made of conductive material.
- After mounting, printed circuit boards should be stored and shipped in conductive bags or containers.
- Work platforms, tools, and instruments should be properly grounded.
- Working personnel should be grounded with resistance of 250 kΩ to 1 MΩ in series between body and ground.

5. Do not apply negative voltages.

   The use of negative voltages below -0.3 V may cause the parasitic transistor to be activated on LSI lines, which can cause malfunctions.

6. When all channels are operating, the reliability level is designed under the condition that the average ambient temperature Ta=+60°C, the typical input voltage, the typical output voltage and the typical output current condition are used.

27. Ordering Information

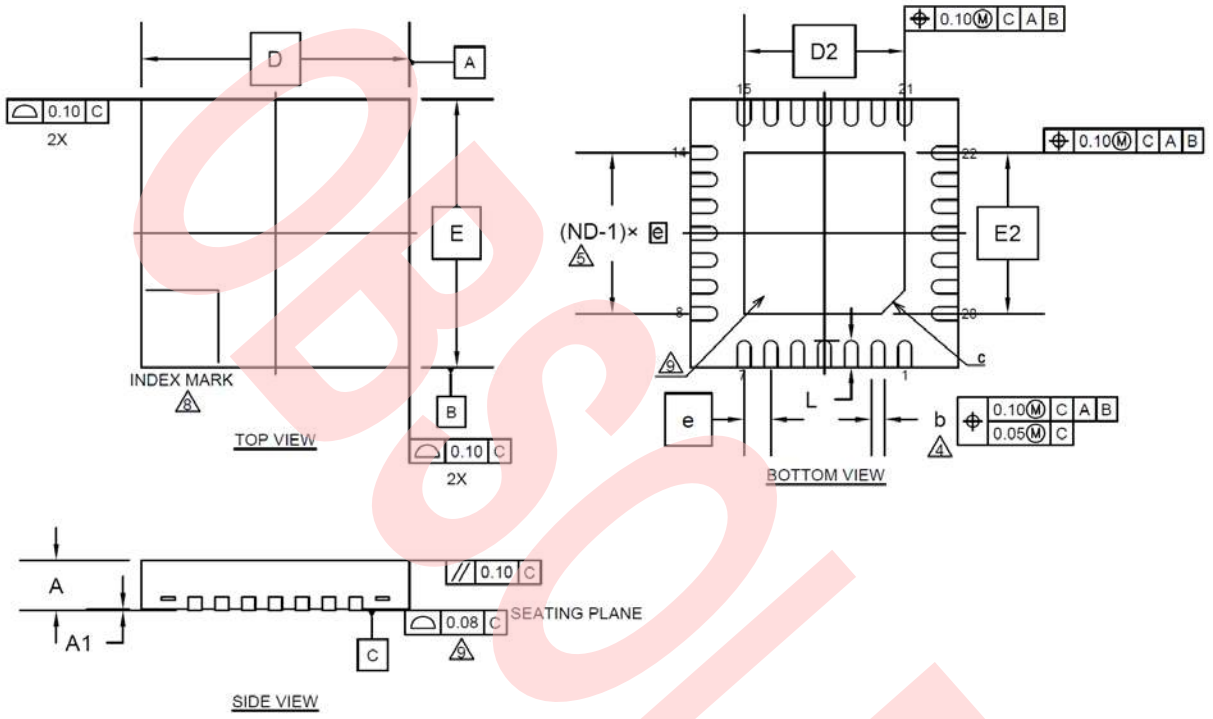
Part Number	Package	Remarks
CY39C31WQN	28-pin plastic QFN (WNO028)	–

28. Preset Code (CY39C031)

Preset Code	DD1 Output Voltage Preset Code Value	DD2 Output Voltage Preset Code Value	LDO Output Voltage Preset Code Value
111	1.00 V	1.20 V	2.85 V
112	1.00 V	1.20 V	3.30 V
121	1.00 V	1.35 V	2.85 V
122	1.00 V	1.35 V	3.30 V
131	1.00 V	1.50 V	2.85 V
132	1.00 V	1.50 V	3.30 V
141	1.00 V	1.80 V	2.85 V
142	1.00 V	1.80 V	3.30 V
211	1.10 V	1.20 V	2.85 V
212	1.10 V	1.20 V	3.30 V
221	1.10 V	1.35 V	2.85 V
222	1.10 V	1.35 V	3.30 V
231	1.10 V	1.50 V	2.85 V
232	1.10 V	1.50 V	3.30 V
241	1.10 V	1.80 V	2.85 V
242	1.10 V	1.80 V	3.30 V
311	1.20 V	1.20 V	2.85 V
312	1.20 V	1.20 V	3.30 V
321	1.20 V	1.35 V	2.85 V
322	1.20 V	1.35 V	3.30 V
331	1.20 V	1.50 V	2.85 V
332	1.20 V	1.50 V	3.30 V
341	1.20 V	1.80 V	2.85 V
342	1.20 V	1.80 V	3.30 V
411	1.30 V	1.20 V	2.85 V
412	1.30 V	1.20 V	3.30 V
421	1.30 V	1.35 V	2.85 V
422	1.30 V	1.35 V	3.30 V
431	1.30 V	1.50 V	2.85 V
432	1.30 V	1.50 V	3.30 V
441	1.30 V	1.80 V	2.85 V
442	1.30 V	1.80 V	3.30 V

29. Package Dimensions

Package Code: WNO028



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	0.80
A_1	0.00	—	0.05
D		4.00 BSC	
E		4.00 BSC	
b	0.15	0.20	0.25
D_2		2.40 BSC	
E_2		2.40 BSC	
e		0.40 BSC	
c		0.35 REF	
L	0.35	0.40	0.45

NOTE

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCINC CONFORMS TO ASME Y14.5-1994.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP.IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL. THE DIMENSION "b"SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
5. ND REFER TO THE NUMBER OF TERMINALS ON D OR E SIDE.
6. MAX. PACKAGE WARPAGE IS 0.05mm.
7. MAXIMUM ALLOWABLE BURRS IS 0.076mm IN ALL DIRECTIONS.
8. PIN #1 ID ON TOP WILL BE LOCATED WITHIN INDICATED ZONE.
9. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
10. JEDEC SPECIFICATION NO. REF : N/A

002-15159 Rev. **

Document History

Document Title: CY39C031 2ch Buck DC/DC Converter + 1ch LDO with I²C Interface and SW FET
Document Number: 002-08407

Revision	ECN	Submission Date	Description of Change
**	–	11/20/2013	Migrated to Cypress and assigned document number 002-08407. No change to document contents or format.
*A	5132453	03/08/2016	Updated to Cypress template
*B	5734750	05/18/2017	Updated Pin Assignment: Change the package name from LCC-28P-M70 to WNO028 Updated Ordering Information: Change the package name from LCC-28P-M70 to WNO028 Deleted “EV Board Ordering Information” Deleted “Marking Format (Lead Free Version)” Deleted “Labeling Sample (Lead Free Version)” Deleted “MB39C031 Recommended Conditions Of Moisture Sensitivity Level” Updated Package Dimensions: Updated to Cypress format
*C	6531769	04/05/2019	Changed part number to CY39C031
*D	7674486	02/16/2022	Obsoleted

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