2-Bit I2C-Bus and SMBus Low Power I/O Port with Interrupt and Reset

Features

- Operation power supply voltage from 2.3V to 5.5V
- 2-bit I²C-bus GPIO with interrupt and reset
- 5V tolerant I/Os
- Active Low interrupt output
- Active Low reset input
- Polarity inversion register
- Low current consumption
- 0Hz to 1MHz clock frequency
- Noise filter on SCL/SDA inputs
- Power-on reset
- ESD protection (4KV HBM and 1KV CDM)
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- Package offered :UQFN 1.6x1.6-8

Description

The PI4IOE5V9521 provides 2 bits of General Purpose parallel Input/Output (GPIO) expansion for I²C-bus/ SMBus applications. It includes the features such as higher driving capability, 5V tolerance, lower power supply, individual I/O configuration, and smaller packaging. It provides a simple solution when additional I/O is needed for ACPI power switches, sensors, push buttons, LEDs, fans, etc.

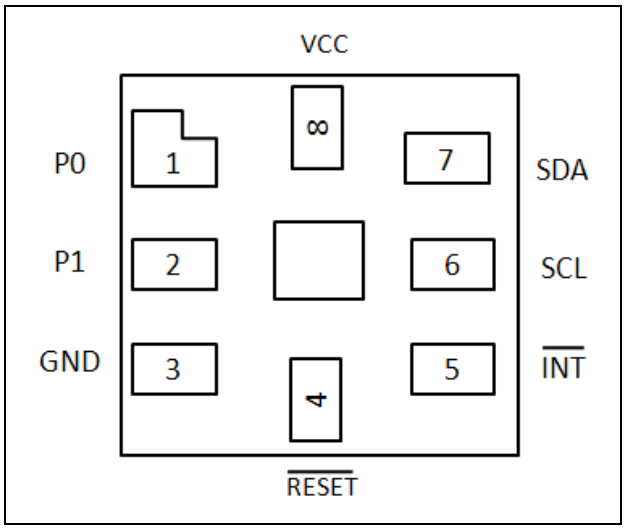
The PI4IOE5V9521 consists of a 2-bit configuration register to configure the I/Os as either inputs or outputs, and a 2-bit polarity register to change the polarity of the input port register data. The data for each input or output is kept in the corresponding Input port or Output port register. All registers can be read by the system master.

The PI4IOE5V9521 open-drain interrupt output ($\overline{\text{INT}}$) is activated when any input state is differed from its corresponding Input Port register and is used to indicate the system master that an input state has changed.

The power-on reset sets the registers to their default values and initializes the device state machine. The Reset pin ($\overline{\text{Reset}}$) causes the same reset/initialization to occur without de-powering the device.

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Pin Configuration



Pin Description

Pin	Name	Type	Description
1	P0	I/O	Input/Output 0
2	P1	I/O	Input/Output 1
3	GND	G	Supply ground
4	$\overline{\text{RESET}}$	I	Reset pin
5	$\overline{\text{INT}}$	O	Interrupt output (open-drain)
6	SCL	I	Serial clock line
7	SDA	I/O	Serial data line
8	VCC	P	Power supply

* I = Input; O = Output; P = Power; G = Ground

Maximum Ratings

Power supply	-0.5V to +6.0V
Voltage on an I/O pin	GND-0.5V to +6.0V
Input current	±20mA
Output current on an I/O pin	±50mA
Supply current	40mA
Ground supply current	50mA
Total power dissipation	200mW
Operation temperature	-40~85℃
Storage temperature	-65~150℃
Maximum Junction temperature ,T j(max)	125℃

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Static Characteristics

VCC = 2.3 V to 5.5 V; GND = 0 V; Tamb = -40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Power Supply						
VCC	Supply voltage		2.3	-	5.5	V
I_{CC}	Supply current	Operating mode; VCC = 5.5 V; no load; fSCL= 100 kHz	-	104	175	µA
I_{stb}	Standby current	Standby mode; VCC = 5.5 V; no load; VI = GND; fSCL= 0 kHz; I/O = inputs	-	0.25	1	µA
		Standby mode; VCC = 5.5 V; no load; VI = VCC; fSCL= 0 kHz; I/O = inputs		0.25	1	µA
V_{POR}	Power-on reset voltage[1]		-	1.16	1.41	V
Input SCL, Input/Output SDA						
V_{IL}	Low level input voltage		-0.5	-	+0.3VCC	V
V_{IH}	High level input voltage		0.7VCC	-	5.5	V
I_{OL}	Low level output current	V_{OL}=0.4V	20	-	-	mA
I_L	Leakage current	V_I = VCC = GND	-1	-	1	µA
C_i	Input capacitance	V_I = GND	-	5	10	pF
I/Os						
V_{IL}	Low level input voltage		-0.5	-	+0.81	V
V_{IH}	High level input voltage		+1.8	-	5.5	V
I_{OL}	Low level output current	VCC = 2.3 V; V_{OL} = 0.5 V[2]	8	10	-	mA
		VCC = 2.3 V; V_{OL} = 0.7 V[2]	10	13	-	mA
		VCC = 3.0 V; V_{OL} = 0.5 V[2]	8	14	-	mA
		VCC = 3.0 V; V_{OL} = 0.7 V[2]	10	19	-	mA
		VCC = 4.5 V; V_{OL} = 0.5 V[2]	8	17	-	mA
		VCC = 4.5 V; V_{OL} = 0.7 V[2]	10	24	-	mA

Static Characteristics Cont.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I/Os						
V_{OH}	High level output voltage	I_{OH} = -8mA; VCC = 2.3V[3]	1.8	-	-	V
		I_{OH} = -10mA; VCC = 2.3V[3]	1.7	-	-	V
		I_{OH} = -8mA; VCC = 3.0V[3]	2.6	-	-	V
		I_{OH} = -10mA; VCC = 3.0V[3]	2.5	-	-	V
		I_{OH} = -8mA; VCC = 4.75V[3]	4.1	-	-	V
		I_{OH} = -10mA; VCC = 4.75V[3]	4.0	-	-	V
I_L	Input leakage current	VCC = 3.6V; V_I = VCC = GND	-1	-	1	µA
C_i	Input capacitance		-	3.7	10	pF
Interrupt $\overline{\text{INT}}$						
I_{OL}	Low level output current	V_{OL} = 0.4V	3	13	-	mA
I_{OH}	High level output current	V_{OL} = 0.4V	-1		+1	uA
Reset $\overline{\text{RESET}}$						
V_{IL}	Low level input voltage		-0.5	-	+0.81	V
V_{IH}	High level input voltage		+1.8	-	5.5	V
I_L	Input leakage current	V_I = VCC = GND	-1		1	µA

Note:
[1]: VCC must be lowered to 0.2 V for at least 5 us in order to reset part.
[2]: Each I/O must be externally limited to a maximum of 25 mA and the device must be limited to a maximum current of 50 mA.
[3]: The total current sourced by all I/Os must be limited to 40 mA.

Dynamic Characteristics

Symbol	Parameter	Conditions	Standard mode I^2C		Fast mode I^2C		Fast mode Plus I^2C		Unit
			Min	Max	Min	Max	Min	Max	
f_{SCL}	SCL clock frequency		0	100	0	400	0	1000	kHz
t_{BUF}	Bus free time between a STOP and START condition		4.7	-	1.3	-	0.5	-	µs
$t_{HD;STA}$	Hold time (repeated) START condition		4.0	-	0.6	-	0.26	-	µs
$t_{SU;STA}$	Set-up time for a repeated START condition		4.7	-	0.6	-	0.26	-	µs
$t_{SU;STO}$	Set-up time for STOP condition		4.0	-	0.6	-	0.26	-	µs
$t_{VD;ACK}$[1]	Data valid acknowledge time		-	3.45	-	0.9	-	0.45	µs
$t_{HD;DAT}$[2]	Data hold time		0	-	0	-	0	-	ns
$t_{VD;DAT}$	Data valid time		-	3.45	-	0.9	-	0.45	us
$t_{SU;DAT}$	Data set-up time		250	-	100	-	50	-	ns
t_{LOW}	LOW period of the SCL clock		4.7	-	1.3	-	0.5	-	µs
t_{HIGH}	HIGH period of the SCL clock		4.0	-	0.6	-	0.26	-	µs
t_f	Fall time of both SDA and SCL signals		-	300	-	300	-	120	ns
t_r	Rise time of both SDA and SCL signals		-	1000	-	300	-	120	ns
t_{SP}	Pulse width of spikes that must be suppressed by the input filter		-	50	-	50		50	ns
Port Timing									
$t_{v(Q)}$	Data output valid time[3]		-	200	-	200	-	200	ns
$t_{su(D)}$	Data input set-up time		100	-	100	-	100	-	ns
$t_{h(D)}$	Data input hold time		1	-	1	-	1	-	µs
Interrupt Timing									
$t_{v(INT)}$	Valid time on pin $\overline{INT}$		-	4	-	4	-	4	µs
$t_{rst(INT)}$	Reset time on pin $\overline{INT}$		-	4	-	4	-	4	µs
Reset Timing									
$t_{w(rst)}$	Reset pulse width		25	-	25	-	25	-	ns
$t_{rec(rst)}$	Reset recovery time[4]		0	-	0	-	0	-	ns
t_{rst}	Reset time		1	-	1	-	1	-	us

Note:
[1]: $t_{VD;ACK}$ = time for acknowledgement signal from SCL LOW to SDA (out) LOW.
[2]: $t_{VD;DAT}$ = minimum time for SDA data out to be valid following SCL LOW.
[3]: $t_{v(Q)}$measured from 0.7VCC on SCL to 50% I/O output.
[4]: To reset the device while actively communicating on the bus may cause glitches or errant STOP conditions. Upon reset, the full delay will be the sum of t_{rst} and RC time constant of SDA bus.

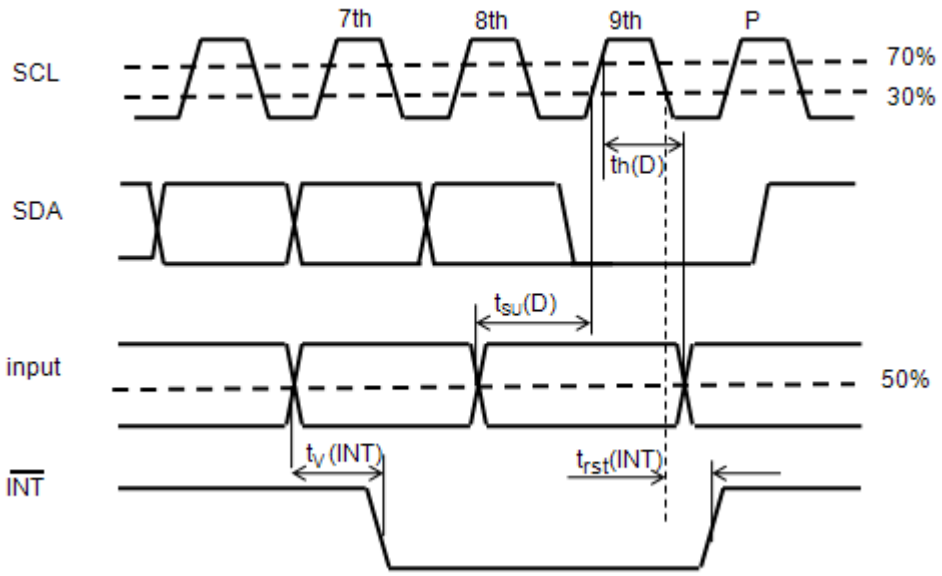
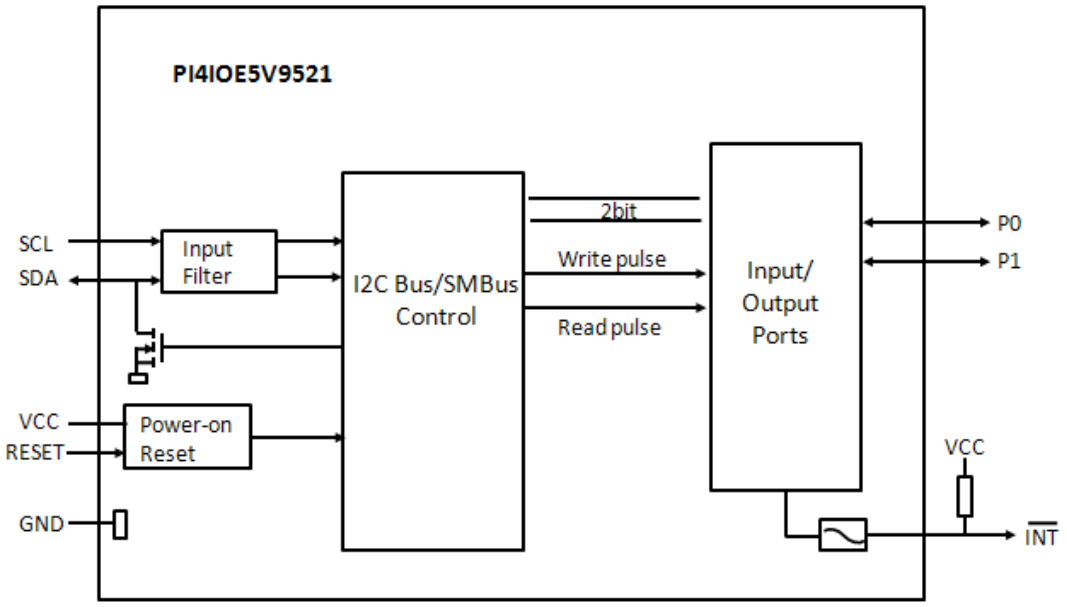


Figure 1: Timing Diagram for INT Timing and Port Timing

Block Diagram



Note: All I/Os are set to inputs at reset.

Details Description

a. Device Address

Table 1: Device address

	b7(MSB)	b6	b5	b4	b3	b2	b1	b0
Address Byte	1	0	0	1	0	0	1	R/W

Note: Read "1", Write "0"

b. Registers

i. Command Byte

The command byte is the first byte to follow the address byte during a write transmission. It is used as a pointer to determine which of the following registers will be written or read.

Table 2: Command byte

Command	Register
0	Input port register
1	Output port register
2	Polarity inversion register
3	Configuration register

ii. Register 0 : Input Port Register

This register is a read-only port. It reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by Register 2. Writes to this register have no effect.
The default value 'X' is determined by the externally applied logic level.

Table 3: Register 0 – Description of Input Port register bit

Bit	7	6	5	4	3	2	1	0
Symbol	I7	I6	I5	I4	I3	I2	I1	I0
Default	1	1	1	1	1	1	X	X

iii. Register 1 : Output Port Register

This register is an output-only port. It reflects the outgoing logic levels of the pins defined as outputs by Registers 3. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, not the actual pin value.

Table 4: Register 1 – Description of Output Port register bit

Bit	7	6	5	4	3	2	1	0
Symbol	O7	O6	O5	O4	O3	O2	O1	O0
Default	1	1	1	1	1	1	1	1

iv. Register 2 : Polarity Inversion Register

This register allows the user to invert the polarity of the Input port register data. If a bit in this register is set (written with '1'), the Input port data polarity is inverted. If a bit in this register is cleared (written with a '0'), the Input port data polarity is retained.

Table 5: Register 2 – Description of Polarity Inversion register bit

Bit	7	6	5	4	3	2	1	0
Symbol	N7	N6	N5	N4	N3	N2	N1	N0
Default	0	0	0	0	0	0	0	0

v. Register 3 : Configuration Register

This register configures the directions of the I/O pins. If a bit in this register is set (written with '1'), the corresponding port pin is enabled as an input with high-impedance output driver. If a bit in this register is cleared (written with '0'), the corresponding port pin is enabled as an output. At reset, the IOs are configured as inputs.

Table 6: Register 3 – Description of Configuration register bit

Bit	7	6	5	4	3	2	1	0
Symbol	C7	C6	C5	C4	C3	C2	C1	C0
Default	1	1	1	1	1	1	1	1

c. Power-on Reset

When power is applied to VCC, an internal power-on reset holds the PI4IOE5V9521 in a reset condition until VCC has reached VPOR. At that point, the reset condition is released and the PI4IOE5V9521 registers and SMBus state machine will initialize to their default states. Thereafter, VCC must be lowered below 0.2 V to reset the device. For a power reset cycle, VCC must be lowered below 0.2 V and then restored to the operating voltage.

d. Interrupt Output ($\overline{\text{INT}}$)

The open-drain interrupt output ($\overline{\text{INT}}$) is activated when one of the port pins changes state and the pin is configured as an input. The interrupt is de-activated when the input returns to its previous state or the Input Port register is read.
Note that changing an I/O from an output to an input may cause a false interrupt to occur if the state of the pin does not match the contents of the input Port register.

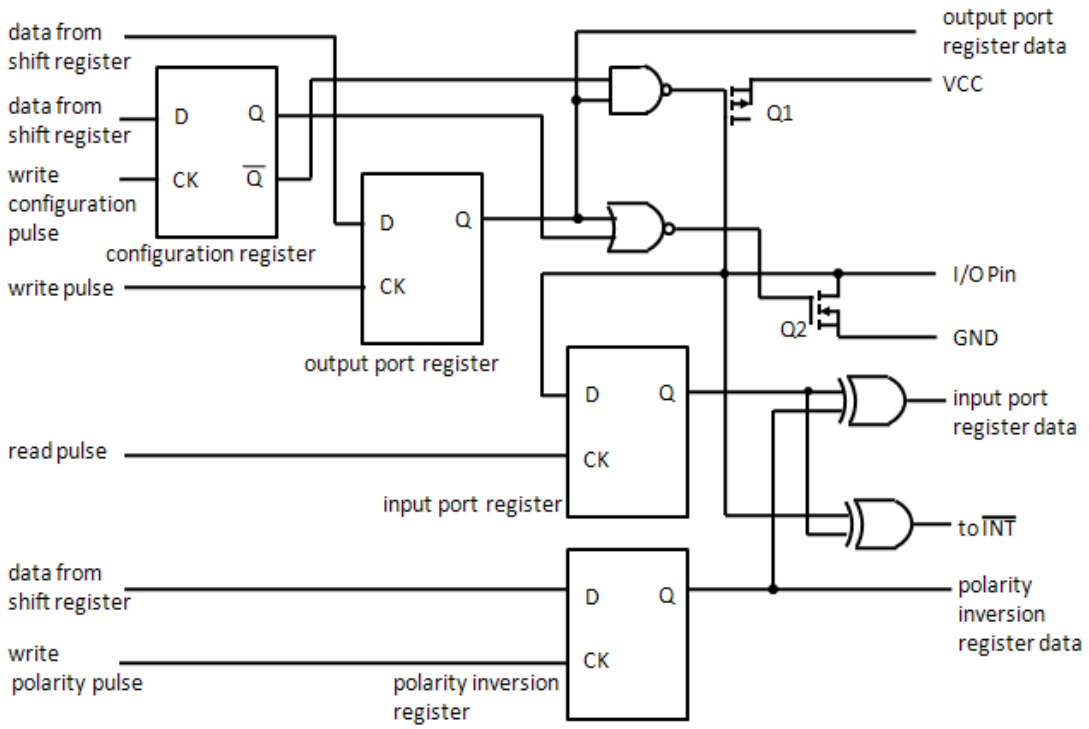
e. $\overline{\text{RESET}}$ Input

A reset can be accomplished by holding the $\overline{\text{RESET}}$ pin LOW for a minimum of tw(rst). The PI4IOE5V9521 registers and I2C-bus state machine will be held in their default state until the $\overline{\text{RESET}}$ input is once again HIGH.

f. I/O Port

When an I/O is configured as an input, FETs Q1 and Q2 are off, creating a high-impedance input. The input voltage may be raised above VCC to a maximum of 5.5 V.
If the I/O is configured as an output, then either Q1 or Q2 is on, depending on the state of the Output Port register. Care should be exercised if an external voltage is applied to an I/O configured as an output because of the low-impedance path that exists between the pin and either VCC or GND.

Figure 2: Simplified schematic of I/Os



After power-on reset, all registers return to default values.

g. Bus Transaction

Data is transmitted to the PI4IOE5V9521 using the Write mode as shown in Figure 5 and Figure 6. Data is read from the PI4IOE5V9521 using the read mode as shown in Figure 7 and Figure 8. These devices do not implement an auto-increment function, so once a command byte has been sent, the register which was addressed will continue to be accessed by reads until a new command byte has been sent.

Figure 3: Write to Output Port register

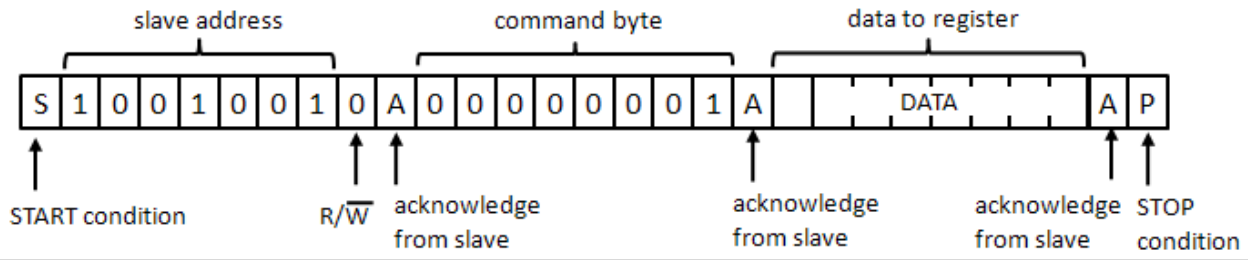


Figure 4: Write to Configuration register or Polarity Inversion register

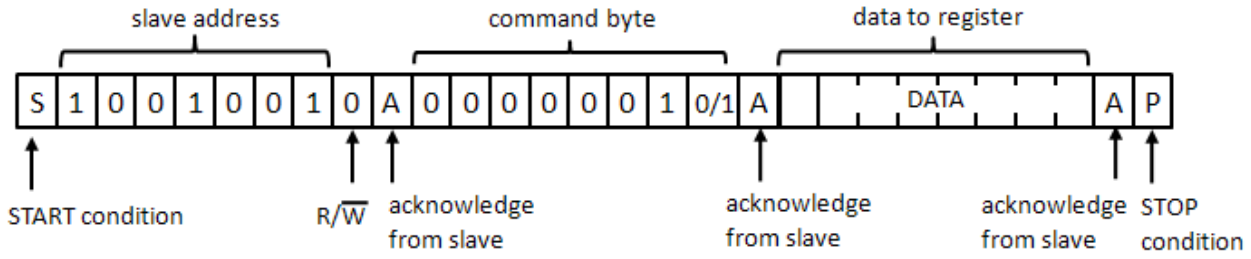
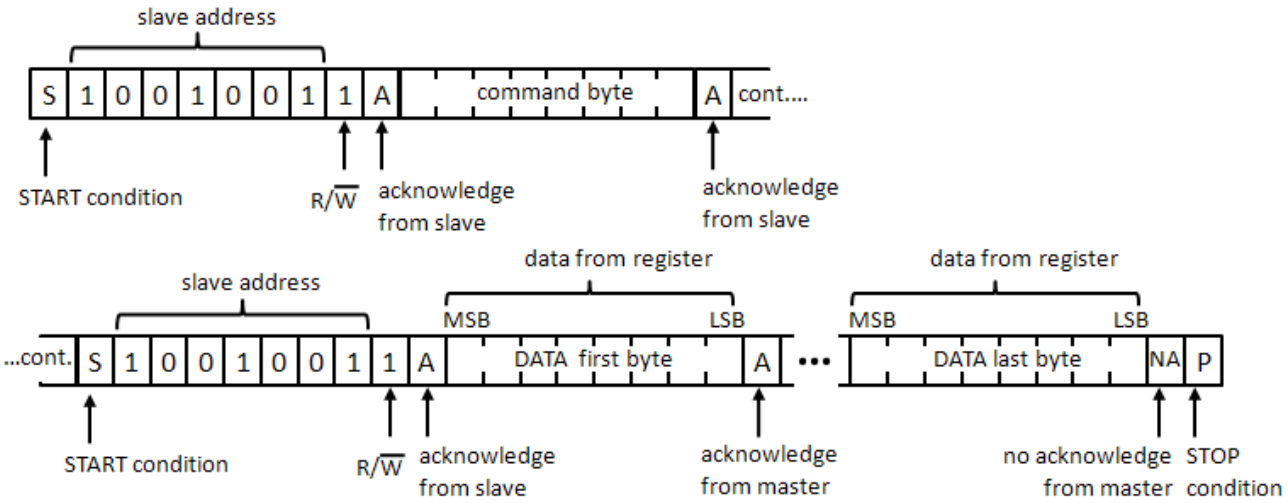
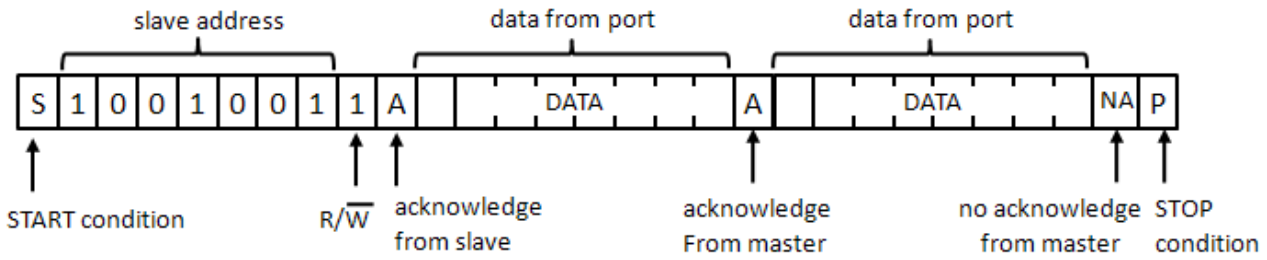


Figure 5: Read from register



Note: Transfer can be stopped at any time by a STOP condition.

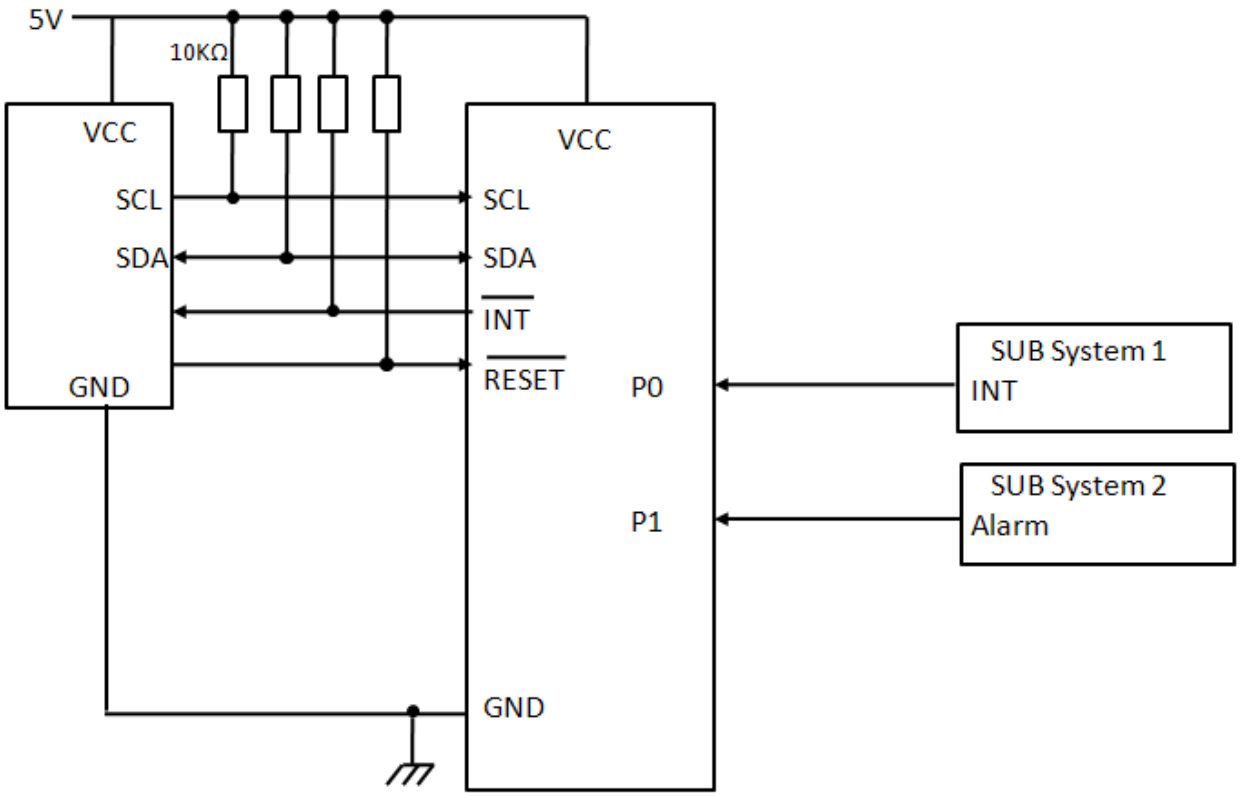
Figure 6: Read Input port register



Note: Transfer of data can be stopped at any moment by a STOP condition. It is assumed that the command byte has previously been set to '00' (read Input Port register).

Application Design-in Information

Figure 7: Typical application



Minimizing ICC when the I/Os are used to control LEDS

When the I/Os are used to control LEDs, they are normally connected to VCC through a resistor as shown in Figure 10. Since the LED acts as a diode, when the LED is off the I/O VI is about 1.2 V less than VCC. The supply current, ICC, increases as VI becomes lower than VCC.

Designs need minimize current consumption, such as battery power applications, should consider maintaining the I/O pins greater than or equal to VCC when the LED is off. Figure 10 shows a high value resistor in parallel with the LED. Figure 11 shows VCC less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O VI at or above VCC and prevent additional supply current consumption when the LED is off.

Figure 8: High value resistor in parallel with the LED

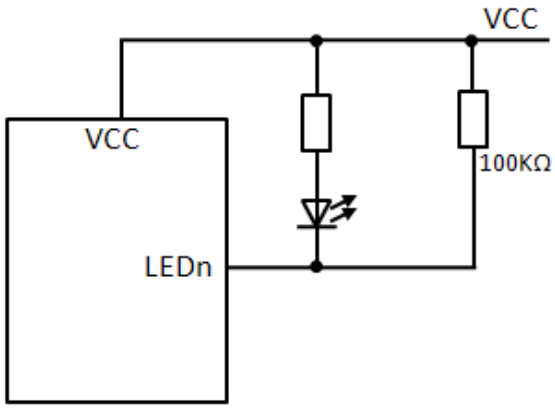
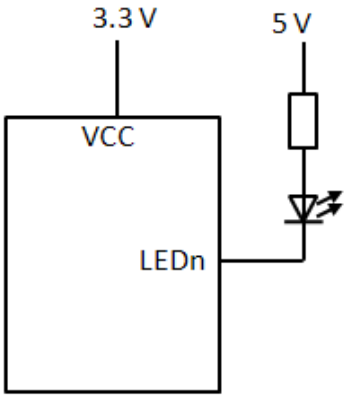
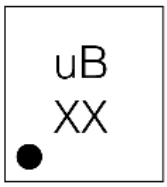


Figure 9: Device supplied by a lower voltage



Part Marking

XT Package

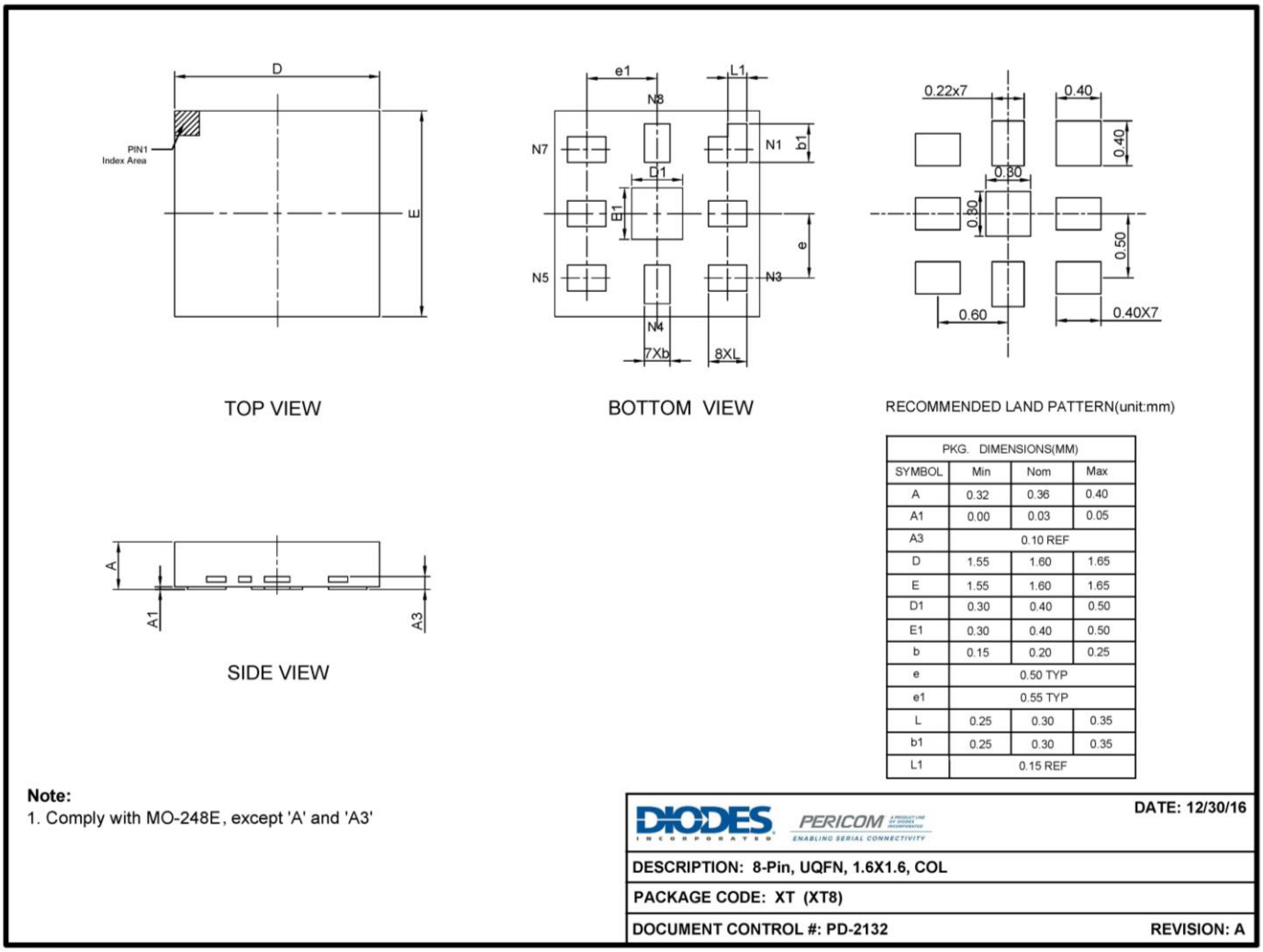


uB: Marking ID for
PI4IOE5V9521XTE

XX: Date Code (Year & Workweek)

Packaging Mechanical

8-UQFN (XT)



PKG. DIMENSIONS(MM)			
SYMBOL	Min	Nom	Max
A	0.32	0.36	0.40
A1	0.00	0.03	0.05
A3		0.10 REF	
D	1.55	1.60	1.65
E	1.55	1.60	1.65
D1	0.30	0.40	0.50
E1	0.30	0.40	0.50
b	0.15	0.20	0.25
e		0.50 TYP	
e1		0.55 TYP	
L	0.25	0.30	0.35
b1	0.25	0.30	0.35
L1		0.15 REF	

Note:
1. Comply with MO-248E, except 'A' and 'A3'

DATE: 12/30/16

DESCRIPTION: 8-Pin, UQFN, 1.6X1.6, COL

PACKAGE CODE: XT (XT8)

DOCUMENT CONTROL #: PD-2132 REVISION: A

16-0286

For latest package info.
please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

Ordering Information

Part No.	Package Code	Package Description
PI4IOE5V9521XTEX	XT	8-Pin, 1.6x1.6 (UQFN) COL

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. E = Pb-free and Green
5. X suffix = Tape/Reel

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