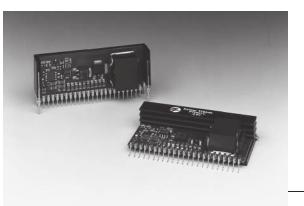
Power Trends Products from Texas Instruments

12 Watt 5V/3.3V Input Plus to Minus Voltage Converter

SLTS041A

(Revised 6/30/2000)



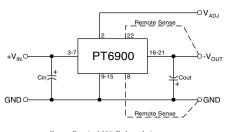
- +5V/+3.3V Input Voltage
- Negative Output
- Remote Sense
- Adjustable Output Voltage
- 23-pin SIP Package

The PT6900 is a series of high-performance ISRs, that provide plus to minus voltage conversion, up to 12 watt in a 23-pin SIP package.

The PT6900 is designed to supply regulated negative voltages for powering the latest ECL (-5.2V) and GaAs (-2.0V) ICs used in high-speed fiber optic communications. A 330µF electrolytic capacitor is required on the input and output for proper operation.

Please note that this product is not short-circuit protected.

Standard Application



 C_{in} = Required 330 μ F electrolytic C_{out} = Required 330 μ F electrolytic

Pin-Out Information

Pin	Function	Pin	Function
1	Do not connect	13	GND
2	V _{out} Adjust	14	GND
3	Vin	15	GND
4	Vin	16	V_{out}
5	Vin	17	V _{out}
6	Vin	18	V _{out}
7	V_{in}	19	V_{out}
8	Remote Sense GND	20	V_{out}
9	GND	21	V _{out}
10	GND	22	Remote Sense Vout
11	GND	23	Do not connect
12	GND		

Ordering Information

+5V Input	+3.3V Input	V _{out}
PT6901□	PT6904□	= -2.0V
PT6902□	PT6905□	= -5.2V
PT6903□		= -1.5V

PT Series Suffix (PT1234X)

Case/Pin Configuration	
Vertical Through-Hole	N
Horizontal Through-Hole	A
Horizontal Surface Mount	C

(For dimensions and PC board layout, see Package Styles 1100 and 1110.)

Specifications

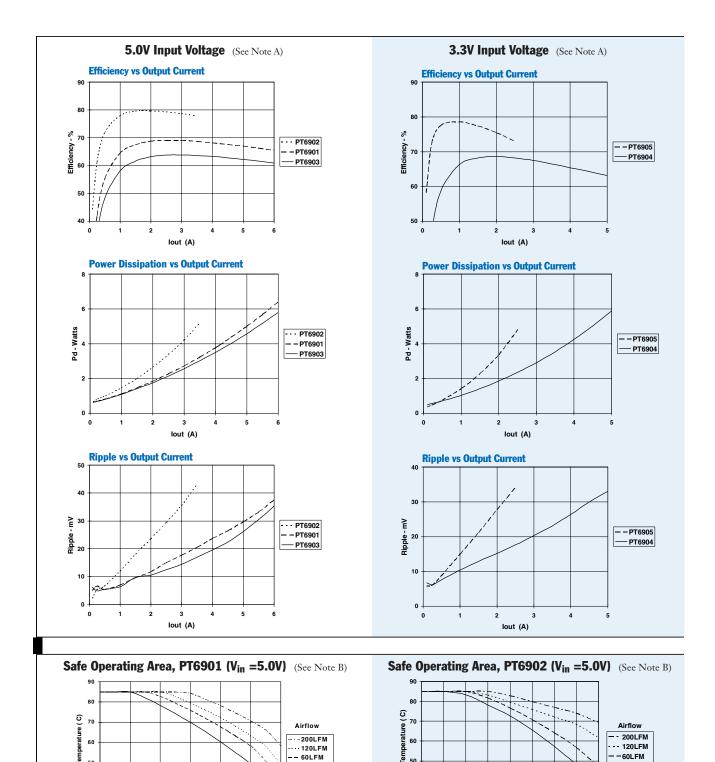
Characteristics			P				
(T _a = 25°C unless noted)	Symbols	Conditions	Min	Min Typ Max		Units	
Output Current	I_{o}	T _a = +25°C, natural con	vection				
		V _{in} =5.0V	$V_o = -2.0V / -1.5V$ $V_o = -5.2V$	0.1 (1) 0.1 (1)	_	6.0 (2) 3.5 (2)	A
		$V_{in} = 3.3 V$	$V_o = -2.0V$ $V_o = -5.2V$	0.1 (1) 0.1 (1)	_	5.0 (2) 2.5 (2)	A
Input Voltage Range		$0.1A \le I_o \le I_{max}$ PT6	901 PT6902/PT6903	4.5	_	5.5	
			PT6904/PT6905	3.1	_	3.6	V
Output Voltage Tolerance	$\Delta m V_o$	Nominal V _{in} , $I_o = I_{max}$ $0^{\circ}C \le T_a \le +60^{\circ}C$		$V_o-0.05$	_	$V_{o} + 0.05$	V
Output Adjust Range	V_{o}	Pin 14 to Vo or GND	$V_o = -2.0V$	-1.4	_	-4.4	
			$V_{o} = -5.2V$	-2.7	_	-6.5	V
			$V_{o} = -1.5V$	-1.2	_	-3.4	
Line Regulation	Regline	Over Vin range, Io =Imax		_	±0.5	±1.0	%
Load Regulation	Reg_{load}	$V_{in} = V_{nom}, 0.1 \le I_o \le I_m$	ax	_	±0.5	±1.0	%
V _o Ripple/Noise	V_n	V_{in} = V_{nom} , I_o = I_{max}	$V_o = -1.5V / -2.0V$ $V_o = -5.2V$	_	40 50	_	mV
Transient Response with C _{out} = 330μF	${ m t_{tr} \over V_{os}}$	I_o step between $0.5xI_{max}$ V_o over/undershoot	and I _{max}	_	200 200	_	μSec mV
Efficiency	η	$V_{in} = +5V, I_{o} = 0.5xI_{max}$	$V_0 = -1.5V$	_	65	_	
,	·	m / 0 max	$V_0 = -2.0V$	_	70	_	%
			$V_0 = -5.2V$	_	77	_	
		$\overline{V_{in}} = +3.3 \text{ V}, I_o = 0.5 \text{x} I_{max}$		_	67	_	%
			$V_0 = -5.2V$	_	75	_	/0
Switching Frequency	f_{0}	Over V _{in} and I _o ranges		500	_	600	kHz
Absolute Maximum Operating Temperature Range	T_a	Over V _{in} Range		0	_	+85 (2)	°C
Storage Temperature	T_s			-40	_	+125	°C
Weight	_	Vertical/Horizontal		_	28/33	_	grams

Notes: (1) ISR-will operate down to no load with reduced specifications.

(2) See SOA curves or contact the factory for the approrpiate derating.



12 Watt 5V/3.3V Input Plus to Minus Voltage Converter



Note A: All data listed in the above graphs has been developed from actual products tested at 25°C. This data is considered typical data for the DC-DC Converter. Note B: SOA curves represent operating conditions at which internal components are at or below manufacturer's maximum operating temperatures

– Nat conv



50

1.5

2.5

lout (A)

3.5

0.5

-Nat conv



Adjusting the Output Voltage of the PT6900/PT6910 Positive to Negative Converter Series

The negative output voltage of the Power Trends PT6900 Series ISRs may be adjusted higher or lower than the factory trimmed pre-set voltage with the addition of a single external resistor. Table 1 gives the allowable adjustment range for each model in the series as V_a (min) and V_a (max).

Adjust Up: An increase in the output voltage is obtained by adding a resistor R2, between pin 2 (V_o adjust) and pin 8 (Remote Sense GND).

Add a resistor (R1), between pin 2 (V_o adjust) and pin 22 (Remote Sense V_o).

Refer to Figure 1 and Table 2 for both the placement and value of the required resistor, either (R1) or R2 as appropriate.

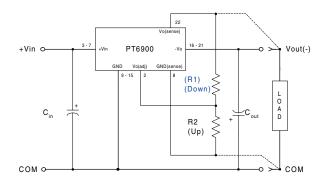
Notes:

- Only a single 1% resistor is required in either the (R1) or R2 location. Do not use (R1) and R2 simultaneously. Place the resistor as close to the ISR as possible.
- 2. Never connect capacitors from $V_{_{o}}$ adjust to either GND, $V_{_{out}}$, or the Sense pins. Any capacitance added to the $V_{_{o}}$ adjust pin will affect the stability of the ISR.
- 3. If the sense pins are not being used, the resistors (R1) and R2 can be connected to $V_{\rm out}$ and GND respectively.
- 4. An increase in the output voltage must be accompanied by a corresponding reduction in the maximum output current. The revised maximum output current must be reduced to the equivalent of 12Watts.

i.e.
$$I_{out}$$
 (max) = $\frac{12}{V_a}$ Adc,

where V_a is the adjusted output voltage.

Figure 1



The respective values of (R1) [adjust down], and R2 [adjust up], can also be calculated using the following formulas.

$$\label{eq:R1} \begin{array}{ll} \mbox{(R1)} & = & \frac{24.9 \; (\mbox{(V_a} - \mbox{V}_r)}{(\mbox{(V_o} - \mbox{V}_a)} \; - \; \mbox{R}_s \; \; \mbox{k} \Omega \\ \end{array}$$

$$R2 = \frac{24.9 \text{ V}_r}{(\text{V}_a - \text{V}_o)} - \text{R}_s$$
 kG

Where:

V_o = Original output voltage

V_a = Adjusted output voltage

V_r = Reference voltage in Table 1

 R_s = The resistance given in Table 1

Table 1

910 ADIUSIMENI									
PT6900/PT6910 ADJUSTMENT RANGE AND FORMULA PARAMETERS									
PT6903/13	PT6901/11	PT6902/12							
	PT6904/14	PT6905/15							
-1.5V	-2.0V	-5.2V							
-1.2V	-1.4V	-2.7V							
-3.4V	-4.5V	-6.5V							
-1.0V	-1.0V	-0.92V							
12.7	10.0	17.4							
	-1.5V -1.2V -3.4V -1.0V	-1.5V -2.0V -1.2V -1.4V -3.4V -4.5V -1.0V -1.0V							

Application Notes continued

PT6900/6910 Series

Table 2

Series Pt #				Series Pt #			
5.0V Bus	PT6903/13	PT6901/11	PT6902/12	5.0V Bus	PT6903/13	PT6901/11	PT6902/12
3.3V Bus	110303/13	PT6904/14	PT6905/15	3.3V Bus	110000,10	PT6904/14	PT6905/15
V _o (nom)	-1.5Vdc	-2.0Vdc	-5.2Vdc	V _o (nom)	-1.5Vdc	-2.0Vdc	-5.2Vdc
V _a (req'd)				V _a (req'd)			
-1.2	(3.9)kΩ			-3.9		3.1kΩ	(39.7) k Ω
-1.3	(24.7)kΩ			-4.0		2.5kΩ	(46.5)kΩ
-1.4	(86.9)kΩ	(6.6)kΩ		-4.1		1.9kΩ	(54.6)kΩ
-1.5		(14.9)kΩ		-4.2		1.3kΩ	(64.3)kΩ
-1.6	236.0kΩ	(27.4)kΩ		-4.3		$0.8 \mathrm{k}\Omega$	(76.1) k Ω
-1.7	112.0kΩ	(48.1)kΩ		-4.4		$0.4 \mathrm{k}\Omega$	(90.9) k Ω
-1.8	70.3kΩ	(89.6)kΩ		-4.5		$0.0 \mathrm{k}\Omega$	(106.0) k Ω
-1.9	49.6kΩ	(214.0) k Ω		-4.6			(135.0) k Ω
-2.0	37.1kΩ			-4.7			(171.0) k Ω
-2.1	28.8kΩ	239.0 k Ω		-4.8			(224.0) k Ω
-2.2	22.9kΩ	$115.0 \mathrm{k}\Omega$		-4.9			(313.0) k Ω
-2.3	18.4kΩ	73.0kΩ		-5.0			(491.0) k Ω
-2.4	15.0kΩ	52.3kΩ		-5.1			(1020.0) k Ω
-2.5	12.2kΩ	39.8kΩ		-5.2			
-2.6	9.9kΩ	31.5kΩ		-5.3			212.0kΩ
-2.7	8.1kΩ	25.6kΩ	(0.3) k Ω	_5.4			97.1kΩ
-2.8	6.5kΩ	21.1kΩ	(2.1) k Ω	_5.5			59.0kΩ
-2.9	5.1kΩ	17.7kΩ	(4.0) k Ω	-5.6			39.9kΩ
-3.0	3.9kΩ	14.9kΩ	(6.1) k Ω				28.4kΩ
-3.1	2.9kΩ	12.6kΩ	(8.5) k Ω				20.8kΩ
-3.2	2.0kΩ	10.8kΩ	(11.0) k Ω	_5.9			15.3kΩ
-3.3	1.1kΩ	9.2kΩ	(13.8) k Ω	-6.0			11.2kΩ
-3.4	0.4kΩ	$7.8 \mathrm{k}\Omega$	(16.9) k Ω	-6.1			8.1kΩ
-3.5		$6.6 \mathrm{k}\Omega$	(20.4) k Ω	-6.2			$5.5 \mathrm{k}\Omega$
-3.6		5.6kΩ	(24.3) k Ω	-6.3			3.4kΩ
-3.7		$4.7 \mathrm{k}\Omega$	(28.7) k Ω	-6.4			$1.7 \mathrm{k}\Omega$
-3.8		$3.8 \mathrm{k}\Omega$	(33.8)kΩ	-6.5			$0.2 \mathrm{k}\Omega$

R1 = (Blue)

R2 = Black



PACKAGE OPTION ADDENDUM

2-Feb-2014

PACKAGING INFORMATION

www.ti.com

Orderable Device	Status	Package Type	_	Pins	Package	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)	(6)	(3)		(4/5)	
PT6903A	OBSOLETI	SIP MODULE	EJJ	23		TBD	Call TI	Call TI			
PT6903C	OBSOLETI	SIP MODULE	EJK	23		TBD	Call TI	Call TI			
PT6903N	OBSOLETI	SIP MODULE	EJH	23		TBD	Call TI	Call TI			
PT6904A	OBSOLETI	SIP MODULE	EJJ	23		TBD	Call TI	Call TI			
PT6904C	OBSOLETI	SIP MODULE	EJK	23		TBD	Call TI	Call TI			
PT6904N	OBSOLETI	SIP MODULE	EJH	23		TBD	Call TI	Call TI			

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.



PACKAGE OPTION ADDENDUM

2-Feb-2014

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