

# FDW2511NZ

## Dual N-Channel 2.5V Specified PowerTrench® MOSFET

### Features

- 7.1A, 20V  $r_{DS(ON)} = 0.020\Omega$ ,  $V_{GS} = 4.5V$   
 $r_{DS(ON)} = 0.025\Omega$ ,  $V_{GS} = 2.5V$
- Extended  $V_{GS}$  range ( $\pm 12V$ ) for battery applications
- HBM ESD Protection Level of 3.5kV Typical (note 3)
- High performance trench technology for extremely low  $r_{DS(ON)}$
- Low profile TSSOP-8 package

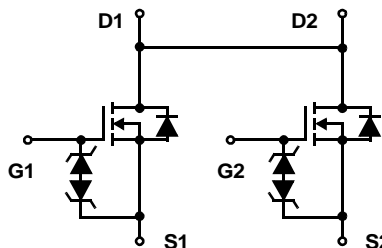
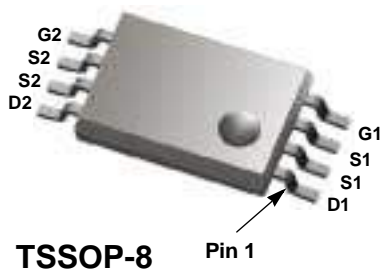
### Applications

- Load switch
- Battery charge
- Battery disconnect circuits



### General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain low gate charge for superior switching performance. These devices are well suited for portable electronics applications.



**Absolute Maximum Ratings**  $T_A=25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DSS}$	Drain to Source Voltage	20	V
$V_{GS}$	Gate to Source Voltage	$\pm 12$	V
$I_D$	Drain Current		
	Continuous ( $T_C = 25^\circ\text{C}$ , $V_{GS} = 4.5\text{V}$ , $R_{\theta JA} = 77^\circ\text{C/W}$ )	7.1	A
	Continuous ( $T_C = 100^\circ\text{C}$ , $V_{GS} = 2.5\text{V}$ , $R_{\theta JA} = 77^\circ\text{C/W}$ )	4.0	A
	Pulsed	Figure 4	A
$P_D$	Power dissipation	1.6	W
	Derate above $25^\circ\text{C}$	13	mW/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature	-55 to 150	$^\circ\text{C}$

**Thermal Characteristics**

$R_{\theta JA}$	Thermal Resistance Junction to Ambient (Note 1)	77	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient (Note 2)	114	$^\circ\text{C/W}$

**Package Marking and Ordering Information**

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
2511NZ	FDW2511NZ	TSSOP-8	13"	12 mm	2500 units

**Electrical Characteristics**  $T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
--------	-----------	-----------------	-----	-----	-----	-------

**Off Characteristics**

$B_{VDSS}$	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}$ , $V_{GS} = 0\text{V}$	20	-	-	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 16\text{V}$ $V_{GS} = 0\text{V}$	-	-	1	$\mu\text{A}$
		$T_A = 100^\circ\text{C}$	-	-	5	
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 12\text{V}$	-	-	$\pm 10$	$\mu\text{A}$
		$V_{GS} = \pm 4.5\text{V}$			$\pm 250$	nA

**On Characteristics**

$V_{GS(TH)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\mu\text{A}$	0.6	0.8	1.5	V
$r_{DS(ON)}$	Drain to Source On Resistance	$I_D = 7.1\text{A}$ , $V_{GS} = 4.5\text{V}$	-	0.015	0.020	$\Omega$
		$I_D = 6.9\text{A}$ , $V_{GS} = 4.0\text{V}$	-	0.015	0.021	$\Omega$
		$I_D = 6.5\text{A}$ , $V_{GS} = 3.1\text{V}$	-	0.016	0.024	$\Omega$
		$I_D = 6.3\text{A}$ , $V_{GS} = 2.5\text{V}$	-	0.017	0.025	$\Omega$

**Dynamic Characteristics**

$C_{ISS}$	Input Capacitance	$V_{DS} = 10\text{V}$ , $V_{GS} = 0\text{V}$ , $f = 1\text{MHz}$	-	1000	-	pF	
$C_{OSS}$	Output Capacitance		-	250	-	pF	
$C_{RSS}$	Reverse Transfer Capacitance		-	175	-	pF	
$R_G$	Gate Resistance	$V_{GS} = 0.5\text{V}$ , $f = 1\text{MHz}$	-	2.8	-	$\Omega$	
$Q_{g(TOT)}$	Total Gate Charge at 4.5V	$V_{GS} = 0\text{V}$ to 4.5V	$V_{DD} = 10\text{V}$ $I_D = 7.1\text{A}$ $I_g = 1.0\text{mA}$	-	11.5	17.3	nC
$Q_{g(2.5)}$	Total Gate Charge at 2.5V	$V_{GS} = 0\text{V}$ to 2.5V		-	7.6	11.4	nC
$Q_{gs}$	Gate to Source Gate Charge			-	1.7	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge			-	3.5	-	nC

**Switching Characteristics** ( $V_{GS} = 4.5V$ )

$t_{ON}$	Turn-On Time	$V_{DD} = 10V, I_D = 7.1A$ $V_{GS} = 4.5V, R_{GS} = 6.8\Omega$	-	-	146	ns
$t_{d(ON)}$	Turn-On Delay Time		-	13	-	ns
$t_r$	Rise Time		-	84	-	ns
$t_{d(OFF)}$	Turn-Off Delay Time		-	41	-	ns
$t_f$	Fall Time		-	55	-	ns
$t_{OFF}$	Turn-Off Time		-	-	144	ns

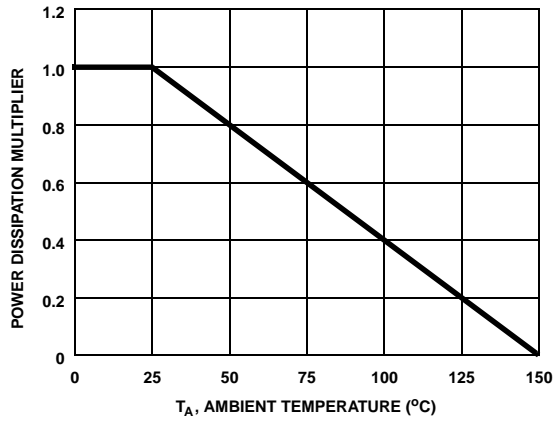
**Drain-Source Diode Characteristics**

$V_{SD}$	Source to Drain Diode Voltage	$I_{SD} = 1.3A$	-	0.7	1.2	V
$t_{rr}$	Reverse Recovery Time	$I_{SD} = 7.1A, di_{SD}/dt = 100A/\mu s$	-	-	27	ns
$Q_{RR}$	Reverse Recovered Charge	$I_{SD} = 7.1A, di_{SD}/dt = 100A/\mu s$	-	-	16	nC

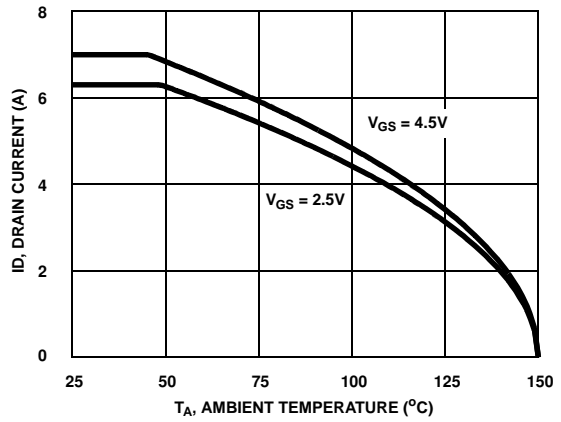
**Notes:**

- $R_{\theta JA}$  is 77 °C/W (steady state) when mounted on a 1 inch<sup>2</sup> copper pad on FR-4.
- $R_{\theta JA}$  is 114 °C/W (steady state) when mounted on a minimum copper pad on FR-4.
- The diode connected to the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

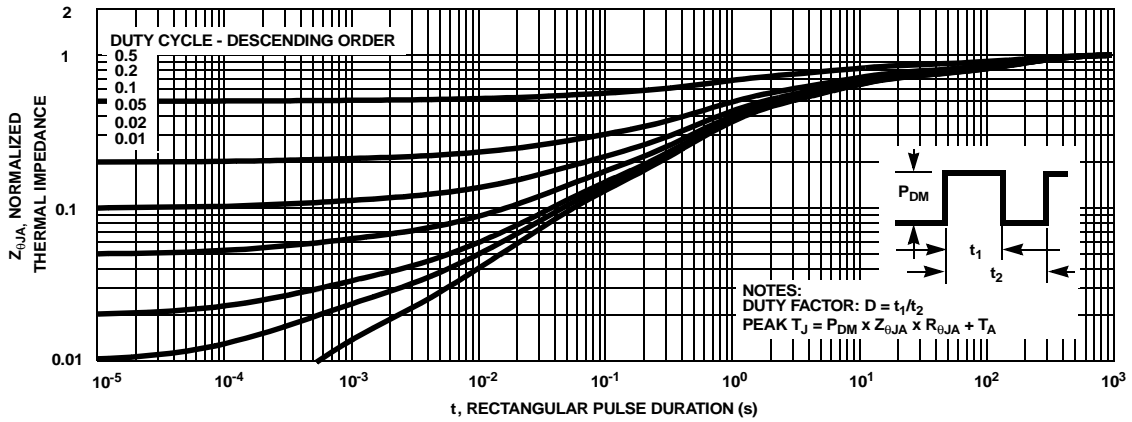
**Typical Characteristic**  $T_A = 25^\circ\text{C}$  unless otherwise noted



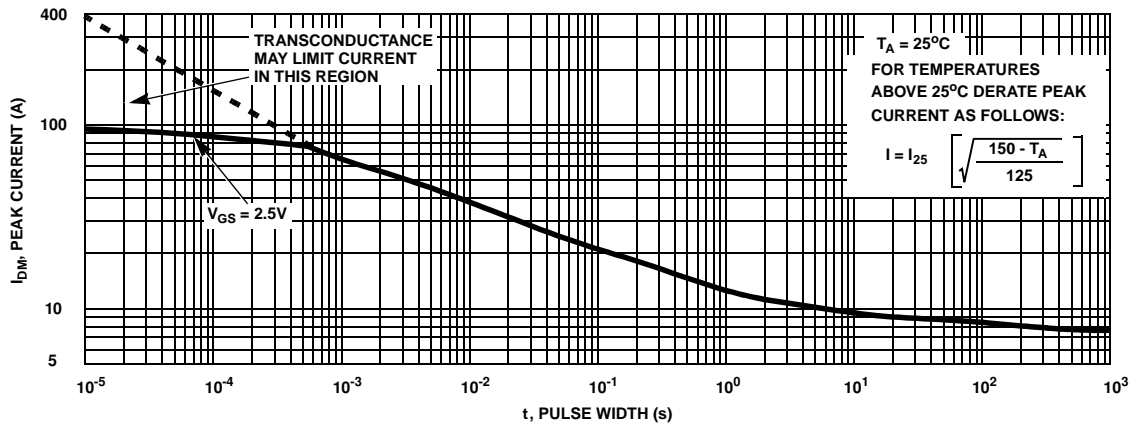
**Figure 1. Normalized Power Dissipation vs Ambient Temperature**



**Figure 2. Maximum Continuous Drain Current vs Ambient Temperature**

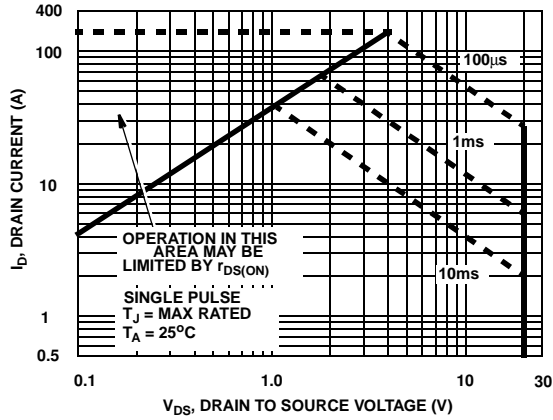


**Figure 3. Normalized Maximum Transient Thermal Impedance**

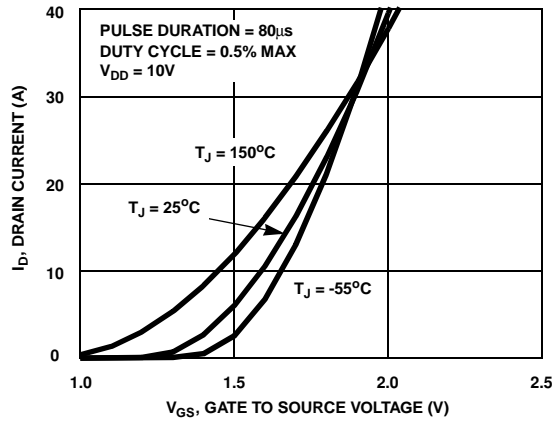


**Figure 4. Peak Current Capability**

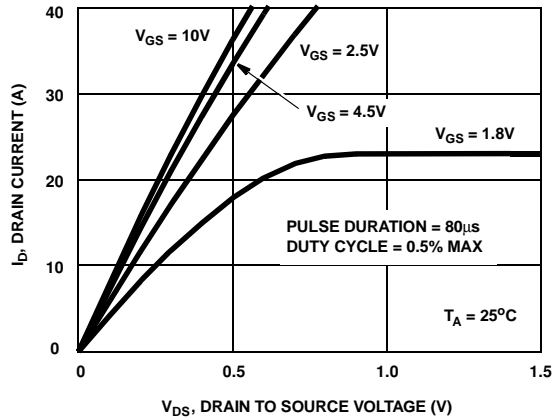
**Typical Characteristic** (Continued)  $T_A = 25^\circ\text{C}$  unless otherwise noted



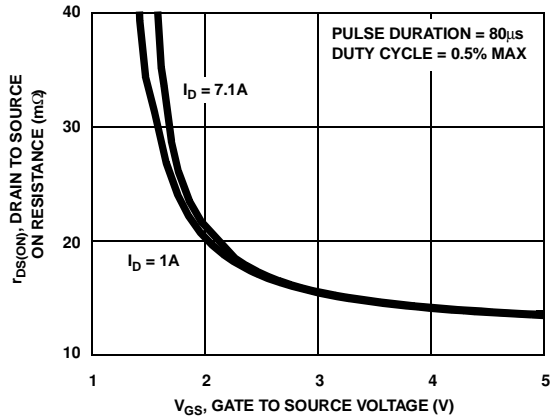
**Figure 5. Forward Bias Safe Operating Area**



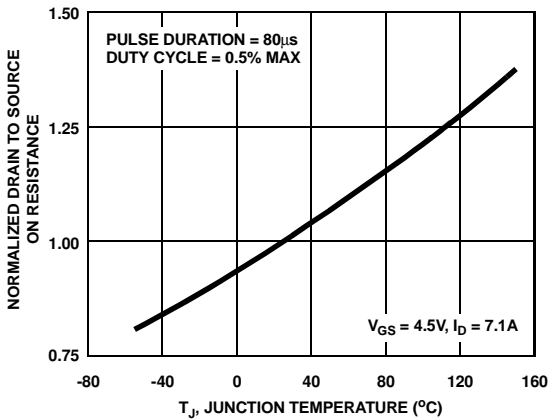
**Figure 6. Transfer Characteristics**



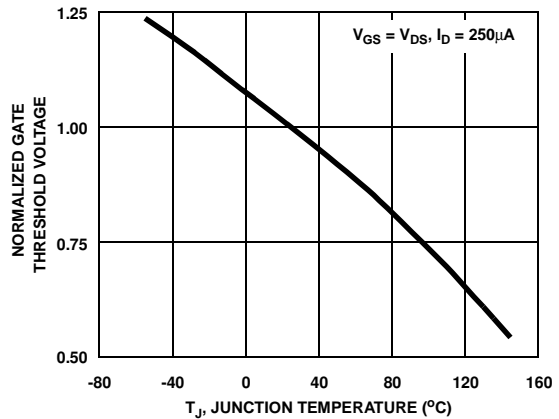
**Figure 7. Saturation Characteristics**



**Figure 8. Drain to Source On Resistance vs Gate Voltage and Drain Current**

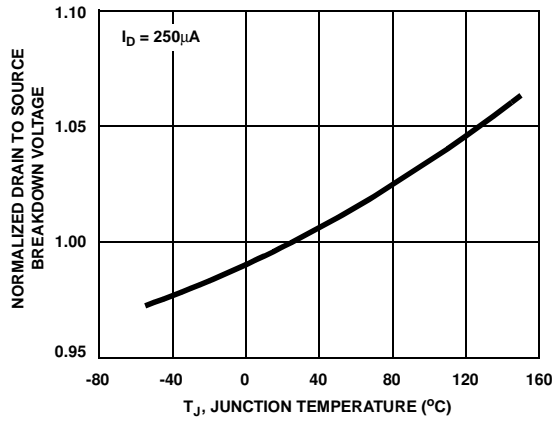


**Figure 9. Normalized Drain to Source On Resistance vs Junction Temperature**

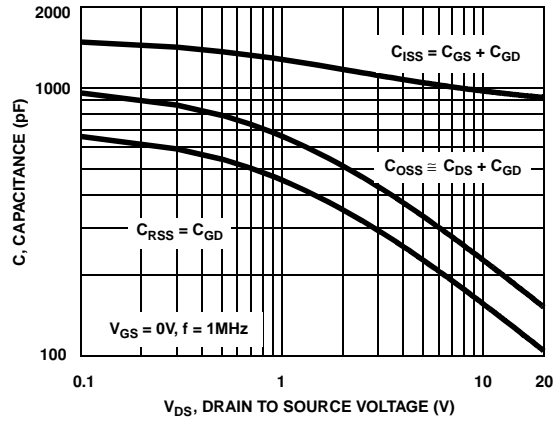


**Figure 10. Normalized Gate Threshold Voltage vs Junction Temperature**

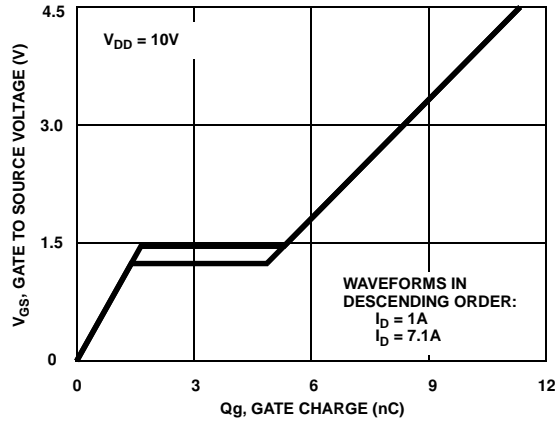
**Typical Characteristic** (Continued)  $T_A = 25^\circ\text{C}$  unless otherwise noted



**Figure 11. Normalized Drain to Source Breakdown Voltage vs Junction Temperature**



**Figure 12. Capacitance vs Drain to Source Voltage**



**Figure 13. Gate Charge Waveforms for Constant Gate Currents**

### Test Circuits and Waveforms

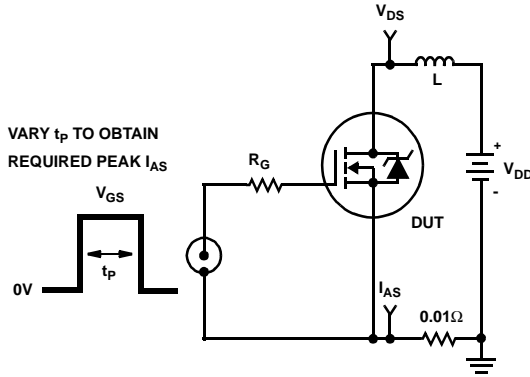


Figure 14. Unclamped Energy Test Circuit

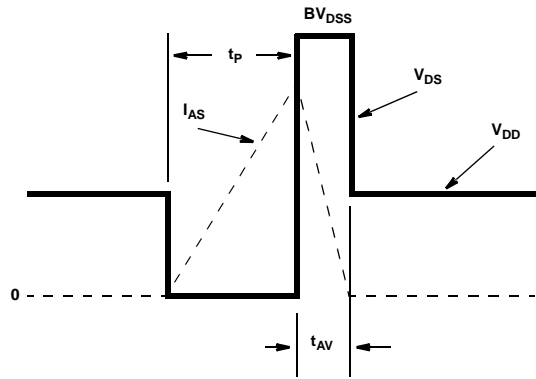


Figure 15. Unclamped Energy Waveforms

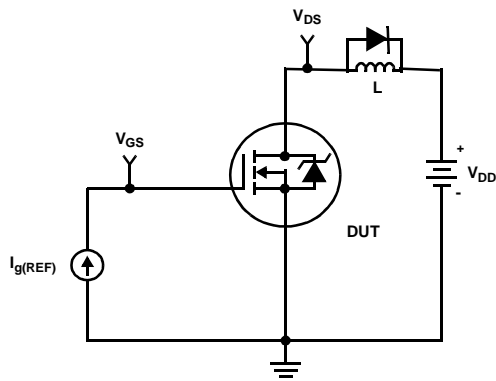


Figure 16. Gate Charge Test Circuit

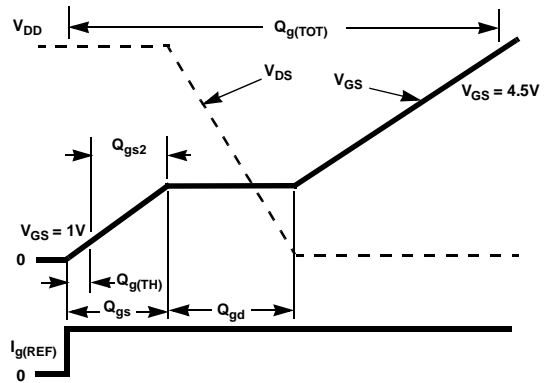


Figure 17. Gate Charge Waveforms

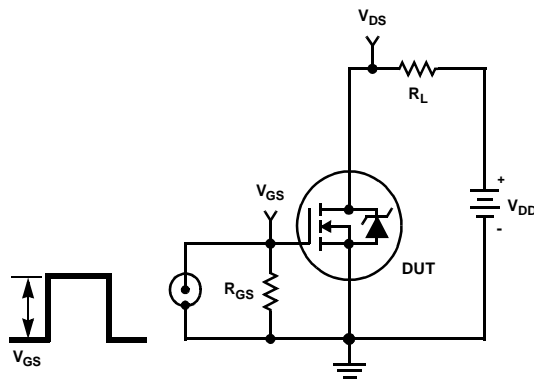


Figure 18. Switching Time Test Circuit

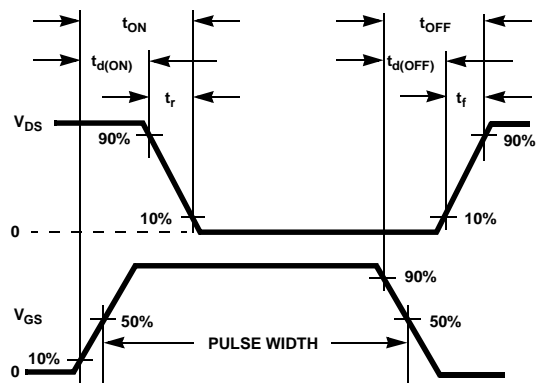


Figure 19. Switching Time Waveforms

## PSPICE Electrical Model

.SUBCKT FDW2511NZ 2 1 3 ; rev July 2004

Ca 12 8 1.1e-9  
Cb 15 14 1.1e-9  
Cin 6 8 0.8e-9

Dbody 7 5 DbodyMOD  
Dbreak 5 11 DbreakMOD  
DESD2 91 9 DESD2MOD  
DESD1 91 7 DESD1MOD  
Dplcap 10 5 DplcapMOD

Ebreak 11 7 17 18 24  
Eds 14 8 5 8 1  
Egs 13 8 6 8 1  
Esg 6 10 6 8 1  
Evthres 6 21 19 8 1  
Etemp 20 6 18 22 1

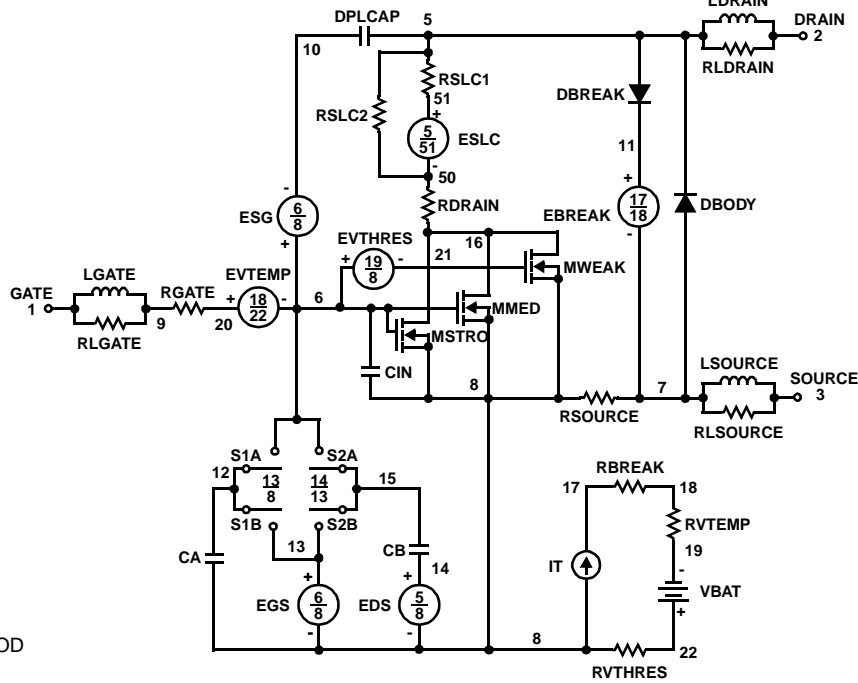
It 8 17 1

Lgate 1 9 9.1e-10  
Ldrain 2 5 1e-9  
Lsource 3 7 2.1e-10

RLgate 1 9 9.1  
RLdrain 2 5 10  
RLsource 3 7 2.1

Mmed 16 6 8 8 MmedMOD  
Mstro 16 6 8 8 MstroMOD  
Mweak 16 21 8 8 MweakMOD

Rbreak 17 18 RbreakMOD 1  
Rdrain 50 16 RdrainMOD 1.0e-2  
Rgate 9 20 2.75  
RSLC1 5 51 RSLCMOD 1e-6  
RSLC2 5 50 1e3  
Rsource 8 7 RsourceMOD 1.7e-3  
Rvthres 22 8 RvthresMOD 1  
Rvtemp 18 19 RvtempMOD 1  
S1a 6 12 13 8 S1AMOD  
S1b 13 12 13 8 S1BMOD  
S2a 6 15 14 13 S2AMOD  
S2b 13 15 14 13 S2BMOD  
Sbat 22 19 DC 1  
ESLC 51 50 VALUE={(V(5,51)/ABS(V(5,51)))\*(PWR(V(5,51))/(1e-6\*120),2.5))}  
MODEL DbodyMOD D (IS=3.5E-11 RS=1.08e-2 IKF=.5 N= TRS1=8e-4 TRS2=6e-6 XTI=.1  
+CJO=3.2e-10 TT=1.07e-8 M=0.68 TIKF=0.001)  
.MODEL DbreakMOD D (RS=1e-1 TRS1=9e-3 TRS2=-2.0e-5)  
.MODEL DESD1MOD D (BV=15.0 RS=1)  
.MODEL DESD2MOD D (BV=14.3 RS=1)  
.MODEL DplcapMOD D (CJO=0.70e-9 IS=1e-30 N=10 M=0.3)  
MODEL MstroMOD NMOS (VTO=1.21 KP=147 IS=1e-30 N=10 TOX=1 L=1u W=1u)  
.MODEL MmedMOD NMOS (VTO=0.93 KP=1.7 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=2.75)  
.MODEL MweakMOD NMOS (VTO=0.752 KP=0.05 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=27.5 RS=.1)  
MODEL RbreakMOD RES (TC1=5.0e-4 TC2=8e-7)  
.MODEL RdrainMOD RES (TC1=2.1e-3 TC2=3.4e-6)  
.MODEL RSLCMOD RES (TC1=1e-3 TC2=1e-5)  
.MODEL RsourceMOD RES (TC1=5e-3 TC2=1e-6)  
.MODEL RvtempMOD RES (TC1=-.9e-3 TC2=1e-7)  
.MODEL RvthresMOD RES (TC1=-1.1e-3 TC2=-4.0e-6)  
MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-6 VOFF=-1.5)  
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-1.5 VOFF=-6)  
.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-0.5 VOFF=0.3)  
.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=0.3 VOFF=-0.5)  
ENDS  
\*\$



Note: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.



## SABER Electrical Model

REV July 2004

template fdw2511nz n2,n1,n3

electrical n2,n1,n3

```
{
var i iscl
dp..model dbodymod = (isl=3.5e-11,rs=1.08e-2,ikf=.5,trs1=8e-4,trs2=6e-6,xti=.1,cjo=3.2e-10,tt=1.07e-8,m=0.68,tikf=0.001)
dp..model dbreakmod = (rs=1e-1,trs1=9e-3,trs2=-2.0e-5)
dp..model dplcapmod = (cjo=0.70e-9,isl=10e-30,nl=10,m=0.3)
m..model mstrongmod = (type=_n,vto=1.21,kp=147,is=1e-30,tox=1)
m..model mmedmod = (type=_n,vto=0.93,kp=1.7,is=1e-30,tox=1)
m..model mweakmod = (type=_n,vto=0.752,kp=0.05,is=1e-30,tox=1,rs=0.1)
sw_vcsp..model s1amod = (ron=1e-5,roff=0.1,von=-6,voff=-1.5)
sw_vcsp..model s1bmod = (ron=1e-5,roff=0.1,von=-1.5,voff=-6)
sw_vcsp..model s2amod = (ron=1e-5,roff=0.1,von=-0.5,voff=0.3)
sw_vcsp..model s2bmod = (ron=1e-5,roff=0.1,von=0.3,voff=-0.5)
c.ca n12 n8 = 1.1e-9
c.cb n15 n14 = 1.1e-9
c.cin n6 n8 = 0.8e-9
```

```
dp.dbody n7 n5 = model=dbodymod
dp.dbreak n5 n11 = model=dbreakmod
desd2 91 9 desd2mod
desd1 91 7 desd1mod
dp.dplcap n10 n5 = model=dplcapmod
```

```
spe.ebreak n11 n7 n17 n18 = 24
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n6 n10 n6 n8 = 1
spe.evthres n6 n21 n19 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1
```

```
i.it n8 n17 = 1
```

```
l.lgate n1 n9 = 9.1e-10
l.lldrain n2 n5 = 1e-9
l.lsource n3 n7 = 2.1e-10
```

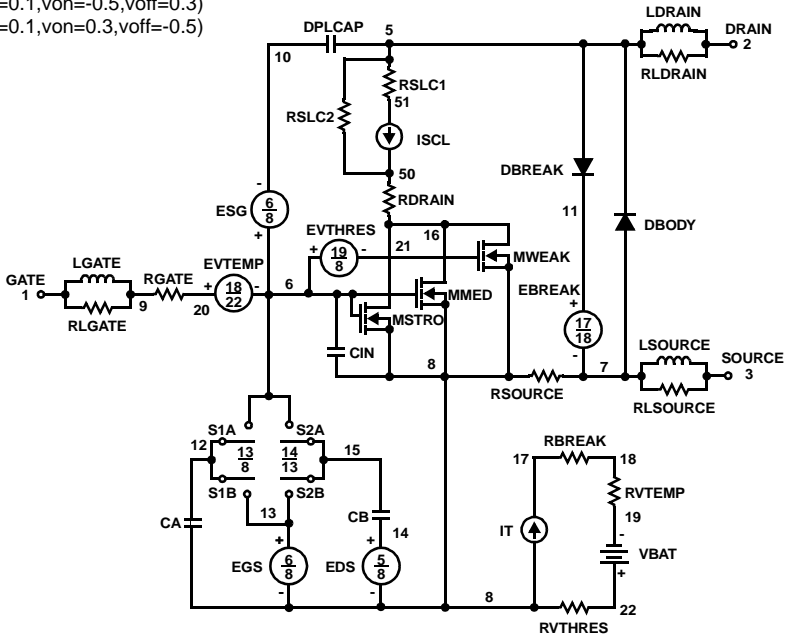
```
res.rlgate n1 n9 = 9.1
res.rldrain n2 n5 = 10
res.rlsource n3 n7 = 2.1
```

```
m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u
m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u
m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u
```

```
res.rbreak n17 n18 = 1, tc1=5.0e-4,tc2=8e-7
m.desd1mod bv=15.0 rs=1)
m.desd2mod bv=14.3 rs=1)
res.rdrain n50 n16 = 1.0e-2, tc1=2.1e-3,tc2=3.4e-6
res.rgate n9 n20 = 2.75
res.rslc1 n5 n51 = 1e-6, tc1=1e-3,tc2=1e-5
res.rslc2 n5 n50 = 1e3
res.rsource n8 n7 = 1.7e-3, tc1=5e-3,tc2=1e-6
res.rvthres n22 n8 = 1, tc1=-1.1e-3,tc2=-4.0e-6
res.rvtemp n18 n19 = 1, tc1=-.9e-3,tc2=1e-7
sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod
```

```
v.vbat n22 n19 = dc=1
```

```
equations {
i (n51->n50) +=iscl
iscl: v(n51,n50) = ((v(n5,n51))/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51)*1e6/120))** 2.5))
}
}
```



### SPICE Thermal Model

REV July 2004  
 FDW2511NZ\_JA Junction Ambient  
 Minimum copper pad area

CTHERM1 Junction c2 5.7e-4  
 CHERM2 c2 c3 5.72e-4  
 CHERM3 c3 c4 5.8e-4  
 CHERM4 c4 c5 4.7e-3  
 CHERM5 c5 c6 5.1e-3  
 CHERM6 c6 c7 0.02  
 CHERM7 c7 c8 0.2  
 CHERM8 c8 Ambient 6

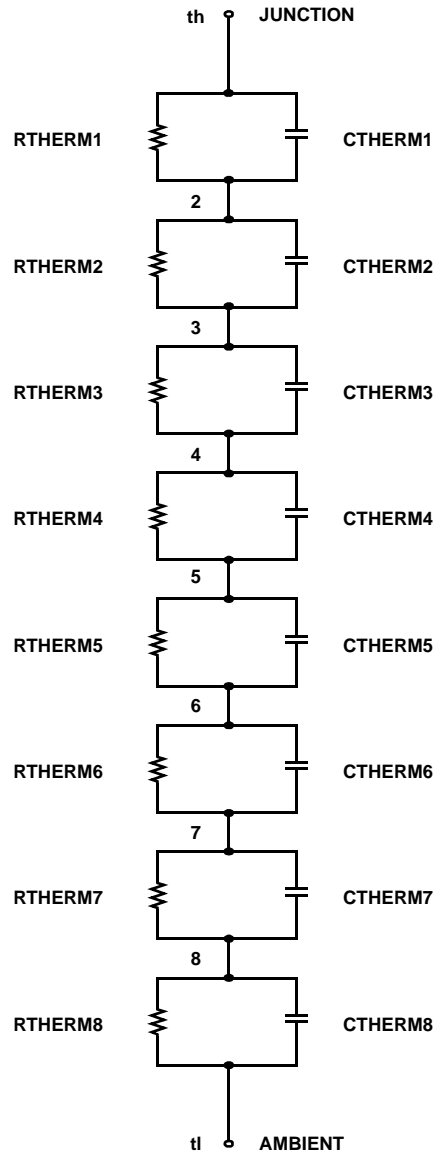
RHERM1 Junction c2 0.003  
 RHERM2 c2 c3 0.25  
 RHERM3 c3 c4 1.0  
 RHERM4 c4 c5 1.1  
 RHERM5 c5 c6 7.5  
 RHERM6 c6 c7 33.6  
 RHERM7 c7 c8 33.7  
 RHERM8 c8 Ambient 33.8

### SABER Thermal Model

SABER thermal model FDW2511NZ  
 Minimum copper pad area  
 template thermal\_model th tl  
 thermal\_c th, tl

```
{
    ctherm.ctherm1 th c2 = 5.7e-4
    ctherm.ctherm2 c2 c3 = 5.72e-4
    ctherm.ctherm3 c3 c4 = 5.8e-4
    ctherm.ctherm4 c4 c5 = 4.7e-3
    ctherm.ctherm5 c5 c6 = 5.1e-3
    ctherm.ctherm6 c6 c7 = 0.02
    ctherm.ctherm7 c7 c8 = 0.2
    ctherm.ctherm8 c8 tl = 6
}
```





```
rtherm.rtherm1 th c2 = 0.003
rtherm.rtherm2 c2 c3 = 0.25
rtherm.rtherm3 c3 c4 = 1.0
rtherm.rtherm4 c4 c5 = 1.1
rtherm.rtherm5 c5 c6 = 7.5
rtherm.rtherm6 c6 c7 = 33.6
rtherm.rtherm7 c7 c8 = 33.7
rtherm.rtherm8 c8 tl = 33.8
}
```





**TRADEMARKS**

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

- |   |   |   |   |
|---|---|---|---|
| ACEx®   | FPS™  | PDP-SPM™  | The Power Franchise®  |
| Build it Now™   | F-PFS™  | Power-SPM™  | <b>power</b><br>the franchise   |
| CorePLUS™   | FRFET®  | PowerTrench®  | TinyBoost™  |
| CorePOWER™  | Global Power ResourceSM   | Programmable Active Droop™  | TinyBuck™   |
| CROSSVOLT™  | Green FPS™  | QFET®   | TinyLogic®  |
| CTL™  | Green FPS™ e-Series™  | QS™   | TINYOPTO™   |
| Current Transfer Logic™   | GTO™  | Quiet Series™   | TinyPower™  |
| EcoSPARK®   | IntelliMAX™   | RapidConfigure™   | TinyPWM™  |
| EfficientMax™   | ISOPLANAR™  | Saving our world 1mW at a time™   | TinyWire™   |
| EZSWITCH™ *   | MegaBuck™   | SmartMax™   | µSerDes™  |
|  | MICROCOUPLER™   | SMART START™  |  |
|  | MicroFET™   | SPM®  | UHC®  |
| Fairchild®  | MicroPak™   | STEALTH™  | Ultra FRFET™  |
| Fairchild Semiconductor®  | MillerDrive™  | SuperFET™   | UniFET™   |
| FACT Quiet Series™  | MotionMax™  | SuperSOT™-3   | VCX™  |
| FACT®   | Motion-SPM™   | SuperSOT™-6   | VisualMax™  |
| FAST®   | OPTOLOGIC®  | SuperSOT™-8   |   |
| FastvCore™  | OPTOPLANAR®   | SuperMOS™   |   |
| FlashWriter® *  |  |  |   |

\* EZSWITCH™ and FlashWriter® are trademarks of System General Corporation, used under license by Fairchild Semiconductor.

**DISCLAIMER**

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

- Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
- A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

**PRODUCT STATUS DEFINITIONS**

**Definition of Terms**

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	This datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.